SBOS249H − JUNE 2003 − REVISED AUGUST 2008

Dual, Wideband, High Output Current, Operational Amplifier with Current Limit

FEATURES

- LOW INPUT NOISE VOLTAGE: 1.8nV/√Hz
- HIGH UNITY-GAIN BANDWIDTH: 230MHz
- HIGH GAIN BANDWIDTH PRODUCT: 125MHz
- HIGH OUTPUT CURRENT: 350mA
- LOW INPUT OFFSET VOLTAGE: ±0.2mV
- FLEXIBLE SUPPLY RANGE:
  Single +5V to +12V Operation
  Dual ±2.5V to ±6V Operation
- LOW SUPPLY CURRENT: 6.0mA/ch

DESCRIPTION

The OPA2613 offers very low 1.8nV√Hz input noise in a wideband, unity-gain stable, voltage-feedback architecture. Intended for xDSL driver applications, the OPA2613 also supports this low input noise with exceptionally low harmonic distortion, particularly in differential configurations. Adequate output current is provided to drive the potentially heavy load of a twisted-pair line. Harmonic distortion for a $2V_{PP}$ differential output operating from +5V to +12V supplies is ≤ −95dBc through 1MHz input frequencies. Operating on a low 6.0mA/ch supply current, the OPA2613 can satisfy most xDSL driver requirements over a wide range of possible supply voltage—from a single +5V condition, to ±5V, on up to a single +12V design.

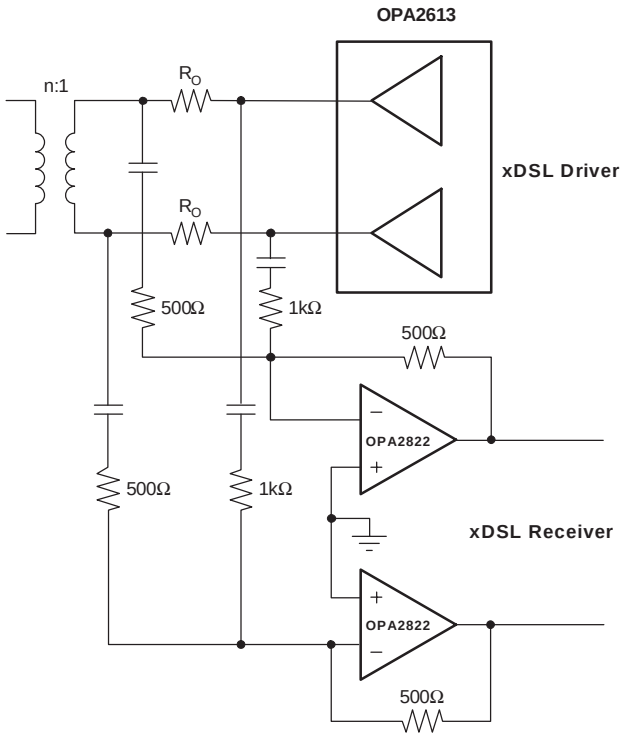
General-purpose applications on a single +5V supply will benefit from the high input and output voltage swing available on this reduced supply voltage. Low-cost precision integrators for PLLs will also benefit from the low voltage noise and offset voltage. Baseband I/Q receiver channels can achieve almost perfect channel match with noise and distortion to support signals through 5MHz with > 14-bit dynamic range.

APPLICATIONS

- xDSL DIFFERENTIAL LINE DRIVERS
- 16-BIT ADC DRIVER
- LOW NOISE PLL INTEGRATORS
- TRANSIMPEDANCE AMPLIFIERS
- PRECISION BASEBAND I/Q AMPLIFIERS
- ACTIVE FILTERS
- TS613 IMPROVED REPLACEMENT

OPA2613 RELATED PRODUCTS

FEATURES	SINGLES	DUALS	TRIPLES
High Gain Stable	—	OPA2614	—
High Slew Rate VFB	OPA690	OPA2690	OPA3690
R/R Input/Output VFB	OPA353	OPA2353	—
Current-Feedback	OPA691	OPA2691	OPA3691
Current-Feedback	—	OPA2677	—



ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage (−40°C to +85°C)	±6.5V
Supply Voltage (0°C to +70°C)	±6.65V
Internal Power Dissipation	See Thermal Characteristics
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range	−65°C to +125°C
Lead Temperature (SO-8)	+260°C
Junction Temperature (T_J)	+150°C
ESD Rating (Human Body Model)	2000V
(Machine Model)	200V
(Charge Device Model)	1500V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

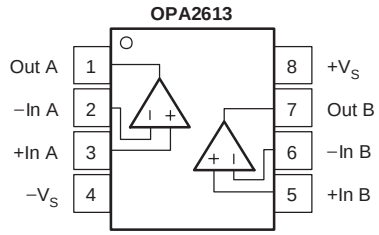
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2613	SO-8	D	−40°C to +85°C	OPA2613	OPA2613ID OPA2613IDR	Rails, 100 Tape and Reel, 2500

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN CONFIGURATION

Top View **SO**



ELECTRICAL CHARACTERISTICS: $V_S = \pm 6V$

Boldface limits are tested at **+25°C.**

$R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2, unless otherwise noted. See Figure 1 for AC performance only.

PARAMETER	TEST CONDITIONS	OPA2613ID TYP +25°C	OPA2613ID MIN/MAX OVER TEMPERATURE +25°C(1)	0°C to +70°C(2)	−40°C to +85°C(2)	UNITS	MIN/MAX	TEST LEVEL (3)
AC Performance (see Figure 1)								
Small-Signal Bandwidth	G = +1, $V_O = 0.1V_{PP}$, $R_F = 0\Omega$	230				MHz	typ	C
	G = +2, $V_O = 0.1V_{PP}$	110	80	75	70	MHz	min	B
	G = +10, $V_O = 0.1V_{PP}$	13	10	9	9	MHz	min	B
Gain-Bandwidth Product	G ≥ 20	125	95	80	75	MHz	min	B
Bandwidth for 0.1dB Gain Flatness	G = +2, $V_O < 0.1V_{PP}$	5				MHz	typ	C
Peaking at a Gain of +1	$V_O < 0.1V_{PP}$	1				dB	typ	C
Large-Signal Bandwidth	G = +2, $V_O = 2V_{PP}$	22				MHz	typ	C
Slew Rate	G = +2, 4V Step	70	56	51	50	V/µs	min	B
Rise-and-Fall Time	G = +2, V_O = 0.2V Step	3.6	4.8	5.4	5.5	ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	55	68	71	72	ns	typ	C
0.1%	G = +2, V_O = 2V Step	40	51	53	54	ns	typ	C
Harmonic Distortion	G = +2, f = 1MHz, $V_O = 2V_{PP}$							
2nd-Harmonic	$R_L = 20\Omega$	−70	−63	−61	−60	dBc	max	B
	$R_L \geq 500\Omega$	−95	−90	−88	−87	dBc	max	B
3rd-Harmonic	$R_L = 20\Omega$	−84	−80	−78	−77	dBc	max	B
	$R_L \geq 500\Omega$	−97	−92	−90	−89	dBc	max	B
Input Voltage Noise	f > 10kHz	1.8	2.0	2.1	2.3	nV/√Hz	max	B
Input Current Noise	f > 10kHz	1.7	2.1	2.2	2.4	pA/√Hz	max	B
Differential Gain	G = +2, PAL, $V_O = 1.4V_{PP}$, $R_L = 150\Omega$	0.02				%	typ	C
Differential Phase	G = +2, PAL, $V_O = 1.4V_{PP}$, $R_L = 150\Omega$	0.03				deg	typ	C
Channel-to-Channel Crosstalk	f = 1MHz, Input-Referred	−80				dBc	typ	C
DC Performance(4)								
Open-Loop Gain (A_{OL})	V_O = 0V, $R_L = 100\Omega$	97	**92**	92	91	dB	min	A
Input Offset Voltage	V_{CM} = 0V	±0.2	**±1.0**	±1.15	±1.2	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			±3.3	±3.3	µV/°C	max	B
Input Bias Current	V_{CM} = 0V	−6	**−12**	−13	−14.5	µA	max	A
Average Bias Current Drift (Magnitude)	V_{CM} = 0V			−30	−35	nA/°C	max	B
Input Offset Current	V_{CM} = 0V	±50	**±300**	±520	±750	nA	max	A
Average Offset Bias Current Drift	V_{CM} = 0V			±5	±7	nA/°C	max	B
Input								
Common-Mode Input Range (CMIR)(5)		±4.7	**±4.5**	±4.5	±4.4	V	min	A
Common-Mode Rejection Ratio (CMRR)	$V_{CM} = \pm 1V$	100	**88**	87	86	dB	min	A
Input Impedance								
Differential-Mode	V_{CM} = 0	18 ||0.6				kΩ ||pF	typ	C
Common-Mode	V_{CM} = 0	7 ||1				MΩ ||pF	typ	C
Output								
Output Voltage Swing	No Load	±5.0	**±4.8**	±4.8	±4.7	V	min	A
	100Ω	±4.9	**±4.7**	±4.7	±4.6	V	min	A
Current Output, Sourcing	V_O = 0, Linear Operation	+350	**+280**	+240	+220	mA	min	A
Current Output, Sinking	V_O = 0, Linear Operation	−350	**−280**	−240	−220	mA	min	A
Short-Circuit Current	Output Shorted to Ground	500				mA	typ	C
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.01				Ω	typ	C

(1) Junction temperature = ambient for +25°C tested specifications.
(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature tested specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive-out-of-node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum CMRR specification at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = ±6V (continued)

Boldface limits are tested at **+25°C.**

R_F = 402Ω, R_L = 100Ω, and G = +2, unless otherwise noted. See Figure 1 for AC performance only.

PARAMETER	TEST CONDITIONS	OPA2613ID						TEST LEVEL (3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to +70°C(2)	−40°C to +85°C(2)	UNITS	MIN/ MAX	
Power Supply								
Specified Operating Voltage		±6				V	typ	C
Maximum Operating Voltage Range			**±6.3**	±6.3	±6.3	V	max	A
Maximum Quiescent Current	V_S = ±6V, Both Channels	12	**12.4**	12.8	13	mA	max	A
Minimum Quiescent Current	V_S = ±6V, Both Channels	12	**11.6**	11.2	11	mA	min	A
Power-Supply Rejection Ratio (−PSRR)	Input-Referred	95	**90**	88	87	dB	min	A
Thermal Characteristics								
Specified Operating Range D Package		−40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C

(1) Junction temperature = ambient for +25°C tested specifications.
(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature tested specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive-out-of-node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum CMRR specification at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

R_F = 402Ω, R_L = 100Ω, and G = +2, unless otherwise noted. See Figure 3 for AC performance only.

PARAMETER	TEST CONDITIONS	OPA2613ID						TEST LEVEL (3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to +70°C(2)	−40°C to +85°C(2)	UNITS	MIN/ MAX	
AC Performance (see Figure 3)								
Small-Signal Bandwidth	G = +1, V_O = 0.1V_{PP}, R_F = 0Ω	230				MHz	typ	C
	G = +2, V_O = 0.1V_{PP}	105	75	69	68	MHz	min	B
	G = +10, V_O = 0.1V_{PP}	12	10	8	8	MHz	min	B
Gain-Bandwidth Product	G ≥ 20	118	93	78	76	MHz	min	B
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O < 0.1V_{PP}	5				MHz	typ	C
Peaking at a Gain of +1	V_O < 0.1V_{PP}	2.6				dB	typ	C
Large-Signal Bandwidth	G = +2, V_O = 2V_{PP}	21				MHz	typ	C
Slew Rate	G = +2, 2V Step	60	47	46	46	V/µs	min	B
Rise-and-Fall Time	G = +2, V_O = 0.2V Step	3.8	5.0	5.6	5.7	ns	typ	B
Settling Time to 0.02%	G = +2, V_O = 2V Step	63	78	80	81	ns	typ	B
0.1%	G = +2, V_O = 2V Step	52	62	64	64	ns	typ	B
Harmonic Distortion	G = +2, f = 1MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 20Ω to V_S/2	−67	−60	−58	−57	dBc	max	B
	R_L ≥ 500Ω to V_S/2	−82	−79	−77	−76	dBc	max	B
3rd-Harmonic	R_L = 20Ω to V_S/2	−84	−78	−76	−75	dBc	max	B
	R_L ≥ 500Ω to V_S/2	−94	−89	−87	−86	dBc	max	B
Input Voltage Noise	f > 10kHz	1.9	2.1	2.2	2.4	nV/√Hz	max	B
Input Current Noise	f > 10kHz	1.7	2.1	2.2	2.4	pA/√Hz	max	B
Channel-to-Channel Crosstalk	f = 1MHz, Input-Referred	−80				dBc	typ	C
DC Performance(4)								
Open-Loop Gain (A_{OL})	V_O = 0V, R_L = 100Ω	95	**91**	89	88	dB	min	A
Input Offset Voltage	V_{CM} = 0V	±0.2	**±1.0**	±1.15	±1.2	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			±3.3	±3.3	µV/°C	max	B
Input Bias Current	V_{CM} = 0V	−6	**−11**	−12	−13.5	µA	max	A
Average Bias Current Drift (Magnitude)	V_{CM} = 0V			−35	−35	nA/°C	max	B
Input Offset Current	V_{CM} = 0V	±50	**±300**	±520	±750	nA	max	A
Average Offset Bias Current Drift	V_{CM} = 0V			±5	±7	nA/°C	max	B
Input								
Least Positive Input Voltage		1.2	**1.4**	1.4	1.5	V	max	A
Most Positive Input Voltage		3.8	**3.6**	3.6	3.5	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = ±1V	95	**85**	84	83	dB	min	A
Input Impedance								A
Differential-Mode	V_{CM} = 0	15 ‖ 1				kΩ ‖ pF	typ	C
Common-Mode	V_{CM} = 0	5 ‖ 1.3				MΩ ‖ pF	typ	C
Output								
Most Positive Output Voltage	No Load	4.0	**3.85**	3.8	3.75	V	min	A
	100Ω Load to 2.5V	3.95	**3.8**	3.75	3.7	V	min	A
Least Positive Output Voltage	No Load	1.0	**1.15**	1.2	1.25	V	min	A
	100Ω Load to 2.5V	1.05	**1.20**	1.25	1.3	V	min	A
Current Output, Sourcing	V_O = 0, Linear Operation	+300				mA	typ	C
Current Output, Sinking	V_O = 0, Linear Operation	−300				mA	typ	C
Short-Circuit Current	Output Shorted to Mid-Supply	±400				mA	typ	C
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.01				Ω	typ	C

(1) Junction temperature = ambient for +25°C tested specifications.
(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature tested specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive-out-of-node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum CMRR specification at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +5V (continued)

Boldface limits are tested at **+25°C.**

R_F = 402Ω, R_L = 100Ω, and G = +2, unless otherwise noted. See Figure 3 for AC performance only.

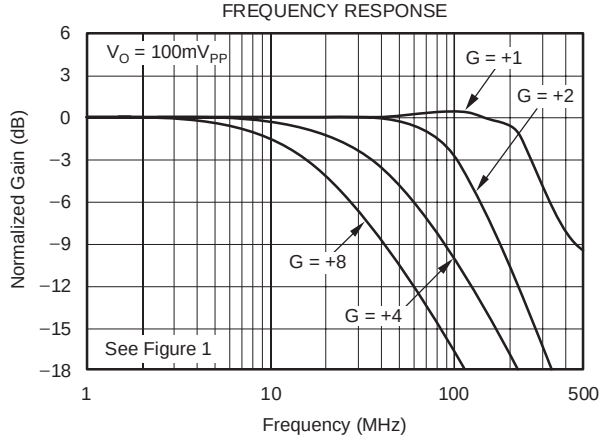
PARAMETER	TEST CONDITIONS	OPA2613ID						TEST LEVEL (3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to +70°C(2)	−40°C to +85°C(2)	UNITS	MIN/ MAX	
Power Supply								
Specified Operating Voltage		5				V	typ	C
Maximum Operating Voltage Range			**12.6**	12.6	12.6	V	max	A
Maximum Quiescent Current	V_S = ±6V, Both Channels	10.5	**11.0**	11.3	11.5	mA	max	A
Minimum Quiescent Current	V_S = ±6V, Both Channels	10.5	**9.4**	9.4	9.1	mA	min	A
Power-Supply Rejection Ratio (−PSRR)	Input-Referred	95				dB	typ	C
Thermal Characteristics								
Specified Operating Range D Package		−40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C

(1) Junction temperature = ambient for +25°C tested specifications.
(2) Junction temperature = ambient at low temperature limit; junction temperature = ambient +23°C at high temperature limit for over temperature tested specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive-out-of-node. V_{CM} is the input common-mode voltage.
(5) Tested < 3dB below minimum CMRR specification at ± CMIR limits.

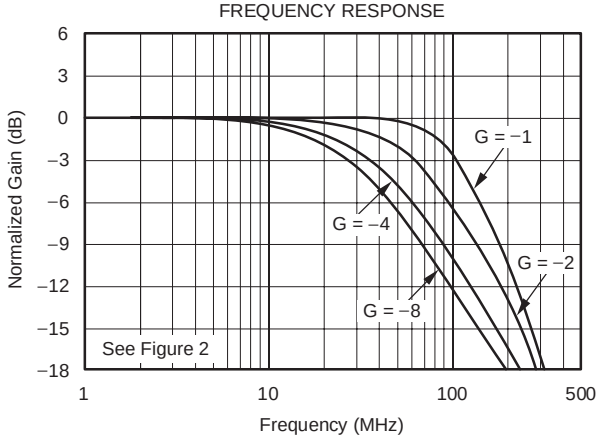
TYPICAL CHARACTERISTICS: $V_S = \pm 6V$

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

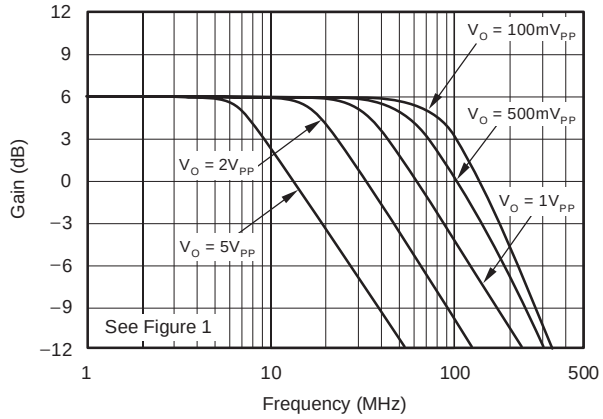
NONINVERTING SMALL−SIGNAL FREQUENCY RESPONSE



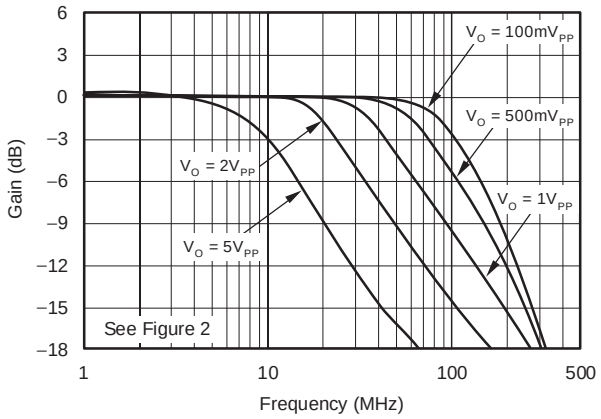
INVERTING SMALL−SIGNAL FREQUENCY RESPONSE



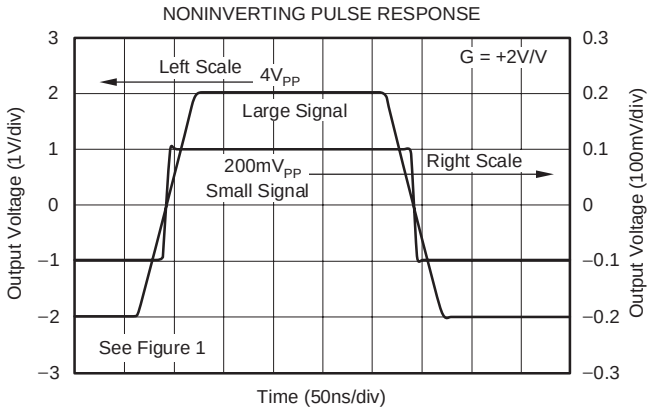
NONINVERTING LARGE−SIGNAL FREQUENCY RESPONSE



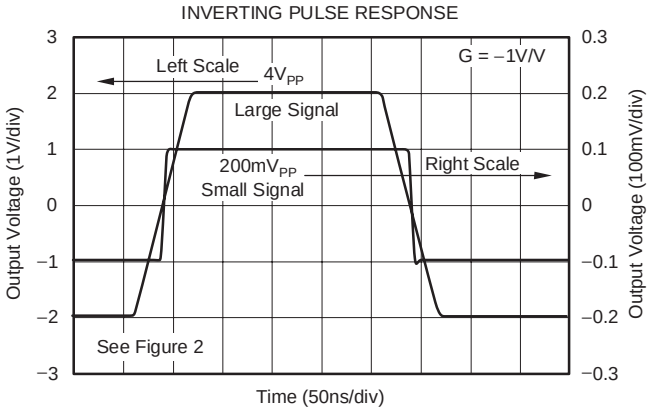
INVERTING LARGE−SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



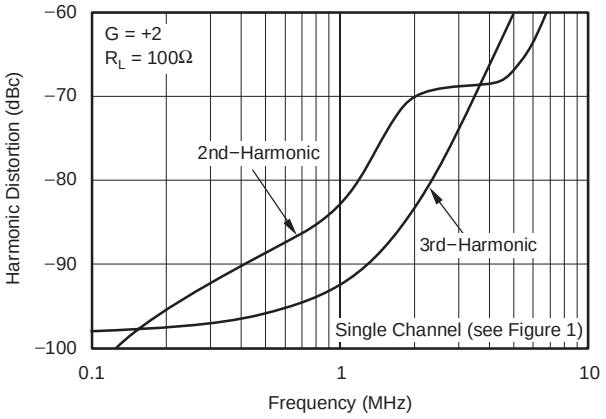
INVERTING PULSE RESPONSE



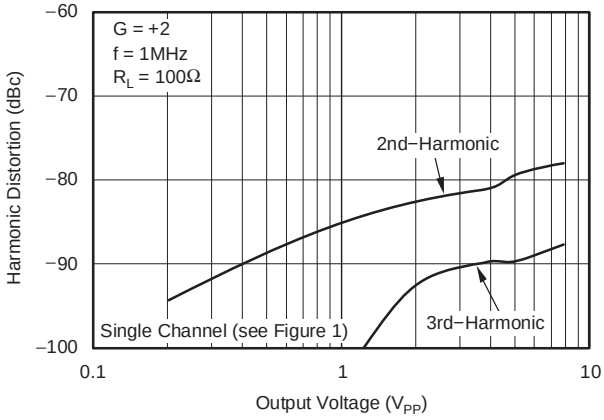
TYPICAL CHARACTERISTICS: $V_S = \pm 6V$ (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

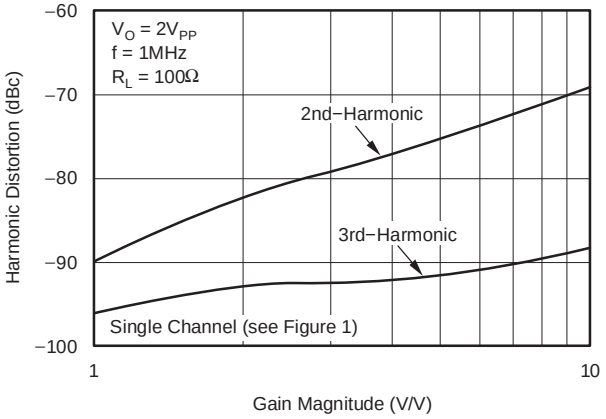
HARMONIC DISTORTION vs FREQUENCY



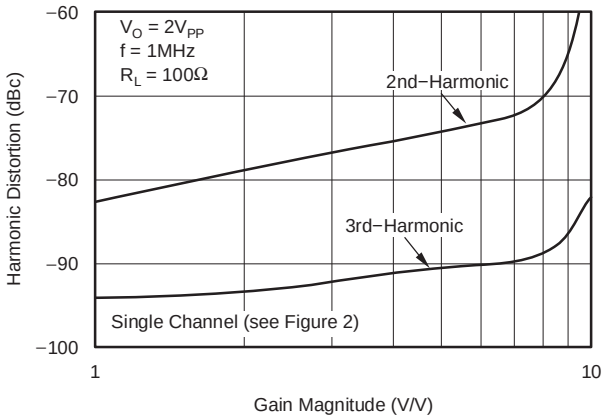
HARMONIC DISTORTION vs OUTPUT VOLTAGE



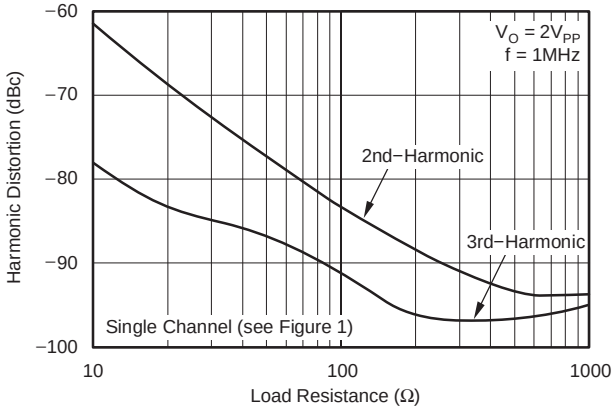
HARMONIC DISTORTION vs NONINVERTING GAIN



HARMONIC DISTORTION vs INVERTING GAIN



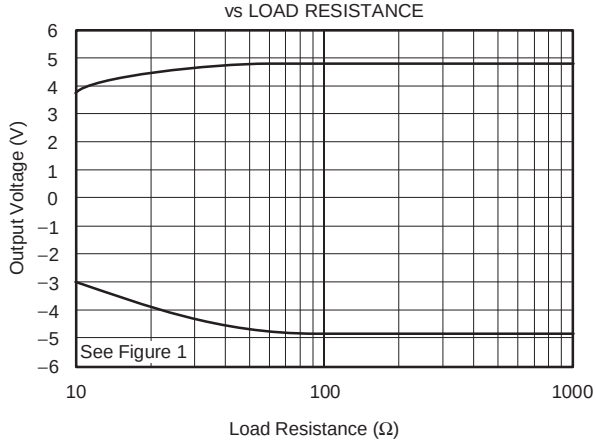
HARMONIC DISTORTION vs LOAD RESISTANCE



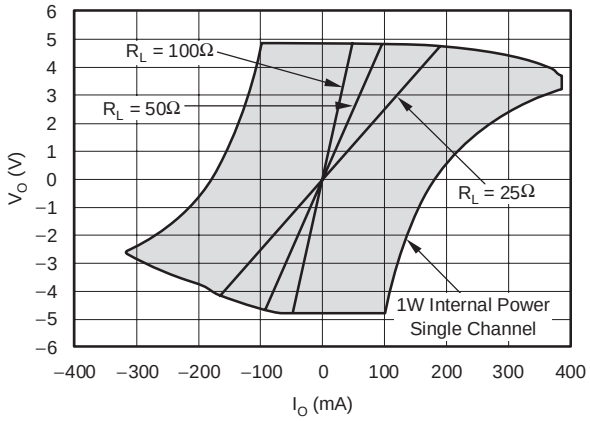
TYPICAL CHARACTERISTICS: V_S = ±6V (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

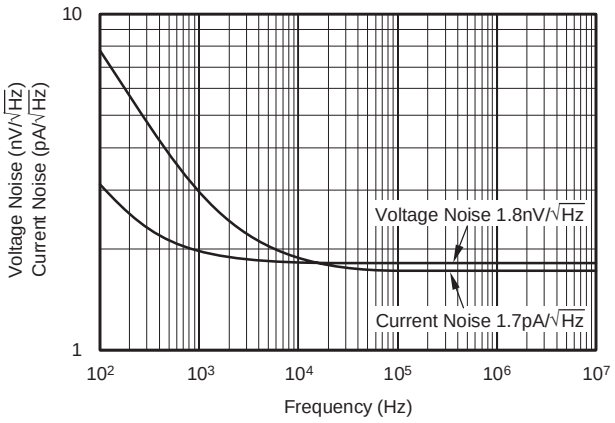
MAXIMUM OUTPUT SWING vs LOAD RESISTANCE



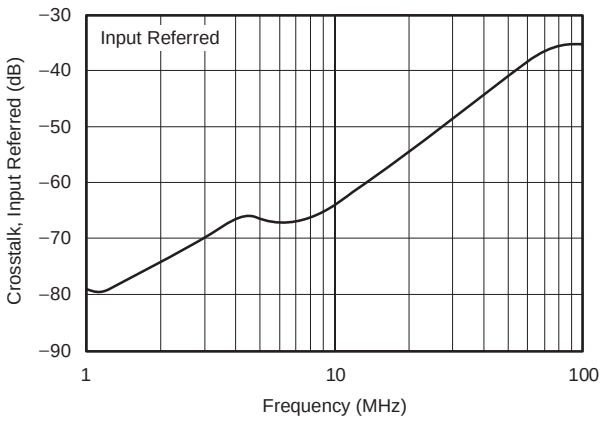
OUTPUT VOLTAGE AND CURRENT LIMITATIONS



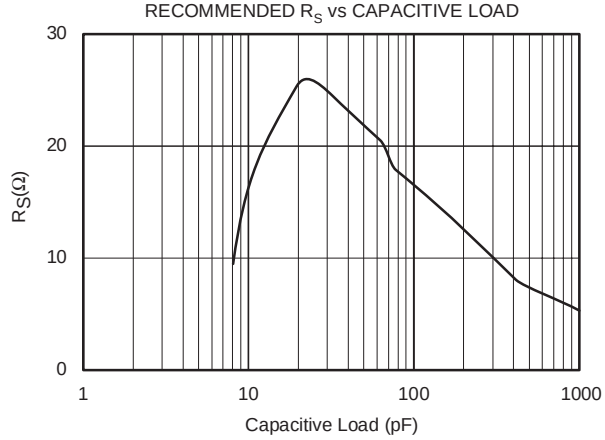
INPUT VOLTAGE AND CURRENT NOISE DENSITY



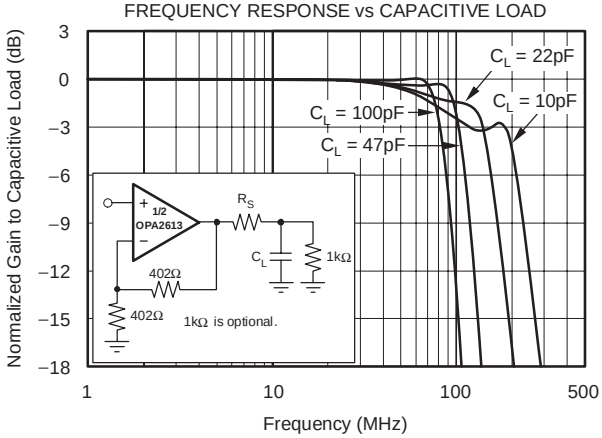
CHANNEL−TO−CHANNEL CROSSTALK



RECOMMENDED R_S vs CAPACITIVE LOAD



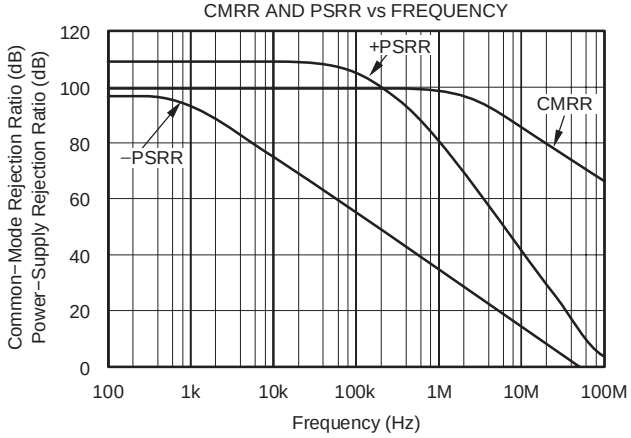
FREQUENCY RESPONSE vs CAPACITIVE LOAD



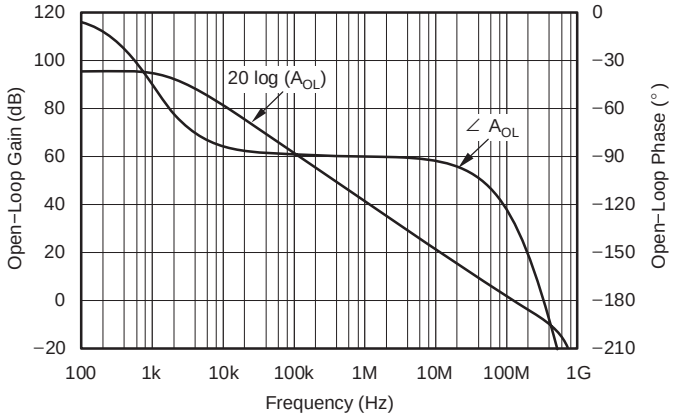
TYPICAL CHARACTERISTICS: $V_S = \pm 6V$ (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

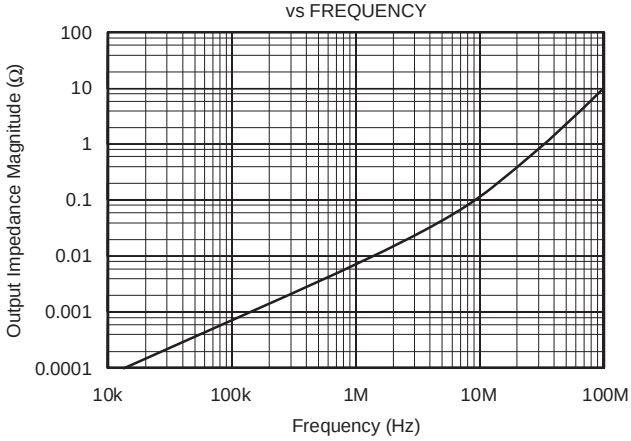
CMRR AND PSRR vs FREQUENCY



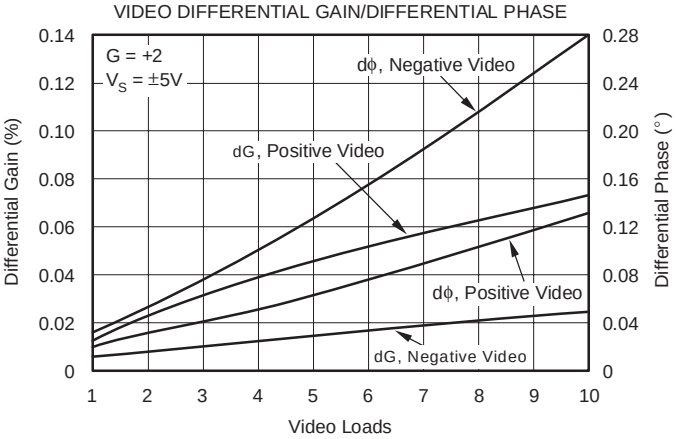
OPEN−LOOP GAIN AND PHASE



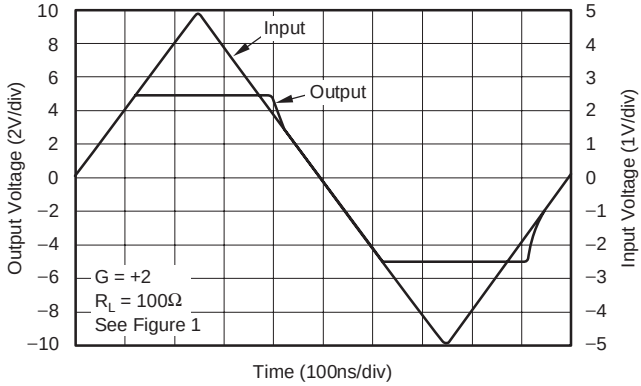
CLOSED−LOOP OUTPUT IMPEDANCE vs FREQUENCY



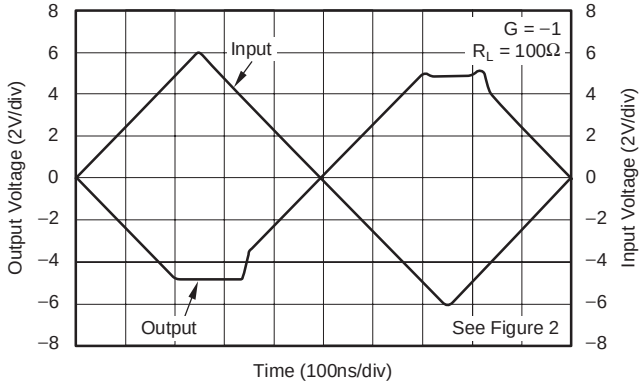
VIDEO DIFFERENTIAL GAIN/DIFFERENTIAL PHASE



NONINVERTING OVERDRIVE RECOVERY



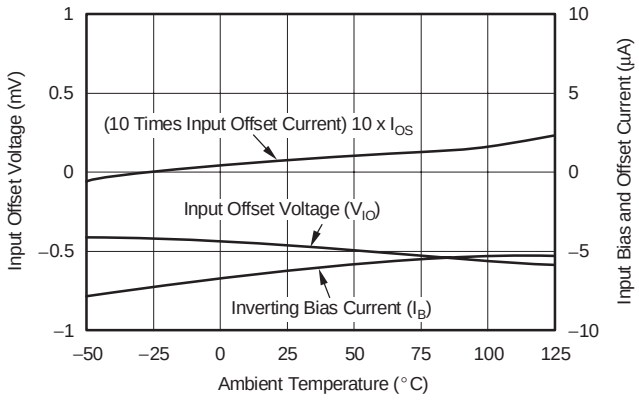
INVERTING OVERDRIVE RECOVERY



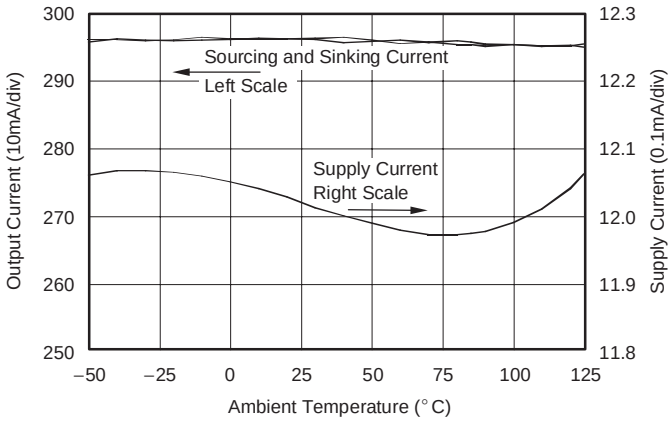
TYPICAL CHARACTERISTICS: V_S = ±6V (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

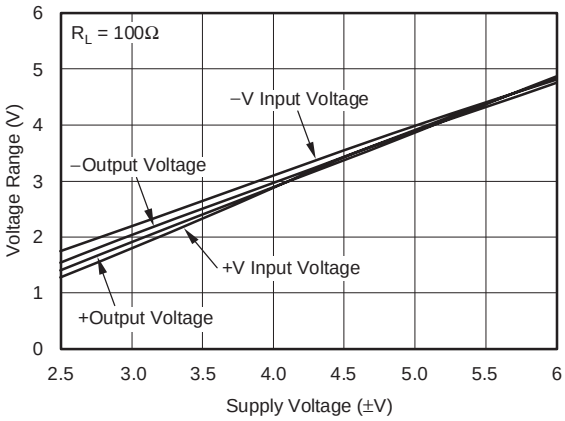
TYPICAL DC DRIFT OVER TEMPERATURE



SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



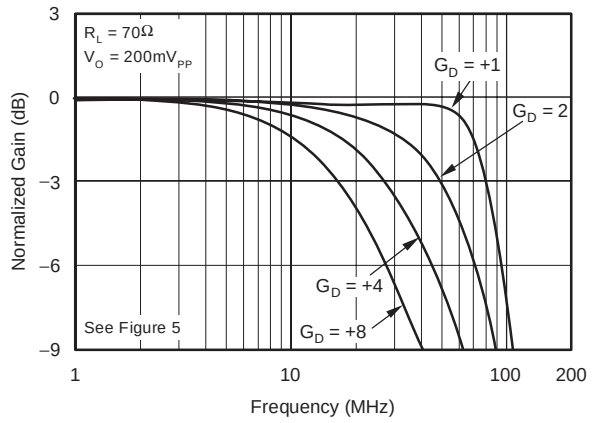
COMMON−MODE INPUT RANGE AND OUTPUT SWING vs SUPPLY VOLTAGE



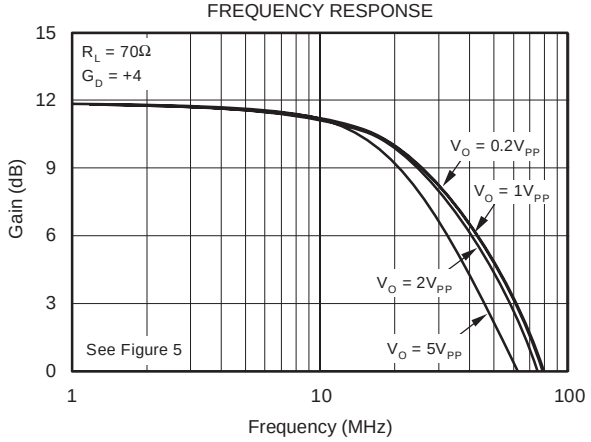
TYPICAL CHARACTERISTICS: V_S = ±6V, Differential Configuration

At T_A = +25°C, Differential Gain = 4, R_F = 402Ω, and R_L = 70Ω, unless otherwise noted. See Figure 5 for AC performance only.

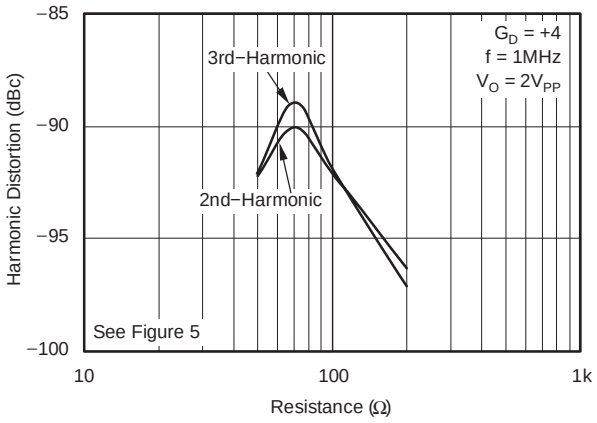
DIFFERENTIAL SMALL−SIGNAL FREQUENCY RESPONSE



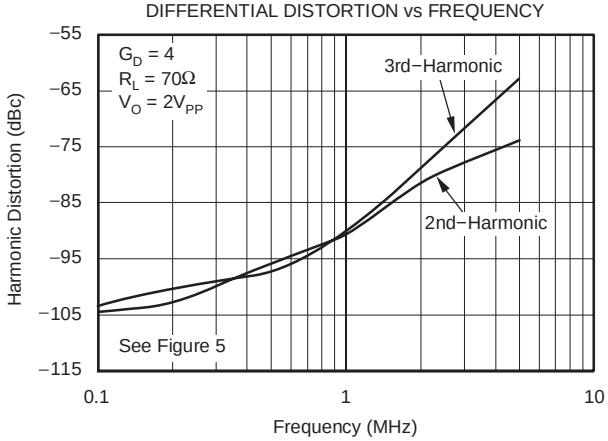
DIFFERENTIAL LARGE−SIGNAL FREQUENCY RESPONSE



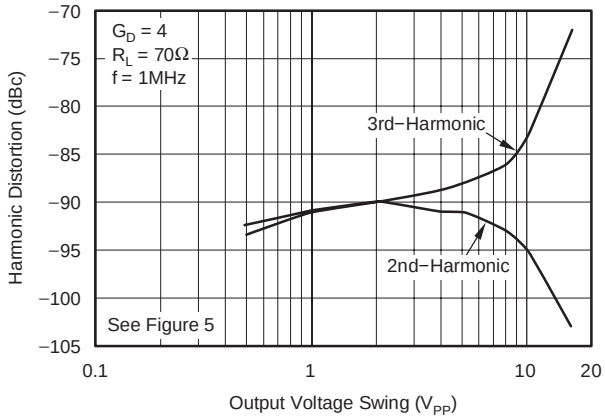
DIFFERENTIAL DISTORTION vs LOAD RESISTANCE



DIFFERENTIAL DISTORTION vs FREQUENCY



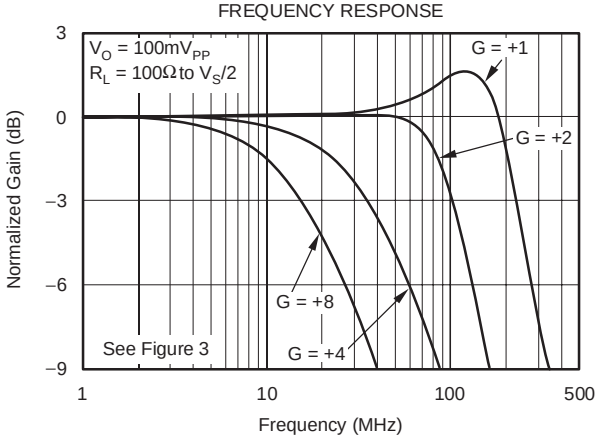
DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE



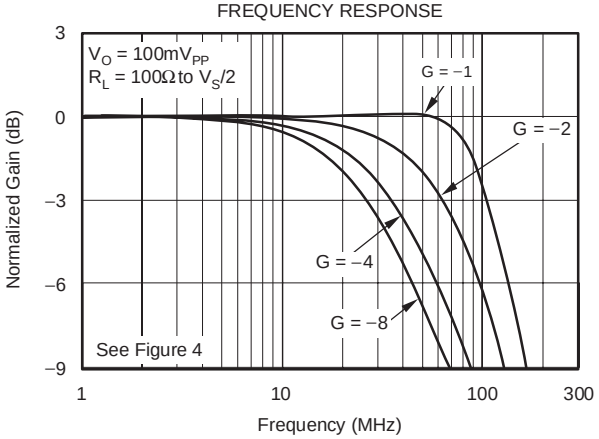
TYPICAL CHARACTERISTICS: V_S = +5V

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

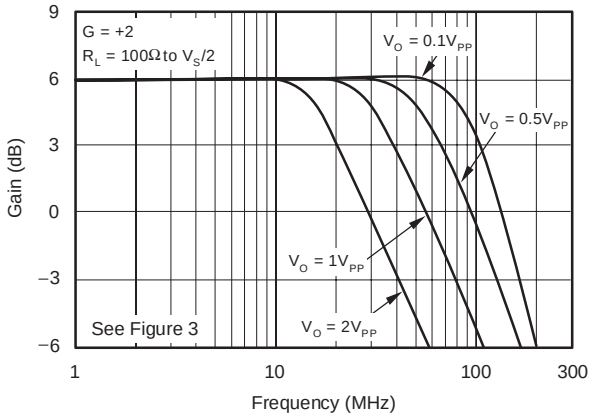
NONINVERTING SMALL−SIGNAL FREQUENCY RESPONSE



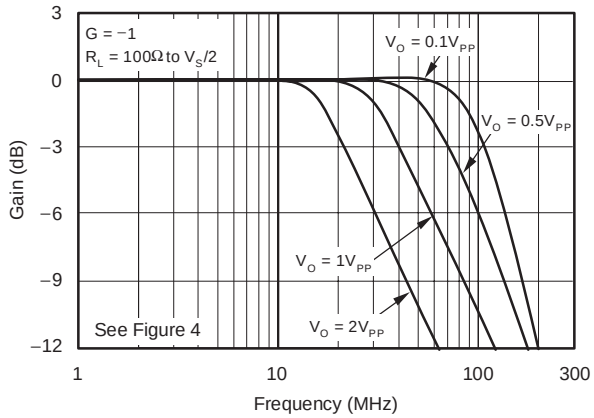
INVERTING SMALL−SIGNAL FREQUENCY RESPONSE



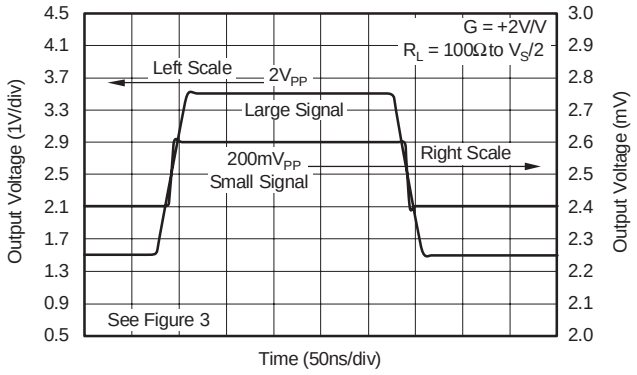
NONINVERTING LARGE−SIGNAL FREQUENCY RESPONSE



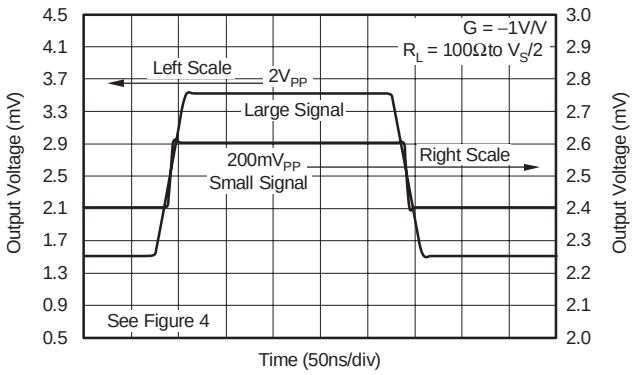
INVERTING LARGE−SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



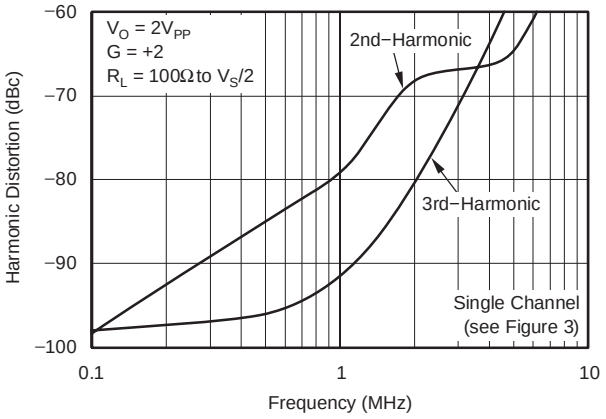
INVERTING PULSE RESPONSE



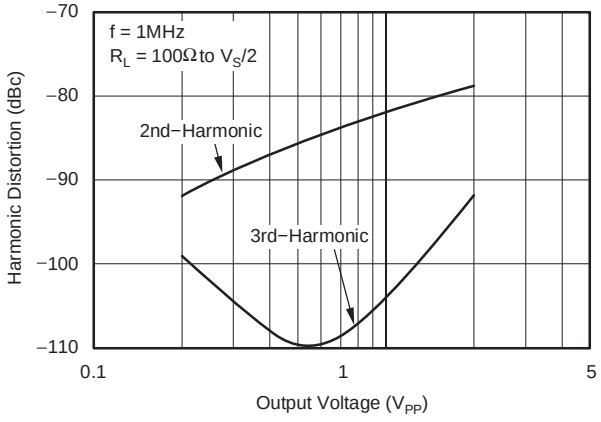
TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted.

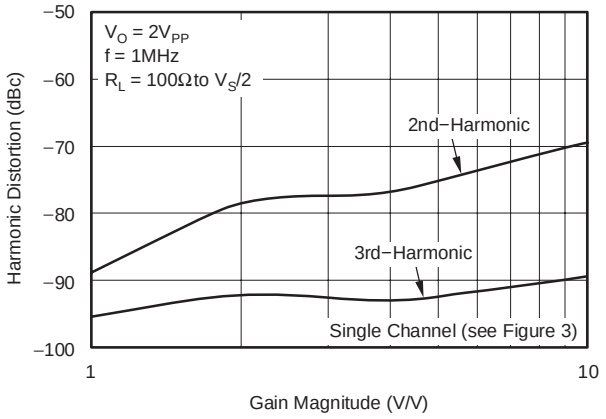
HARMONIC DISTORTION vs FREQUENCY



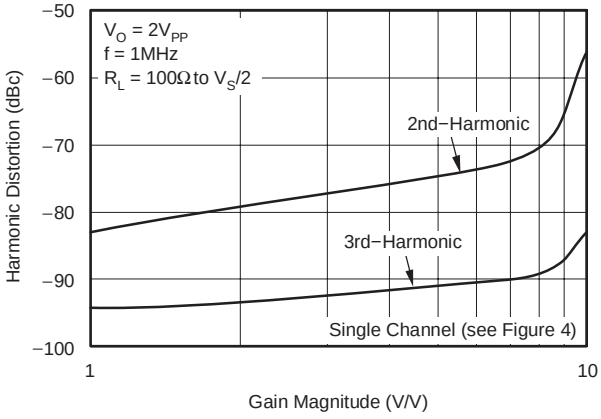
HARMONIC DISTORTION vs OUTPUT VOLTAGE



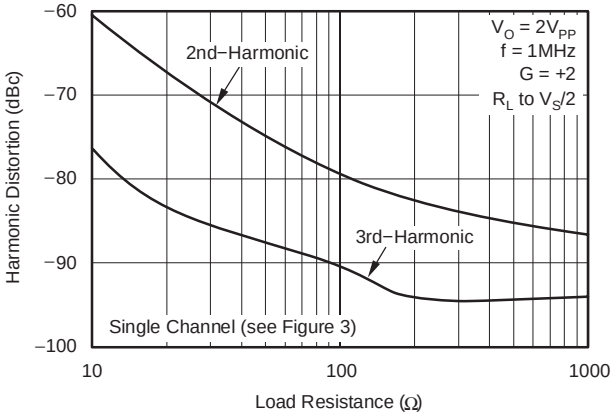
HARMONIC DISTORTION vs NONINVERTING GAIN



HARMONIC DISTORTION vs INVERTING GAIN

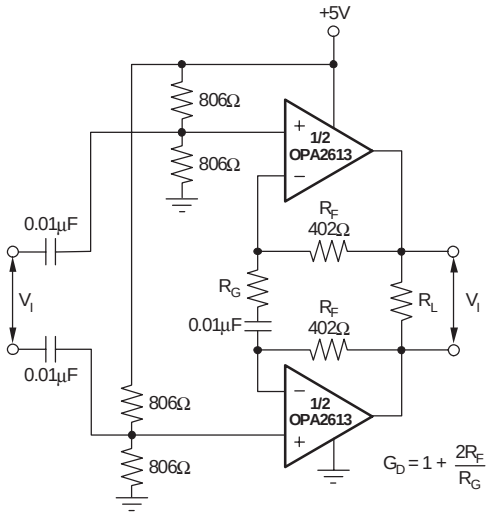


HARMONIC DISTORTION vs LOAD RESISTANCE

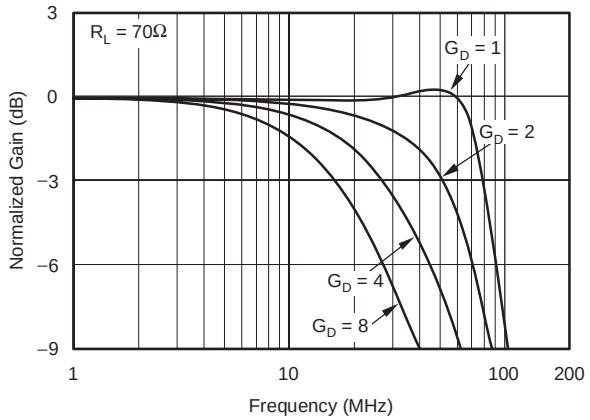


TYPICAL CHARACTERISTICS: V_S = +5V, Differential Configuration

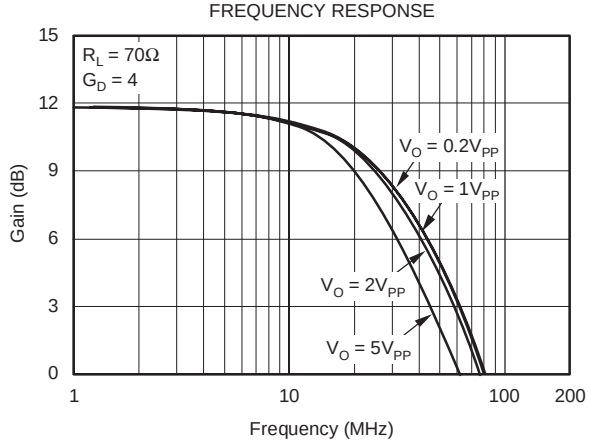
At T_A = +25°C, G_D = 4, R_F = 402Ω, and R_L = 70Ω, unless otherwise noted.



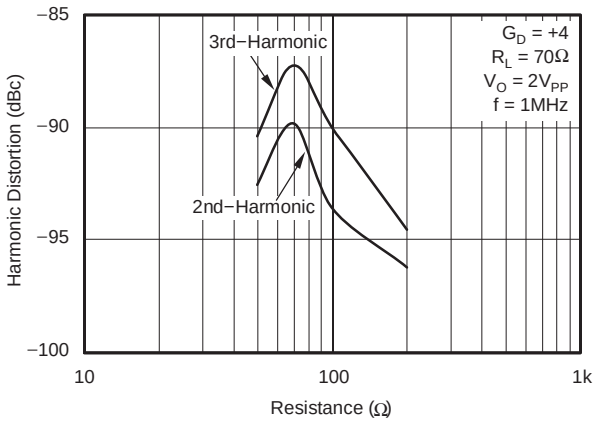
DIFFERENTIAL SMALL−SIGNAL FREQUENCY RESPONSE



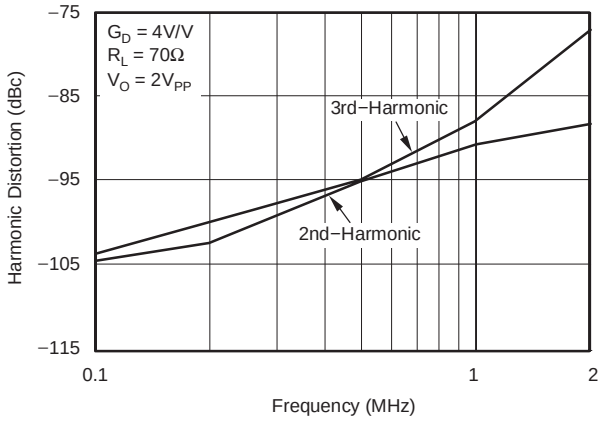
DIFFERENTIAL LARGE−SIGNAL FREQUENCY RESPONSE



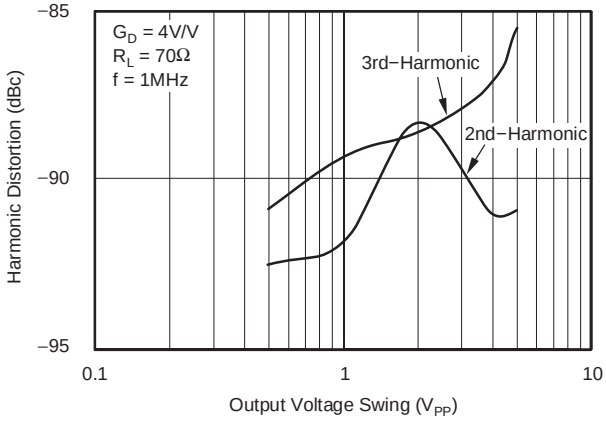
DIFFERENTIAL DISTORTION vs LOAD RESISTANCE



DIFFERENTIAL DISTORTION vs FREQUENCY



DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE



APPLICATION INFORMATION

WIDEBAND VOLTAGE-FEEDBACK OPERATION

The OPA2613 gives the exceptional AC performance of a wideband voltage-feedback op amp with a highly linear, high-power output stage. Requiring only 6mA/ch quiescent current, the OPA2613 swings to within 1.0V of either supply rail and delivers in excess of 280mA at room temperature. This low-output headroom requirement, along with supply voltage independent biasing, gives remarkable single (+5V) supply operation. The OPA2613 delivers greater than 20MHz bandwidth driving a $2V_{PP}$ output into 100Ω on a single +5V supply. Previous boosted output stage amplifiers typically suffer from very poor crossover distortion as the output current goes through zero. The OPA2613 achieves exceptional power gain with much better linearity. Figure 1 shows the DC-coupled, gain of +2, dual power-supply circuit configuration used as the basis of the ±6V Electrical and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground; and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the electrical characteristics are taken directly at the input and output pins, whereas load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 1, the total effective load is 100Ω || 804Ω = 89Ω.

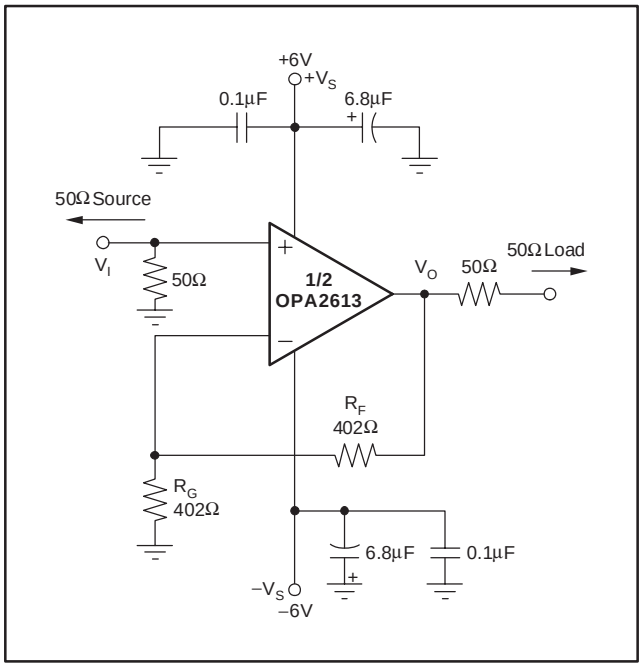


Figure 1. DC-Coupled, G = +2, Bipolar Supply, Specification and Test Circuit

Figure 2 shows the DC-coupled, bipolar supply circuit configuration used as the basis for the Inverting Gain −1V/V Typical Characteristics. Key design considerations of the inverting configuration are developed in the *Inverting Amplifier Operation* section.

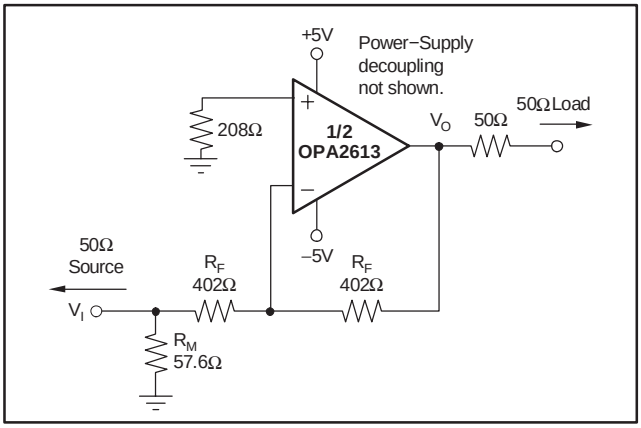


Figure 2. DC-Coupled, G = −1, Bipolar Supply, Specification and Test Circuit

Figure 3 shows the AC-coupled, gain of +2, single-supply circuit configuration used as the basis of the +5V Electrical and Typical Characteristics. Though not a *rail-to-rail* design, the OPA2613 requires minimal input and output voltage headroom compared to other very wideband voltage-feedback op amps. It will deliver a $2.6V_{PP}$ output swing on a single +5V supply with greater than 20MHz bandwidth. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the usable voltage ranges at both the input and the output. The circuit of Figure 3 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 806Ω resistors). The input signal is then AC-coupled into this midpoint voltage bias. The input voltage can swing to within 1.4V of either supply pin, giving a $2.2V_{PP}$ input signal range centered between the supply pins. The input impedance matching resistor (57.6Ω) used for testing is adjusted to give a 50Ω input match when the parallel combination of the biasing divider network is included. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of +1—which puts the input DC bias voltage (2.5V) on the output as well. Again, on a single +5V supply, the output voltage can swing to within 1.1V of either supply pin while delivering more than 100mA output current. A demanding 100Ω load to a midpoint bias is used in this characterization circuit. The new output stage used in the OPA2613 can deliver large bipolar output currents into this midpoint load with minimal crossover distortion, as shown by the +5V supply, harmonic distortion plots.

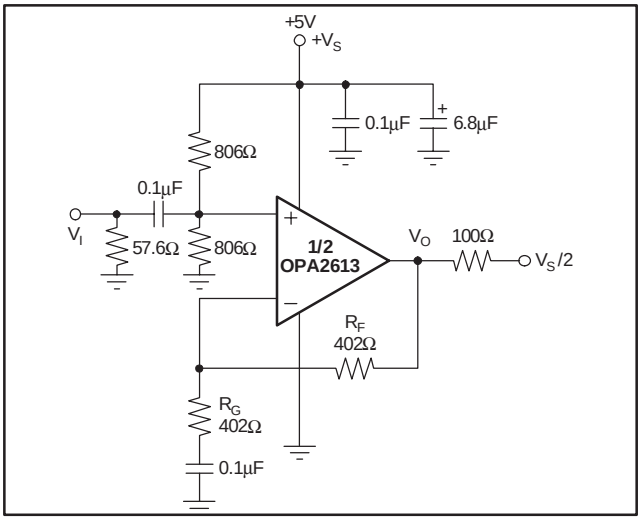


Figure 3. AC-Coupled, G = +2, Single-Supply, Specification and Test Circuit

The last configuration used as the basis of the +5V Electrical and Typical Characteristics is shown in Figure 4. Design considerations for this inverting, bipolar supply configuration are covered either in single-supply configuration (as shown in Figure 3) or in the *Inverting Amplifier Operation* section.

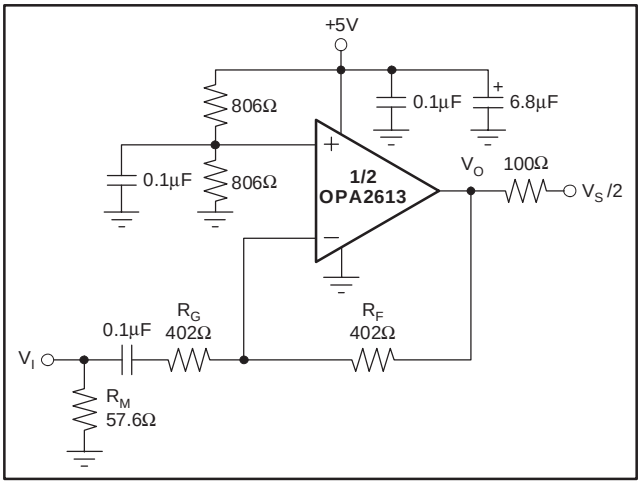


Figure 4. AC-Coupled, G = −1, Single-Supply, Specification and Test Circuit

DIFFERENTIAL INTERFACE APPLICATIONS

Dual op amps are particularly suitable to differential input to differential output applications. Typically, these fall into either Analog-to-Digital Converter (ADC) input interface or line driver applications. Two basic approaches to differential I/O are noninverting or inverting configurations. Since the output is differential, the signal polarity is somewhat meaningless—the noninverting and inverting terminology applies here to where the input is brought into the OPA2613. Each has its advantages and disadvantages. Figure 5 shows a basic starting point for noninverting input differential I/O applications.

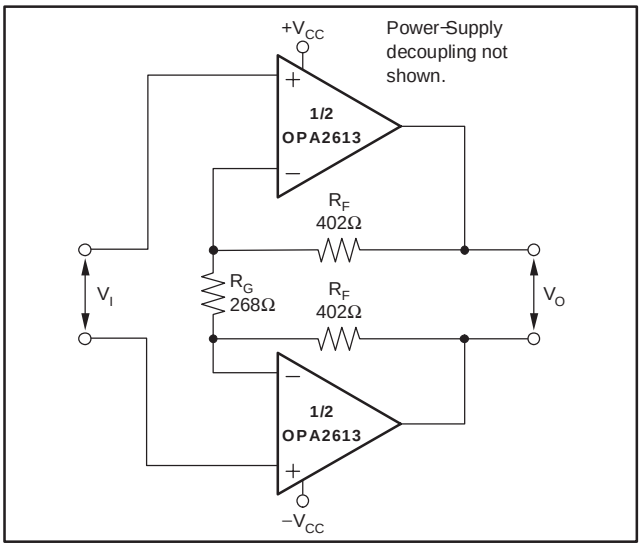


Figure 5. Noninverting Differential I/O Amplifier

This approach provides for a source termination impedance that is independent of the signal gain. For instance, simple differential filters may be included in the signal path right up to the noninverting inputs without interacting with the gain setting. The differential signal gain for the circuit of Figure 5 is:

$$A_D = 1 + 2 \times \frac{R_F}{R_G} \quad (1)$$

Since the OPA2613 is a voltage-feedback (VFB) amplifier, its bandwidth is principally controlled by the noise gain. The equivalent noise gain for Figure 5 is:

$$1 + 2 \times \frac{402\Omega}{268\Omega} = 4V/V \quad (2)$$

Various combinations of single-supply or AC-coupled gain can also be delivered using the basic circuit of Figure 5. Common-mode bias voltages on the two noninverting inputs pass on to the output with a gain of 1 since an equal DC voltage at each inverting node creates no current through R_G. This circuit does show a common-mode gain of 1 from input to output. The source connection should either remove this common-mode signal if undesired (using an input transformer can provide this function), or the common-mode voltage at the inputs can be used to set the output common-mode bias. If the low common-mode rejection of this circuit is a problem, the output interface may also be used to reject that common-mode. For instance, most modern differential input ADCs reject common-mode signals very well, while a line driver application through a transformer will also remove the common-mode signal through to the line.

SINGLE-SUPPLY ADSL UPSTREAM DRIVER

Figure 6 shows an example of a single-supply ADSL upstream driver. The dual OPA2613 is configured as a differential gain stage to provide signal drive to the primary of the transformer (here, a step-up transformer with a turns ratio of 1:2). The main advantage of this configuration is the cancellation of all even harmonic distortion products. Another important advantage for ADSL is that each amplifier needs only to swing half of the total output required driving the load.

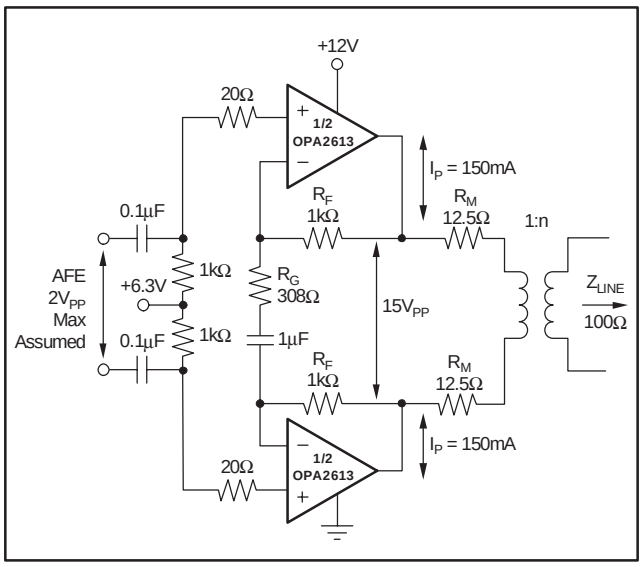


Figure 6. Single-Supply ADSL Upstream Driver

The analog front-end (AFE) signal is AC-coupled to the driver, and the noninverting input of each amplifier is biased slightly above the mid-supply voltage (+6.3V in this case). In addition to providing the proper biasing to the amplifier, this approach also provides a high-pass filtering with a corner frequency, set here at 1.6kHz. As the upstream signal bandwidth starts at 26kHz, this high-pass filter does not generate any problems and has the advantage of filtering out unwanted lower frequencies.

The input signal is amplified with a gain set by the following equation:

$$G_D = 1 + \frac{2 \times R_F}{R_G} \quad (3)$$

With R_F = 1kΩ and R_G = 308Ω, the gain for this differential amplifier is 7.5. This gain boosts the AFE signal, assumed to be a maximum of $2V_{PP}$, to a maximum of $15V_{PP}$.

The two back-termination resistors (12.5Ω each) added at each input of the transformer make the impedance of the modem match the impedance of the phone line, and also provide a means of detecting the received signal for the receiver. The value of these resistors (R_M) is a function of the line impedance and the transformer turns ratio (n), given by the following equation:

$$R_M = \frac{Z_{LINE}}{2n^2} \quad (4)$$

LINE DRIVER HEADROOM MODEL

The first step in a transformer-coupled, twisted-pair driver design is to compute the peak-to-peak output voltage from the target specifications. This is done using the following equations:

$$P_L = 10 \times \log \frac{V_{RMS}^2}{(1mW) \times R_L} \quad (5)$$

With P_L power and V_{RMS} voltage at the load, and R_L load impedance, this gives the following:

$$V_{RMS} = \sqrt{(1mW) \times R_L \times 10^{\frac{P_L}{10}}} \quad (6)$$

$$V_P = \text{Crest Factor} \times V_{RMS} = CF \times V_{RMS} \quad (7)$$

with V_P peak voltage at the load and CF Crest Factor.

$$V_{LPP} = 2 \times CF \times V_{RMS} \quad (8)$$

with V_{LPP}: peak-to-peak voltage at the load.

Consolidating Equations 4 through 7 allows expressing the required peak-to-peak voltage at the load as a function of the crest factor, the load impedance, and the power at the load. Thus,

$$V_{LPP} = 2 \times CF \times \sqrt{(1mW) \times R_L \times 10^{\frac{P_L}{10}}} \quad (9)$$

This V_{LPP} is usually computed for a nominal line impedance and may be taken as a fixed design target.

The next step for the driver is to compute the individual amplifier output voltage and currents as a function of V_{PP} on the line and transformer turns ratio. As the turns ratio changes, the minimum allowed supply voltage changes along with it. The peak current in the amplifier output is given by:

$$\pm I_P = \frac{1}{2} \times \frac{2 \times V_{LPP}}{n} \times \frac{1}{4R_M} \quad (10)$$

With V_{LPP} as defined in Equation 8, and R_M as defined in Equation 4 and shown in Figure 7.

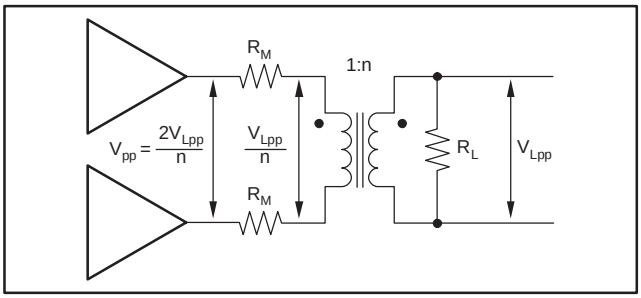


Figure 7. Driver Peak Output Voltage

With the previous information available, it is now possible to select a supply voltage and the turns ratio desired for the transformer as well as calculate the headroom for the OPA2613.

The model (shown in Figure 8) can be described with the following set of equations:

1. First, as available output swing:

$$V_{PP} = V_{CC} - (V_1 + V_2) - I_P \times (R_1 + R_2) \quad (11)$$

2. Or as required supply voltage:

$$V_{CC} = V_{PP} + (V_1 + V_2) + I_P \times (R_1 + R_2) \quad (12)$$

The minimum supply voltage for a power and load requirement is given by Equation 11.

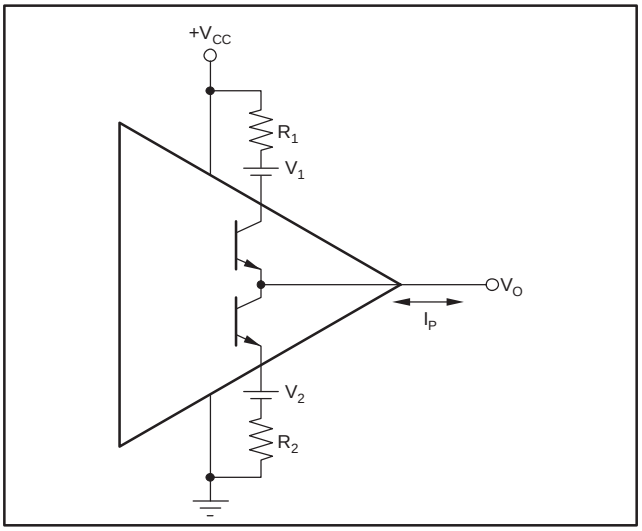


Figure 8. Line Driver Headroom Model

V_1, V_2, R_1, and R_2 are given in Table 1 for both +12V and +5V operation.

Table 1. Line Driver Headroom Model Values

	V_1	R_1	V_2	R_2
+5V	1.0V	2Ω	1.0V	5.5Ω
+12V	1.0V	2Ω	1.0V	5.5Ω

TOTAL DRIVER POWER FOR xDSL APPLICATIONS

The total internal power dissipation for the OPA2613 in an xDSL line driver application will be the sum of the quiescent power and the output stage power. The OPA2613 holds a relatively constant quiescent current versus supply voltage—giving a power contribution that is simply the quiescent current times the supply voltage used (the supply voltage will be greater than the solution given in Equation 12). The total output stage power may be computed with reference to Figure 9.

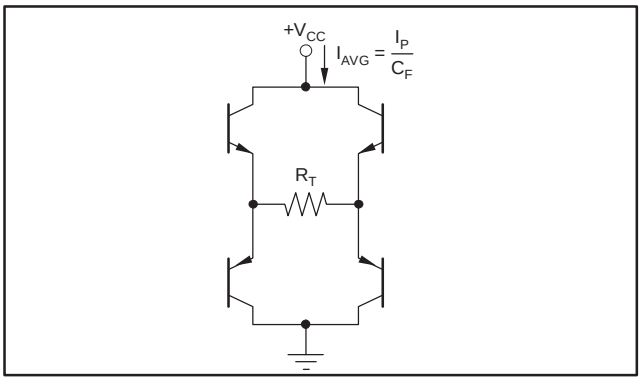


Figure 9. Output Stage Power Model

The two output stages used to drive the load of Figure 7 can be seen as an H-Bridge in Figure 9. The average current drawn from the supply into this H-Bridge and load will be the peak current in the load given by Equation 10 divided by the crest factor (CF) for the xDSL modulation. This total power from the supply is then reduced by the power in R_T to leave the power dissipated internal to the drivers in the four output stage transistors. That power is simply the target line power used in Equation 5 plus the power lost in the matching elements (R_M). In the examples here, a perfect match is targeted giving the same power in the matching elements as in the load. The output stage power is then set by Equation 13.

$$P_{OUT} = \frac{I_P}{CF} \times V_{CC} - 2P_L \quad (13)$$

The total amplifier power is then:

$$P_{TOT} = I_q \times V_{CC} + \frac{I_P}{CF} \times V_{CC} - 2P_L \quad (14)$$

For the ADSL CPE upstream driver design of Figure 6, the peak current is 150mA for a signal that requires a crest factor of 5.33 with a target line power of 13dBm into 100Ω (20mW). With a typical quiescent current of 12mA and a nominal supply voltage of +12V, the total internal power dissipation for the solution of Figure 6 will be:

$$P_{TOT} = 12mA(12V) + \frac{150mA}{5.33}(12V) - 2(20mW) = 400mW \quad (15)$$

DESIGN-IN TOOLS

DEMONSTRATION FIXTURE

A printed circuit board (PCB) is available to assist in the initial evaluation of circuit performance using the OPA2613. The fixture is offered free of charge as an unpopulated PCB, delivered with a user's guide. The summary information for this fixture is shown in Table 2.

Table 2. Demonstration Fixture

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA2613ID	SO-8	DEM-OPA-SO-2A	SBOU003

The demonstration fixture can be requested at the Texas Instruments web site (www.ti.com) through the OPA2613 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA2613 is available through the TI web site (www.ti.com). This model does a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions, but does not do as well in predicting the harmonic distortion or video d_G/d_P characteristics. This model does not attempt to distinguish between the package types in small-signal AC performance, nor does it attempt to simulate channel-to-channel coupling.

INVERTING AMPLIFIER OPERATION

As the OPA2613 is a general-purpose, wideband voltage-feedback op amp, most of the familiar op amp application circuits are available to the designer. Wideband inverting operation is particularly suited to the OPA2613. Figure 10 shows a typical inverting configuration where the I/O impedances and signal gain from Figure 1 are retained in an inverting circuit configuration.

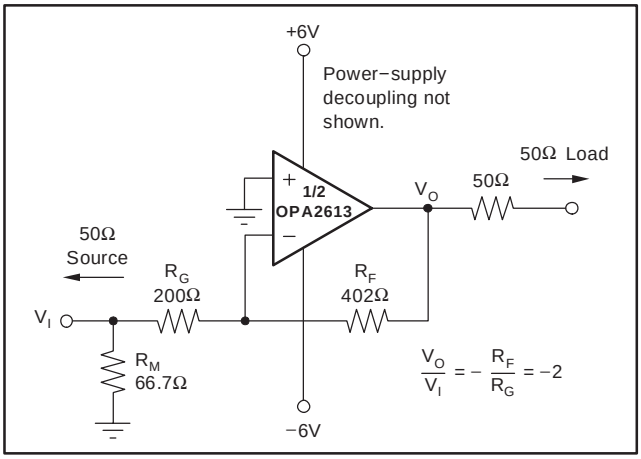


Figure 10. Inverting Gain of −1 with Impedance Matching

In the inverting configuration, two key design considerations must be noted. The first is that the gain resistor (R_G) becomes part of the input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted-pair, long PC board trace, or other transmission line conductor), it is normally necessary to add an additional matching resistor to ground. R_G, by itself, is not normally set to the required input impedance since its value, along with the desired gain, will determine an R_F, which may be non-optimal from a frequency response standpoint. The total input impedance for the source becomes the parallel combination of R_G and R_M.

The second major consideration, touched on in the previous paragraph, is that the signal source impedance becomes part of the noise gain equation and has an effect on the bandwidth. In the example of Figure 10, the R_M value combines in parallel with the external 50Ω source impedance, yielding an effective driving impedance of 50Ω || 66.7Ω = 28.6Ω. This impedance is added in series with R_G for calculating the noise gain—which gives NG = 2.76. Note that the noninverting input in this bipolar supply inverting application is connected to ground through a 146Ω resistor. It is often suggested that an additional resistor be connected to ground on the noninverting input to achieve bias current error cancellation at the output.

OUTPUT CURRENT AND VOLTAGE

The OPA2613 provides output voltage and current capabilities that are unsurpassed in a low-cost dual monolithic op amp. Under no-load conditions at 25°C, the output voltage typically swings closer than 1V to either supply rail; tested at +25°C, swing limit is within 1.1V of either rail. Into a 12Ω load (the minimum tested load), it delivers more than ±280mA continuous output current.

The specifications described previously, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage times current (or V-I product) that is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* plot in the Typical Characteristics. The X and Y axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA2613 output drive capabilities, noting that the graph is bounded by a safe operating area of 1W maximum internal power dissipation (in this case, for one channel only). Superimposing resistor load lines onto the plot shows that the OPA2613 can drive +4.8 and −4.1 into 25Ω without exceeding the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test circuit load) shows the full ±4.9V output swing capability, as shown in the Electrical Characteristics tables. The minimum specified output voltage and current over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the Electrical Characteristics tables. As the output transistors deliver power, the junction temperatures increase, decreasing the V_{BE}s (increasing the available output voltage swing), and increasing the current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications, since the output stage junction temperatures will be higher than the minimum specified operating ambient.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance that may be recommended to improve the ADC linearity. A high-speed, high open-loop gain amplifier like the OPA2613 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested.

When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability. The Typical Characteristics show the Recommended R_S vs Capacitive Load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA2613. Long PCB traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA2613 output pin (see the *Board Layout Guidelines* section).

The very high output current and unity gain stability for the OPA2613 can be used to drive large capacitive loads with moderate slew rates. An example is shown in Figure 11 where a 5000pF load cap is driven with a 1MHz square wave to give a ±5V swing. The supplies were slightly increased to give more headroom for the charging current through the 2Ω isolation resistor.

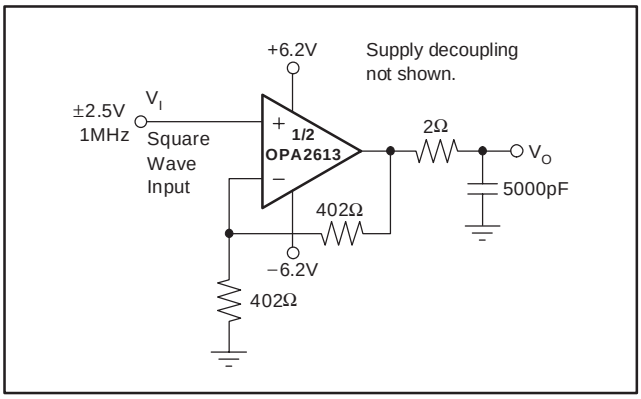


Figure 11. Large Capacitive Load Driver

Figure 12 shows a comparison of 2 × Input voltage to the capacitor voltage. The transition time is set by the 70V/µs slew rate for the OPA2613. For this controlled dV/dT, the charging current into the 5000pF load will be given by:

Slew Rate = I_P/C

Solving for I_P gives:

$$I_P = 5000pF \times 70V/\mu s = 350mA \text{ peak current} \quad (16)$$

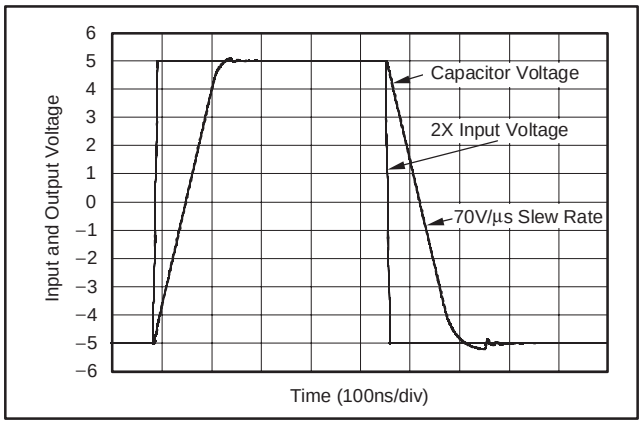


Figure 12. Large-Signal Capacitive Load Drive

At these larger capacitive loads, very low series R will maintain stability—but some R is always required.

DISTORTION PERFORMANCE

The OPA2613 provides good distortion performance into a 100Ω load on ±6V supplies. Generally, until the fundamental signal reaches high frequency or power levels, the 2nd-harmonic dominates the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration (see Figure 1), this is the sum of $R_F + R_G$, whereas in the inverting configuration, it is just R_F. Also, providing an additional supply decoupling capacitor (0.01µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. The Typical Characteristics show the 2nd-harmonic increasing at a little less than the expected 2x rate whereas the 3rd-harmonic increases at a little less than the expected 3x rate. Where the test power doubles, the difference between it and the 2nd-harmonic decreases less than the expected 6dB, whereas the difference between it and the 3rd-harmonic decreases by less than the expected 12dB. Operating differentially will suppress the 2nd-order harmonics below the 3rd.

Operating as a differential I/O stage will also suppress the 2nd-harmonic distortion.

NOISE PERFORMANCE

Wideband voltage-feedback op amps generally have a lower output noise than comparable current-feedback op amps. The OPA2613 offers an excellent balance between voltage and current noise terms to achieve low output noise. The input voltage noise (1.8nV/$\sqrt{Hz}$) is lower than most unity-gain stable, wideband voltage-feedback op amps. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 13 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

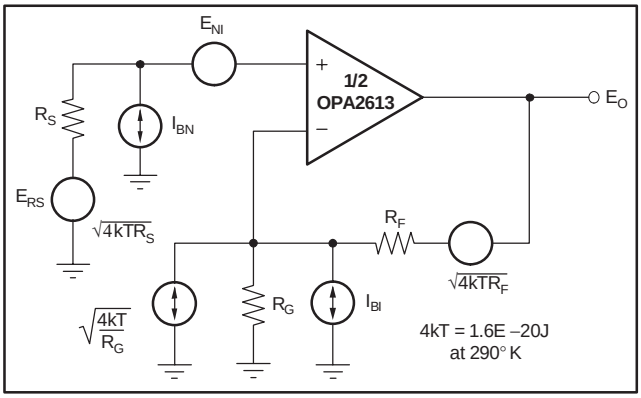


Figure 13. Op Amp Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 17 shows the general form for the output noise voltage using the terms given in Figure 13.

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN} \times R_S\right)^2 + 4kTR_S\right) NG^2 + \left(I_{BI} \times R_F\right)^2 + 4kTR_F NG} \quad (17)$$

Dividing this expression by the noise gain (NG = (1 + R_F/R_G)) gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 18.

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN} \times R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI} \times R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (18)$$

Evaluating these two equations for the OPA2613 circuit and component values (see Figure 1) gives a total output spot noise voltage of 6.34nV/$\sqrt{Hz}$ and a total equivalent input spot noise voltage of 3.2nV/$\sqrt{Hz}$. This total input referred spot noise voltage is higher than the 1.8nV/$\sqrt{Hz}$ specification for the op amp voltage noise alone. This reflects the noise added to the output by the inverting current noise times the feedback resistor.

DIFFERENTIAL NOISE PERFORMANCE

As the OPA2613 is used as a differential driver in xDSL applications, it is important to analyze the noise in such a configuration. Figure 14 shows the op amp noise model for the differential configuration.

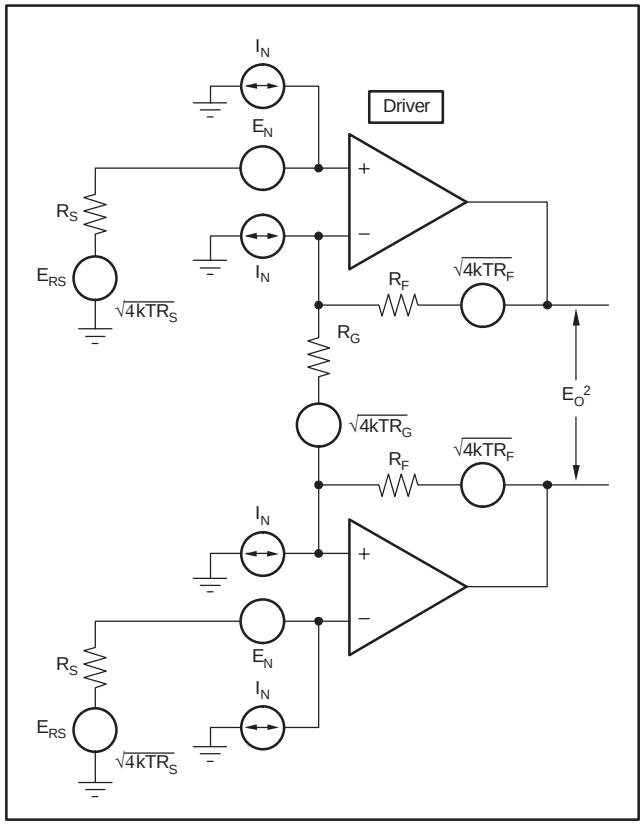


Figure 14. Differential Op Amp Noise Analysis Model

As a reminder, the differential gain is expressed as:

$$G_D = 1 + \frac{2 \times R_F}{R_G} \quad (19)$$

The output noise can be expressed as shown below:

(20)

$$e_O = \sqrt{2 \times G_D^2 \times \left(e_N^2 + \left(i_N \times R_S\right)^2 + 4kTR_S\right) + 2\left(i_I R_F\right)^2 + 2\left(4kTR_F G_D\right)}$$

Dividing this expression by the differential noise gain ($G_D = (1 + 2R_F/R_G)$) gives the equivalent input referred spot noise voltage at the noninverting input, as shown in Equation 21.

(21)

$$e_i = \sqrt{2 \times \left(e_N^2 + \left(i_N \times R_S\right)^2 + 4kTR_S\right) + 2\left(\frac{i_I R_F}{G_D}\right)^2 + 2\left(\frac{4kTR_F}{G_D}\right)}$$

Evaluating these equations for the OPA2613 ADSL circuit and component values of Figure 6 gives a total output spot noise voltage of 23.3nV/$\sqrt{Hz}$ and a total equivalent input spot noise voltage of 3.2nV/$\sqrt{Hz}$.

In order to minimize the output noise due to the noninverting input bias current noise, it is recommended to keep the noninverting source impedance as low as possible.

DC ACCURACY AND OFFSET CONTROL

The OPA2613 can provide excellent DC signal accuracy due to its high open-loop gain, high common-mode rejection, high power-supply rejection, and low input offset voltage and bias current offset errors. To take full advantage of the low input offset voltage (±1.0mV maximum at 25°C), careful attention to input bias current cancellation is also required. The high-speed input stage for the OPA2613 has relatively high input bias current (6µA typical into the pins) but with a very close match between the two input currents, typically 50nA input offset current. The total output offset voltage may be reduced considerably by matching the source impedances looking out of the two inputs. For example, one way to add bias current cancellation to the circuit of Figure 1 would be to insert a 175Ω series resistor into the noninverting input from the 50Ω terminating resistor. If the 50Ω source resistor is DC-coupled, this will increase the source impedance for the noninverting input bias current to 200Ω. Since this is now equal to the impedance looking out of the inverting input ($R_F \parallel R_G$), the circuit will cancel the bias current effects, leaving only the offset current times the feedback resistor as a residual DC error term at the output. Evaluating the configuration of Figure 1 adding a 175Ω in series with the noninverting input pin, using worst-case +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$V_{OFF} = \pm (NG \times V_{OS(MAX)}) \pm (I_{OS} \times R_F)$

where NG = noninverting signal gain

$= \pm (2 \times 1.0mV) \pm (402\Omega \times 300nA)$

$= \pm 2.0mV \pm 0.12mV$

$V_{OFF} = \pm 2.12mV$

THERMAL ANALYSIS

Due to the high output power capability of the OPA2613, heat-sinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature sets the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 150°C. Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipation in the output stage (P_{DL}) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the part. P_{DL} depends

on the required output signal and load, but for a grounded resistive load, P_{DL} is at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \times R_L)$ where R_L includes feedback network loading. Note that it is the power in the output stage and not into the load that determines internal power dissipation. As a worst-case example, compute the maximum T_J using an OPA2613 SO-8 in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C with both outputs driving a grounded 20Ω load to +3.0V.

$P_D = 12V \times 13.0mA + 2 \times [6^2/ (4 \times (20\Omega \;||\; 804\Omega))] = 1.\ 08W$

Maximum $T_J = +85°C + (1.08W \times 125°C/W) = 220°C$

This absolute worst-case condition exceeds specified maximum junction temperature. This extreme case is not normally encountered. Where high internal power dissipation is anticipated, consider the thermal slug package version. Under the same worst case conditions the junction temperature will drop to 139°C with the 50°C/W thermal impedance available using the PSO-8 package.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA2613 requires careful attention to board layout parasitic and external component types. Recommendations that optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25″) from the power-supply pins to high-frequency 0.1μF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections (on pins 4 and 7) should always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) improves 2nd-harmonic distortion performance. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at a lower frequency, should also be used on the main supply pins. These can be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components preserve the high-frequency performance of the OPA2613. Resistors should be of a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors can also provide good high-frequency performance. Again, keep the leads and PC board trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Although the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The 402Ω feedback resistor used in the Typical Characteristics at a gain of +2 on ±6V supplies is a good starting point for design.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of Recommended R_S vs Capacitive Load. Low parasitic capacitive loads (< 5pF) may not need an R_S because the OPA2613 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board; in fact, a higher impedance environment improves distortion (see the distortion versus load plots). With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA2613 is used, as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device.

This total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA2613 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of R_S vs Capacitive Load. However, this does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA2613 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2613 onto the board.

INPUT AND ESD PROTECTION

The OPA2613 is built using a high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices and are reflected in the absolute maximum ratings table. All device pins have limited ESD protection using internal diodes to the power supplies, as shown in Figure 15.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA2613), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible, because high values degrade both noise performance and frequency response.

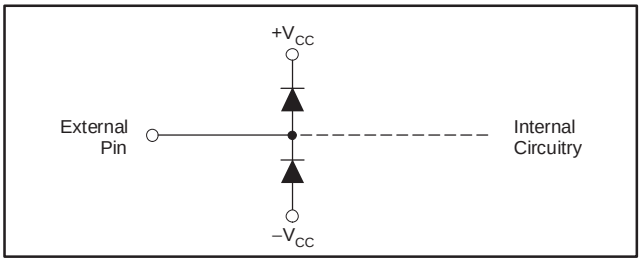


Figure 15. Internal ESD Protection

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
8/08	H	2	Absolute Maximum Ratings	Changed Storage Temperature minimum value from −40°C to −65°C.
9/07	G	—	—	Deleted all references to PSO−8 (OPA2613H) package.
		1	Description	Deleted last paragraph.
		25	Board Layout Guidelines	Deleted paragraph (F).

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2613ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2613	Samples
OPA2613IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2613	Samples
OPA2613IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 2613	Samples
OPA2613IDTJG3	OBSOLETE	HSOP	DTJ	8		TBD	Call TI	Call TI	-40 to 85		
OPA2613IDTJR	OBSOLETE	HSOP	DTJ	8		TBD	Call TI	Call TI	-40 to 85		
OPA2613IDTJRG3	OBSOLETE	HSOP	DTJ	8		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

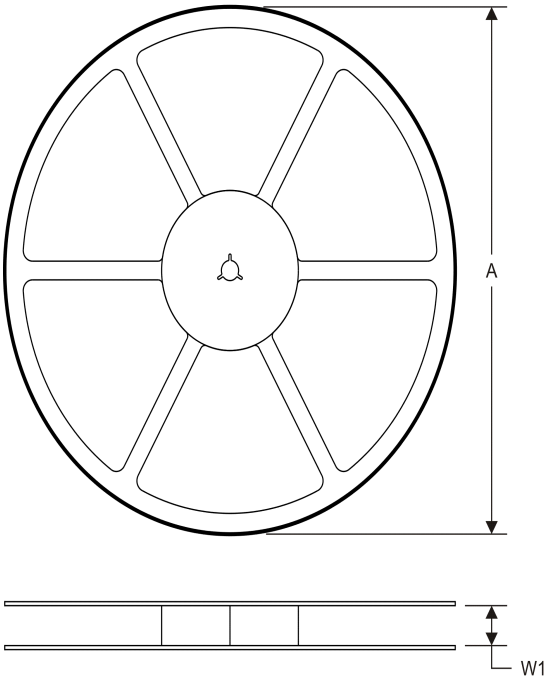
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

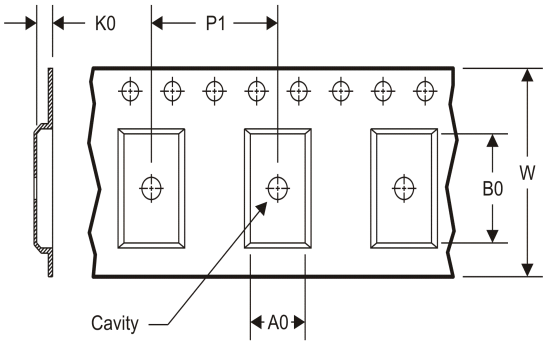
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



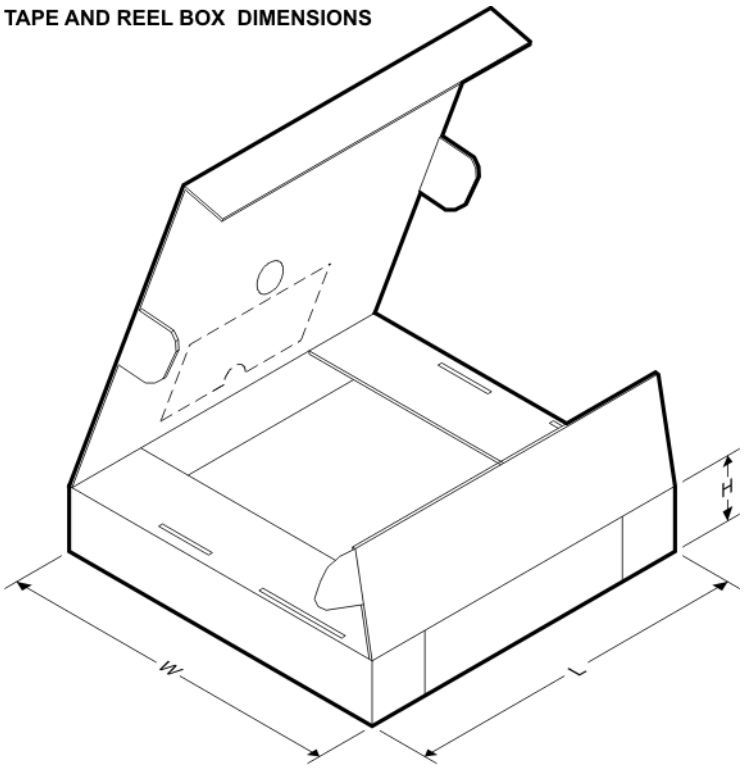
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2613IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

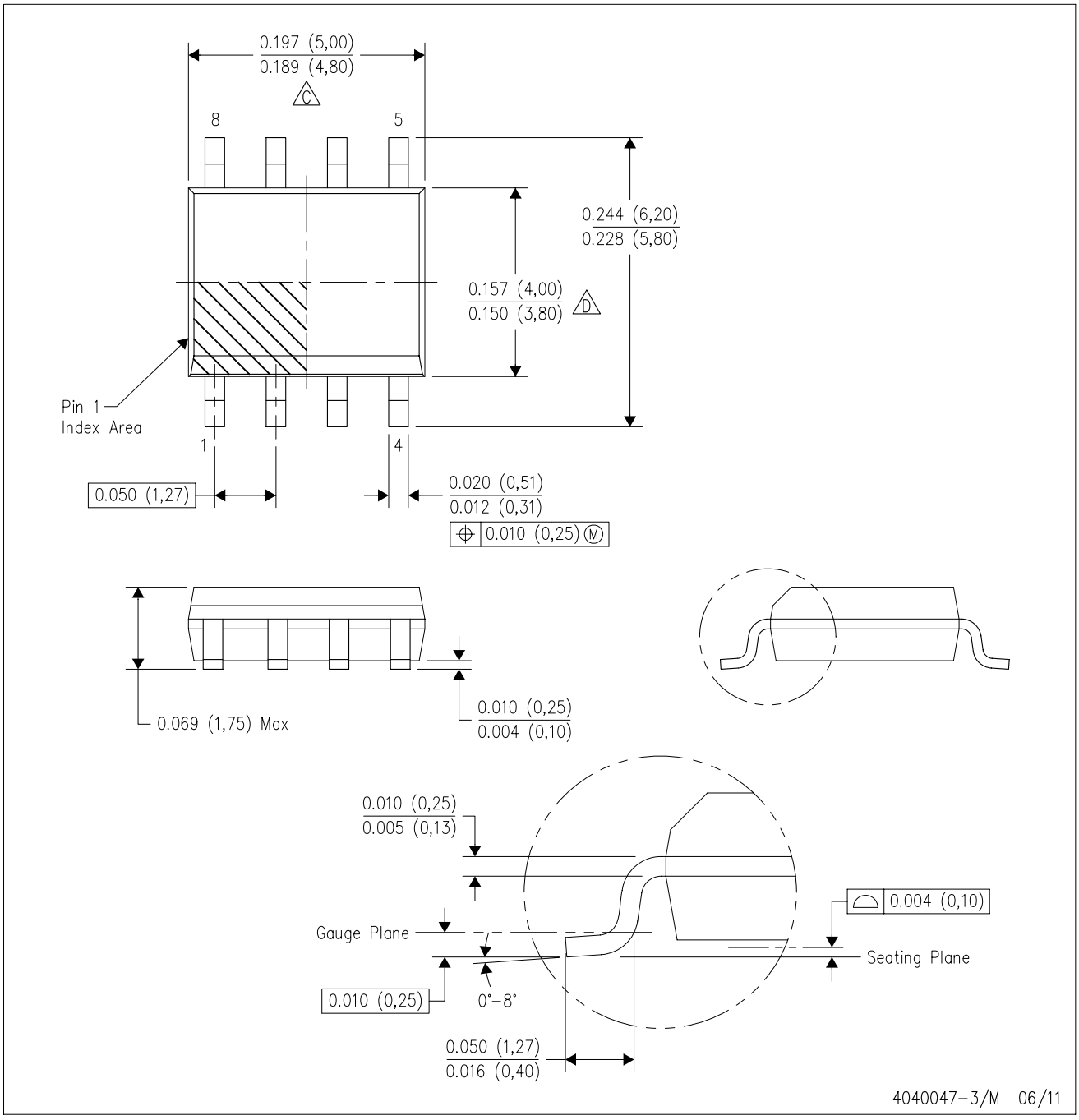
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

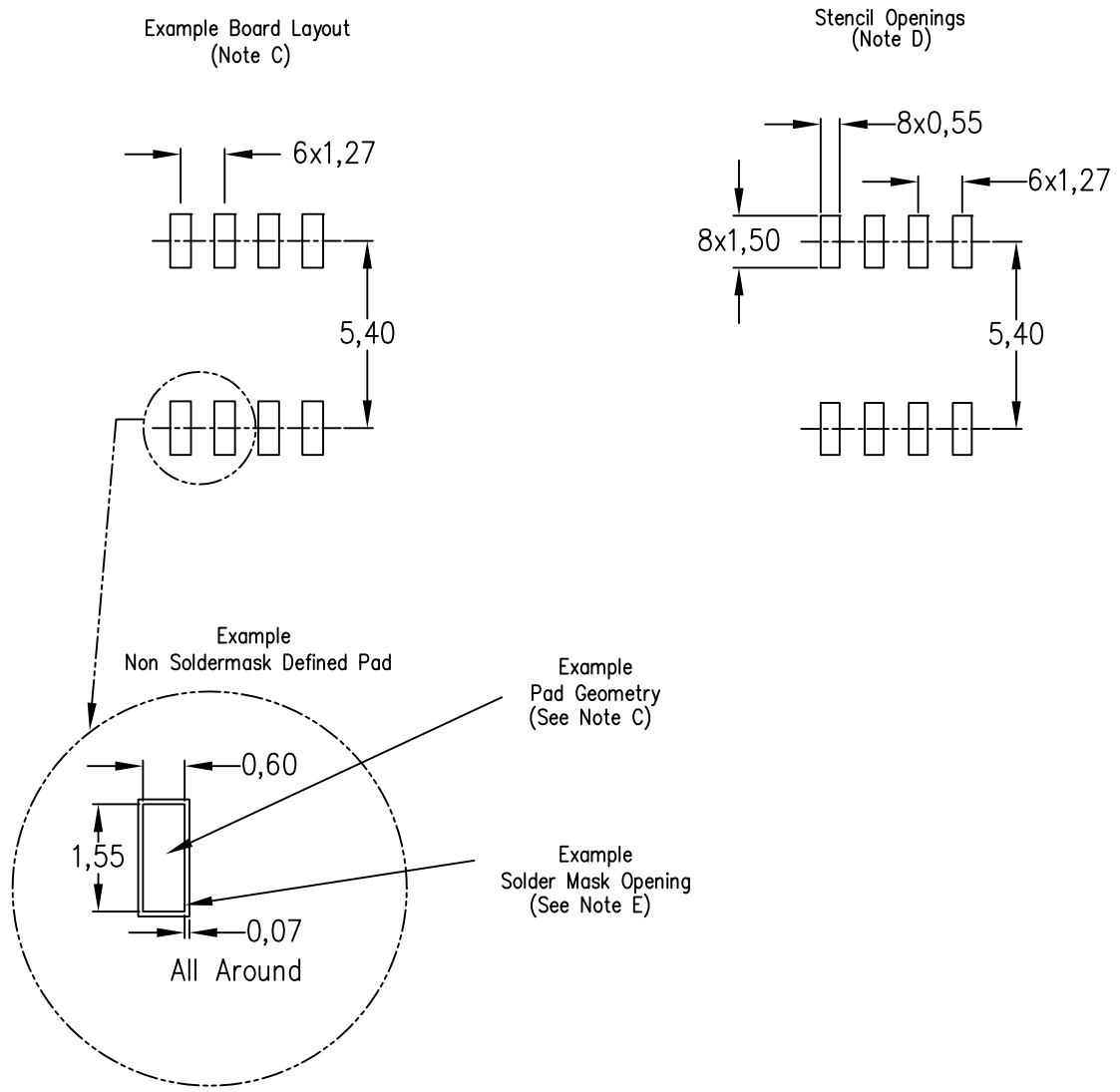
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2613IDR	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

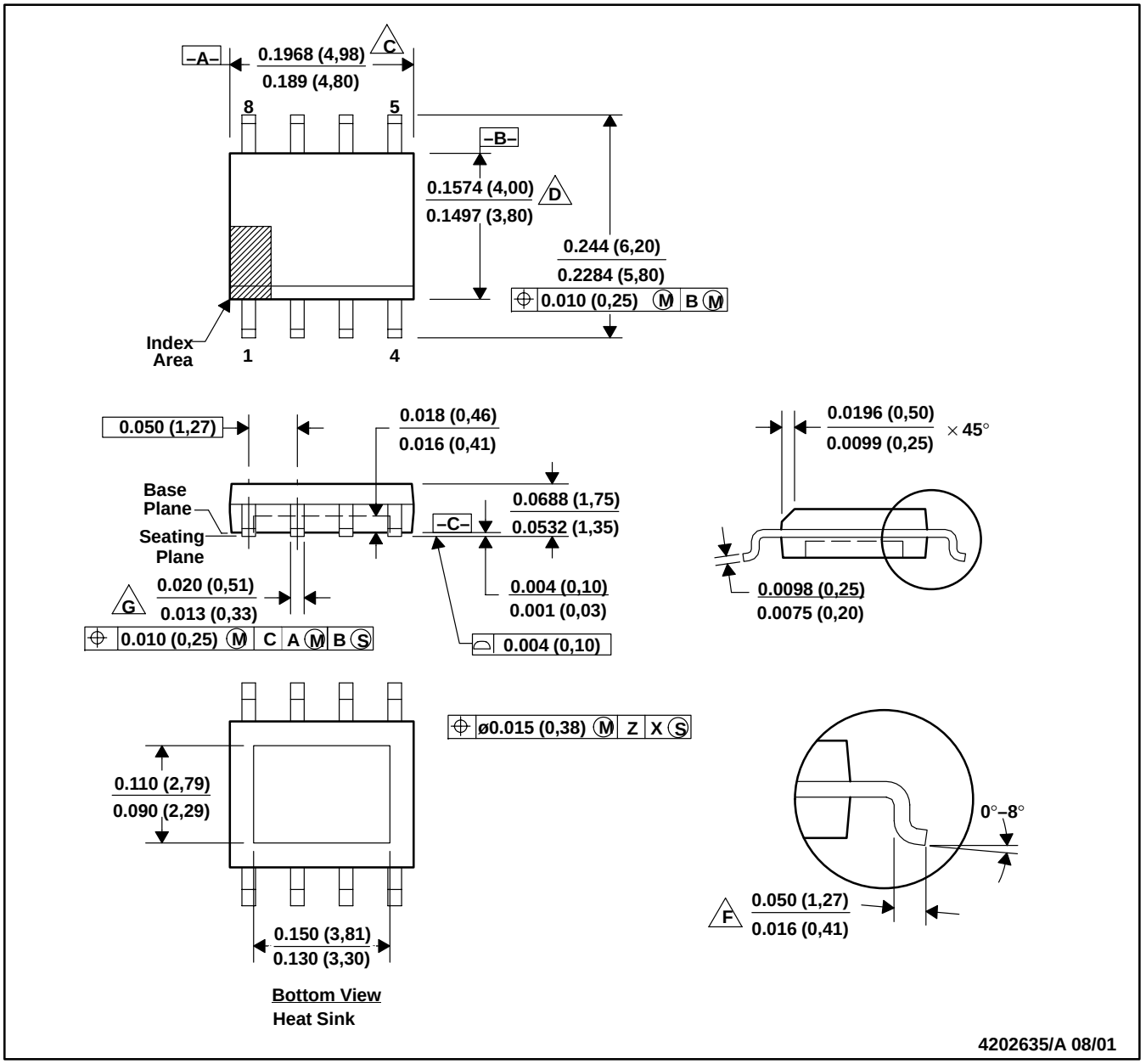
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MPDS100 – AUGUST 2001

DTJ (R-PDSO-G8) **PLASTIC SMALL–OUTLINE**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.006 (0,15) per side.
D. Body width dimension does not include inter–lead flash or protrusions. Inter–lead flash and protrusions shall not exceed 0.010 (0,25) per side.
E. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
F. Lead dimension is the length of terminal for soldering to a substrate.
G. The lead width, as measured 0.014 (0,36) or greater above the seating plane, shall not exceed a maximum value of 0.024 (0,61).
H. Lead-to-lead coplanarity shall be less than 0.004 (0,10) from Seating Plane.
I. Falls within JEDEC MS-012-AA.