3.3V Radiation Tolerant CAN Transceiver with Listen Mode and Loopback

ISL72026SEH

The Intersil ISL72026SEH is a radiation tolerant 3.3V CAN transceiver that is compatible with the ISO11898-2 standard for applications calling for Controller Area Network (CAN) serial communication in satellites and aerospace communications and telemetry data processing in harsh industrial environments.

The transceiver can transmit and receive at bus speeds up to 5Mbps. It can drive a 40m cable at 1Mbps per the ISO11898-2 specification. The device is designed to operate over a common-mode range of -7V to +12V with a maximum of 120 nodes. The device has three discrete selectable driver rise/fall time options, a listen mode feature and loopback test capability.

Receiver (Rx) inputs feature a "full fail-safe" design, which ensures a logic high Rx output if the Rx inputs are floating, shorted, or terminated but undriven.

The ISL72026SEH is available in an 8 Ld hermetic ceramic flatpack and die form that operate across the temperature range of -55°C to +125°C. The logic inputs are tolerant with 5V systems.

Other CAN transceivers available are the ISL72027SEH and ISL72028SEH. For a list of differences see Table 1 on page 2.

Related Literature

- UG051, "ISL7202xSEHEVAL1Z Evaluation Board User Guide"

- TR018, "SEE Testing of the ISL72027SEH CAN Transceiver"

- TR022, "Total Dose Testing of the ISL72026SEH, ISL72027SEH and ISL72028SEH CAN Transceivers"

Features

- Electrically screened to SMD 5962-15228

- ESD protection on all pins . . . . 4kV HBM

- Compatible with ISO11898-2

- Operating supply range . . . . 3.0V to 3.6V

- Bus pin fault protection to ±20V

- Undervoltage lockout

- Cold spare: powered down devices/nodes will not affect active devices operating in parallel

- Three selectable driver rise and fall times

- Glitch free bus I/O during power-up and power-down

- Full fail-safe (open, short, terminated/undriven) receiver

- Hi Z input allows for 120 nodes on the bus

- High data rates . . . . up to 5Mbps

- Quiescent supply current . . . . 7mA (max)

- Listen mode supply current . . . . 2mA (max)

- -7V to +12V common mode input voltage range

- 5V tolerant logic inputs

- Thermal shutdown

- Acceptance tested to 75krad(Si) (LDR) wafer-by-wafer

- Radiation tolerance

  - SEL/B immune to LET 60MeV•cm^2/mg

  - Low dose rate (0.01rad(Si)/s) . . . . 75krad(Si)

Applications

- Satellites and aerospace communications

- Telemetry data processing
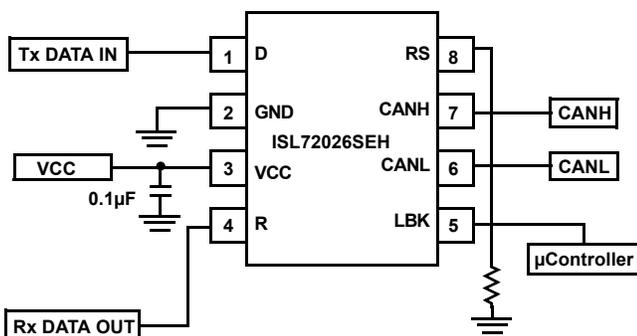
- High-end industrial environments

- Harsh environments

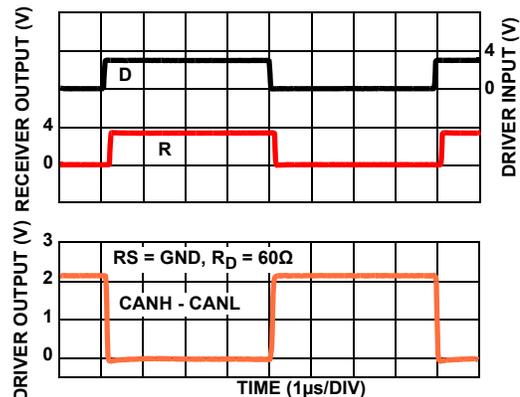
FIGURE 1. TYPICAL APPLICATION

FIGURE 2. FAST DRIVER AND RECEIVER WAVEFORMS

Ordering Information

ORDERING / SMD NUMBER (Note 1)	PART NUMBER (Note 2)	TEMPERATURE RANGE (°C)	PACKAGE (RoHS Compliant)	PACKAGE DRAWING #
5962L1522801VXC	ISL72026SEHVF	-55 to +125	8 Ld Ceramic Flat Pack	K8.A
N/A	ISL72026SEHF/PROTO	-55 to +125	8 Ld Ceramic Flat Pack	K8.A
5962L1522801V9A	ISL72026SEHVX	-55 to +125	Die	
N/A	ISL72026SEHX/SAMPLE	-55 to +125	Die	
N/A	ISL72026SEHEVAL1Z	Evaluation Board		

NOTES:

1. Specifications for Radiation Tolerant QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the "Ordering Information" table must be used when ordering.

2. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
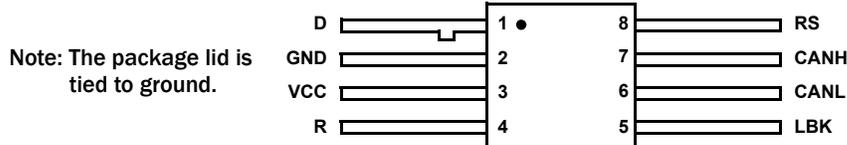
TABLE 1. ISL7202xSEH PRODUCT FAMILY FEATURE TABLE

SPEC	ISL72026SEH	ISL72027SEH	ISL72028SEH
Loopback Feature	Yes	No	No
VREF Output	No	Yes	Yes
Listen Mode	Yes	Yes	No
Shutdown Mode	No	No	Yes
VTHRLM	1150mV (Max)	1150mV (Max)	N/A
VTHFLM	525mV (Min)	525mV (Min)	N/A
VHYSLM	50mV (Min)	50mV (Min)	N/A
Supply Current, Listen Mode	2mA (Max)	2mA (Max)	N/A
Supply Current, Shutdown Mode	N/A	N/A	50µA (Max)
VREF Leakage Current	N/A	±25µA (Max)	±25µA (Max)

N/A: Not Applicable

Pin Configuration

ISL72026SEH
(8 LD CERAMIC FLATPACK)
TOP VIEW

Note: The package lid is tied to ground.

```
        D  ┤ 1 ●      8 ├  RS
      GND  ┤ 2        7 ├  CANH
      VCC  ┤ 3        6 ├  CANL
        R  ┤ 4        5 ├  LBK
```

Pin Descriptions

| PIN NUMBER	PIN NAME	FUNCTION
1	D	CAN driver digital input. The bus states are LOW = Dominant and HIGH = Recessive. Internally tied HIGH.
2	GND	Ground connection.
3	VCC	System power supply input (3.0V to 3.6V). The typical voltage for the device is 3.3V.
4	R	CAN Data Receiver Output. The bus states are LOW = Dominant and HIGH = Recessive.
8	RS	A resistor to GND from this pin controls the rise and fall time of the CAN output waveform. Drive RS HIGH to put into Listen Mode.
6	CANL	CAN bus line for low level output
7	CANH	CAN bus line for high level output
5	LBK	A HIGH on this pin places CANH and CANL pins in a high impedance state. The rest of the circuit remains active so that the TX and RX can loopback diagnostic information. Internally tied LOW.

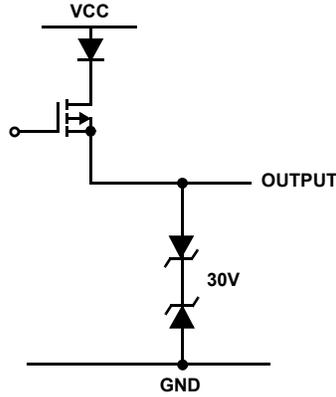# Equivalent Input and Output Schematic Diagrams
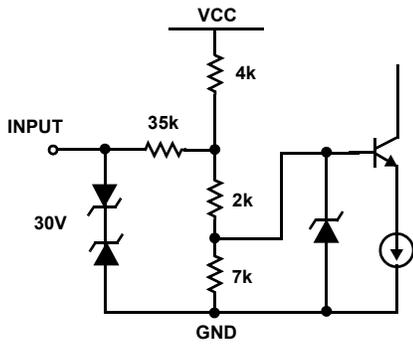
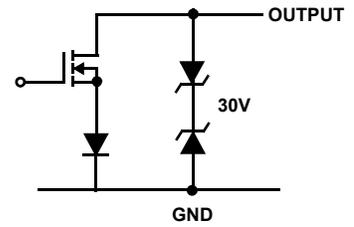**FIGURE 3. CANH AND CANL INPUTS**
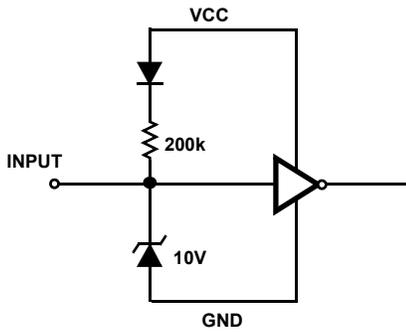
FIGURE 4. CANH OUTPUT

FIGURE 5. CANL OUTPUT

FIGURE 6. D INPUT

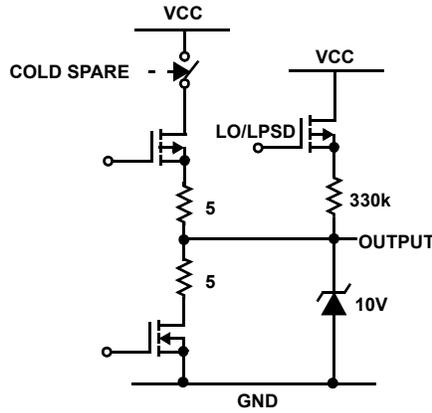**FIGURE 7. R OUTPUT**
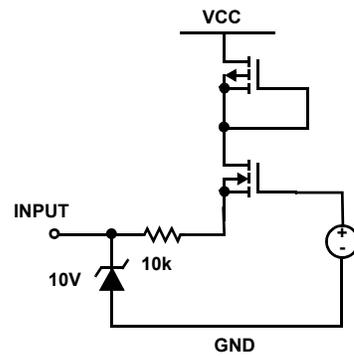
FIGURE 8. RS INPUT
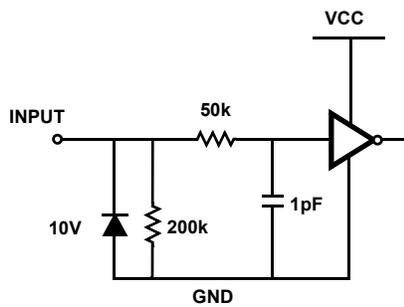
FIGURE 9. LBK INPUT

Absolute Maximum Ratings

VCC to GND with/without Ion Beam. . . . . -0.3V to 5.5V
CANH, CANL, VREF Under Ion Beam . . . . ±18V
CANH, CANL, VREF . . . . ±20V
I/O Voltages
   D, R, RS . . . . -0.5V to 7V
Receiver Output Current . . . . -10mA to 10mA
Output Short-Circuit Duration . . . . Continuous
ESD Rating:
Human Body Model (Tested per MIL-PRF-883 3015.7)
   CANH, CANL Bus Pins 4kV
   All Other Pins 4kV
Charged Device Model (Tested per JESD22-C101D) 750V
Machine Model (Tested per JESD22-A115-A) 200V

Thermal Information

Thermal Resistance (Typical) θ_{JA} (°C/W). θ_{JC} (°C/W)
8 Ld FP Package (Notes 3, 4) Direct Attach .   39   7
Maximum Junction Temperature . . . . +175°C
Storage Temperature Range. . . . . -65°C to +150°C

Operating Conditions

Temperature Range . . . . -55°C to +125°C
V_{CC} Supply Voltage. . . . . 3.0V to 3.6V
Voltage on CAN I/O. . . . . -7V to 12V
V_{IH} D Logic Pins (D, LBK). . . . . .2V to 5.5V
V_{IL} D Logic Pins (D, LBK) . . . . 0V to 0.8V
I_{OH} Driver (CANH - CANL = 1.5V, V_{CC} = 3.3V) . . . . - 40mA
I_{OH} Receiver (V_{OH} = 2.4V) . . . . -4mA
I_{OL} Driver (CANH - CANL = 1.5V, V_{CC} = 3.3V) . . . . +40mA
I_{OL} Receiver (V_{OL} = 0.4V). . . . . +4mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board (two buried 1oz copper planes) with "direct attach" features (package base mounted to PCB thermal land with a 10 mil gap fill material having a k of 1W/m-K. See Tech Brief TB379.

4. For θ_{JC}, the "case temp" location is the center of the package underside.

Electrical Specifications
Test Conditions: VCC = 3.0V to 3.6V; Typicals are at T_A = +25°C (Note 7); unless otherwise specified (Note 5). **Boldface limits apply across the operating temperature range, -55°C to +125°C or over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNIT
DRIVER ELECTRICAL CHARACTERISTICS								
Dominant Bus Output Voltage	$V_{O(DOM)}$	D = 0V, CANH, RS = 0V, Figures 10 and 11	3.0V ≤ V_{CC} ≤ 3.6V	Full	**2.25**	2.85	**V_{CC}**	V
		D = 0V, CANL, RS = 0V, Figures 10 and 11		Full	**0.1**	0.65	**1.25**	V
Recessive Bus Output Voltage	$V_{O(REC)}$	D = 3V, CANH, RS = 0V, 60Ω and no load, Figures 10 and 11	3.0V≤ V_{CC} ≤ 3.6V	Full	**1.80**	2.3	**2.70**	V
		D = 3V, CANL, RS = 0V, 60Ω and no load, Figures 10 and 11		Full	**1.80**	2.3	**2.80**	V
Dominant Output Differential Voltage	$V_{OD(DOM)}$	D = 0V, RS = 0V, 3.0V ≤ V_{CC} ≤ 3.6V, Figures 10 and 11		Full	**1.5**	2.2	**3**	V
		D = 0V, RS = 0V, 3.0V ≤ V_{CC} ≤ 3.6V, Figures 11 and 12		Full	**1.2**	2.1	**3**	V
Recessive Output Differential Voltage	$V_{OD(REC)}$	D=3V, RS = 0V, 3.0V ≤ V_{CC} ≤ 3.6V, Figures 10 and 11		Full	**-120**	0.2	**12**	mV
		D = 3V, RS = 0V, 3.0V ≤ V_{CC} ≤ 3.6V, no load		Full	**-500**	-34	**50**	mV
Logic Input High Voltage (D, LBK)	V_{IH}	3.0V ≤ V_{CC} ≤ 3.6V, Note 8		Full	**2.0**	-	**5.5**	V
Logic Input Low Voltage (D, LBK)	V_{IL}	3.0V ≤ V_{CC} ≤ 3.6V, Note 8		Full	**0**	-	**0.8**	V
Logic High Level Input Current (D, LBK)	I_{IH}	D = 2.0V, 3.0V ≤ V_{CC} ≤ 3.6V, Note 9		Full	**-30**	-3	**30**	µA
Logic Low Level Input Current (D, LBK)	I_{IL}	D = 0.8V, 3.0V ≤ V_{CC} ≤ 3.6V, Note 9		Full	**-30**	-7	**30**	µA
RS Input Voltage for Listen Mode	$V_{IN(RS)}$	3.0V ≤ V_{CC} ≤ 3.6V		Full	**0.75 VCC**	1.9	**5.5**	V

Electrical Specifications
Test Conditions: VCC = 3.0V to 3.6V; Typicals are at T_A = +25°C (Note 7); unless otherwise specified (Note 5). **Boldface limits apply across the operating temperature range, -55°C to +125°C or over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNIT
Output Short-Circuit Current	I_{OSC}	V_{CANH} = -7V, CANL = OPEN, 3.0V ≤ V_{CC} ≤ 3.6V, Figure 19	Full	**-250**	-100	-	mA
		V_{CANH} = +12V, CANL = OPEN, 3.0V ≤ V_{CC} ≤ 3.6V, Figure 19	Full	-	0.4	**1**	mA
		V_{CANL} = -7V, CANH = OPEN, 3.0V ≤ V_{CC} ≤ 3.6V, Figure 19	Full	**-1**	-0.4	-	mA
		V_{CANL} = +12V, CANH = OPEN, 3.0V ≤ V_{CC} ≤ 3.6V, Figure 19	Full	-	100	**250**	mA
Thermal Shutdown Temperature	T_{SHDN}	3.0V < V_{IN} < 3.6V	-	**-**	163	-	°C
Thermal Shutdown Hysteresis	T_{HYS}	3.0V < V_{IN} < 3.6V	-	**-**	12	-	°C
RECEIVER ELECTRICAL CHARACTERISTICS							
Input Threshold Voltage (Rising)	V_{THR}	LBK = 0V, RS = 0V, 10k, 50k, (recessive to dominant), Figures 14 and 15	Full	-	750	**900**	mV
Input Threshold Voltage (Falling)	V_{THF}	LBK = 0V, RS = 0V, 10k, 50k, (dominant to recessive), Figures 14 and 15	Full	**500**	650	-	mV
Input Hysteresis	V_{HYS}	(V_{THR} - V_{THF}), RS = 0V, 10k, 50k, Figures 14 and 15	Full	**40**	90	-	mV
Listen Mode Input Threshold Voltage (Rising)	V_{THRLM}	RS = V_{CC}, (recessive to dominant), Figure 14	Full	-	920	**1150**	mV
Listen Mode Input Threshold Voltage (Falling)	V_{THFLM}	RS = V_{CC}, (dominant to recessive), Figure 14	Full	**525**	820	-	mV
Listen Mode Input Hysteresis	V_{HYSLM}	(V_{THR} - V_{THF}), RS = V_{CC}, Figure 14	Full	**50**	100	-	mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA	Full	**2.4**	V_{CC} - 0.2	-	V
Receiver Output Low Voltage	V_{OL}	I_O = +4mA	Full	-	0.2	**0.4**	V
Input Current for CAN Bus	I_{CAN}	CANH or CANL at 12V, D = 3V, other bus pin at 0V, LBK = RS = 0V	Full	-	420	**500**	µA
		CANH or CANL at 12V, D = 3V, V_{CC} = 0V, other bus pin at 0V, LBK = RS = 0V	Full	-	150	**250**	µA
		CANH or CANL at -7V, D = 3V, other bus pin at 0V, LBK = RS = 0V	Full	**-400**	-300	-	µA
		CANH or CANL at -7V, D = 3V, V_{CC} = 0V, other bus pin at 0V, LBK = RS = 0V	Full	**-150**	-85	-	µA
Input Capacitance (CANH or CANL)	C_{IN}	Input to GND, D = 3V, LBK = RS = 0V	25	-	35	-	pF
Differential Input Capacitance	C_{IND}	Input to Input, D = 3V, LBK = RS = 0V	25	-	15	-	pF
Input Resistance (CANH or CANL)	R_{IN}	Input to GND, D = 3V, LBK = RS = 0V	Full	**20**	40	**50**	kΩ
Differential Input Resistance	R_{IND}	Input to Input, D = 3V, LBK = RS = 0V	Full	**40**	80	**100**	kΩ
SUPPLY CURRENT							
Supply Current, Listen Mode	$I_{CC(L)}$	RS = D = V_{CC}, LBK = 0V, 3.0V≤ V_{CC} ≤ 3.6V	Full	-	1	**2**	mA
Supply Current, Dominant	$I_{CC(DOM)}$	D = LBK = RS = 0V, no load, 3.0V ≤ V_{CC} ≤ 3.6V	Full	-	5	**7**	mA
Supply Current, Recessive	$I_{CC(REC)}$	D = V_{CC}, LBK = RS = 0V, no load, 3.0V ≤ V_{CC} ≤ 3.6V	Full	-	2.6	**5**	mA
COLD SPARING BUS CURRENT							
CANH Leakage Current	$I_{L(CANH)}$	V_{CC} = 0.2V, CANH = -7V or 12V, CANL = float, D = V_{CC}, RS = 0V	Full	**-25**	-4	**25**	µA
CANL Leakage Current	$I_{L(CANL)}$	V_{CC} = 0.2V, CANL = -7V or 12V, CANH = float, D = V_{CC}, RS = 0V	Full	**-25**	-4	**25**	µA

Electrical Specifications
Test Conditions: VCC = 3.0V to 3.6V; Typicals are at T_A = +25°C (Note 7); unless otherwise specified (Note 5). **Boldface limits apply across the operating temperature range, -55°C to +125°C or over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.** (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNIT
DRIVER SWITCHING CHARACTERISTICS							
Propagation Delay LOW to HIGH	t_{PDLH1}	RS = 0V, Figure 13	Full	-	75	**150**	ns
Propagation Delay LOW to HIGH	t_{PDLH2}	RS = 10kΩ, Figure 13	Full	-	520	**850**	ns
Propagation Delay LOW to HIGH	t_{PDLH3}	RS = 50kΩ, Figure 13	Full	-	850	**1400**	ns
Propagation Delay HIGH to LOW	t_{PDHL1}	RS = 0V, Figure 13	Full	-	80	**155**	ns
Propagation Delay HIGH to LOW	t_{PDHL2}	RS = 10kΩ, Figure 13	Full	-	460	**800**	ns
Propagation Delay HIGH to LOW	t_{PDHL3}	RS = 50kΩ, Figure 13	Full	-	725	**1300**	ns
Output Skew	t_{SKEW1}	RS = 0V, ($|t_{PHL} - t_{PLH}|$), Figure 13	Full	-	5	**50**	ns
Output Skew	t_{SKEW2}	RS = 10kΩ, ($|t_{PHL} - t_{PLH}|$), Figure 13	Full	-	60	**510**	ns
Output Skew	t_{SKEW3}	RS = 50kΩ, ($|t_{PHL} - t_{PLH}|$), Figure 13	Full	-	110	**800**	ns
Output Rise Time	t_{r1}	RS = 0V, (fast speed) Figure 13	Full	**20**	55	**100**	ns
Output Fall Time	t_{f1}		Full	**10**	25	**75**	ns
Output Rise Time	t_{r2}	RS = 10kΩ, (medium speed - 250kbps) Figure 13	Full	**200**	400	**780**	ns
Output Fall Time	t_{f2}		Full	**175**	300	**500**	ns
Output Rise Time	t_{r3}	RS = 50kΩ, (slow speed - 125kbps) Figure 13	Full	**400**	700	**1400**	ns
Output Fall Time	t_{f3}		Full	**300**	650	**1000**	ns
Total Loop Delay, Driver Input to Receiver Output, Recessive to Dominant	$t_{(LOOP1)}$	RS = 0V, Figure 17	Full	-	115	**210**	ns
		RS = 10kΩ, Figure 17	Full	-	550	**875**	ns
		RS = 50kΩ, Figure 17	Full	-	850	**1400**	ns
Total Loop Delay, Driver Input to Receiver Output, Dominant to Recessive	$t_{(LOOP2)}$	RS = 0V, Figure 17	Full	-	130	**270**	ns
		RS = 10kΩ, Figure 17	Full	-	500	**825**	ns
		RS = 50kΩ, Figure 17	Full	-	750	**1300**	ns
Listen to Valid Dominant Time	t_{L-DOM}	Figure 16	Full	-	5	**15**	µs
RECEIVER SWITCHING CHARACTERISTICS							
Propagation Delay LOW to HIGH	t_{PLH}	Figure 14	Full	-	50	**110**	ns
Propagation Delay HIGH to LOW	t_{PHL}	Figure 14	Full	-	50	**110**	ns
Rx Skew	t_{SKEW1}	$|(t_{PHL} - t_{PLH})|$, Figure 14	Full	-	2	**35**	ns
Rx Rise Time	t_r	Figure 14	Full	-	2	-	ns
Rx Fall Time	t_f	Figure 14	Full	-	2	-	ns
LBK Delay I/O to Rx Output	t_{LBK}	Figure 18, Note 9	Full	-	35	**75**	ns
RS PIN CHARACTERISTICS							
RS Input Current	$I_{RS(H)}$	RS = 0.75 x V_{CC}	Full	**-10**	-0.2	-	µA
	$I_{RS(L)}$	V_{RS} = 0V	Full	**-450**	-125	**0**	µA

NOTES:
5. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
6. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C and +125°C, unless otherwise specified.
7. Typical values are at 3.3V. Parameters with a single entry in the "TYP" column apply to 3.3V. Typical values shown are not guaranteed.
8. Parameter included in functional testing.
9. Performed during the 100% screening operations over the full operating temperature range. Not performed as part of TCI Group E and Group C. Radiation characterization testing performed as part of the initial release and any major changes in design.
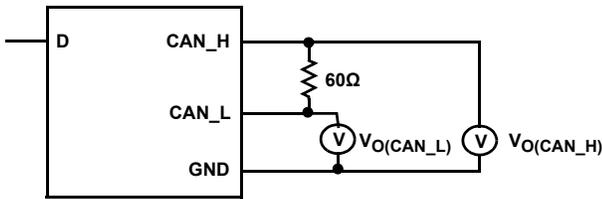
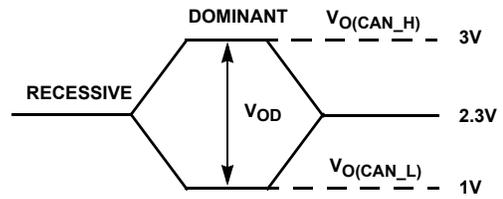# Test Circuits and Waveforms

FIGURE 10. DRIVER TEST CIRCUIT
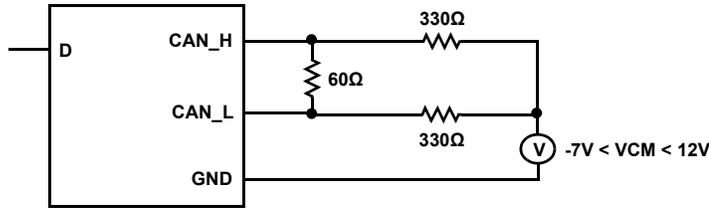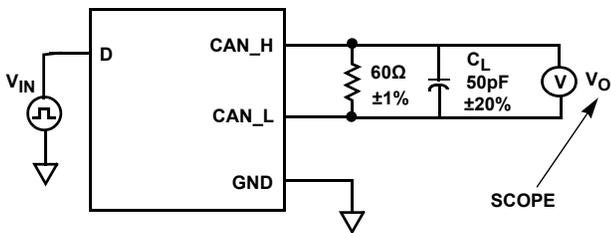

FIGURE 11. DRIVER BUS VOLTAGE DEFINITIONS

FIGURE 12. DRIVER COMMON MODE CIRCUIT

V_{IN} = 125kHz, 0V to V_{CC}, Duty Cycle 50%, $t_r = t_f \leq 6ns$, $Z_O = 50\Omega$
C_L includes fixture and instrumentation capacitance.
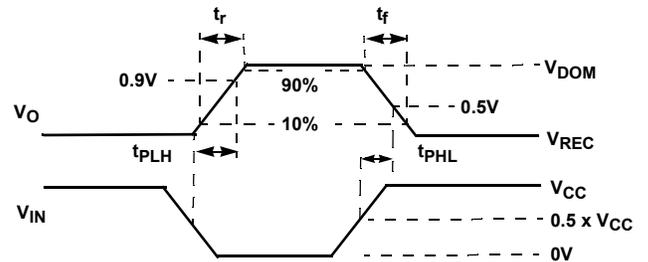
FIGURE 13A. DRIVER TIMING TEST CIRCUIT

FIGURE 13B. DRIVER TIMING MEASUREMENT POINTS

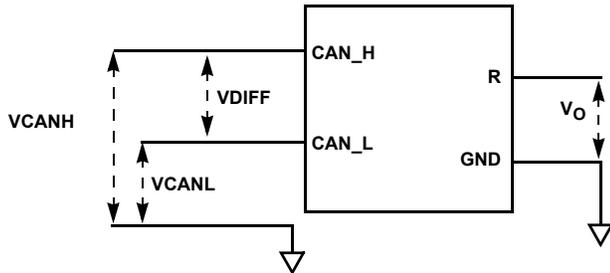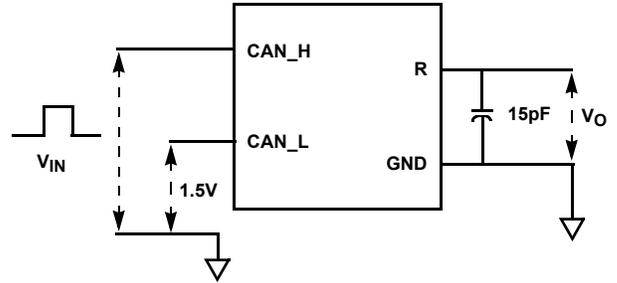FIGURE 13. DRIVER TIMING

Test Circuits and Waveforms (Continued)

FIGURE 14A. RECEIVER VOLTAGE DEFINITIONS

V_{IN} = 125kHz, Duty Cycle 50%, $t_r = t_f$ = 6ns, Z_O = 50Ω
C_L includes test setup capacitance

FIGURE 14B. RECEIVER TEST CIRCUIT
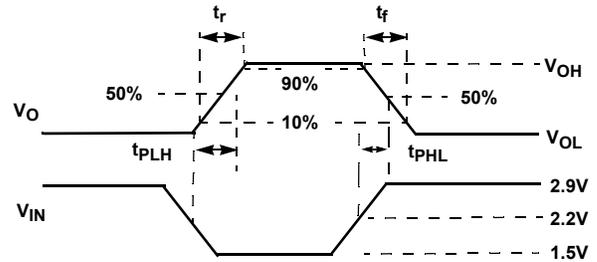
FIGURE 14C. RECEIVER TEST MEASUREMENT POINTS

FIGURE 14. RECEIVER TEST

TABLE 2.

INPUT		OUTPUT	MEASURED
VCANH	VCANL	R	VDIFF
−6.1V	−7V	L	900mV
12V	11.1V	L	900mV
−1V	−7V	L	6V
12V	6V	L	6V
−6.5V	−7V	H	500mV
12V	11.5V	H	500mV
−7V	−1V	H	6V
6V	12V	H	6V

FIGURE 15. DIFFERENTIAL INPUT VOLTAGE THRESHOLD TEST

Test Circuits and Waveforms (Continued)
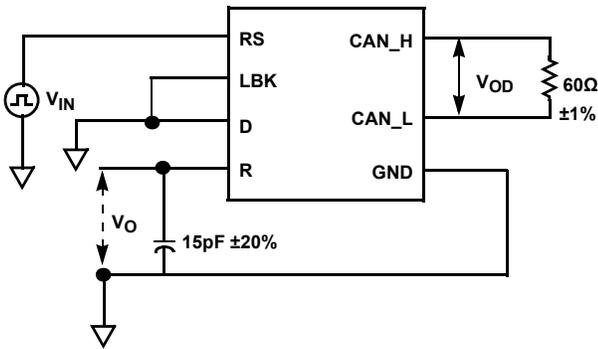
V_{IN} = 125kHz, 0V to V_{CC}, Duty Cycle 50%, t_r = t_f ≤ 6ns

FIGURE 16A. LISTEN TO VALID DOMINANT TIME TEST CIRCUIT
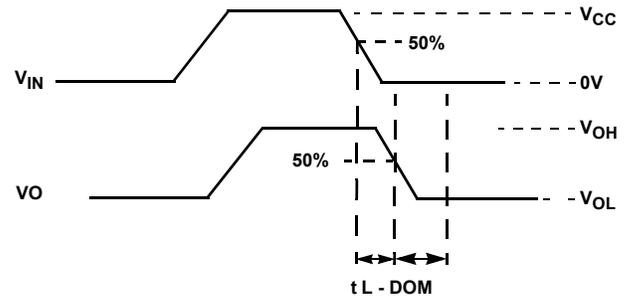
FIGURE 16B. LISTEN TO VALID DOMINANT TIME MEASUREMENT POINTS

FIGURE 16. LISTEN TO VALID DOMINANT TIME
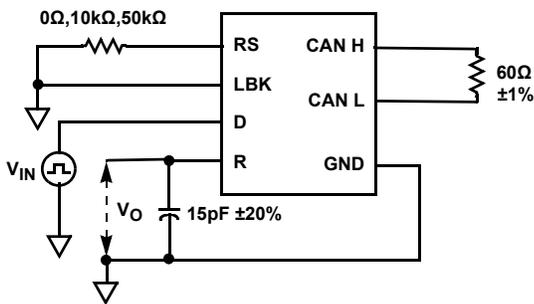
V_{IN} = 125kHz, Duty Cycle 50%, t_r = t_f ≤ 6ns.

FIGURE 17A. TOTAL LOOP DELAY TEST CIRCUIT
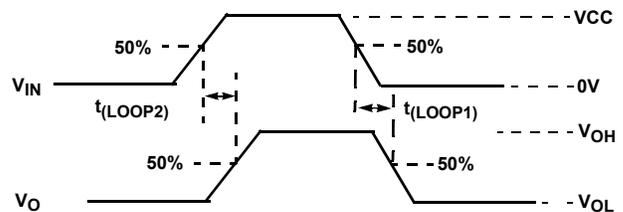
FIGURE 17B. TOTAL LOOP DELAY MEASUREMENT POINTS

FIGURE 17. TOTAL LOOP DELAY
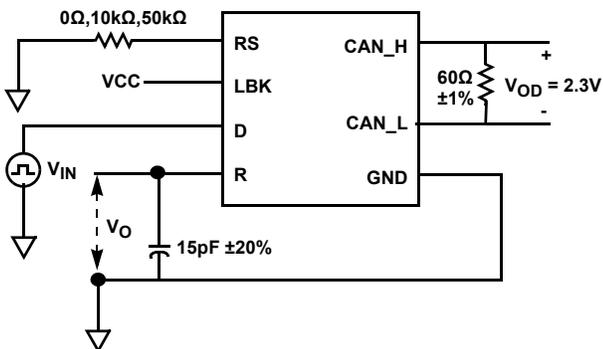
V_{IN} = 125kHz, 0V to V_{CC}, Duty Cycle 50%, t_r = t_f ≤ 6ns

FIGURE 18A. LOOP BACK DELAY TO DOMINANT TIME TEST CIRCUIT
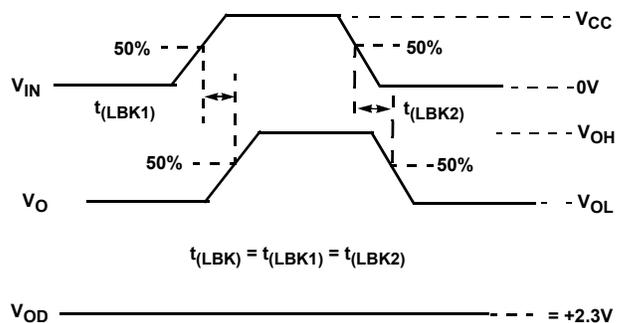
FIGURE 18B. LOOP BACK DELAY TO DOMINANT MEASUREMENT POINTS

FIGURE 18. LOOP BACK DELAY

Test Circuits and Waveforms (Continued)
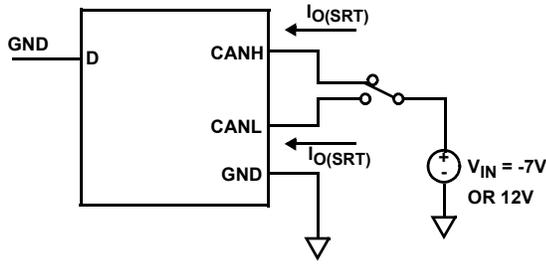
FIGURE 19A. OUTPUT SHORT CIRCUIT CURRENT TEST CIRCUIT
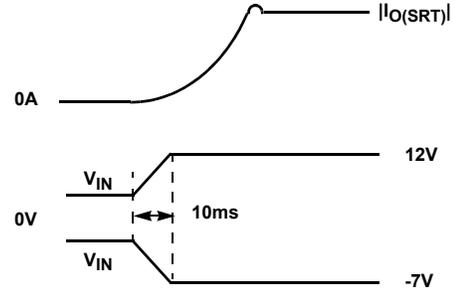
FIGURE 19B. OUTPUT SHORT CIRCUIT CURRENT WAVEFORMS

FIGURE 19. OUTPUT SHORT CIRCUIT CURRENT

Functional Description

Overview

The Intersil ISL72026SEH is a 3.3V radiation tolerant CAN transceiver that is compatible with the ISO11898-2 standard for use in CAN (Controller Area Network) serial communication systems.

The device performs transmit and receive functions between the CAN controller and the CAN differential bus. It can transmit and receive at bus speeds of up to 5Mbps. It is designed to operate over a common mode range of -7V to +12V with a maximum of 120 nodes. The device is capable of withstanding ±20V on the CANH and CANL bus pins outside of ion beam and ±16V under ion beam.

Slope Adjustment

The output driver rise and fall time has three distinct selections that may be chosen by using a resistor from the RS pin to GND. Connecting the RS pin directly to GND results in output switching times that are the fastest, limited only by the drive capability of the output stage. RS = 10kΩ provides for a typical slew rate of 8V/µs and RS = 50kΩ provides for a typical slew rate of 4V/µs.

Putting a high logic level to the RS pin places the device in a low current listen mode. The protocol controller uses this mode to switch between low power listen mode and normal transmit mode.

Cable Length

The device can work per ISO11898 specification with a 40m cable and stub length of 0.3m and 60 nodes at 1Mbps. This is greater than the ISO requirement of 30 nodes. The cable type specified is twisted pair (shielded or unshielded) with a characteristic impedance of 120Ω. Resistors equal to this are to be terminated at both ends of the cable. Stubs should be kept as short as possible to prevent reflections.

Cold Spare

High reliability system designers implementing data communications have to be sensitive to the potential for single point failures. To mitigate the risk of a failure they will use redundant bus transceivers in parallel. In this arrangement both active and quiescent devices can be present simultaneously on the bus. The quiescent devices are powered down for cold spare and do not affect the communication of the other active nodes.

To achieve this, a powered down transceiver (V_{CC} < 200mV) has a resistance between the CANH or CANL bus pin and the V_{CC} supply rail of > 480kΩ (max) with a typical resistance > 2MΩ. The resistance between CANH and CANL of a powered-down transceiver has a typical resistance of 80kΩ.

Listen Mode

When a high level is applied to the RS pin, the device enters a low power listen mode. The driver of the transceiver is switched off to conserve power while the receiver remains active. In listen mode the transceiver draws 2mA (max) of current.

A low level on the RS pin brings the device back to normal operation.

Loopback Mode

When a high level is applied to the LBK pin, the device enters the loopback state. The transceiver CANH and CANL pins are disconnected from the bus. The driver and receiver circuitry of the transceiver remains active to allow for diagnostic testing of the node.

Using 3.3V Devices in 5V Systems

Looking at the differential voltage of both the 3.3V and 5V devices, the differential voltage is the same, the recessive common mode output is the same. The dominant common mode output voltage is slightly lower than the 5V counterparts. The receiver specs are also the same. Though the electrical parameters appear compatible it is advised that necessary system testing be performed to verify interchangeable operation.

Typical Performance Curves C_L = 15pF, T_A = +25°C; Unless Otherwise Specified.
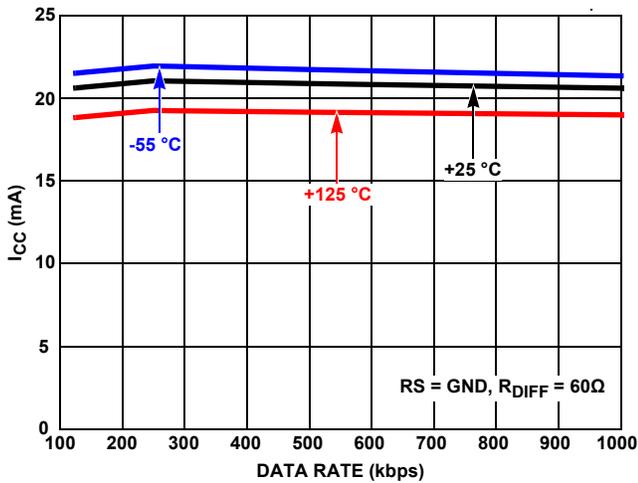

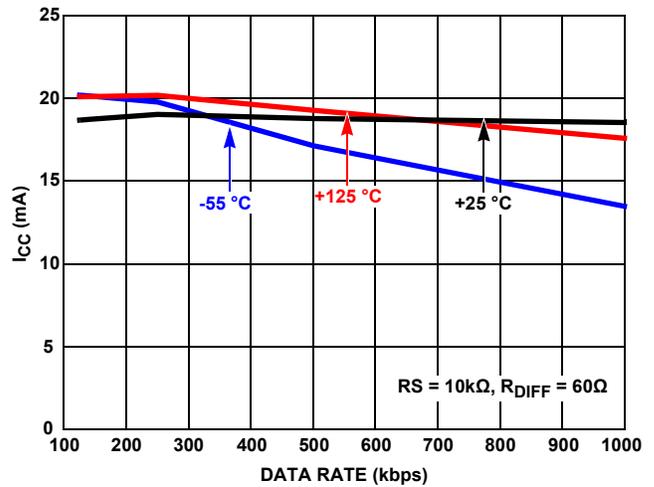FIGURE 20. SUPPLY CURRENT vs FAST DATA RATE vs TEMPERATURE

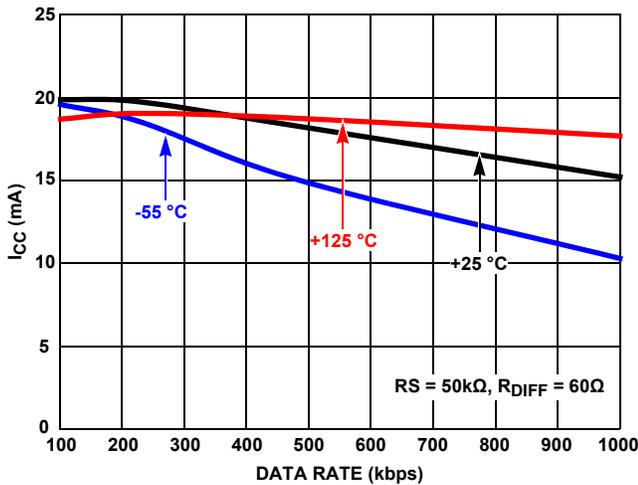FIGURE 21. SUPPLY CURRENT vs MEDIUM DATA RATE vs TEMPERATURE

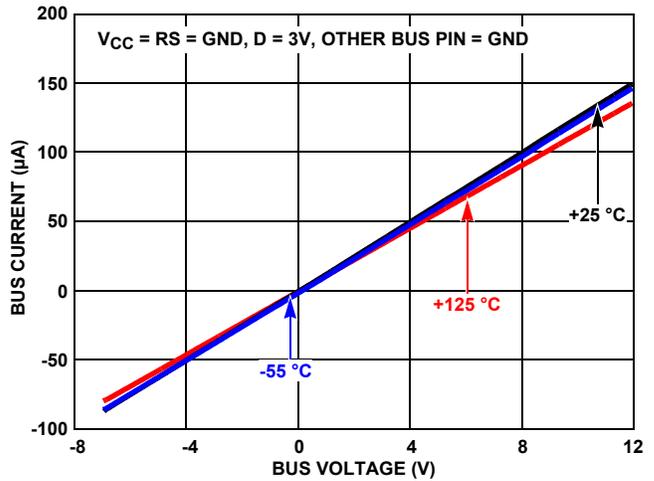FIGURE 22. SUPPLY CURRENT vs SLOW DATA RATE vs TEMPERATURE
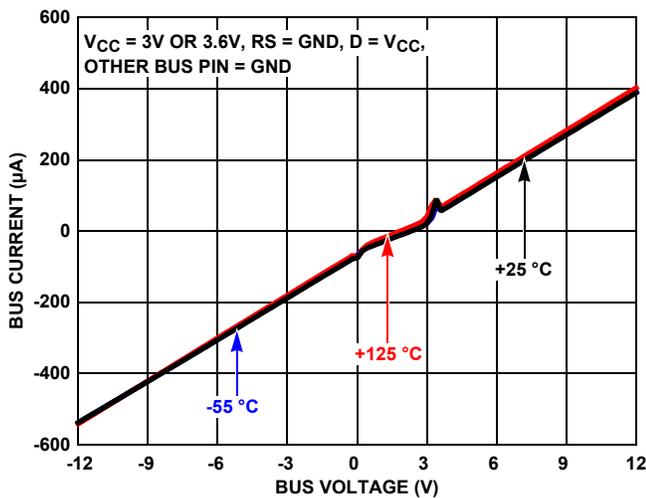

FIGURE 23. BUS PIN LEAKAGE vs VCM AT V_{CC} = 0V

FIGURE 24. BUS PIN LEAKAGE vs ±12V VCM

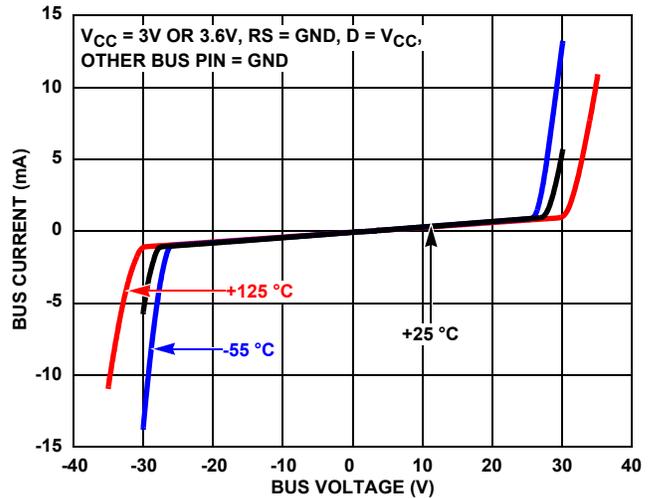FIGURE 25. BUS PIN LEAKAGE vs ±35V VCM

Typical Performance Curves C_L = 15pF, T_A = +25°C; Unless Otherwise Specified. (Continued)
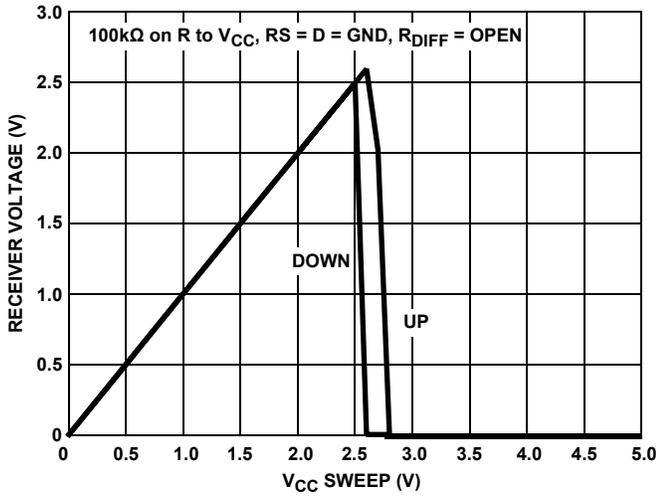
FIGURE 26. V_{CC} UNDERVOLTAGE LOCKOUT
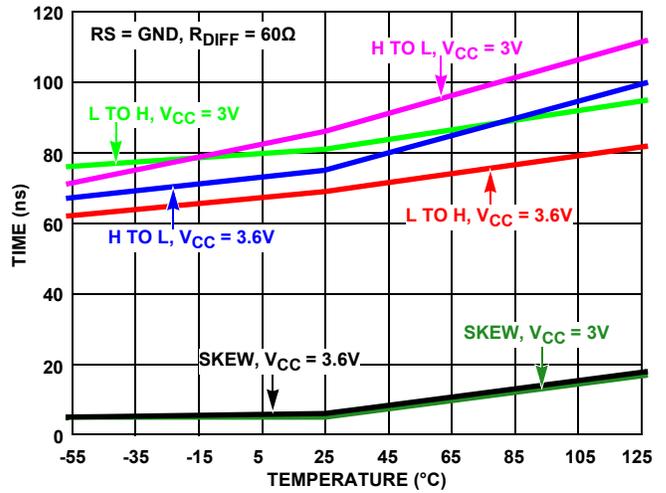
FIGURE 27. TRANSMITTER PROPAGATION DELAY AND SKEW vs TEMPERATURE AT FAST SPEED
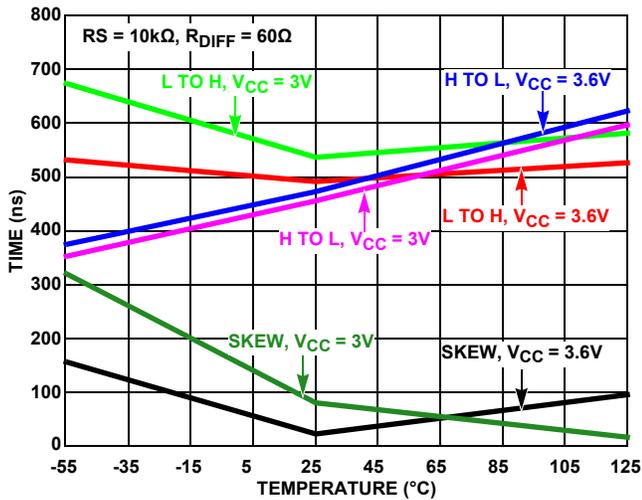
FIGURE 28. TRANSMITTER PROPAGATION DELAY AND SKEW vs TEMPERATURE AT MEDIUM SPEED
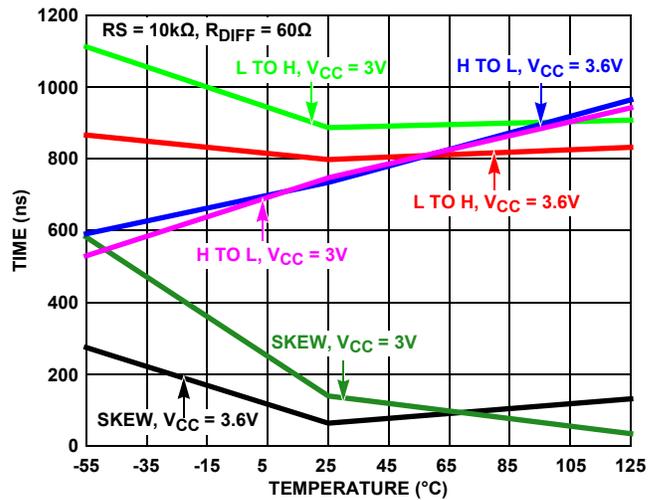
FIGURE 29. TRANSMITTER PROPAGATION DELAY AND SKEW vs TEMPERATURE AT SLOW SPEED
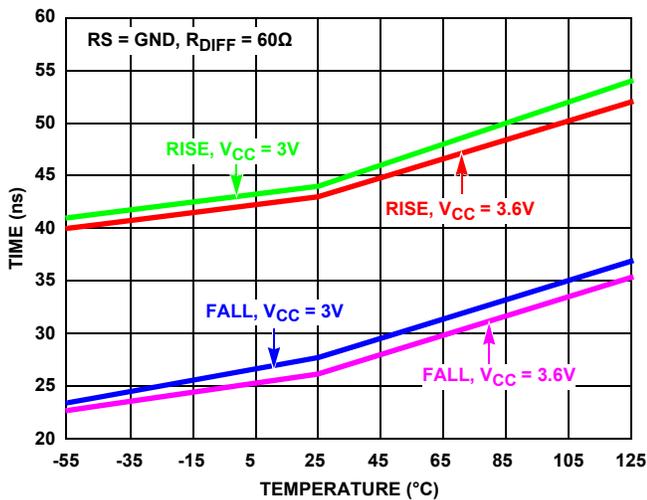
FIGURE 30. TRANSMITTER RISE AND FALL TIMES vs TEMPERATURE AT FAST SPEED
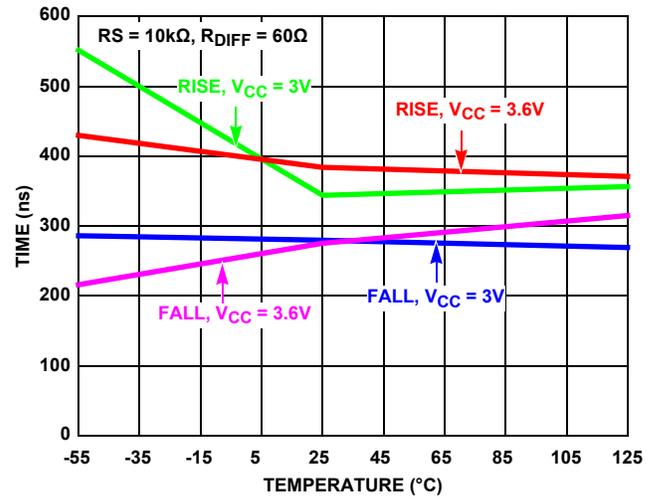
FIGURE 31. TRANSMITTER RISE AND FALL TIMES vs TEMPERATURE AT MEDIUM SPEED

Typical Performance Curves C_L = 15pF, T_A = +25°C; Unless Otherwise Specified. (Continued)
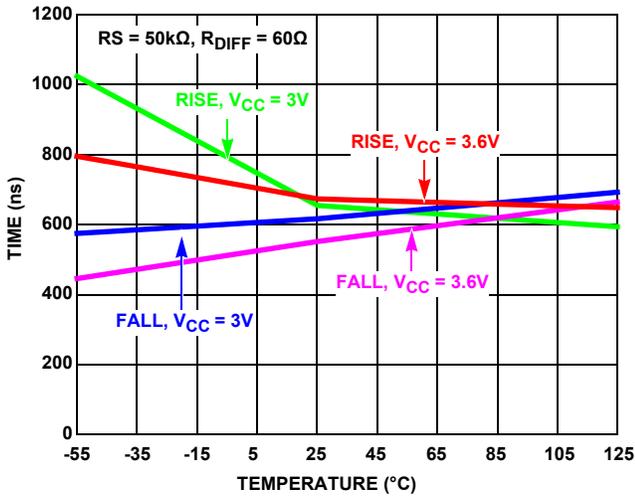
FIGURE 32. TRANSMITTER RISE AND FALL TIMES vs TEMPERATURE AT SLOW SPEED
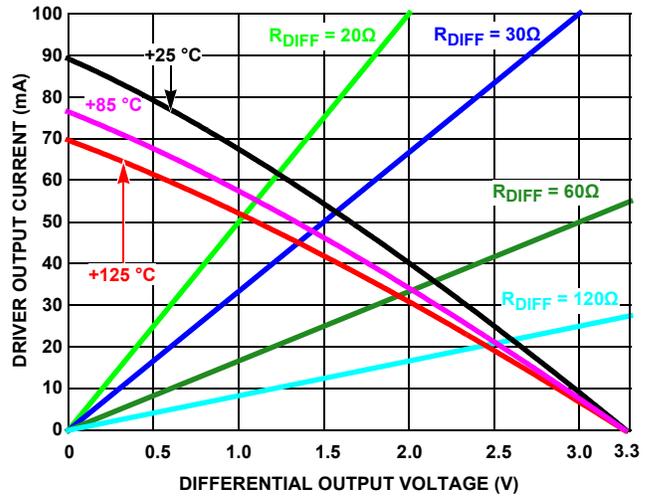
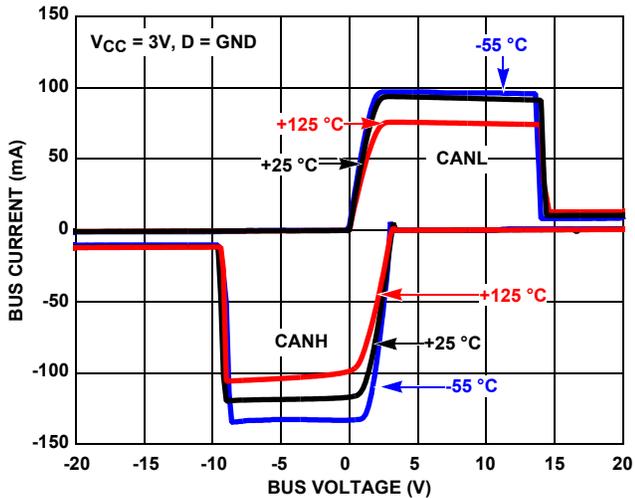FIGURE 33. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

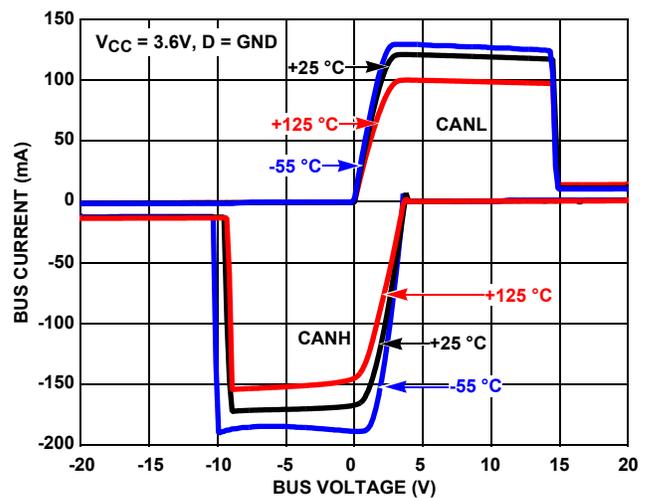FIGURE 34. DRIVER OUTPUT CURRENT vs SHORT CIRCUIT VOLTAGE vs TEMPERATURE

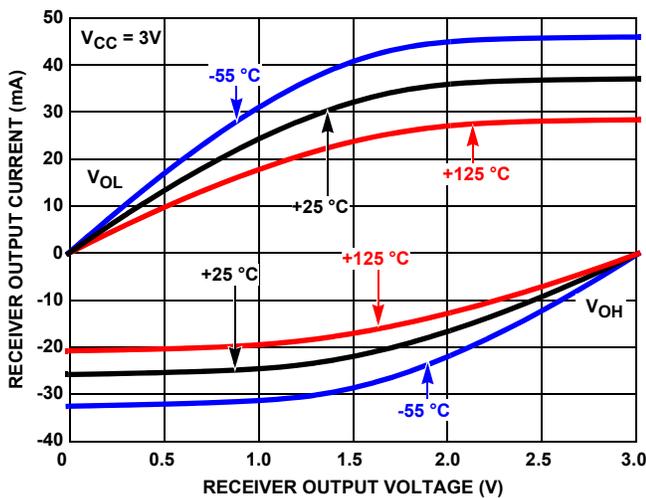FIGURE 35. DRIVER OUTPUT CURRENT vs SHORT CIRCUIT VOLTAGE vs TEMPERATURE

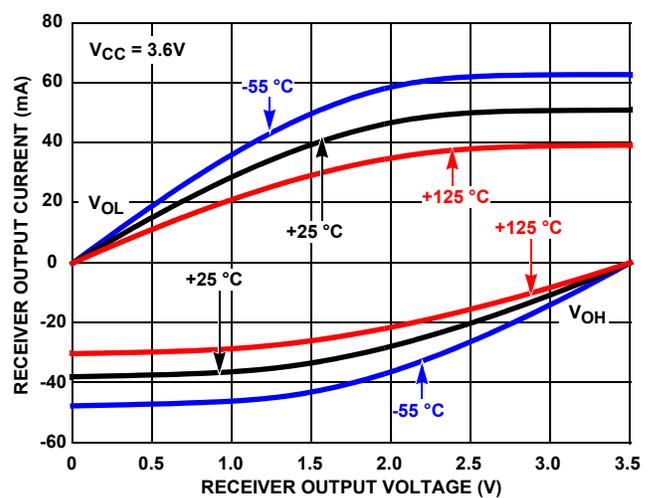FIGURE 36. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE AT V_{CC} = 3V

FIGURE 37. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE AT V_{CC} = 3.6V

Typical Performance Curves $C_L = 15pF$, $T_A = +25°C$; Unless Otherwise Specified. **(Continued)**
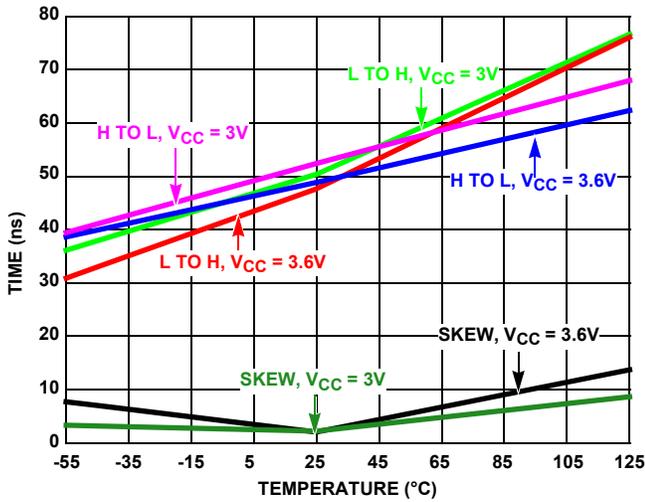

FIGURE 38. RECEIVER PROPAGATION DELAY AND SKEW vs TEMPERATURE
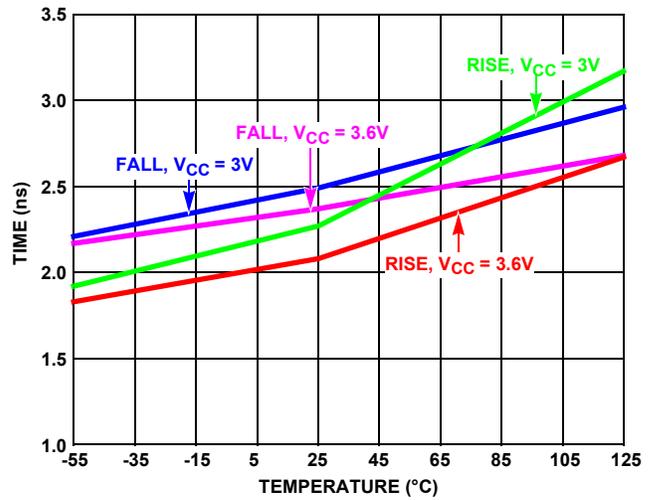

FIGURE 39. RECEIVER RISE AND FALL TIMES vs TEMPERATURE
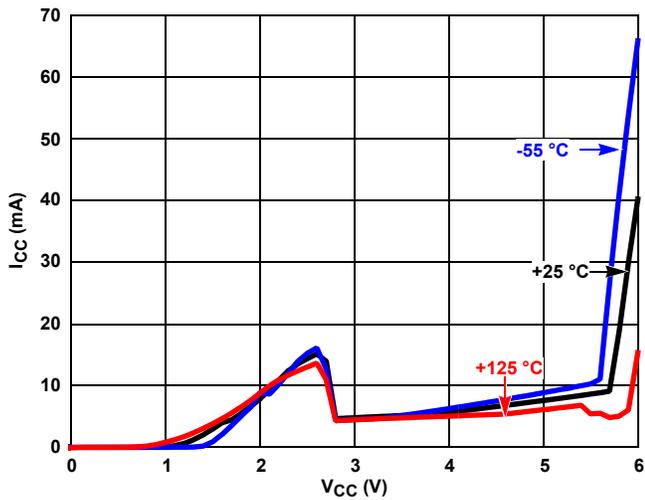

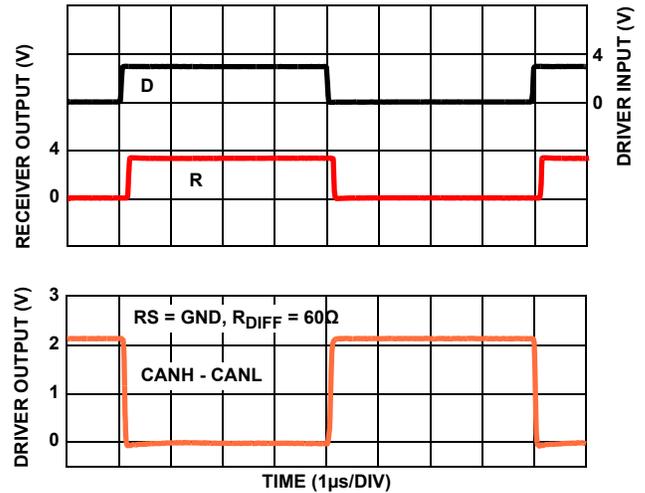FIGURE 40. SUPPLY CURRENT vs SUPPLY VOLTAGE vs TEMPERATURE
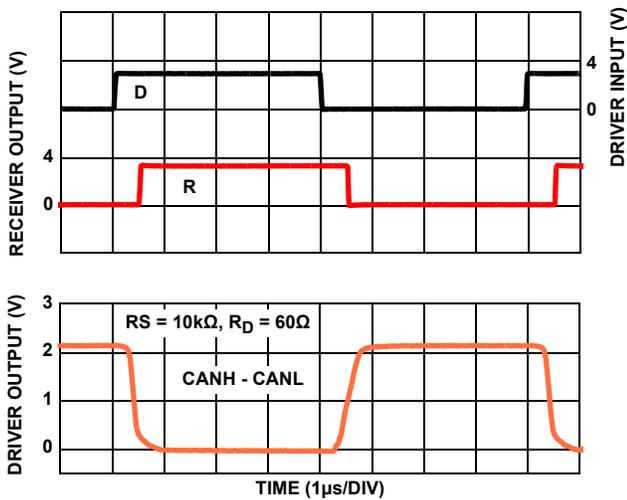

FIGURE 41. FAST DRIVER AND RECEIVER WAVEFORMS

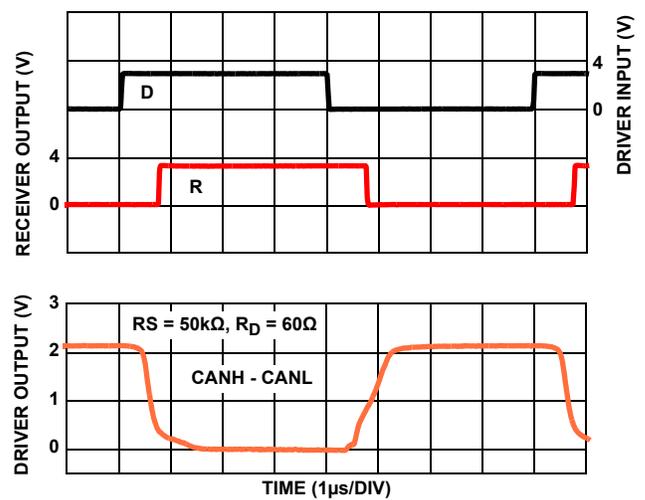
FIGURE 42. MEDIUM DRIVER AND RECEIVER WAVEFORMS

FIGURE 43. SLOW DRIVER AND RECEIVER WAVEFORMS

ISL72026SEH

Die Dimensions

2413µm x 3322µm (95 mils x 130.79 mils)
Thickness: 305µm ±25µm (12 mils ±1 mil)

Interface Materials

GLASSIVATION

Type: 12kÅ Silicon Nitride on 3kÅ Oxide

TOP METALLIZATION

Type: 300Å TiN on 2.8µm AlCu
In Bondpads, TiN has been removed.

BACKSIDE FINISH

Silicon

PROCESS

P6SOI

Assembly Related Information

SUBSTRATE POTENTIAL

Floating

Additional Information

WORST CASE CURRENT DENSITY

$1.6 \times 10^5 A/cm^2$
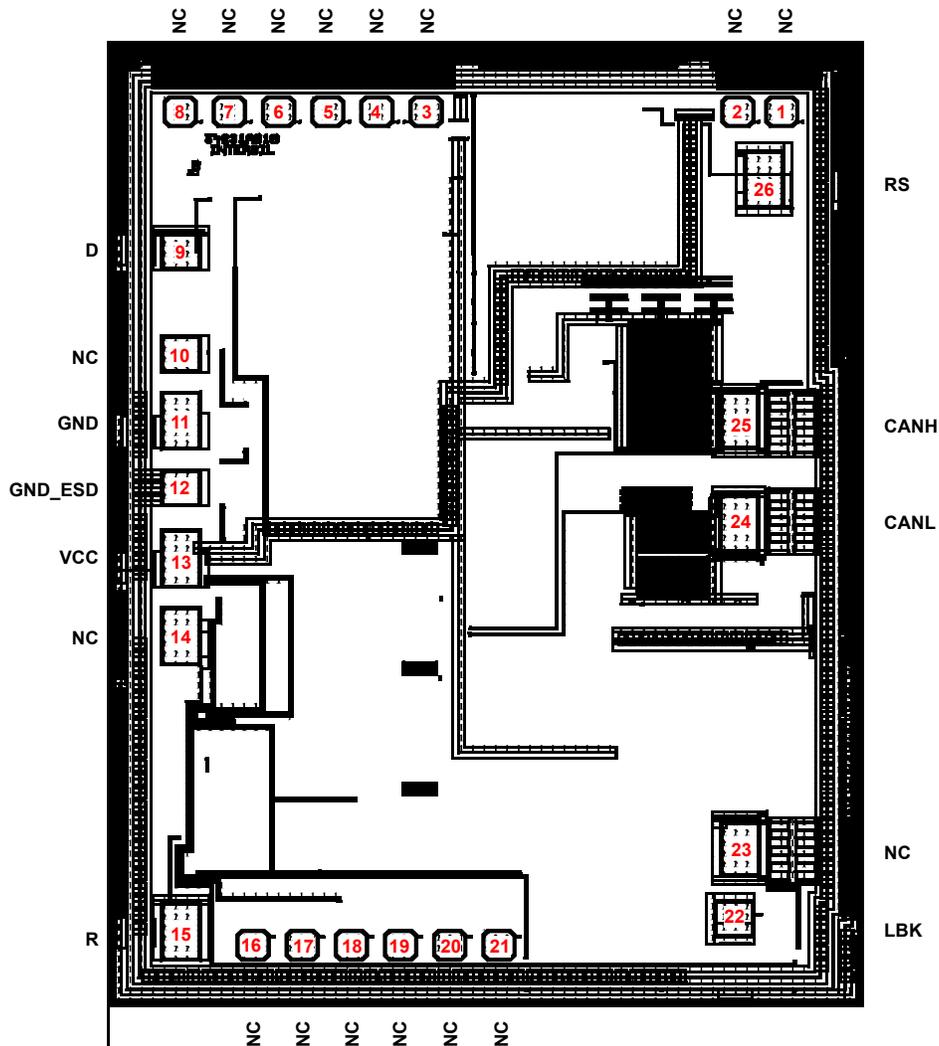
TRANSISTOR COUNT

4055

Weight of Packaged Device

0.31 grams

Lid Characteristics

Finish: Gold
Potential: Grounded, tied to package pin 2

Metalization Mask Layout

TABLE 3. ISL72026SEH DIE LAYOUT X-Y COORDINATES

PAD NUMBER	PAD NAME	X (µm)	Y (µm)	X	Y
1	NC	90.0	90.0	901.4	1365.6
2	NC	90.0	90.0	767.4	1365.6
3	NC	90.0	90.0	-183.23	1365.6
4	NC	90.0	90.0	-333.25	1365.6
5	NC	90.0	90.0	-483.25	1365.6
6	NC	90.0	90.0	-633.25	1365.6
7	NC	90.0	90.0	-783.25	1365.6
8	NC	90.0	90.0	-933.25	1365.6
9	D	110.0	110.0	-931.1	901.85
10	NC	110.0	110.0	-931.1	563.25
11	GND	110.0	180.0	-931.1	342.25
12	GND_ESD	110.0	110.05	-931.1	119.42
13	VCC	110.0	180.0	-931.1	-115.05
14	NC	110.0	180.05	-931.1	-371.08
15	R	110.0	180.0	-931.1	-1350.0
16	NC	90.0	90.0	-711.1	-1394.95
17	NC	90.0	90.0	-561.1	-1394.95
18	NC	90.0	90.0	-411.1	-1394.95
19	NC	90.0	90.0	-261.1	-1394.95
20	NC	90.0	90.0	-111.1	-1394.95
21	NC	90.0	90.0	38.9	-1394.95
22	LBK	110.0	110.0	756.9	-1307.3
23	NC	110.0	180.0	775.3	-1072.3
24	CANL	110.0	180.0	772.1	2.15
25	CANH	110.0	180.05	772.1	343.33
26	RS	110.0	180.0	848.1	1140.6

NOTE: Origin of coordinates is the center of the die. NC - No Connect

Revision History
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
August 16, 2016	FN8762.3	"Absolute Maximum Ratings" on page 4 changed voltage value in VCC to GND With/Without Ion Beam From: -0.3V to 4.5V To: -0.3V to 5.5V.

April 28, 2016	FN8762.2	- Updated title.
		- Updated the test condition for Output Rise Time on page 6.
		- Changed maximum data rate from 1Mbps to 5Mbps in the following locations:
		    - Second paragraph and "Features" section on page 1.
		    - In "Overview" on page 10.

November 9, 2015	FN8762.1	Absolute Maximum Ratings table on page 4: changed the value for "CANH, CANL, VREF Under Ion Beam" from ±16V to ±18V.
October 26, 2015	FN8762.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

For additional products, see www.intersil.com/en/products.html
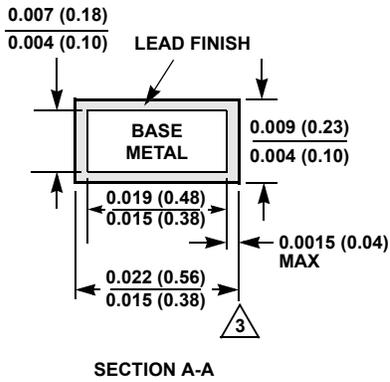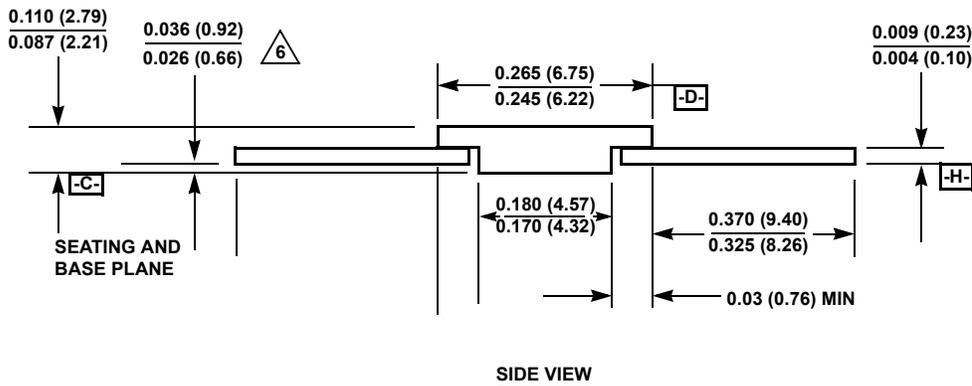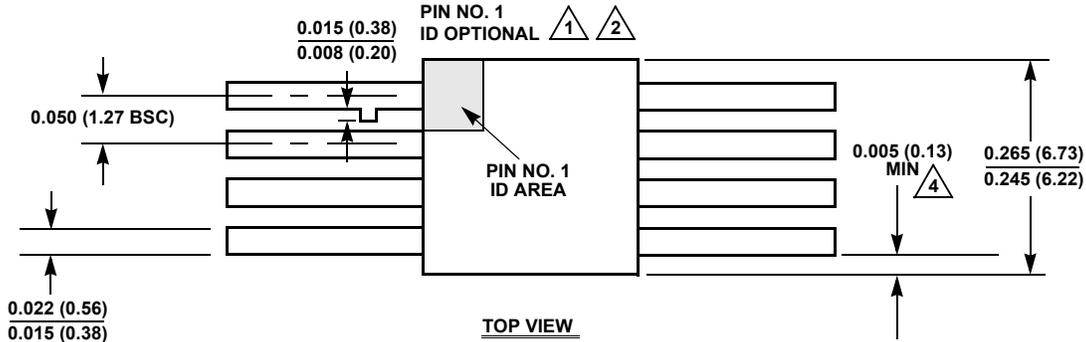
For information regarding Intersil Corporation and its products, see www.intersil.com

Package Outline Drawing

K8.A
8 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE
Rev 4, 12/14

PIN NO. 1
ID OPTIONAL /1\ /2\

$\frac{0.015 (0.38)}{0.008 (0.20)}$

0.050 (1.27 BSC)

PIN NO. 1
ID AREA

$\frac{0.022 (0.56)}{0.015 (0.38)}$

0.005 (0.13)
MIN /4\

$\frac{0.265 (6.73)}{0.245 (6.22)}$

TOP VIEW

$\frac{0.110 (2.79)}{0.087 (2.21)}$

$\frac{0.036 (0.92)}{0.026 (0.66)}$ /6\

$\frac{0.265 (6.75)}{0.245 (6.22)}$ -D-

$\frac{0.009 (0.23)}{0.004 (0.10)}$

-C-

-H-

SEATING AND
BASE PLANE

$\frac{0.180 (4.57)}{0.170 (4.32)}$

$\frac{0.370 (9.40)}{0.325 (8.26)}$

0.03 (0.76) MIN

SIDE VIEW

$\frac{0.007 (0.18)}{0.004 (0.10)}$

LEAD FINISH

BASE
METAL

$\frac{0.009 (0.23)}{0.004 (0.10)}$

$\frac{0.019 (0.48)}{0.015 (0.38)}$

0.0015 (0.04)
MAX

$\frac{0.022 (0.56)}{0.015 (0.38)}$

/3\

SECTION A-A

NOTES:

/1.\ Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.

/2.\ If a pin one identification mark is used in addition to or instead of a tab, the limits of the tab dimension do not apply.

/3.\ The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.

/4.\ Measure dimension at all four corners.

5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

/6.\ Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.

7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.

8. Controlling dimension: INCH.