NCV7351

High Speed CAN Transceiver

The NCV7351 CAN transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus and may be used in both 12 V and 24 V systems. The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller.

The NCV7351 is an addition to the CAN high−speed transceiver family complementing NCV734x CAN stand−alone transceivers and previous generations such as AMIS42665, AMIS3066x, etc. Due to the wide common−mode voltage range of the receiver inputs and other design features, the NCV7351 is able to reach outstanding levels of electromagnetic susceptibility (EMS). Similarly, extremely low electromagnetic emission (EME) is achieved by the excellent matching of the output signals.

KEY FEATURES

General

- Compatible with the ISO 11898−2 Standard
- High Speed (up to 1 Mbps)
- V_{IO} Pin on NCV7351D13 Version Allowing Direct Interfacing with 3 V to 5 V Microcontrollers
- EN Pin on NCV7351D1E Version Allowing Switching the Transceiver to a Very Low Current OFF Mode
- Excellent Electromagnetic Susceptibility (EMS) Level Over Full Frequency Range. Very Low Electromagnetic Emissions (EME) Low EME also Without Common Mode (CM) Choke
- Bus Pins Protected Against >15 kV System ESD Pulses
- Transmit Data (TxD) Dominant Time−out Function
- Under all Supply Conditions the Chip Behaves Predictably. No Disturbance of the Bus Lines with an Unpowered Node
- Bus Pins Short Circuit Proof to Supply Voltage and Ground
- Bus Pins Protected Against Transients in an Automotive Environment
- Thermal Protection
- These are Pb−Free Devices

Quality

- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

Typical Applications

- Automotive
- Industrial Networks

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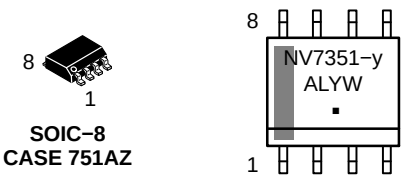
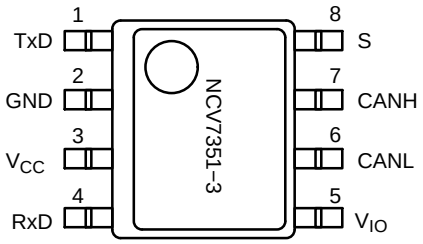
http://onsemi.com

MARKING DIAGRAM

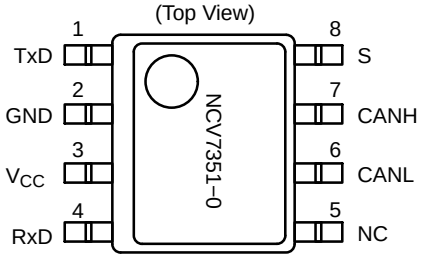


NV7351− = Specific Device Code
y = 3, 0, or E
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

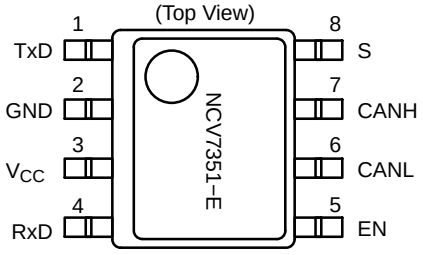
PIN ASSIGNMENT



NCV7351D13R2G
(Top View)



NCV7351D10R2G
(Top View)



NCV7351D1ER2G
(Top View)

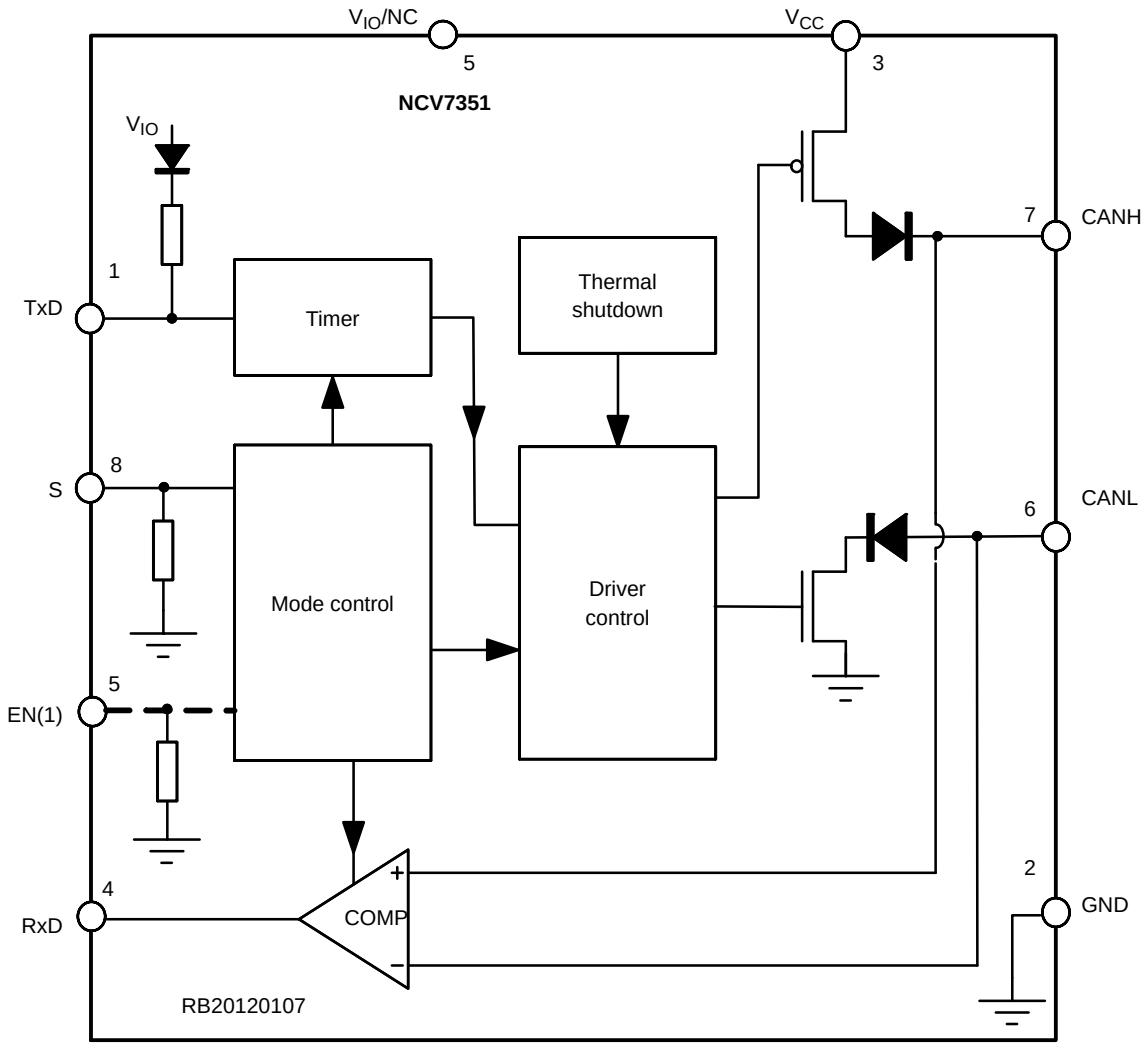
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

Table 1. KEY TECHNICAL CHARACTERISTICS AND OPERATING RANGES

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Power supply voltage		4.5	5.5	V
V_{UV}	Undervoltage detection voltage on pin V_{CC}		3.5	4.5	V
V_{CANH}	DC voltage at pin CANH	$0 < V_{CC} < 5.5$ V; no time limit	−50	+50	V
V_{CANL}	DC voltage at pin CANL	$0 < V_{CC} < 5.5$ V; no time limit	−50	+50	V
$V_{CANH,L}$	DC voltage between CANH and CANL pin	$0 < V_{CC} < 5.5$ V	−50	+50	V
$V_{CANH,Lmax}$	DC voltage at pin CANH and CANL during load dump condition	$0 < V_{CC} < 5.5$ V, less than one second	−	+58	V
V_{ESD}	Electrostatic discharge voltage	IEC 61000−4−2 at pins CANH and CANL	−15	15	kV
$V_{O(dif)(bus\_dom)}$	Differential bus output voltage in dominant state	$45\ \Omega < R_{LT} < 65\ \Omega$	1.5	3	V
CM−range	Input common−mode range for comparator	Guaranteed differential receiver threshold and leakage current	−30	+35	V
I_{CC}	Supply current	Dominant; $V_{TxD} = 0$ V Recessive; $V_{TxD} = V_{CC}$	− 2.5	72 7.5	mA
I_{CCS}	Supply current in silent mode		1.4	3.5	mA
t_{pd}	Propagation delay TxD to RxD	See Figure 5	90	245	ns
T_J	Junction temperature		−40	150	°C

BLOCK DIAGRAM



(1) Only present in the NCV7351D1ER2G
(2) Connected to V_{CC} on versions without V_{IO} pin

Figure 1. Block Diagram of NCV7351

Table 2. NCV7351: PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Pin Type	Pin Function
1	TxD	digital input, internal pull−up	Transmit data input; low input → dominant driver
2	GND	ground	Ground
3	V_{CC}	supply	Supply voltage
4	RxD	digital output	Receive data output; dominant bus → low output
5	NC	not connected	Not connected, NCV7351−0 version only
	V_{IO}	supply	Supply voltage for digital inputs/outputs, NCV7351−3 Version only
	EN	digital input, internal pull−down	Enable control input, NCV7351−E version only
6	CANL	high voltage input/output	Low−level CAN bus line (low in dominant mode)
7	CANH	high voltage input/output	High−level CAN bus line (high in dominant mode)
8	S	digital input, internal pull−down	Silent mode control input

APPLICATION INFORMATION

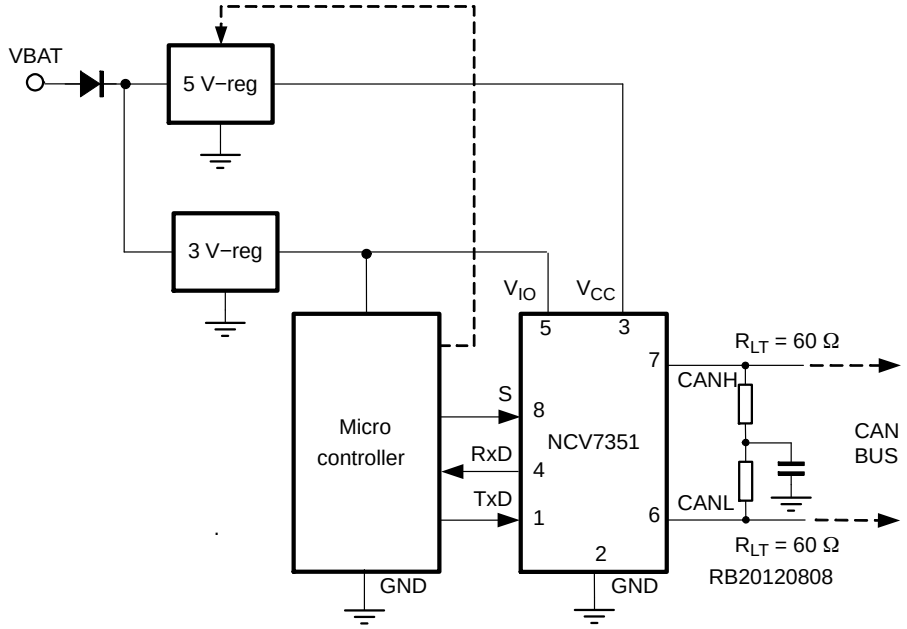


Figure 2. NCV7351−3 Application Diagram

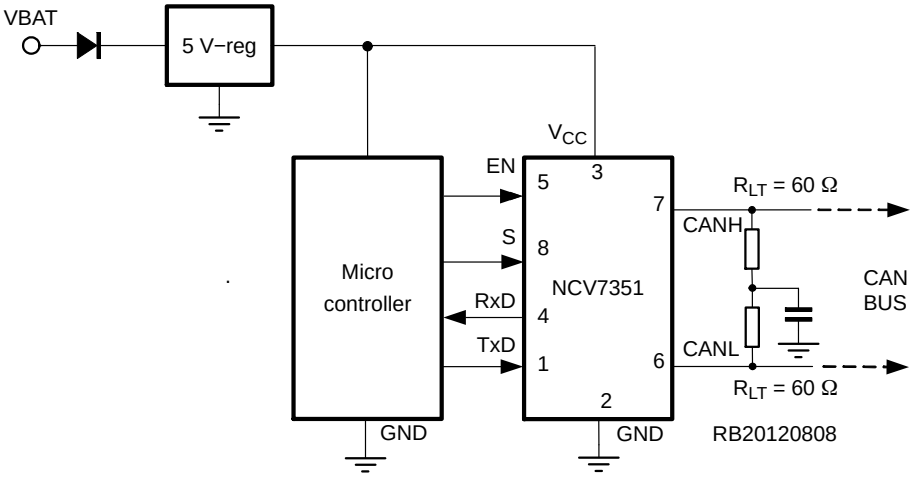


Figure 3. NCV7351−E Application diagram

FUNCTIONAL DESCRIPTION

NCV7351 has three versions which differ from each other only by function of pin 5. (See also Table 2)

NCV7351−3: Pin 5 is V_{IO} pin, which is supply pin for transceiver digital inputs/output (supplying pins TxD, RxD, S, EN). The V_{IO} pin should be connected to microcontroller supply pin. By using V_{IO} supply pin shared with microcontroller the I/O levels between microcontroller and transceiver are properly adjusted. This allows in applications with microcontroller supply down to 3 V to easy communicate with the transceiver. (See Figure 2)

NCV7351−0: Pin 5 is not connected. This version is full replacement of the previous generation CAN transceiver AMIS30660.

NCV7351−E: Pin 5 is digital enable pin which allows transceiver to be switched off with very low supply current.

OPERATING MODES

The NCV7351 modes of operation are provided as illustrated in Table 3. These modes are selectable through pin S and also EN in case of NCV7351−E.

Table 3. OPERATING MODES

Mode	Pin S	Pin EN (Note 1)	Pin TxD	CANH,L Pins	RxD
Normal	0	1	0	Dominant	0
	0	1	1	Recessive	1
Silent	1	1	X	Recessive	1
	1	1	X	Dominant (Note 3)	0
Off (Note 1)	X	0	X	floating	floating

1. Only applicable to NCV7351−E
2. 'X' = don't care
3. CAN bus driven to dominant by another transceiver on the bus

Normal Mode

In the normal mode, the transceiver is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the pins TxD and RxD. The slopes on the bus lines outputs are optimized to give low EME.

Silent Mode

In the silent mode, the transmitter is disabled. The bus pins are in recessive state independent of TxD input. Transceiver listens to the bus and provides data to controller, but controller is prevented from sending any data to the bus.

Off Mode

In Off mode, complete transceiver is disabled and consumes very low current. The CAN pins are floating not loading the CAN bus.

Over−temperature Detection

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds a value of approximately 180°C. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off−state resets when the temperature decreases below the shutdown threshold and pin TxD goes high. The thermal protection circuit is particularly needed in case of the bus line short circuits.

TxD Dominant Time−out Function

A TxD dominant time−out timer circuit prevents the bus lines being driven to a permanent dominant state (blocking all network communication) if pin TxD is forced permanently low by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TxD. If the duration of the low−level on pin TxD exceeds the internal timer value t_{dom}, the transmitter is disabled, driving the bus into a recessive state. The timer is reset by a positive edge on pin TxD. This TxD dominant time−out time ($t_{dom(TxD)}$) defines the minimum possible bit rate to 12 kbps.

Fail Safe Features

A current−limiting circuit protects the transmitter output stage from damage caused by accidental short circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

The pins CANH and CANL are protected from automotive electrical transients (according to ISO 7637; Figure 4). Internally, pin TxD is pulled high, pin EN and S low should the input become disconnected. Pins TxD, S, EN and RxD will be floating, preventing reverse supply should the V_{CC} supply be removed.

Definitions: All voltages are referenced to GND (pin 2). Positive currents flow into the IC. Sinking current means the current is flowing into the pin; sourcing current means the current is flowing out of the pin.

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{sup}	Supply voltage V_{CC}		−0.3	+6	V
V_{CANH}	DC voltage at pin CANH	$0 < V_{CC} < 5.5$ V; no time limit	−50	+50	V
V_{CANL}	DC voltage at pin CANL	$0 < V_{CC} < 5.5$ V; no time limit	−50	+50	V
V_{IOs}	DC voltage at pin TxD, RxD, S, EN, V_{IO}	Notes 4 and 5	−0.3	6	V
V_{esd}	Electrostatic discharge voltage at all pins according to EIA−JESD22	Note 6	−6	6	kV
	Electrostatic discharge voltage at CANH,CANL, pins according to EIA−JESD22	Note 6	−8	8	kV
	Electrostatic discharge voltage at CANH, CANL pins According to IEC 61000−4−2	Note 7	−15	15	kV
	Standardized charged device model ESD pulses according to ESD−STM5.3.1−1999		750	750	V
V_{schaff}	Transient voltage at CANH, CANL pins, See Figure 4	Note 8	−150	100	V
Latch−up	Static latch−up at all pins	Note 9		150	mA
T_{stg}	Storage temperature		−55	+150	°C
T_J	Maximum junction temperature		−40	+170	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. EN pin Only available on NCV7351−E version
5. V_{IO} pin Only available on NCV7351−3 version
6. Standardized human body model electrostatic discharge (ESD) pulses in accordance to EIA−JESD22. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
7. System human body model electrostatic discharge (ESD) pulses. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor referenced to GND. Verified by external test house
8. Pulses 1, 2a,3a and 3b according to ISO 7637 part 3. Results were verified by external test house.
9. Static latch−up immunity: Static latch−up protection level when tested according to EIA/JESD78.

Table 5. THERMAL CHARACTERISTICS

Symbol	Parameter	Conditions	Value	Unit
$R_{\theta JA\_1}$	Thermal Resistance Junction−to−Air, 1S0P PCB (Note 10)	Free air	125	K/W
$R_{\theta JA\_2}$	Thermal Resistance Junction−to−Air, 2S2P PCB (Note 11)	Free air	75	K/W

10. Test board according to EIA/JEDEC Standard JESD51−3, signal layer with 10% trace coverage.
11. Test board according to EIA/JEDEC Standard JESD51−7, signal layers with 10% trace coverage.

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to 5.5 V; T_J = −40°C to +150°C; R_{LT} = 60 Ω unless specified otherwise.
On chip versions without V_{IO} pin reference voltage for all digital inputs and outputs is V_{CC} instead of V_{IO}.

Table 6. CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY (Pin V_{CC})						
I_{CC}	Supply current in normal mode	Dominant; V_{TxD} = 0 V Recessive; V_{TxD} = V_{IO}	− 2.5	50 4.6	72 7.5	mA
I_{CCS}	Supply current in silent mode		1.4	2.3	3.5	mA
I_{CCOFF}	Supply current in OFF mode on NCV7351−E version only		−	7	18	μA
I_{CCOFF}	Supply current in OFF mode NCV7351−E version only	$T_J \leq 100°C$, Note 13	−	7	10	μA
V_{UVDVCC}	Undervoltage detection voltage on V_{CC} pin		3.5	4	4.5	V
SUPPLY (Pin V_{IO}) on NCV7351−3 Version Only						
$V_{iorange}$	Supply voltage range on pin V_{IO}		2.8	−	5.5	V
I_{IO}	Supply current on pin V_{IO} normal mode	Dominant; V_{TxD} = 0 V Recessive; V_{TxD} = V_{IO}	100 50	240 125	500 265	μA
I_{IOS}	Supply current on pin V_{IO} silent mode	Bus is recessive; V_{TxD} = V_{IO}	−	2	16	μA
V_{UVDVIO}	Undervoltage detection voltage on V_{IO} pin		2.1	2.4	2.7	V
TRANSMITTER DATA INPUT (Pin TxD)						
V_{IH}	High−level input voltage, on NCV7351−3 version only	Output recessive	0.7 x V_{IO}	−	V_{IO} + 0.3	V
V_{IH}	High−level input voltage, on NCV7351−1 and NCV7351−E versions only	Output recessive	2.7	−	V_{CC} + 0.3	V
V_{IL}	Low−level input voltage	Output dominant	−0.3	−	+0.3 x V_{IO}	V
R_{TxD}	TxD pin pull up		22	30	50	kΩ
C_i	Input capacitance	Note 13	−	5	10	pF
TRANSMITTER MODE SELECT (Pin S and EN)						
V_{IH}	High−level input voltage, on NCV7351−3 version only	Silent mode	0.7 x V_{IO}	−	V_{IO} + 0.3	V
V_{IH}	High−level input voltage on NCV7351−1 and NCV7351−E versions only	Silent or enable mode	2.7	−	V_{CC} + 0.3	V
V_{IL}	Low−level input voltage	Normal mode	−0.3	−	0.3 x V_{IO}	V
$R_{S,EN}$	S and EN pin pull down	Note 12	0.55	1.1	1.5	MΩ
C_i	Input capacitance	Note 13	−	5	10	pF
RECEIVER DATA OUTPUT (Pin RxD)						
I_{OH}	High−level output current	Normal mode V_{RxD} = V_{IO} – 0.4 V	−1	−0.4	−0.1	mA
I_{OL}	Low−level output current	V_{RxD} = 0.4 V	1.5	6	11	mA
BUS LINES (Pins CANH and CANL)						

12. EN pin Only available on NCV7351−E version
13. Not tested in production. Guaranteed by design and prototype evaluation.

Table 6. CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BUS LINES (Pins CANH and CANL)						
$V_{o(reces)(norm)}$	Recessive bus voltage on pins CANH and CANL	$V_{TxD} = V_{IO}$; no load normal mode	2.0	2.5	3.0	V
$I_{o(reces)(CANH)}$	Recessive output current at pin CANH	−30 V < V_{CANH}< +35 V; 0 V < V_{CC} < 5.5 V	−2.5	−	+2.5	mA
$I_{o(reces)\ (CANL)}$	Recessive output current at pin CANL	−30 V < V_{CANL} < +35 V; 0 V < V_{CC} < 5.5 V	−2.5	−	+2.5	mA
$I_{LI(CANH)}$	Input leakage current to pin CANH	0 Ω < R(V_{CC} to GND) < 1 MΩ $V_{CANL} = V_{CANH}$ = 5 V	−10	0	10	μA
$I_{LI(CANL)}$	Input leakage current to pin CANL		−10	0	10	μA
$V_{o(dom)(CANH)}$	Dominant output voltage at pin CANH	V_{TxD} = 0 V; V_{CC} = 4.75 V to 5.25 V	3.0	3.6	4.25	V
$V_{o(dom)\ (CANL)}$	Dominant output voltage at pin CANL	V_{TxD} = 0 V; V_{CC} = 4.75 V to 5.25 V	0.5	1.4	1.75	V
$V_{o(dif)(bus\_dom)}$	Differential bus output voltage (V_{CANH} − V_{CANL})	V_{TxD} = 0 V; dominant; V_{CC} = 4.75 V to 5.25 V 45 Ω < R_{LT} < 65 Ω	1.5	2.25	3.0	V
$V_{o(dif)\ (bus\_rec)}$	Differential bus output voltage (V_{CANH} − V_{CANL})	$V_{TxD} = V_{IO}$; recessive; no load	−120	0	+50	mV
$V_{o(sym)(bus\_dom)}$	Bus output voltage symmetry V_{CANH} + V_{CANL}	V_{TxD} = 0 V V_{CC} = 4.75 V to 5.25 V	0.9	−	1.1	V_{CC}
$I_{o(sc)\ (CANH)}$	Short circuit output current at pin CANH	V_{CANH} = 0 V; V_{TxD} = 0 V	−90	−70	−40	mA
$I_{o(sc)\ (CANL)}$	Short circuit output current at pin CANL	V_{CANL} = 36 V; V_{TxD} = 0 V	40	70	100	mA
$V_{i(dif)\ (th)}$	Differential receiver threshold voltage	−12 V < V_{CANL} < +12 V; −12 V < V_{CANH} < +12 V;	0.5	0.7	0.9	V
$V_{ihcm(dif)\ (th)}$	Differential receiver threshold voltage for high common−mode	−30 V < V_{CANL} < +35 V; −30 V < V_{CANH} < +35 V;	0.40	0.7	1.0	V
$R_{i(cm)\ (CANH)}$	Common−mode input resistance at pin CANH		15	26	37	kΩ
$R_{i(cm)\ (CANL)}$	Common−mode input resistance at pin CANL		15	26	37	kΩ
$R_{i(cm)\ (m)}$	Matching between pin CANH and pin CANL common mode input resistance	$V_{CANH} = V_{CANL}$	−0.8	0	+0.8	%
$R_{i(dif)}$	Differential input resistance		25	50	75	kΩ
$C_{i(CANH)}$	Input capacitance at pin CANH	$V_{TxD} = V_{IO}$; not tested	−	7.5	20	pF
$C_{i(CANL)}$	Input capacitance at pin CANL	$V_{TxD} = V_{IO}$; not tested	−	7.5	20	pF
$C_{i(dif)}$	Differential input capacitance	$V_{TxD} = V_{IO}$; not tested	−	3.75	10	pF
THERMAL SHUTDOWN						
$T_{J(sd)}$	Shutdown junction temperature	Junction temperature rising	160	180	200	°C
TIMING CHARACTERISTICS (see Figures 5 and 6)						
$t_{d(TxD-BUSon)}$	Delay TxD to bus active	C_i = 100 pF between CANH to CANL	−	75	−	ns
$t_{d(TxD-BUSoff)}$	Delay TxD to bus inactive	C_i = 100 pF between CANH to CANL	−	65	−	ns
$t_{d(BUSon-RxD)}$	Delay bus active to RxD	C_{rxd} = 15 pF	−	70	−	ns
$t_{d(BUSoff-RxD)}$	Delay bus inactive to RxD	C_{rxd} = 15 pF	−	70	−	ns
t_{pd}	Propagation delay TxD to RxD (both edges)	C_i = 100 pF between CANH to CANL	90	140	245	ns
$t_{dom(TxD)}$	TxD dominant time for time−out	V_{TxD} = 0 V	1.5	2.5	5	ms

12. EN pin Only available on NCV7351−E version
13. Not tested in production. Guaranteed by design and prototype evaluation.

MEASUREMENT SETUPS AND DEFINITIONS

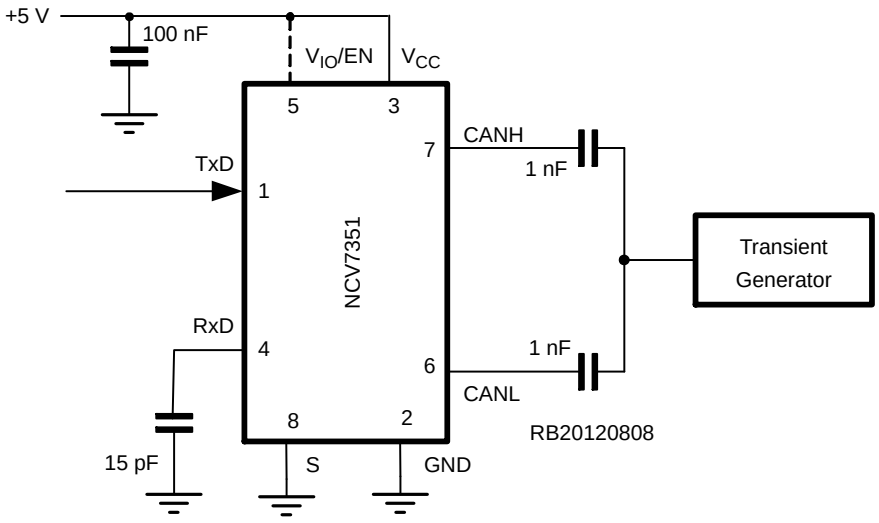


Figure 4. Test Circuit for Automotive Transients

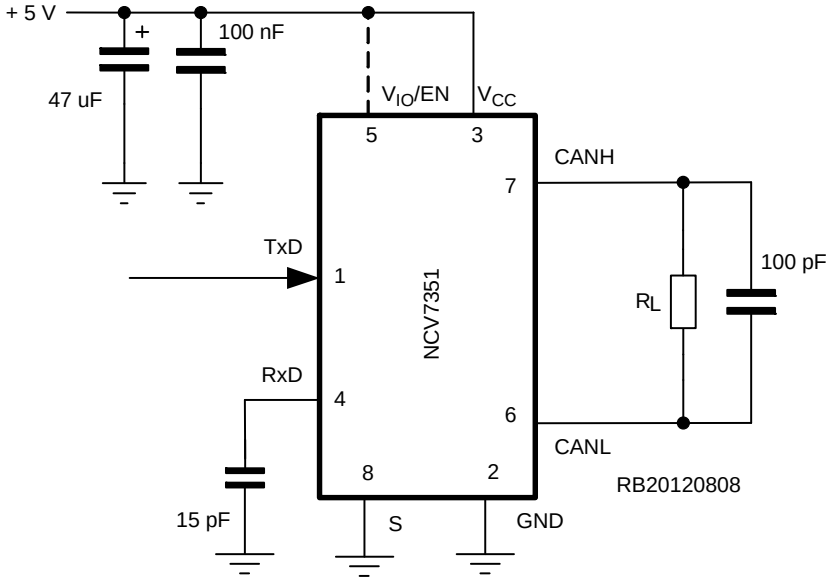


Figure 5. Test Circuit for Timing Characteristics

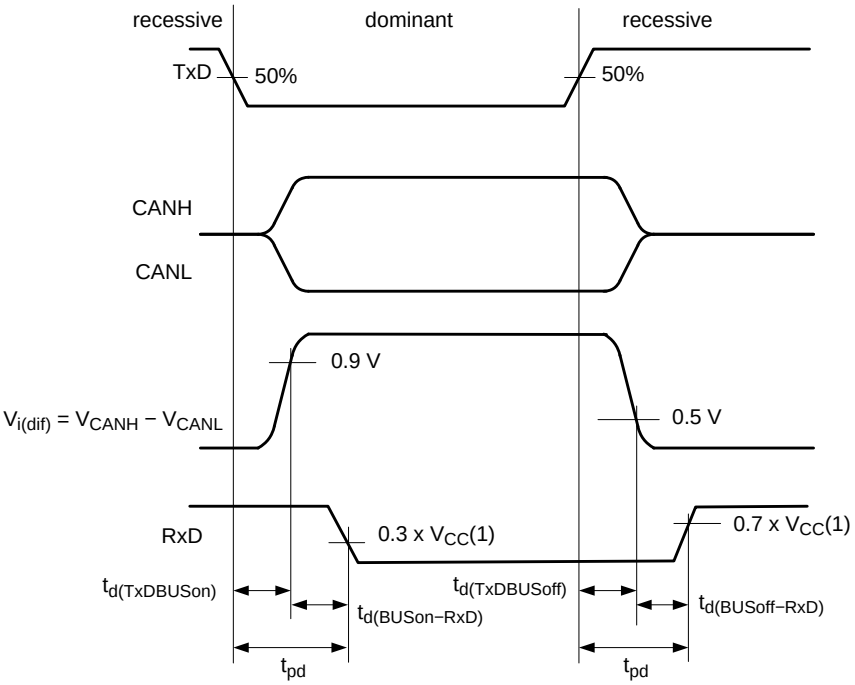


Figure 6. Transceiver Timing Diagram

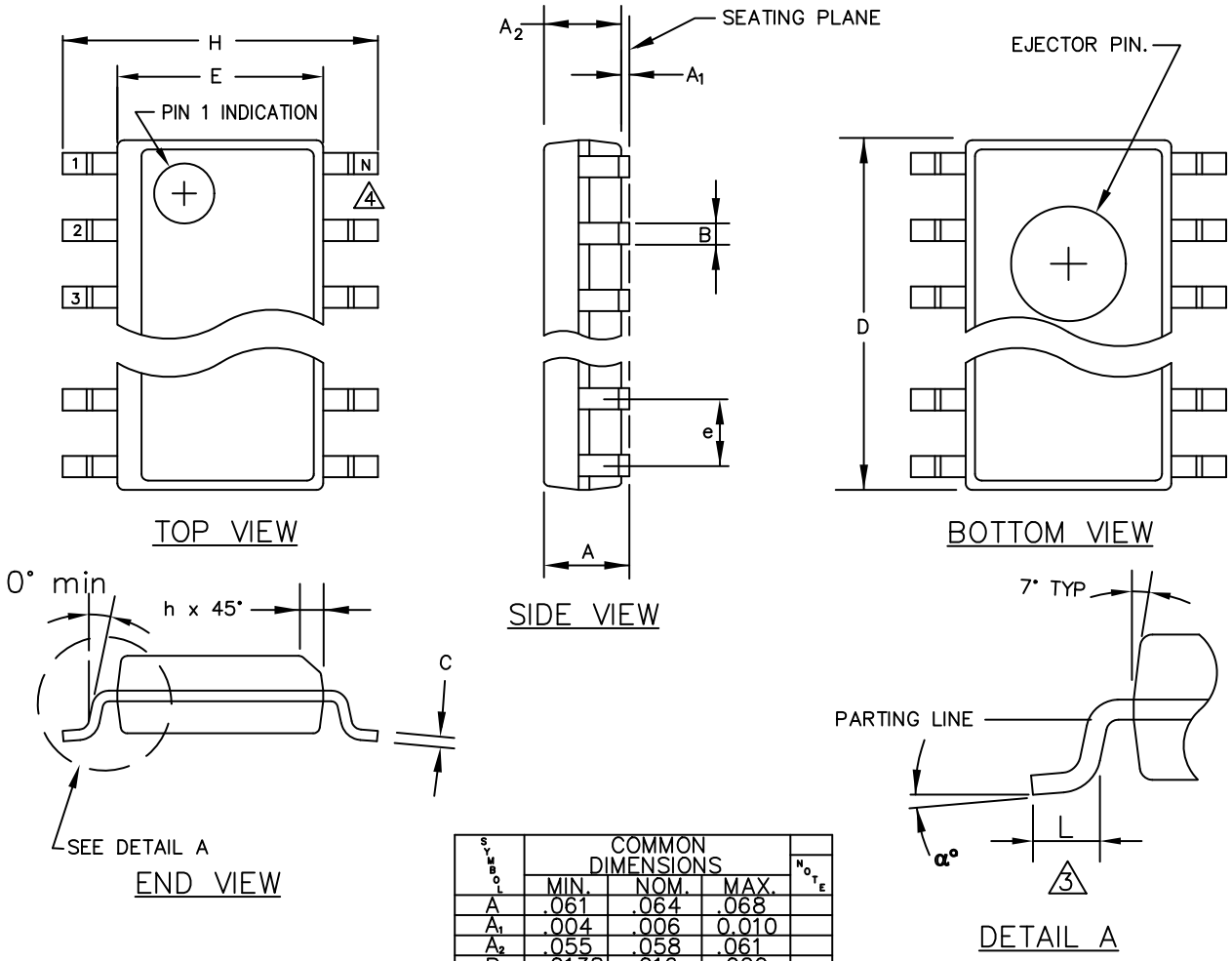
DEVICE ORDERING INFORMATION

Part Number	Description	Temperature Range	Package	Shipping†
NCV7351D13R2G	High Speed CAN Transceiver with V_{IO} pin	−40°C to +125°C	SOIC 150 8 GREEN (Matte Sn, JEDEC MS−012) (Pb−Free)	3000 / Tape & Reel
NCV7351D10R2G	High Speed CAN Transceiver with pin 5 NC			
NCV7351D1ER2G	High Speed CAN Transceiver with EN pin			

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

SOIC 8
CASE 751AZ
ISSUE O



SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	.061	.064	.068	
A_1	.004	.006	0.010	
A_2	.055	.058	.061	
B	.0138	.016	.020	
C	.0075	.008	.0098	
D	SEE VARIATIONS			1
E	.150	.155	.157	
e	.050 BSC			
H	.230	.236	.244	
h	.010	.013	.016	
L	.016	.025	.035	
N	SEE VARIATIONS			2
α°	0°	5°	8°	

VARIATIONS				
	1			2
	D			N
NOTE	MIN.	NOM.	MAX.	
AA	.189	.194	.196	8
AB	.337	.342	.344	14
AC	.386	.391	.393	16

1. ALL DIMENSIONS ARE IN MILLIMETERS.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
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NCV7351/D