5.0Gbps, 1-Lane, PCIe 2.0 ReDriver™ with I²C Programming Interface

Features

- PCIe 2.0 compatible
- Two 5.0Gbps differential signal pairs
- Adjustable Receiver Equalization
- 100Ω Differential CML I/O's
- Pin Configured Output Emphasis and Output Swing Control
- Input signal level detect and squelch for each channel
- Automatic Receiver Detect
- Low Power : ~330mW (3.3V)/~150mW (1.5V)
- Industrial Temp Support -40°C~ +85°C
- Stand-by Mode – Power Down State
- Two power options: 3.3V or 1.5V
- Packaging: 20-Pin TQFN (4x4mm)

Figure 1. Pin Diagram (Top Side View)

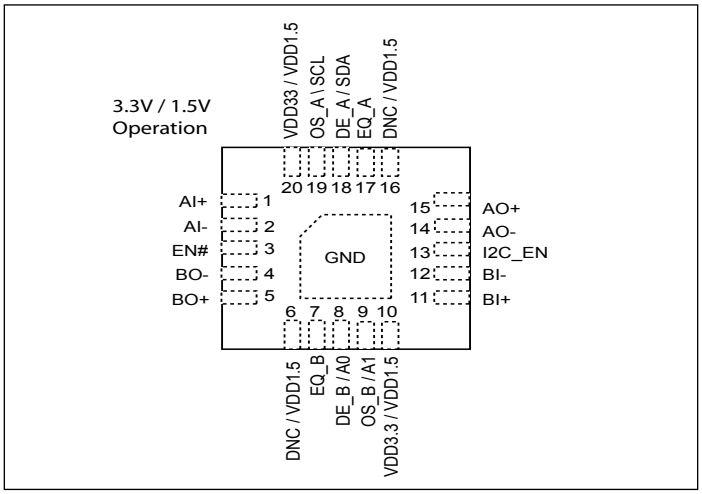
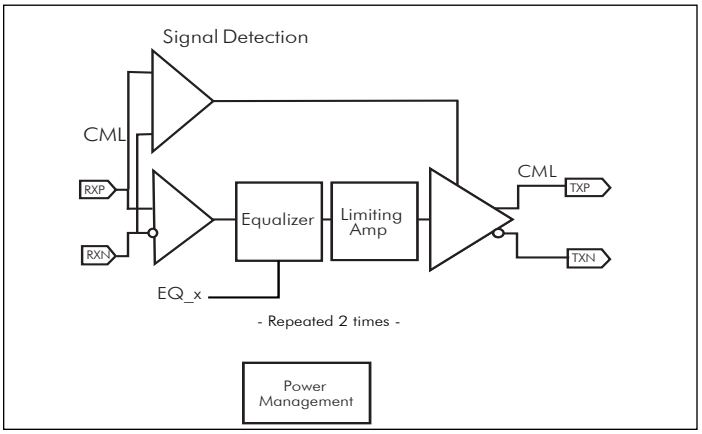


Figure 2. Block Diagram

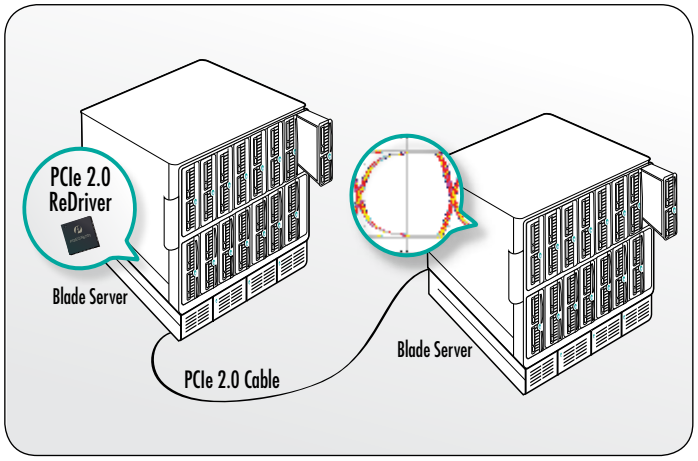


Description

Pericom Semiconductor's PI3EQX5801 is a low power, high performance 5.0 Gbps signal ReDriver™ designed specifically for the PCIe 2.0 protocol. The device provides programmable equalization, De-Emphasis, and output swing controls to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference. PI3EQX5801 supports two 100Ω Differential CML data I/O's between the Protocol ASIC to a switch fabric, over cable, or to extend the signals across other distant data pathways on the user's platform. The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver. A low-level input signal detection and output squelch function is provided for each channel.

When the channels are enabled, EN# = 0, and operating, that channels' input signal level (on xI+/-) determines whether the output is active. If the input signal level of the channel falls below the active threshold level (Vth-) then the outputs are driven to the common mode voltage. In addition to signal conditioning, when EN# = 1, the device enters a low power standby mode. The PI3EQX5801 also includes a fully programmable I²C interface. When I²C control mode is enabled, I2C_EN = 1, equalization, output swing, and de-emphasis settings can be adjusted by programming the related registers.

Figure 3



Pin Description

Pin #	Pin Name	Type	Description
1 2 11 12	AI+ AI- BI+ BI-	Input	CML input channels with selectable input termination between 50Ω to internal V_{bias} or internal 60kΩ pull-down to GND.
3	EN#	Input	Chip Enable. When the pin is driven "Low", chip is in normal operation. When the pin is driven “High”, chip is in power down mode. With internal 200kΩ pull-down resistor.
4 5 14 15	BO- BO+ AO- AO+	Output	Selectable output termination between 50Ω to internal V_{bias} 2kΩ to internal V_{bias}, or Hi-Z.
6 16	DNC / VDD1.5	DNC / Power	Do Not Connect / 1.5V Voltage Supply
7 17	EQ_B, EQ_A	Input	Set the equalization of two channels. These are Tri-level input pins. When set to "HIGH" the pin becomes Logic "1"; when set to "open", the pin becomes "open", when set to "low", the pin becomes logic "0". Please refer to Mode Adjustment on page 3.
8	DE_B / A0	Input	Set the de-emphasis of the output CML buffer for Channel B. This is a Tri-level input pins When set to "high", the pin becomes logic "1"; when set to "open", the pin becomes "open"; when set to "low", the pin becomes logic "0". Please refer to Mode Adjustment on page 3. This pin is also used for I²C programming interface. When set to "high" or floating I²C address bit A0 is set to "1". When set to "low" I²C address bit A0 is set to "0".
9	OS_B / A1	Input	Set the output swing of Channel B. This is a Tri-level input pins When set to "HIGH", the pin becomes Logic "1"; when set to "open", the pin becomes "open", when set to "low", the pin becomes logic "0". This pin is also used for I²C programming interface. When set to "high" or floating I²C address bit A1 is set to "1". When set to "low" I²C address bit A1 is set to "0".
10 20	VDD3.3 / VDD1.5	Power	3.3V Voltage Supply / 1.5V Voltage Supply
13	I2C_EN	Input	I²C Control Enable. When the pin is driven “High”, chip is in I²C Control Mode. When the pin is driven “Low”, chip is in pin strap control mode. With internal 200kΩ pull-down resistor.
18	DE_A / SDA	Input / Output	Set the de-emphasis of the output CML buffer for Channel A. These is a Tri-level input pin. When set to "high", the pin becomes logic "1"; when set to "open", the pin becomes "open"; when set to "low", the pin becomes logic "0". Please refer to Mode Adjustment on page 3. This pin is also used as Data Line for I²C programming interface 3.3V tolerant.
19	OS_A / SCL	Input	Set the output swing of Channel A. This is a Tri-level input pins When set to "HIGH", the pin becomes Logic "1"; when set to "open", the pin becomes "open", when set to "low", the pin becomes logic "0". This pin is also used as Clock Line for I²C programming interface3.3 tolerant.
Center Pad	GND	GND	Supply Ground.

Configuration Table

EN#	Function	Input R	Output R
1	Channels disable if EN# is high, Chip Power Down	60kΩ to GND	Hi-Z
0	Chip and channels enabled	50Ω	50Ω

I2C_EN	Function
1	I²C Mode is enabled when I²C_EN pin is pulled up to "1"
0	I²C Mode is disabled and configured in Pin-strap control when I²C_EN pin is pulled down to "0"

Mode Adjustment

Equalization Setting through Pin Strap:

EQ_A/B are the selection pins for the equalization selection for each direction.

Equalizer setting	
EQ_A/B	@ 2.5GHz
0	3.3 dB
NC	8.1 dB (Default)
1	11.7 dB

Equalization Setting through I²C Programming Interface:

Equalizer setting	
A/B_CH Byte Register [7:4]*	@ 2.5GHz
0000	0 dB
0001	3.3 dB
0010	4.5 dB
0011	5.6 dB
0100	6.8 dB
0101	7.4 dB
0110	8.1 dB (Default)
0111	8.7 dB
1000	9.3 dB
1001	10 dB
1010	10.8 dB
1011	11.7 dB
1100	12.5 dB
1101	13.3 dB
1110	14.2 dB
1111	15 dB

Note: *Bits A/B_CH[3:0] are for other settings, see I²C register definition

Output Swing Setting through Pin Strap:

OS_A/B are the selection pins for the output swing selection for each direction.

Output swing setting	
OS_A/B	Output swing @ 5Gbps
0	900mVppd
NC (Default)	1000mVppd (Default)
V_{DD}	1200mVppd

Output Swing Setting through I²C Programming Interface:

Output swing setting	
A/B_CH[3:2]*	Output swing @ 5Gbps
00	900mVppd
01	1000mVppd (Default)
10	1100mVppd
11	1200mVppd

Note: *Bits A/B_CH[7:4,1:0] are for other settings, see I²C register definition

De-emphasis Setting through Pin Strap:

DE_A/B are the selection pins for the de-emphasis selection for each direction.

De-emphasis setting	
DE_A/B	De-emphasis @ 5Gbps
0	0dB
NC	-3.5dB (Default)
V_{DD}	-6dB

De-emphasis Setting through I2C Programming Interface:

De-emphasis setting	
A/B_CH[1:0]*	De-emphasis @ 5Gbps
00	0dB
01	-2dB
10	-3.5dB (Default)
11	-6dB

Note: *Bits A/B_CH[7:2] are for other settings, see I2C register definition

Transferring Data

Every byte put on the SDA line must be 8-bits long. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (see the I2C Data Transfer diagram). The PI3EQX5801 will never hold the clock line SCL LOW to force the master into a wait state.

Note: Block-write and Block-read transfers have a fixed offset of 0x00, because of the very small number of configuration bytes. An offset byte presented by a host to the PI3EQX5801 is not used.

Addressing

Up to four PI3EQX5801 devices can be connected to a single I2C bus. The PI3EQX5801 supports 7-bit addressing, with the LSB indicating either a read or write operation. The address for a specific device is determined by the A0 and A1 input pins.

Address Assignment							
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/W**
1	1	0	0	0	Programmable		1=R, 0=W

Acknowledge

Data transfer with acknowledge is required from the master. When the master releases the SDA line (HIGH) during the acknowledge clock pulse, the PI3EQX5801 will pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse as indicated in the I2C Data Transfer diagram. The PI3EQX5801 will generate an acknowledge after each byte has been received.

Data Transfer

A data transfer cycle begins with the master issuing a start bit. After recognizing a start bit, the PI3EQX5801 will watch the next byte of information for a match with its address setting. When a match is found it will respond with a read or write of data on the following clocks. Each byte must be followed by an acknowledge bit, except for the last byte of a read cycle which ends with a stop bit. For a write cycle, the first data byte following the address byte is a dummy or fill byte that is not used by the PI3EQX5801. This byte is provided to provided compatibility with systems implementing 10-bit addressing. Data is transferred with the most significant bit (MSB) first.

I2C Data Transfer

Start & Stop Conditions

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition, as shown in the figure below.

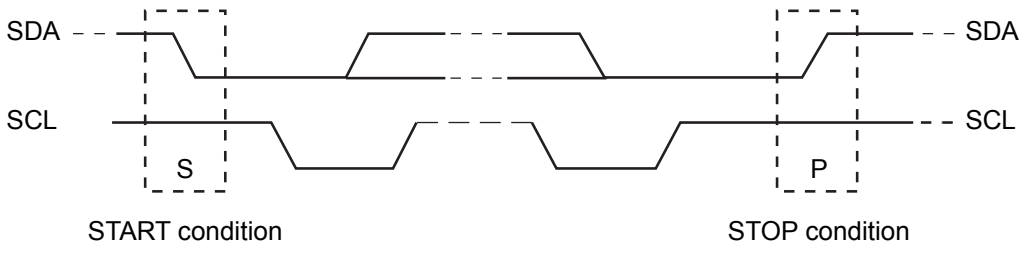
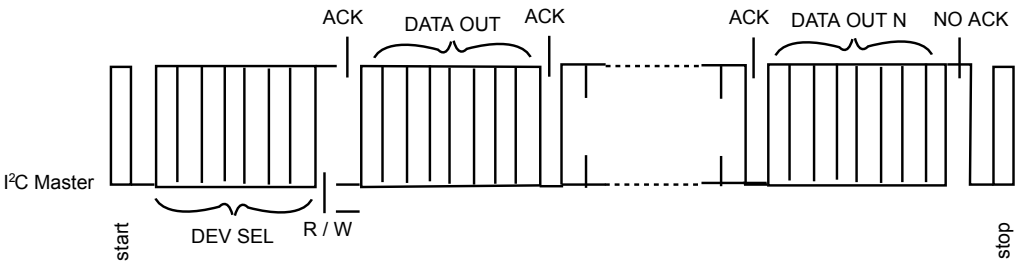


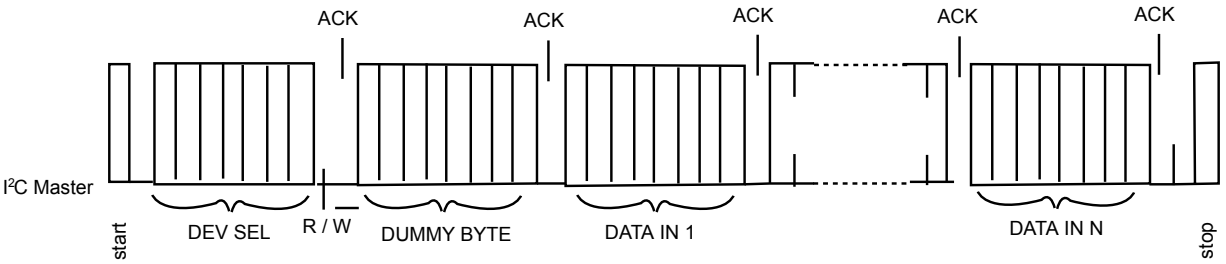
Figure 4. I2C START and STOP conditions.

I²C Data Transfer

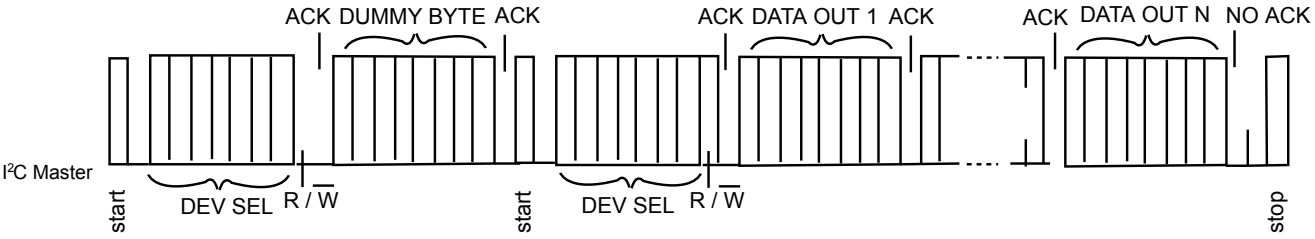
1. Read sequence



2. Write sequence



3. Combined sequence



Notes:
1. only block read and block write from the lowest byte are supported for this application.
2. for some I2C application, an offset address byte will be presented at the second byte in write command, which is called dummy byte here and will be simply ignored in this application for correct interoperation.

Register Description

BYTE 0 - Channel A Setting Register (A_CH[7:0])

Bit	Type	Power-on State	Control Signal	Description
7	R/W	latch from pin	A_EQ[3]	Controls Equalization setting of CH A
6	R/W	latch from pin	A_EQ[2]	Default setting is 8.1dB; latched from pin A_EQ
5	R/W	latch from pin	A_EQ[1]	
4	R/W	latch from pin	A_EQ[0]	
3	R/W	0	A_OS[1]	Controls output swing of CH A.
2	R/W	1	A_OS[0]	Default setting is 1000mVppd; A_OS[1:0]="01"
1	R/W	1	A_DE[1]	Controls output de-emphasis of CH A
0	R/W	0	A_DE[0]	Default setting is -3.5dB; A_DE[1:0]="10"

BYTE 1 - Channel B Setting Register (B_CH[7:0])

Bit	Type	Power-on State	Control Signal	Description
7	R/W	latch from pin	B_EQ[3]	Controls Equalization setting of CH B
6	R/W	latch from pin	B_EQ[2]	Default setting is 8.1dB; latched from pin B_EQ
5	R/W	latch from pin	B_EQ[1]	
4	R/W	latch from pin	B_EQ[0]	
3	R/W	0	B_OS[1]	Controls output swing of CH B
2	R/W	1	B_OS[0]	Default setting is 1000mVppd; B_OS[1:0]="01"
1	R/W	1	B_DE[1]	Controls output de-emphasis of CH B
0	R/W	0	B_DE[0]	Default setting is -3.5dB; B_DE[1:0]="10"

BYTE 2 - Global Function Setting Register (GBL_FUNC[7:0])

Bit	Type	Power-on State	Control Signal	Description
7	R/W	1	TDET_EN	Termination Detect Enable
6	R/W	0	APD_EN	Auto Slumber Mode Enable
5	R/W	0	ADE_EN	Auto-De-emphasis Enable
4	R/W	0	EM_HALF	Half bit de-emphasis Enable
3	R/W	0	UNPLUG_EN	Unplug detector Enable
2	R/W	1	UNPLUG_VTH	Unplug Detector Threshold
1	R/W	Latch from pin	A_PD	Channel A Power Down; latched from pin EN#
0	R/W	Latch from pin	B_PD	Channel B Power Down, latched from pin EN#

BYTE 3 - Channel A Status Register (A_STAT[7:0])

Bit	Type	Power-on State	Control Signal	Description
7	R	N/A	TDET_A	"HIGH" indicates receiver detected at channel A
6	R	N/A	APD_A	"HIGH" indicates power saving mode at channel A
5	R	N/A	SDET_A	"HIGH" indicates signal detected at channel A
4	R	N/A	ADE_A	"HIGH" indicates de-emphasis enable @5Gbps data only at channel A
3	R	0	Reserved	
2	R	0	Reserved	
1	R	0	Reserved	
0	R	0	Reserved	

BYTE 4 - Channel B Status Register (B_STAT[7:0])

Bit	Type	Power-on State	Control Signal	Description
7	R	N/A	TDET_B	"HIGH" indicates receiver detected at channel B
6	R	N/A	APD_B	"HIGH" indicates power saving mode at channel B
5	R	N/A	SDET_B	"HIGH" indicates signal detected at channel B
4	R	N/A	ADE_B	"HIGH" indicates de-emphasis enable @5Gbps data only at channel B
3	R	0	Reserved	
2	R	0	Reserved	
1	R	0	Reserved	
0	R	0	Reserved	

BYTE 5 - RESREVED, Offset = 0x05, Default Power On State = "00010000"

BYTE 6-14 - RESREVED

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +4.6V
DC SIG Voltage	–0.5V to V_{DD} +0.5V
Current Output	–25mA to +25mA
Power Dissipation Continuous	1W
Operating Temperature	-40 to +85°C
ESD, Human Body Model	–6kv to +6kV
ESD, Machine Model	–200V to +200V
ESD, Charged Device Model	–500V to +500V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC Electrical Characteristics

3.3V/1.5V Power Supply Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD33}	Power Supply Voltage 3.3V		3.0		3.6	V
$P_{STANDBY33}$	Supply Power Standby	EN# = 1		0.18	1.8	mW
P_{DEVICE_UNPLUG}	Supply Power Device Unplug	EN# = 0, TDET = 0		7.3	9	
$P_{ACTIVE33}$	Supply Power Active	EN# = 0, $V_{RX\text{-}DIFF\text{-}P} \geq V_{TH\text{-}SD}$, Output Swing = 900mVppd		330	430	
$V_{DD1.5}$	Power Supply Voltage 1.5V		1.35		1.65	V
$P_{STANDBY1.5}$	Supply Power Standby	EN# = 1		0.08	0.825	mW
P_{DEVICE_UNPLUG}	Supply Power Device Unplug	EN# = 0, TDET = 0		3.3	4.125	
$P_{ACTIVE1.5}$	Supply Power Active	EN# = 0, $V_{RX\text{-}DIFF\text{-}P} \geq V_{TH\text{-}SD}$, Output Swing = 900mVppd		150	198	
$I_{DD\text{-}STANDBY}$	Supply Current Standby	EN# = 1			0.5	mA
$I_{DD\text{-}DEVICE\_UNPLUG}$	Supply Current Device Unplug	EN# = 0, TDET = 0		2.2	2.5	mA
$I_{DD\text{-}ACTIVE}$	Supply Current Active	Output Swing = 900mV_{ppd}		100	120	

AC/DC Electrical Characteristics (Continued..)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{PD}	Latency	From input to output		1	2	ns
CML Receiver Input (100Ω Differential)						
Z_{RX-DC}	DC Input Impedance		40	50	60	Ω
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance		80	100	120	
$V_{RX-DIFFP-P}$	Differential Input Peak-to-peak Voltage		175		1200	mV
$V_{RX-CM-ACP}$	AC Peak Common Mode Input Voltage				150	
V_{TH-SD}	Signal detect Threshold	EN# = 0	65		175	mVppd
J_{RS}	Residual Jitter(1,2)	Total Jitter			0.3	Ulp-p

Notes

1. K28.7 pattern is applied differentially at point A as shown in Figure 5.
2. Total jitter does not include the signal source jitter. Total jitter (TJ) = (14.1 × RJ + DJ) where RJ is random RMS jitter and DJ is maximum deterministic jitter. Signal source is a K28.5 ± pattern (00 1111 1010 11 0000 0101) for the deterministic jitter test and K28.7 (0011111000) or equivalent for random jitter test. Residual jitter is that which remains after equalizing media-induced losses of the environment of Figure 1 or its equivalent. The deterministic jitter at point B must be from media-induced loss, and not from clock source modulation. Jitter is measured at 0V at point C of Figure 5.

AC/DC Electrical Characteristics (Continued..)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
CML Transmitter Output (100Ω differential)[1]						
Z_{OUT}	Output Resistance	Single-Ended	40	50	60	Ω
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance		72	100	120	
$V_{TX-DIFFP-P}$	Differential Peak-to-peak Output Voltage	$V_{TX-DIFFP-P} = 2 * \lvert V_{TX-D+} - V_{TX-D-} \rvert$	900		1200	mV
V_{TX-C}	Common-Mode Voltage	$\lvert V_{TX-D+} + V_{TX-D-} \rvert /2$	0.5		1.2	V
V_{cm_ac}	TX AC common mode voltage				100	mVpp
$V_{TX-Pre-Ratio-max}$	Max TX De-emphasis Level				-6	dB
$C_{AC-coupling}$	AC coupling capacitor		75		200	nF
LVCMOS Control Pins (Pins: 3, 13)						
V_{IH}	Input High Voltage (Bi-Level)		0.65 × V_{DD}			
V_{IL}	Input Low Voltage (Bi-Level)				0.35 × V_{DD}	
Tri-level Control Pins (Pins: 7, 17, 8, 18, 9, 19)						

AC/DC Electrical Characteristics (Continued..)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage (Tri-Level)[2]		$0.8V_{DD}$			V
V_{MID}	Input mid level		$0.4V_{DD}$		$0.6V_{DD}$	
V_{IL}	Input Low Voltage (Tri-Level)				$0.2V_{DD}$	
I_{IH}	Input High Current, $V_{IH} = V_{DD}$				50	µA
I_{IL}	Input Low Current, $V_{IL} = 0V$		-50			

Note:
1. Recommended output coupling capacitor is 75nF to 200nF (on each output)
2. $V_{DD} = V_{DD}33$ or $V_{DD}1.5$

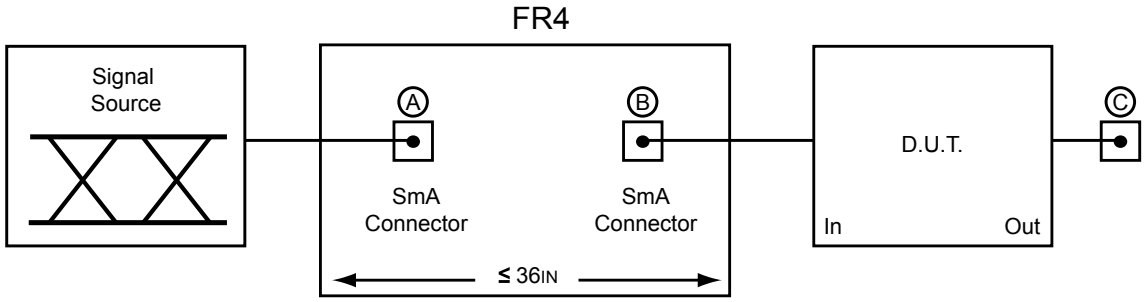
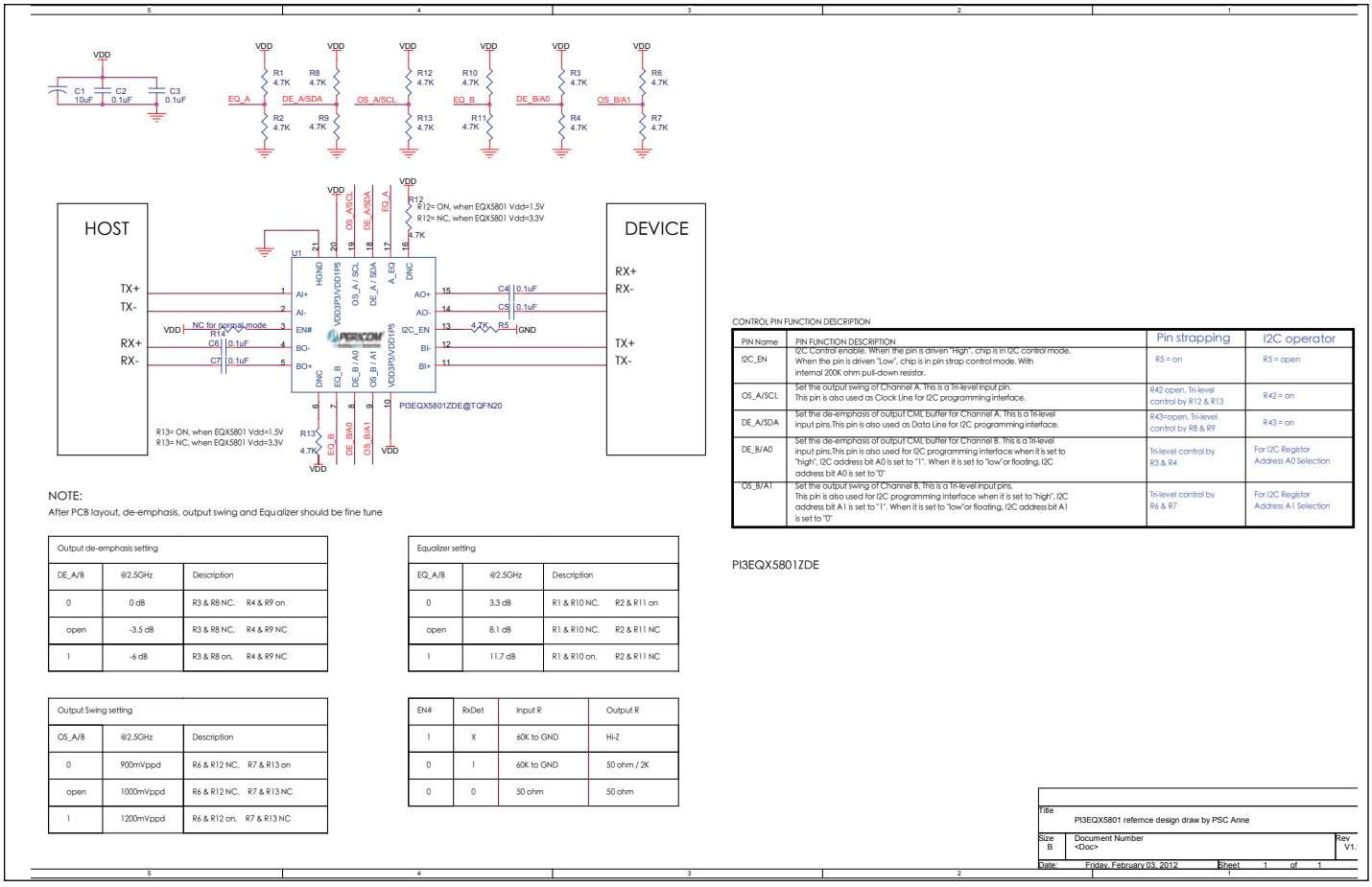


Figure 5. Test Condition Referenced in the Electrical Characteristic Table



NOTE:
After PCB layout, de-emphasis, output swing and Equalizer should be fine tune

Output de-emphasis setting		
DE_A/B	@2.5GHz	Description
0	0 dB	R3 & R8 NC, R4 & R9 on
open	-3.5 dB	R3 & R8 NC, R4 & R9 NC
1	-6 dB	R3 & R8 on, R4 & R9 NC

Equalizer setting		
EQ_A/B	@2.5GHz	Description
0	3.3 dB	R1 & R10 NC, R2 & R11 on
open	8.1 dB	R1 & R10 NC, R2 & R11 NC
1	11.7 dB	R1 & R10 on, R2 & R11 NC

Output Swing setting		
OS_A/B	@2.5GHz	Description
0	900mVppd	R6 & R12 NC, R7 & R13 on
open	1000mVppd	R6 & R12 NC, R7 & R13 NC
1	1200mVppd	R6 & R12 on, R7 & R13 NC

EN#	RxDet	Input R	Output R
1	X	60K to GND	Hi-Z
0	1	60K to GND	50 ohm / 2K
0	0	50 ohm	50 ohm

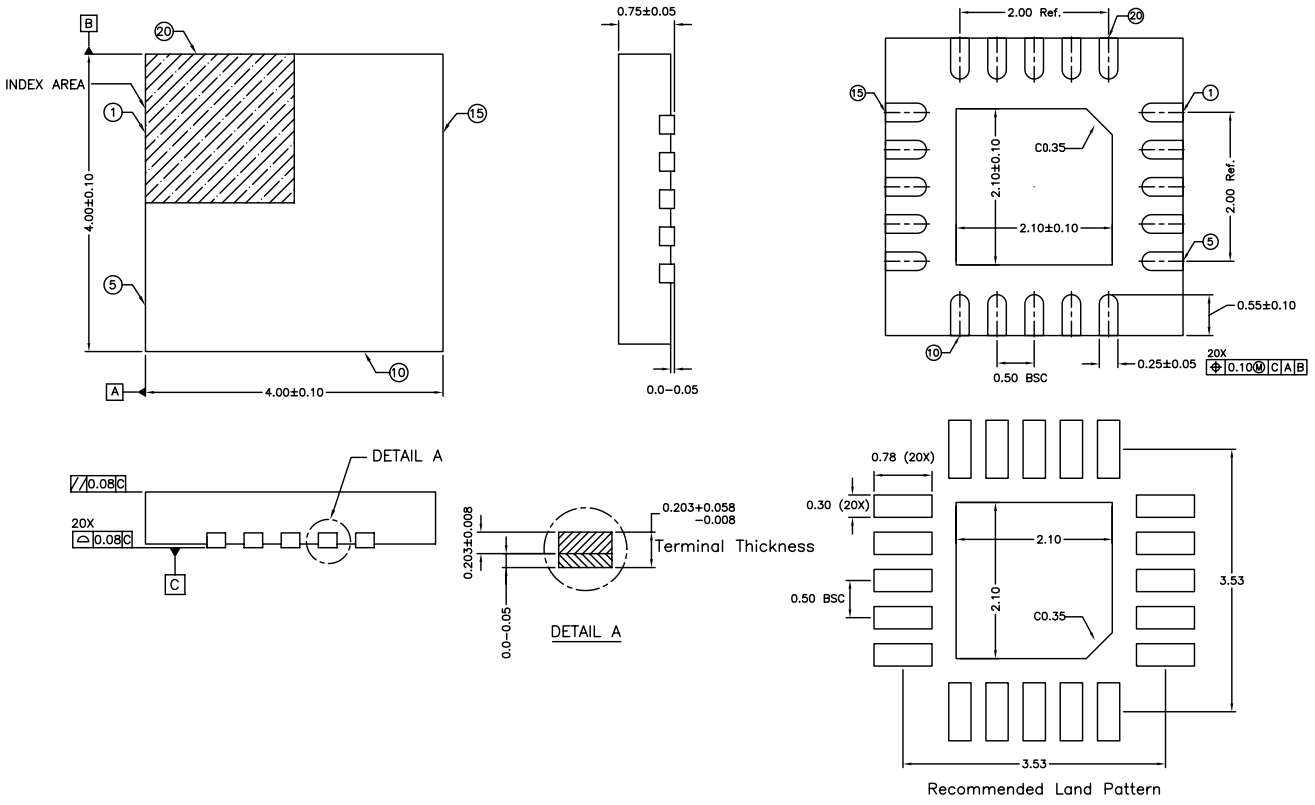
CONTROL PIN FUNCTION DESCRIPTION

PIN Name	PIN FUNCTION DESCRIPTION	Pin strapping	I2C operator
I2C_EN	I2C Control enable. When the pin is driven "High", chip is in I2C control mode. When the pin is driven "Low", chip is in pin strap control mode. With internal 200K ohm pull-down resistor.	R5 = on	R5 = open
OS_A/SCL	Set the output swing of Channel A. This is a tri-level input pin. This pin is also used as Clock Line for I2C programming interface.	R42 open, Tri-level control by R12 & R13	R42 = on
DE_A/SDA	Set the de-emphasis of output CML buffer for Channel A. This is a tri-level input pins.This pin is also used as Data Line for I2C programming interface.	R43=open, Tri-level control by R8 & R9	R43 = on
DE_B/A0	Set the de-emphasis of output CML buffer for Channel B. This is a tri-level input pins.This pin is also used for I2C programming interface when it is set to "high", I2C address bit A0 is set to "1". When it is set to "low"or floating, I2C address bit A0 is set to "0"	Tri-level control by R3 & R4	For I2C Registor Address A0 Selection
OS_B/A1	Set the output swing of Channel B. This is a tri-level input pins. This pin is also used for I2C programming interface when it is set to "high", I2C address bit A1 is set to "1". When it is set to "low"or floating, I2C address bit A1 is set to "0"	Tri-level control by R6 & R7	For I2C Registor Address A1 Selection

PI3EQX5801ZDE

Title: PI3EQX5801 refernce design draw by PSC Anne
Size: B | Document Number: <Doc> | Rev: V1.
Date: Friday, February 03, 2012 | Sheet 1 of 1

Packaging Mechanical: 20-contact TQFN (ZD)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.08 mm.
4. REFER JEDEC MO–220.

PERICOM Semiconductor Corporation

DATE: 09/11/08

DESCRIPTION: 20-Lead, Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZD20

DOCUMENT CONTROL #: PD-2084 **REVISION: --**

Ordering Information

Ordering Number	Package Code	Package Description
PI3EQX5801ZDE	ZD	Pb-Free and Green 20-pin TQFN (4x4mm)

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel