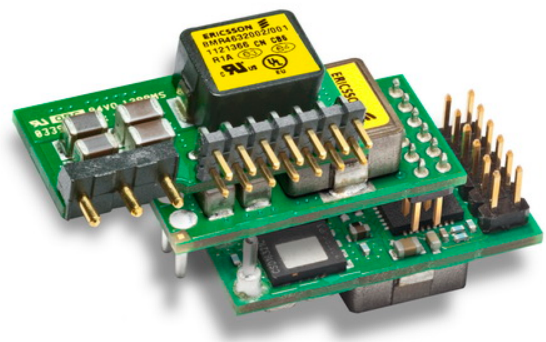
ERICSSON

Technical Specification

BMR 463 series POL Regulators Input 4.5-14 V, Output up to 25 A / 82.5 W	EN/LZT 146 434 R4B February 2014

Key Features

- Small package
  25.65 x 13.8 x 8.2 mm (1.01 x 0.543 x 0.323 in)
  SIP: 26.3 x 7.6 x 15.6 mm (1.035 x 0.30 x 0.614 in)
- 0.6 V - 3.3 V output voltage range
- High efficiency, typ. 97.1% at 5Vin, 3.3Vout half load
- Configuration and Monitoring via PMBus
- Adaptive compensation of PWM control loop & fast loop transient response
- Synchonization & phase spreading
- Current sharing, Voltage Tracking & Voltage margining
- MTBF 20.2 Mh



General Characteristics

- For narrow board pitch applications (15 mm/0.6 in)
- Non-Linear Response for reduction of decoupling cap.
- Input under voltage shutdown
- Over temperature protection
- Output short-circuit & Output over voltage protection
- Remote Control & Power Good
- Voltage setting via pin-strap or PMBus
- Advanced Configurable via Graphical Used Interface
- ISO 9001/14001 certified supplier
- Highly automated manufacturing ensures quality

Safety Approvals

Design for Environment

Meets requirements in high-temperature lead-free soldering processes.

Contents

Ordering Information

Product program	Output
BMR 463 x002/001 (x=0,1,2)	0.6-3.3 V, 20 A/ 66 W
BMR 463 2102/001	0.6-3.3 V, 20 A/ 66 W
BMR 463 x006/001 (x=0,1)	0.6-3.3 V, 20 A/ 66 W
BMR 463 x008/001 (x=0,1,2)	0.6-3.3 V, 25 A/ 82.5 W
BMR 463 x009/001 (x=0,1)	0.6-3.3 V, 25 A/ 82.5 W

Product number and Packaging

BMR 463 $n_1n_2n_3n_4/n_5n_6n_7n_8$									
Options	n_1	n_2	n_3	n_4	/	n_5	n_6	n_7	n_8
Mounting	o				/				
Mechanical		o			/				
Hardware Variants			o	o	/				
Configuration					/	o	o	o	
Packaging					/				o

Options	Description	
n_1	0 1 2	Through hole mount version (TH) Surface mount version (SMD) Single in line (SIP)
n_2	0 1	Standard mechanical option 5.5mm pin length (for SIP)
n_3 n_4	02 06 08 09	20 A, Pin 4A = Voltage Tracking pin 20 A, Pin 4A = Power Good pin 25 A, Pin 4A = Voltage Tracking pin, Dynamic Loop Compensation 25 A, Pin 4A = Power Good pin, Dynamic Loop Compensation
n_5 n_6 n_7	001 002	CTRL pin positive logic (active high) CTRL pin negative logic (active low)
n_8	B C	Antistatic tray of 100 products (SIP only) Antistatic tape & reel of 200 products (Sample delivery available in lower quantities. Not for SIP)

Example: Product number BMR 463 0002/001C equals a through-hole mounted, standard mechanical option, voltage tracking pin at 4A, positive RC logic, package tape&reel.

General Information

Reliability

The failure rate (λ) and mean time between failures (MTBF= $1/\lambda$) is calculated at max output power and an operating ambient temperature (T_A) of +40°C. Ericsson Power Modules uses Telcordia SR-332 Issue 2 Method 1 to calculate the mean steady-state failure rate and standard deviation (σ).

Telcordia SR-332 Issue 2 also provides techniques to estimate the upper confidence levels of failure rates based on the mean and standard deviation.

Mean steady-state failure rate, λ	Std. deviation, σ
49 nFailures/h	12.4 nFailures/h

MTBF (mean value) for the BMR 463 series = 20.2 Mh.
MTBF at 90% confidence level = 15.3 Mh

Compatibility with RoHS requirements

The products are compatible with the relevant clauses and requirements of the RoHS directive 2002/95/EC and have a maximum concentration value of 0.1% by weight in homogeneous materials for lead, mercury, hexavalent chromium, PBB and PBDE and of 0.01% by weight in homogeneous materials for cadmium.

Exemptions in the RoHS directive utilized in Ericsson Power Modules products are found in the Statement of Compliance document.

Ericsson Power Modules fulfills and will continuously fulfill all its obligations under regulation (EC) No 1907/2006 concerning the registration, evaluation, authorization and restriction of chemicals (REACH) as they enter into force and is through product materials declarations preparing for the obligations to communicate information on substances in the products.

Quality Statement

The products are designed and manufactured in an industrial environment where quality systems and methods like ISO 9000, Six Sigma, and SPC are intensively in use to boost the continuous improvements strategy. Infant mortality or early failures in the products are screened out and they are subjected to an ATE-based final test. Conservative design rules, design reviews and product qualifications, plus the high competence of an engaged work force, contribute to the high quality of our products.

Warranty

Warranty period and conditions are defined in Ericsson Power Modules General Terms and Conditions of Sale.

Limitation of Liability

Ericsson Power Modules does not make any other warranties, expressed or implied including any warranty of merchantability or fitness for a particular purpose (including, but not limited to, use in life support applications, where malfunctions of product can cause injury to a person's health or life).

Safety Specification

General information

Ericsson Power Modules DC/DC converters and DC/DC regulators are designed in accordance with safety standards IEC/EN/UL 60950-1 *Safety of Information Technology Equipment*.

IEC/EN/UL 60950-1 contains requirements to prevent injury or damage due to the following hazards:

- Electrical shock
- Energy hazards
- Fire
- Mechanical and heat hazards
- Radiation hazards
- Chemical hazards

On-board DC/DC converters and DC/DC regulators are defined as component power supplies. As components they cannot fully comply with the provisions of any safety requirements without “Conditions of Acceptability”. Clearance between conductors and between conductive parts of the component power supply and conductors on the board in the final product must meet the applicable safety requirements. Certain conditions of acceptability apply for component power supplies with limited stand-off (see Mechanical Information for further information). It is the responsibility of the installer to ensure that the final product housing these components complies with the requirements of all applicable safety standards and regulations for the final product.

Component power supplies for general use should comply with the requirements in IEC 60950-1, EN 60950-1 and UL 60950-1 *Safety of Information Technology Equipment.* There are other more product related standards, e.g. IEEE 802.3 *CSMA/CD (Ethernet) Access Method*, and ETS-300132-2 *Power supply interface at the input to telecommunications equipment, operated by direct current (dc)*, but all of these standards are based on IEC/EN/UL 60950-1 with regards to safety.

Ericsson Power Modules DC/DC converters and DC/DC regulators are UL 60950-1 recognized and certified in accordance with EN 60950-1.

The flammability rating for all construction parts of the products meet requirements for V-0 class material according to IEC 60695-11-10, *Fire hazard testing, test flames* – 50 W horizontal and vertical flame test methods.

The products should be installed in the end-use equipment, in accordance with the requirements of the ultimate application. Normally the output of the DC/DC converter is considered as SELV (Safety Extra Low Voltage) and the input source must be isolated by minimum Double or Reinforced Insulation from the primary circuit (AC mains) in accordance with IEC/EN/UL 60950-1.

Isolated DC/DC converters

It is recommended that a slow blow fuse is to be used at the input of each DC/DC converter. If an input filter is used in the circuit the fuse should be placed in front of the input filter.
In the rare event of a component problem that imposes a short circuit on the input source, this fuse will provide the following functions:

- Isolate the fault from the input power source so as not to affect the operation of other parts of the system.
- Protect the distribution wiring from excessive current and power loss thus preventing hazardous overheating.

The galvanic isolation is verified in an electric strength test. The test voltage (V_{iso}) between input and output is 1500 Vdc or 2250 Vdc (refer to product specification).

24 V DC systems

The input voltage to the DC/DC converter is SELV (Safety Extra Low Voltage) and the output remains SELV under normal and abnormal operating conditions.

48 and 60 V DC systems

If the input voltage to the DC/DC converter is 75 Vdc or less, then the output remains SELV (Safety Extra Low Voltage) under normal and abnormal operating conditions.

Single fault testing in the input power supply circuit should be performed with the DC/DC converter connected to demonstrate that the input voltage does not exceed 75 Vdc.

If the input power source circuit is a DC power system, the source may be treated as a TNV-2 circuit and testing has demonstrated compliance with SELV limits in accordance with IEC/EN/UL60950-1.

Non-isolated DC/DC regulators

The input voltage to the DC/DC regulator is SELV (Safety Extra Low Voltage) and the output remains SELV under normal and abnormal operating conditions.

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Absolute Maximum Ratings

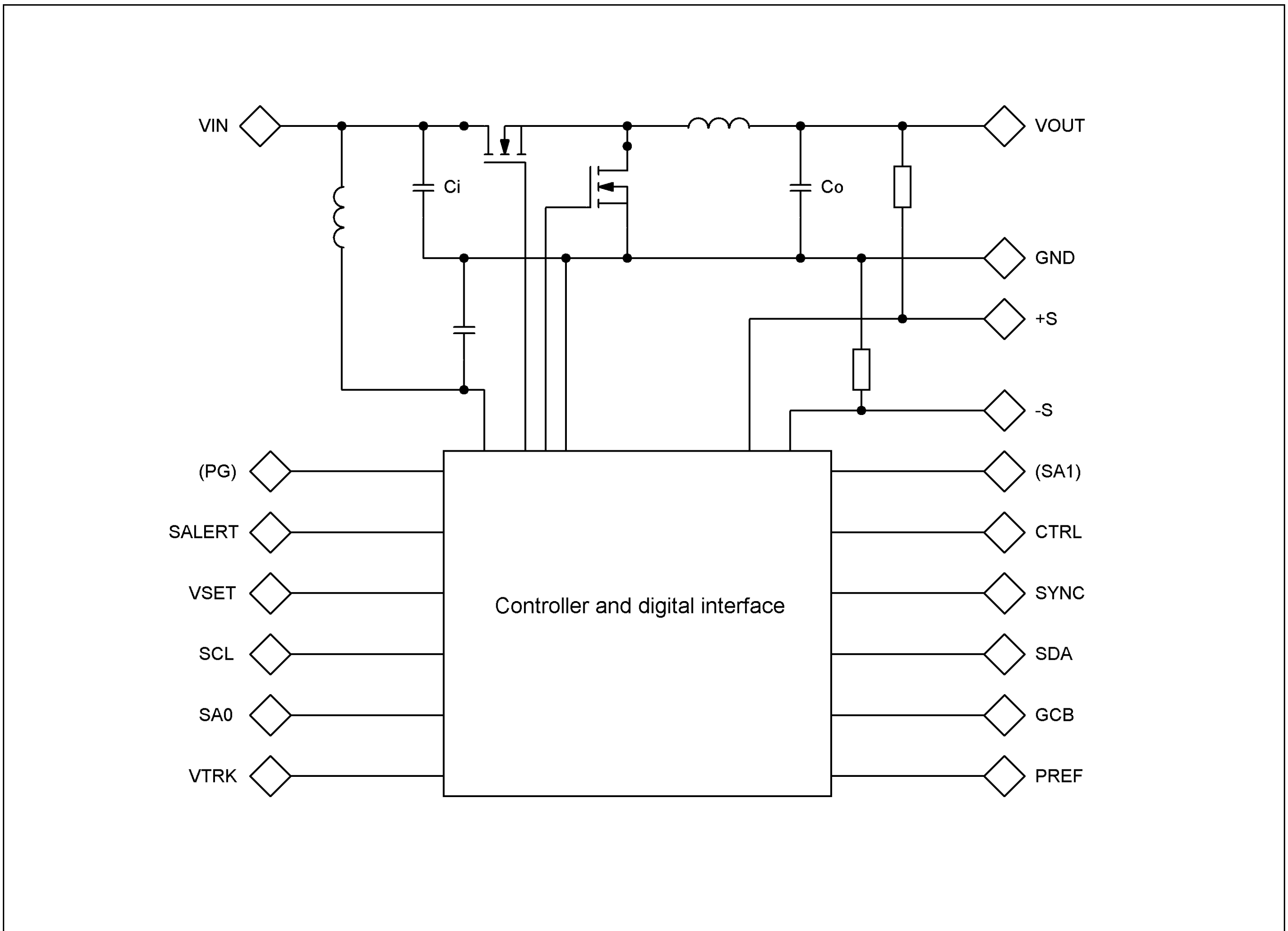
Characteristics		min	typ	max	Unit
T_{P1}	Operating temperature (see Thermal Consideration section)	-40		125	°C
T_S	Storage temperature	-40		125	°C
V_I	Input voltage (See Operating Information Section for input and output voltage relations)	-0.3		16	V
Logic I/O voltage	CTRL, SA0, SA1, SALERT, SCL, SDA, VSET, SYNC, GCB, PG	-0.3		6.5	V
Ground voltage differential	-S, PREF, GND	-0.3		0.3	V
Analog pin voltage	V_O, +S, VTRK	-0.3		6.5	V

Stress in excess of Absolute Maximum Ratings may cause permanent damage. Absolute Maximum Ratings, sometimes referred to as no destruction limits, are normally tested with one parameter at a time exceeding the limits in the Electrical Specification. If exposed to stress above these limits, function and performance may degrade in an unspecified manner.

Configuration File

This product is designed with a digital control circuit. The control circuit uses a configuration file which determines the functionality and performance of the product. The Electrical Specification table shows parameter values of functionality and performance with the default configuration file, unless otherwise specified. The default configuration file is designed to fit most application needs with focus on high efficiency. If different characteristics are required it is possible to change the configuration file to optimize certain performance characteristics. Note that current sharing operation requires changed configuration file. See application notes AN307 and AN312 for further information.
In this Technical specification examples are included to show the possibilities with digital control. See Operating Information section for information about tradeoffs when optimizing certain key performance characteristics.

Fundamental Circuit Diagram



C_i = 70 µF, C_o = 200 µF

Electrical Specification **BMR 463 0002, BMR 463 1002, BMR 463 0006, BMR 463 1006**

T_{P1} = -30 to +95 °C, V_I = 4.5 to 14 V, $V_I > V_O$ + 1.0 V
Typical values given at: T_{P1} = +25 °C, V_I = 12.0 V, max I_O, unless otherwise specified under Conditions.
Default configuration file, 190 10-CDA 102 0175/001.
External C_{IN} = 470 µF/10 mΩ, C_{OUT} = 470 µF/10 mΩ. See Operating Information section for selection of capacitor types.
Sense pins are connected to the output pins.

	Characteristics		Conditions	min	typ	max	Unit
V_I	Input voltage rise time		monotonic			2.4	V/ms
V_O	Output voltage without pin strap				1.2		V
V_O	Output voltage adjustment range			0.60		3.3	V
V_O	Output voltage adjustment including margining		See Note 17	0.54		3.63	V
V_O	Output voltage set-point resolution				±0.025		% V_O
V_O	Output voltage accuracy		Including line, load, temp. See Note 14	-1		1	%
V_O	Output voltage accuracy		Current sharing operation See Note 15	-2		2	%
V_O	Internal resistance +S/-S to VOUT/GND				4.7		Ω
V_O	Line regulation		V_O = 0.6 V		2		mV
			V_O = 1.0 V		2		
			V_O = 1.8 V		2		
			V_O = 3.3 V		3		
V_O	Load regulation; I_O = 0 - 100%		V_O = 0.6 V		3		mV
			V_O = 1.0 V		2		
			V_O = 1.8 V		2		
			V_O = 3.3 V		2		
V_{Oac}	Output ripple & noise C_O = 470 µF (minimum external capacitance). See Note 11		V_O = 0.6 V		20		mVp-p
			V_O = 1.0 V		30		
			V_O = 1.8 V		40		
			V_O = 3.3 V		60		
I_O	Output current			0		20	A
I_S	Static input current at max I_O		V_O = 0.6 V		1.26		A
			V_O = 1.0 V		1.94		
			V_O = 1.8 V		3.31		
			V_O = 3.3 V		5.89		
I_{lim}	Current limit threshold			22		30	A
I_{sc}	Short circuit current	RMS, hiccup mode, See Note 3	V_O = 0.6 V		8		A
			V_O = 1.0 V		6		
			V_O = 1.8 V		5		
			V_O = 3.3 V		4		
η	Efficiency	50% of max I_O	V_O = 0.6 V		84.0		%
			V_O = 1.0 V		89.3		
			V_O = 1.8 V		92.8		
			V_O = 3.3 V		94.8		
		max I_O	V_O = 0.6 V		79.3		%
			V_O = 1.0 V		86.0		
			V_O = 1.8 V		90.7		
			V_O = 3.3 V		93.6		
P_d	Power dissipation at max I_O		V_O = 0.6 V		3.12		W
			V_O = 1.0 V		3.25		
			V_O = 1.8 V		3.68		
			V_O = 3.3 V		4.52		
P_{li}	Input idling power (no load)	Default configuration: Continues Conduction Mode, CCM	V_O = 0.6 V		0.56		W
			V_O = 1.0 V		0.57		
			V_O = 1.8 V		0.68		
			V_O = 3.3 V		0.99		

Characteristics			Conditions	min	typ	max	Unit
P_{CTRL}	Input standby power	Turned off with CTRL-pin	Default configuration: Monitoring enabled, Precise timing enabled		180		mW
C_i	Internal input capacitance				70		µF
C_o	Internal output capacitance				200		µF
C_{OUT}	Total external output capacitance		See Note 9	300		15 000	µF
C_{OUT}	ESR range of capacitors (per single capacitor)		See Note 9	5		30	mΩ

V_{tr1}	Load transient peak voltage deviation Load step 25-75-25% of max I_O	Default configuration di/dt = 2 A/µs C_O = 470 µF (minimum external capacitance) see Note 12	V_O = 0.6 V		85		mV
			V_O = 1.0 V		85		mV
			V_O = 1.8 V		90		mV
			V_O = 3.3 V		135		mV
t_{tr1}	Load transient recovery time, Note 5 Load step 25-75-25% of max I_O	Default configuration di/dt = 2 A/µs C_O = 470 µF (minimum external capacitance) see Note 12	V_O = 0.6 V		80		µs
			V_O = 1.0 V		90		µs
			V_O = 1.8 V		100		µs
			V_O = 3.3 V		100		µs

f_s	Switching frequency			320		kHz
f_s	Switching frequency range	PMBus configurable		200-640		kHz
f_s	Switching frequency set-point accuracy		-5		5	%
	Control Circuit PWM Duty Cycle		5		95	%
	Minimum Sync Pulse Width		150			ns
	Input Clock Frequency Drift Tolerance	External clock source	-13		13	%

Input Under Voltage Lockout, UVLO	UVLO threshold			3.85		V
	UVLO threshold range	PMBus configurable		3.85-14		V
	Set point accuracy		-150		150	mV
	UVLO hysteresis			0.35		V
	UVLO hysteresis range	PMBus configurable		0-10.15		V
	Delay				2.5	µs
	Fault response	See Note 3		Automatic restart, 70 ms		
Input Over Voltage Protection, IOVP	IOVP threshold			16		V
	IOVP threshold range	PMBus configurable		4.2-16		V
	Set point accuracy		-150		150	mV
	IOVP hysteresis			1		V
	IOVP hysteresis range	PMBus configurable		0-11.8		V
	Delay				2.5	µs
	Fault response	See Note 3		Automatic restart, 70 ms		
Power Good, PG, See Note 2	PG threshold			90		% V_O
	PG hysteresis			5		% V_O
	PG delay			10		ms
	PG delay range	PMBus configurable		0-500		s
Output voltage Over/Under Voltage Protection, OVP/UVP	UVP threshold			85		% V_O
	UVP threshold range	PMBus configurable		0-100		% V_O
	UVP hysteresis			5		% V_O
	OVP threshold			115		% V_O
	OVP threshold range	PMBus configurable		100-115		% V_O
	UVP/OVP response time			25		µs
	UVP/OVP response time range	PMBus configurable		5-60		µs
	Fault response	See Note 3		Automatic restart, 70 ms		

Characteristics		Conditions	min	typ	max	Unit
Over Current Protection, OCP	OCP threshold			26		A
	OCP threshold range	PMBus configurable		0-26		A
	Protection delay,	See Note 4		32		T_{sw}
	Protection delay range	PMBus configurable		1-32		T_{sw}
	Fault response	See Note 3		Automatic restart, 70 ms		
Over Temperature Protection, OTP at P1 See Note 8	OTP threshold			120		°C
	OTP threshold range	PMBus configurable		-40…+120		°C
	OTP hysteresis			15		°C
	OTP hysteresis range	PMBus configurable		0-160		°C
	Fault response	See Note 3		Automatic restart, 240 ms		

V_{IL}	Logic input low threshold	SYNC, SA0, SA1, SCL, SDA, GCB, CTRL, VSET			0.8	V
V_{IH}	Logic input high threshold		2			V
I_{IL}	Logic input low sink current	CTRL			0.6	mA
V_{OL}	Logic output low signal level	SYNC, SCL, SDA, SALERT, GCB, PG			0.4	V
V_{OH}	Logic output high signal level		2.25			V
I_{OL}	Logic output low sink current				4	mA
I_{OH}	Logic output high source current				2	mA
t_{set}	Setup time, SMBus	See Note 1	300			ns
t_{hold}	Hold time, SMBus	See Note 1	250			ns
t_{free}	Bus free time, SMBus	See Note 1	2			ms
C_p	Internal capacitance on logic pins			10		pF

Initialization time		See Note 10		35		ms
Output Voltage Delay Time See Note 6	Delay duration	See Note 16		10		ms
	Delay duration range	PMBus configurable		2-500000		ms
	Delay accuracy turn-on	Default configuration: CTRL controlled Precise timing enabled		±0.25		ms
		PMBus controlled Precise timing disabled Current sharing operation		-0.25/+4		ms
	Delay accuracy turn-off			-0.25/+4		ms
Output Voltage Ramp Time See Note 13	Ramp duration			10		ms
	Ramp duration range	PMBus configurable		0-200		ms
	Ramp time accuracy			100		µs
		Current sharing operation		20		%

	Conditions	min	typ	max	Unit
VTRK Input Bias Current	V_{VTRK} = 5.5 V		110	200	µA
VTRK Tracking Ramp Accuracy (V_O - V_{VTRK})	100% tracking, see Note 7	-100		100	mV
	Current sharing operation 2 phases, 100% tracking V_O = 1.0 V, 10 ms ramp		±100		mV
VTRK Regulation Accuracy (V_O - V_{VTRK})	100% Tracking	-1		1	%
	Current sharing operation 100% Tracking	-2		2	%

	Conditions	min	typ	max	Unit
Current difference between products in a current sharing group	Steady state operation		Max 2 x READ_IOUT monitoring accuracy		
	Ramp-up		2		A
Number of products in a current sharing group				7	

		Conditions	min	typ	max	Unit
Monitoring accuracy	READ_VIN vs V_I			3		%
	READ_VOUT vs V_O			1		%
	READ_IOUT vs I_O	I_O =0-20 A, T_{P1} = 0 to +95 °C V_I = 4.5-14 V, V_O = 1.0 V		±1.4		A
	READ_IOUT vs I_O	I_O =0-20 A, T_{P1} = 0 to +95 °C V_I = 4.5-14 V, V_O = 0.6-3.3 V		±2.6		A

Note 1: See section I2C/SMBus Setup and Hold Times – Definitions.
Note 2: Monitorable over PMBus Interface.
Note 3: Automatic restart ~70 or 240 ms after fault if the fault is no longer present. Continuous restart attempts if the fault reappear after restart. See Operating Information and AN302 for other fault response options.
Note 4: T_{sw} is the switching period.
Note 5: Within +/-3% of V_O
Note 6: See section Soft-start Power Up.
Note 7: Tracking functionality is designed to follow a VTRK signal with slew rate < 2.4 V/ms. For faster VTRK signals accuracy will depend on the regulator bandwidth.
Note 8: See section Over Temperature Protection (OTP).
Note 9: See section External Capacitors.
Note 10: See section Initialization Procedure.
Note 11: See graph Output Ripple vs External Capacitance and Operating information section Output Ripple and Noise.
Note 12: See graph Load Transient vs. External Capacitance and Operating information section External Capacitors.
Note 13: Time for reaching 100% of nominal Vout.
Note 14: For Vout < 1.0 V accuracy is +/-10 mV. For further deviations see section Output Voltage Adjust using PMBus.
Note 15: Accuracy here means deviation from ideal output voltage level given by configured droop and actual load. Includes line, load and temperature variations.
Note 16: For current sharing the Output Voltage Delay Time must be reconfigured to minimum 15 ms, see AN307 for details.
Note 17: For steady state operation above 1.05 x 3.3 V, please contact your local Ericsson sales representative.

BMR 463 series POL Regulators
Input 4.5-14 V, Output up to 25 A / 82.5 W

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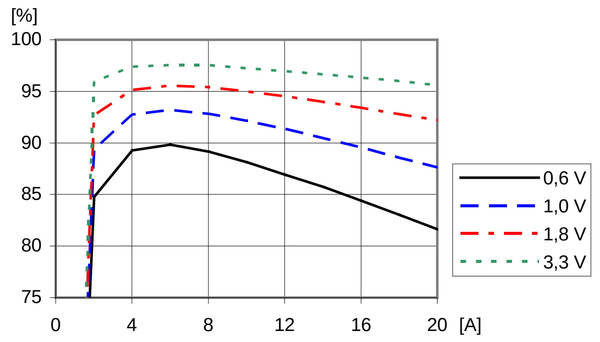
Typical Characteristics
Efficiency and Power Dissipation

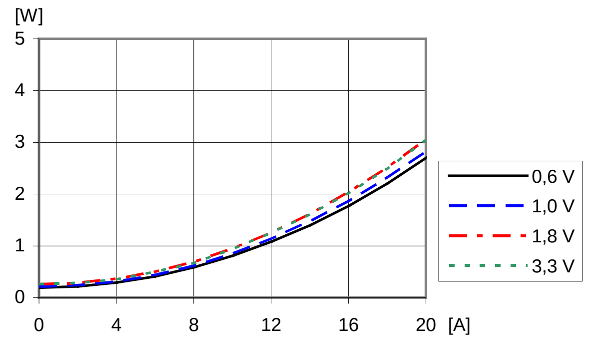
BMR 463 0002, BMR 463 1002
BMR 463 0006, BMR 463 1006

Efficiency vs. Output Current, $V_I = 5$ V



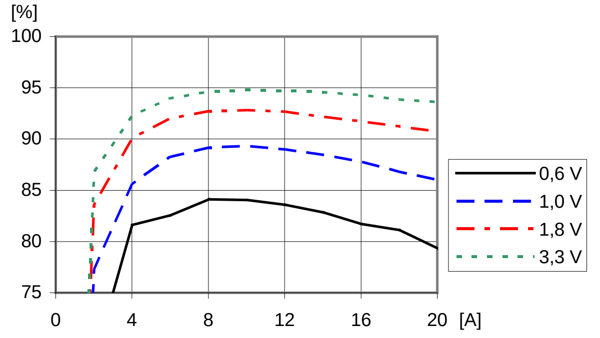
Efficiency vs. load current and output voltage:
T_{P1} = +25 °C, V_I = 5 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Power Dissipation vs. Output Current, $V_I = 5$ V



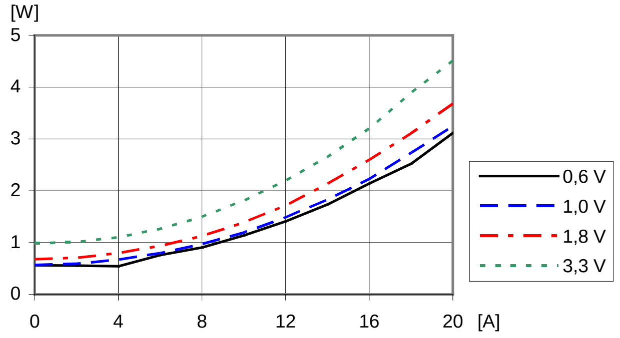
Dissipated power vs. load current and output voltage:
T_{P1} = +25 °C, V_I = 5 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Efficiency vs. Output Current, $V_I = 12$ V



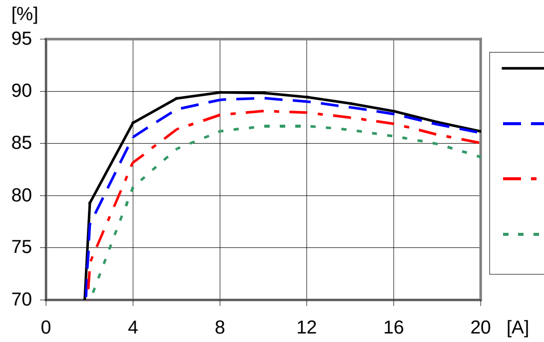
Efficiency vs. load current and output voltage at
T_{P1} = +25 °C, V_I = 12 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Power Dissipation vs. Output Current, $V_I = 12$ V



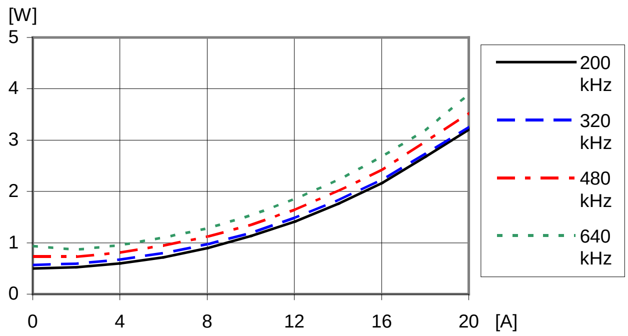
Dissipated power vs. load current and output voltage:
T_{P1} = +25 °C, V_I = 12 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Efficiency vs. Output Current and Switching Frequency



Efficiency vs. load current and switch frequency at
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ
Default configuration except changed frequency

Power Dissipation vs. Output Current and Switching frequency



Dissipated power vs. load current and switch frequency at
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ
Default configuration except changed frequency

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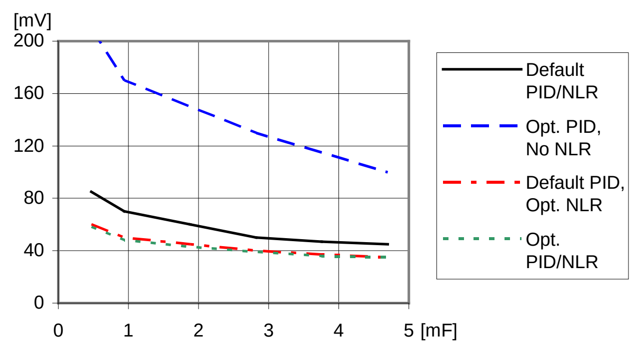
Typical Characteristics
Load Transient

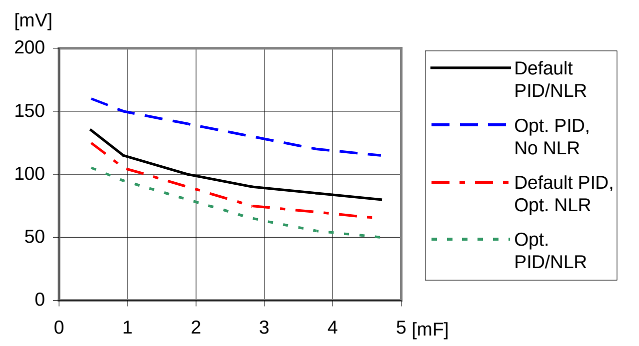
BMR 463 0002, BMR 463 1002
BMR 463 0006, BMR 463 1006

Load Transient vs. External Capacitance, V_O = 1.0 V



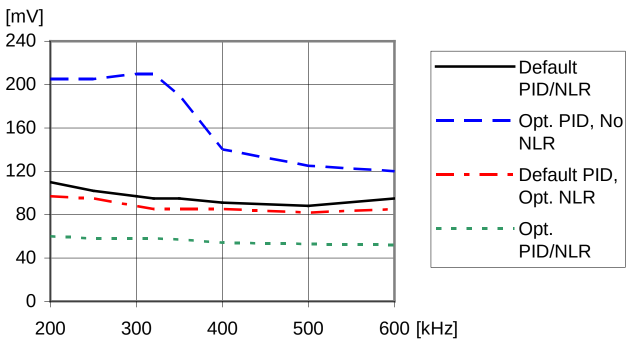
Load transient peak voltage deviation vs. external capacitance.
Step-change (5-15-5 A). Parallel coupling of capacitors with 470 µF/10 mΩ,
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, f_{sw} = 320 kHz, di/dt = 2 A/µs

Load Transient vs. External Capacitance, V_O = 3.3 V



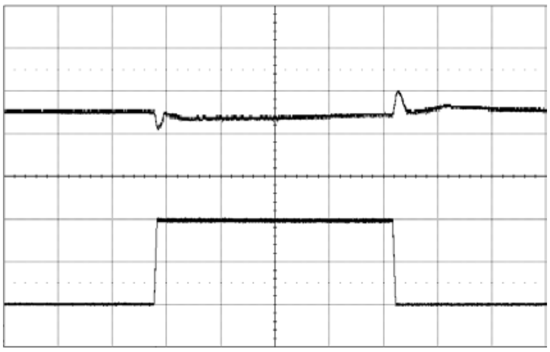
Load transient peak voltage deviation vs. external capacitance.
Step-change (5-15-5 A). Parallel coupling of capacitors with 470 µF/10 mΩ,
T_{P1} = +25 °C, V_I = 12 V, V_O = 3.3 V, f_{sw} = 320 kHz, di/dt = 2 A/µs

Load transient vs. Switch Frequency



Load transient peak voltage deviation vs. frequency.
Step-change (5-15-5 A).
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ

Output Load Transient Response, Default PID/NLR



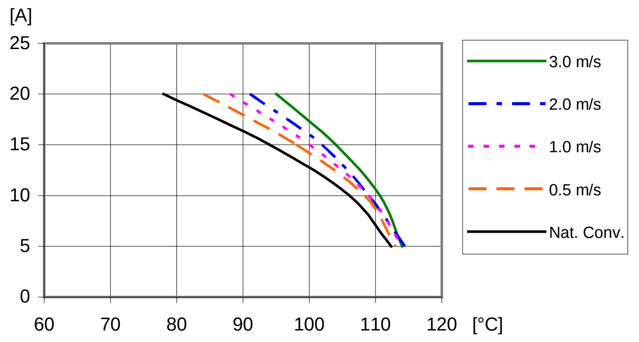
Output voltage response to load current step-change (5-15-5 A) at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
di/dt = 2 A/µs, f_{sw} = 320 kHz,
C_O = 470 µF/10 mΩ

Top trace: output voltage (200 mV/div.).
Bottom trace: load current (5 A/div.).
Time scale: (0.1 ms/div.).

Typical Characteristics
Output Current Characteristic

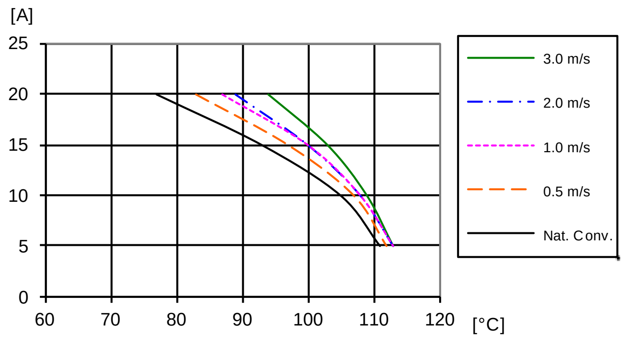
BMR 463 0002, BMR 463 1002
BMR 463 0006, BMR 463 1006

Output Current Derating, $V_O = 0.6$ V



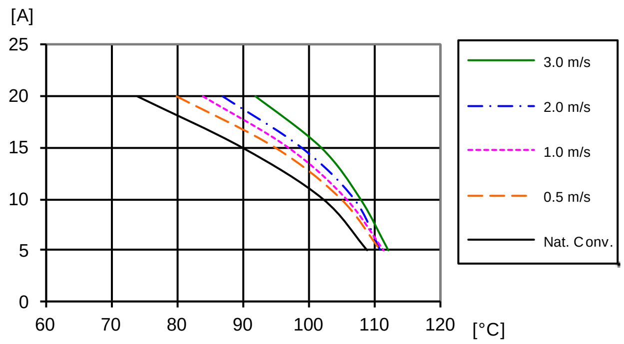
Available load current vs. ambient air temperature and airflow at $V_O = 0.6$ V, $V_I = 12$ V. See Thermal Consideration section.

Output Current Derating, $V_O = 1.0$ V



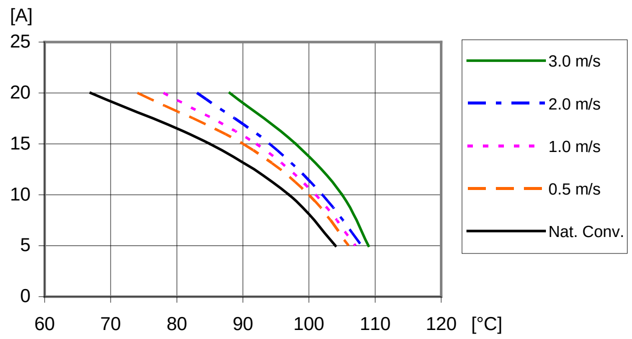
Available load current vs. ambient air temperature and airflow at $V_O = 1.0$ V, $V_I = 12$ V. See Thermal Consideration section.

Output Current Derating, $V_O = 1.8$ V



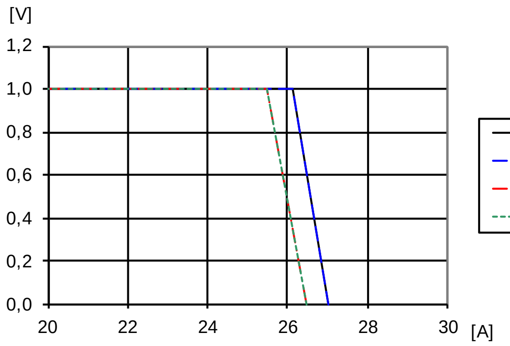
Available load current vs. ambient air temperature and airflow at $V_O = 1.8$ V, $V_I = 12$ V. See Thermal Consideration section.

Output Current Derating, $V_O = 3.3$ V



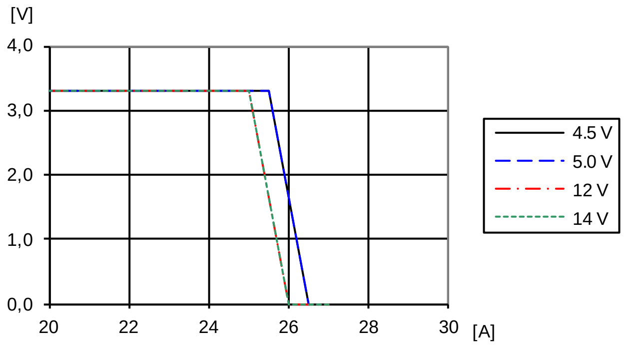
Available load current vs. ambient air temperature and airflow at $V_O = 3.3$ V, $V_I = 12$ V. See Thermal Consideration section.

Current Limit Characteristics, $V_O = 1.0$ V



Output voltage vs. load current at $T_{P1} = +25$ °C, $V_O = 1.0$ V.
Note: Output enters hiccup mode at current limit.

Current Limit Characteristics, $V_O = 3.3$ V

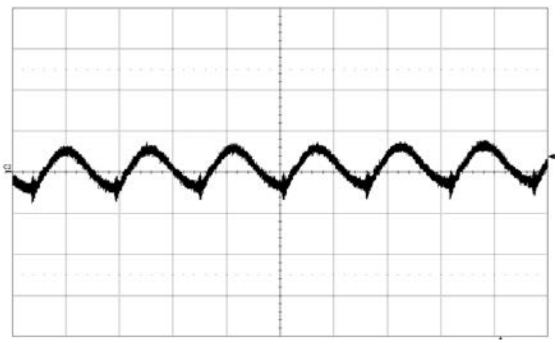


Output voltage vs. load current at $T_{P1} = +25$ °C, $V_O = 3.3$ V.
Output enters hiccup mode at current limit.

Typical Characteristics
Output Voltage

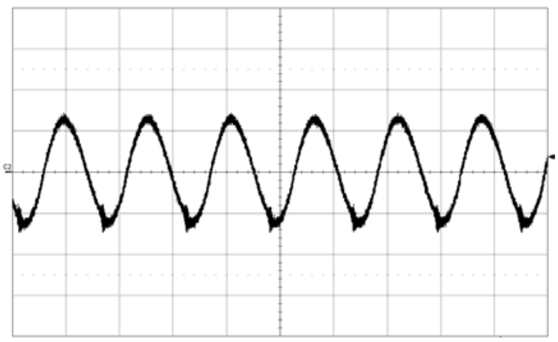
BMR 463 0002, BMR 463 1002
BMR 463 0006, BMR 463 1006

Output Ripple & Noise, V_O = 1.0 V



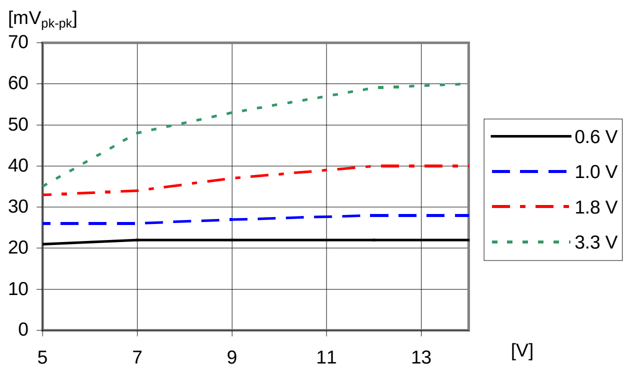
Output voltage ripple at: T_{P1} = +25 °C, V_I = 12 V, C_O =4 70 µF/10 mΩ I_O = 20 A
Trace: output voltage (20 mV/div.). Time scale: (2 µs/div.).

Output Ripple & Noise, V_O = 3.3 V



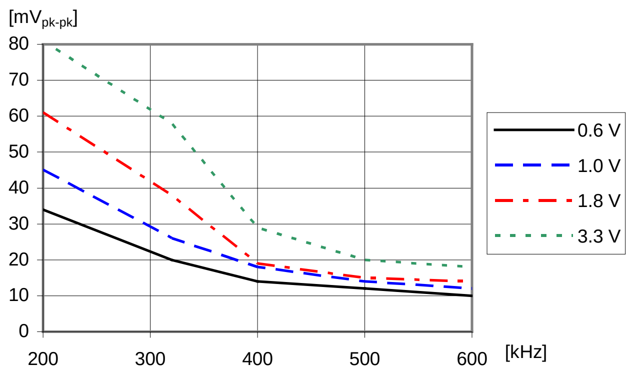
Output voltage ripple at: T_{P1} = +25 °C, V_I = 12 V, C_O = 470 µF/10 mΩ I_O = 20 A
Trace: output voltage (20 mV/div.). Time scale: (2 µs/div.).

Output Ripple vs. Input Voltage



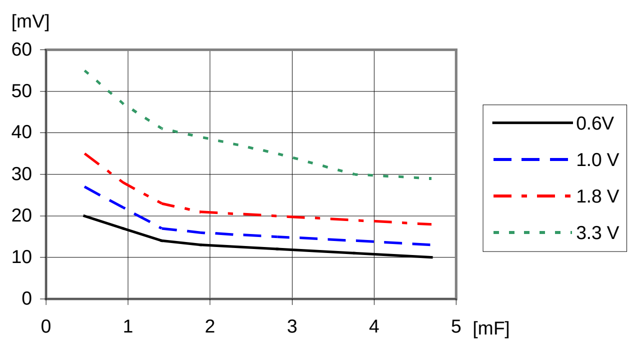
Output voltage ripple V_{pk-pk} at: T_{P1} = +25 °C, C_O = 470 µF/10 mΩ, I_O = 20 A

Output Ripple vs. Frequency



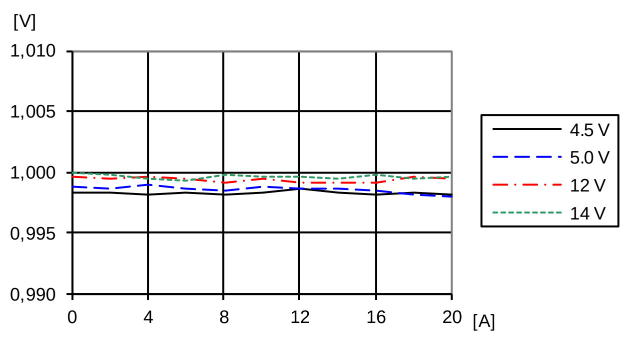
Output voltage ripple V_{pk-pk} at: T_{P1} = +25 °C, V_I = 12 V, C_O = 470 µF/10 mΩ, I_O = 20 A. Default configuration except changed frequency.

Output Ripple vs. External Capacitance



Output voltage ripple V_{pk-pk} at: T_{P1} = +25 °C, V_I = 12 V, I_O = 20 A.
Parallel coupling of capacitors with 470 µF/10 mΩ,

Load regulation, V_O = 1.0 V

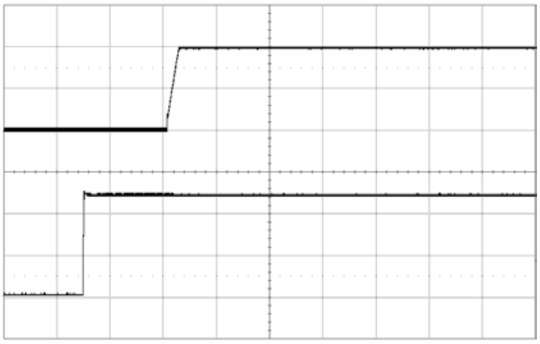


Load regulation at V_o = 1.0 V, T_{P1} = +25 °C, C_O = 470 µF/10 mΩ

Typical Characteristics
Start-up and shut-down

BMR 463 0002, BMR 463 1002
BMR 463 0006, BMR 463 1006

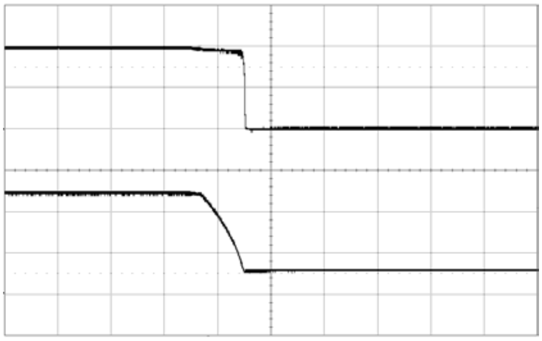
Start-up by input source



Start-up enabled by connecting V_I at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 20 A

Top trace: output voltage (0.5 V/div.).
Bottom trace: input voltage (5 V/div.).
Time scale: (20 ms/div.).

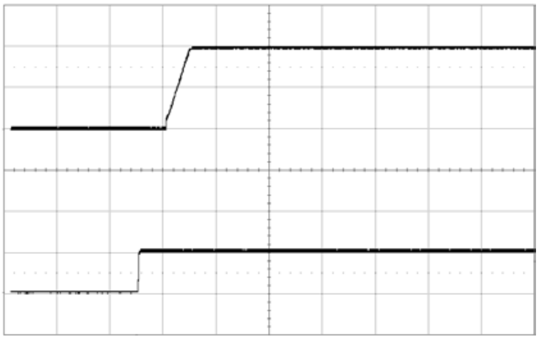
Shut-down by input source



Shut-down enabled by disconnecting V_I at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 20 A

Top trace: output voltage (0.5 V/div.).
Bottom trace: input voltage (5 V/div.).
Time scale: (2 ms/div.).

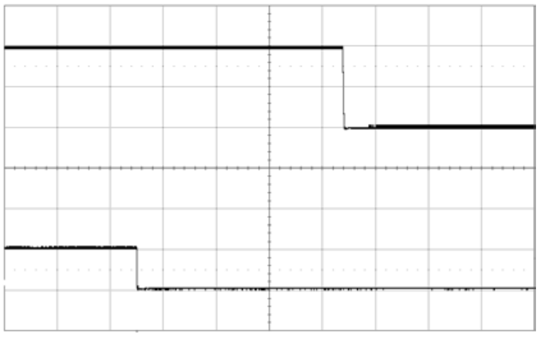
Start-up by CTRL signal



Start-up by enabling CTRL signal at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 20 A

Top trace: output voltage (0.5 V/div.).
Bottom trace: CTRL signal (5 V/div.).
Time scale: (20 ms/div.).

Shut-down by CTRL signal



Shut-down enabled by disconnecting V_I at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 20 A

Top trace: output voltage (0.5 V/div).
Bottom trace: CTRL signal (5 V/div.).
Time scale: (2 ms/div.).

BMR 463 series POL Regulators
Input 4.5-14 V, Output up to 25 A / 82.5 W

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Electrical Specification

BMR 463 2002 (SIP)

T_{P1} = -30 to +95 °C, V_I = 4.5 to 14 V, $V_I > V_O$ + 1.0 V
Typical values given at: T_{P1} = +25 °C, V_I = 12.0 V, max I_O, unless otherwise specified under Conditions.
Default configuration file, 190 10-CDA 102 0258/001.
External C_{IN} = 470 µF/10 mΩ, C_{OUT} = 470 µF/10 mΩ. See Operating Information section for selection of capacitor types.
Sense pins are connected to the output pins.

Characteristics		Conditions	min	typ	max	Unit
V_I	Input voltage rise time	monotonic			2.4	V/ms
V_O	Output voltage without pin strap			1.2		V
	Output voltage adjustment range		0.60		3.3	V
	Output voltage adjustment including margining	See Note 17	0.54		3.63	V
	Output voltage set-point resolution			±0.025		% V_O
	Output voltage accuracy	Including line, load, temp. See Note 14	-1		1	%
		Current sharing operation See Note 15	-2		2	%
	Internal resistance +S/-S to VOUT/GND			4.7		Ω
	Line regulation	V_O = 0.6 V		2		mV
		V_O = 1.0 V		2		
		V_O = 1.8 V		3		
		V_O = 3.3 V		3		
	Load regulation; I_O = 0 - 100%	V_O = 0.6 V		3		mV
		V_O = 1.0 V		2		
		V_O = 1.8 V		2		
		V_O = 3.3 V		2		
V_{Oac}	Output ripple & noise C_O = 470 µF (minimum external capacitance). See Note 11	V_O = 0.6 V		20		mVp-p
		V_O = 1.0 V		30		
		V_O = 1.8 V		40		
		V_O = 3.3 V		60		
I_O	Output current		0		20	A
I_S	Static input current at max I_O	V_O = 0.6 V		1.29		A
		V_O = 1.0 V		1.97		
		V_O = 1.8 V		3.34		
		V_O = 3.3 V		5.92		
I_{lim}	Current limit threshold		22		30	A
I_{sc}	Short circuit current — RMS, hiccup mode, See Note 3	V_O = 0.6 V		8		A
		V_O = 1.0 V		6		
		V_O = 1.8 V		5		
		V_O = 3.3 V		4		
η	Efficiency — 50% of max I_O	V_O = 0.6 V		83.5		%
		V_O = 1.0 V		89.0		
		V_O = 1.8 V		92.7		
		V_O = 3.3 V		94.8		
	Efficiency — max I_O	V_O = 0.6 V		78.0		%
		V_O = 1.0 V		85.3		
		V_O = 1.8 V		90.4		
		V_O = 3.3 V		93.5		
P_d	Power dissipation at max I_O	V_O = 0.6 V		3.40		W
		V_O = 1.0 V		3.45		
		V_O = 1.8 V		3.86		
		V_O = 3.3 V		4.62		
P_{li}	Input idling power (no load) — Default configuration: Continues Conduction Mode, CCM	V_O = 0.6 V		0.56		W
		V_O = 1.0 V		0.57		
		V_O = 1.8 V		0.69		
		V_O = 3.3 V		1.00		

Characteristics			Conditions	min	typ	max	Unit
P_{CTRL}	Input standby power	Turned off with CTRL-pin	Default configuration: Monitoring enabled, Precise timing enabled		180		mW
C_i	Internal input capacitance				70		µF
C_o	Internal output capacitance				200		µF
C_{OUT}	Total external output capacitance		See Note 9	300		15 000	µF
C_{OUT}	ESR range of capacitors (per single capacitor)		See Note 9	5		30	mΩ

V_{tr1}	Load transient peak voltage deviation Load step 25-75-25% of max I_O	Default configuration di/dt = 2 A/µs C_O = 470 µF (minimum external capacitance) see Note 12	V_O = 0.6 V		75		mV
			V_O = 1.0 V		80		mV
			V_O = 1.8 V		105		mV
			V_O = 3.3 V		120		mV
t_{tr1}	Load transient recovery time, Note 5 Load step 25-75-25% of max I_O	Default configuration di/dt = 2 A/µs C_O = 470 µF (minimum external capacitance) see Note 12	V_O = 0.6 V		40		µs
			V_O = 1.0 V		50		µs
			V_O = 1.8 V		100		µs
			V_O = 3.3 V		100		µs

f_s	Switching frequency			320		kHz
f_s	Switching frequency range	PMBus configurable		200-640		kHz
f_s	Switching frequency set-point accuracy		-5		5	%
	Control Circuit PWM Duty Cycle		5		95	%
	Minimum Sync Pulse Width		150			ns
	Input Clock Frequency Drift Tolerance	External clock source	-13		13	%

Input Under Voltage Lockout, UVLO	UVLO threshold			3.85		V
	UVLO threshold range	PMBus configurable		3.85-14		V
	Set point accuracy		-150		150	mV
	UVLO hysteresis			0.35		V
	UVLO hysteresis range	PMBus configurable		0-10.15		V
	Delay				2.5	µs
	Fault response	See Note 3		Automatic restart, 70 ms		
Input Over Voltage Protection, IOVP	IOVP threshold			16		V
	IOVP threshold range	PMBus configurable		4.2-16		V
	Set point accuracy		-150		150	mV
	IOVP hysteresis			1		V
	IOVP hysteresis range	PMBus configurable		0-11.8		V
	Delay				2.5	µs
	Fault response	See Note 3		Automatic restart, 70 ms		
Power Good, PG, See Note 2	PG threshold			90		% V_O
	PG hysteresis			5		% V_O
	PG delay			10		ms
	PG delay range	PMBus configurable		0-500		s
Output voltage Over/Under Voltage Protection, OVP/UVP	UVP threshold			85		% V_O
	UVP threshold range	PMBus configurable		0-100		% V_O
	UVP hysteresis			5		% V_O
	OVP threshold			115		% V_O
	OVP threshold range	PMBus configurable		100-115		% V_O
	UVP/OVP response time			25		µs
	UVP/OVP response time range	PMBus configurable		5-60		µs
	Fault response	See Note 3		Automatic restart, 70 ms		

BMR 463 series POL Regulators Input 4.5-14 V, Output up to 25 A / 82.5 W	EN/LZT 146 434 R4B February 2014 © Ericsson AB

Characteristics		Conditions	min	typ	max	Unit
Over Current Protection, OCP	OCP threshold			26		A
	OCP threshold range	PMBus configurable		0-26		A
	Protection delay,	See Note 4		5		T_{sw}
	Protection delay range	PMBus configurable		1-32		T_{sw}
	Fault response	See Note 3		Automatic restart, 70 ms		
Over Temperature Protection, OTP at P1 See Note 8	OTP threshold			120		°C
	OTP threshold range	PMBus configurable		-40…+120		°C
	OTP hysteresis			15		°C
	OTP hysteresis range	PMBus configurable		0-160		°C
	Fault response	See Note 3		Automatic restart, 240 ms		

V_{IL}	Logic input low threshold	SYNC, SA0, SA1, SCL, SDA, GCB, CTRL, VSET			0.8	V
V_{IH}	Logic input high threshold		2			V
I_{IL}	Logic input low sink current	CTRL			0.6	mA
V_{OL}	Logic output low signal level	SYNC, SCL, SDA, SALERT, GCB, PG			0.4	V
V_{OH}	Logic output high signal level		2.25			V
I_{OL}	Logic output low sink current				4	mA
I_{OH}	Logic output high source current				2	mA
t_{set}	Setup time, SMBus	See Note 1	300			ns
t_{hold}	Hold time, SMBus	See Note 1	250			ns
t_{free}	Bus free time, SMBus	See Note 1	2			ms
C_p	Internal capacitance on logic pins			10		pF

Initialization time		See Note 10		35		ms
Output Voltage Delay Time See Note 6	Delay duration	See Note 16		10		ms
	Delay duration range	PMBus configurable		2-500000		
	Delay accuracy turn-on	Default configuration: CTRL controlled Precise timing enabled		±0.25		ms
		PMBus controlled Precise timing disabled Current sharing operation		-0.25/+4		ms
	Delay accuracy turn-off			-0.25/+4		ms
Output Voltage Ramp Time See Note 13	Ramp duration			10		ms
	Ramp duration range	PMBus configurable		0-200		
	Ramp time accuracy			100		µs
		Current sharing operation		20		%

VTRK Input Bias Current	V_{VTRK} = 5.5 V		110	200	µA
VTRK Tracking Ramp Accuracy (V_O - V_{VTRK})	100% tracking, see Note 7	-100		100	mV
	Current sharing operation 2 phases, 100% tracking V_O = 1.0 V, 10 ms ramp		±100		mV
VTRK Regulation Accuracy (V_O - V_{VTRK})	100% Tracking	-1		1	%
	Current sharing operation 100% Tracking	-2		2	%

Current difference between products in a current sharing group	Steady state operation		Max 2 x READ_IOUT monitoring accuracy		
	Ramp-up		2		A
Number of products in a current sharing group				7	

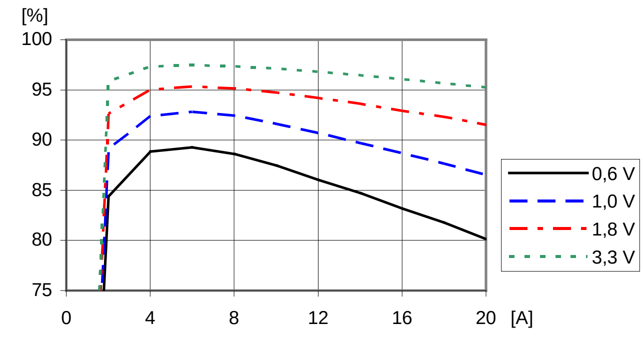
Monitoring accuracy	READ_VIN vs V_I			3		%
	READ_VOUT vs V_O			1		%
	READ_IOUT vs I_O	I_O =0-20 A, T_{P1} = 0 to +95 °C V_I = 4.5-14 V, V_O = 1.0 V		±1.4		A
	READ_IOUT vs I_O	I_O =0-20 A, T_{P1} = 0 to +95 °C V_I = 4.5-14 V, V_O = 0.6-3.3 V		±2.6		A

Note 1: See section I2C/SMBus Setup and Hold Times – Definitions.
Note 2: Monitorable over PMBus Interface.
Note 3: Automatic restart ~70 or 240 ms after fault if the fault is no longer present. Continuous restart attempts if the fault reappear after restart. See Operating Information and AN302 for other fault response options.
Note 4: T_{sw} is the switching period.
Note 5: Within +/-3% of V_O
Note 6: See section Soft-start Power Up.
Note 7: Tracking functionality is designed to follow a VTRK signal with slew rate < 2.4 V/ms. For faster VTRK signals accuracy will depend on the regulator bandwidth.
Note 8: See section Over Temperature Protection (OTP).
Note 9: See section External Capacitors.
Note 10: See section Initialization Procedure.
Note 11: See graph Output Ripple vs External Capacitance and Operating information section Output Ripple and Noise.
Note 12: See graph Load Transient vs. External Capacitance and Operating information section External Capacitors.
Note 13: Time for reaching 100% of nominal Vout.
Note 14: For Vout < 1.0 V accuracy is +/-10 mV. For further deviations see section Output Voltage Adjust using PMBus.
Note 15: Accuracy here means deviation from ideal output voltage level given by configured droop and actual load. Includes line, load and temperature variations.
Note 16: For current sharing the Output Voltage Delay Time must be reconfigured to minimum 15 ms, see AN307 for details.
Note 17: For steady state operation above 1.05 x 3.3 V, please contact your local Ericsson sales representative.

Typical Characteristics
Efficiency and Power Dissipation

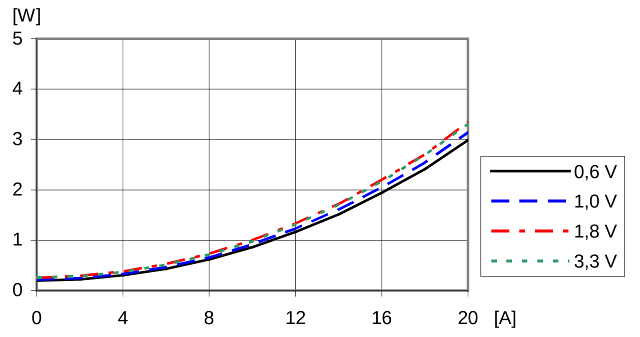
BMR 463 2002 (SIP)

Efficiency vs. Output Current, V_I = 5 V



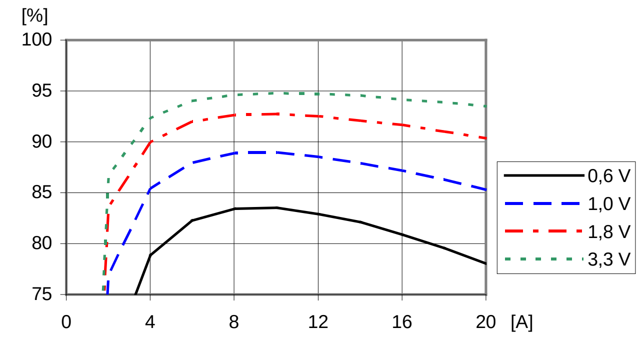
Efficiency vs. load current and output voltage:
T_{P1} = +25 °C, V_I = 5 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Power Dissipation vs. Output Current, V_I = 5 V



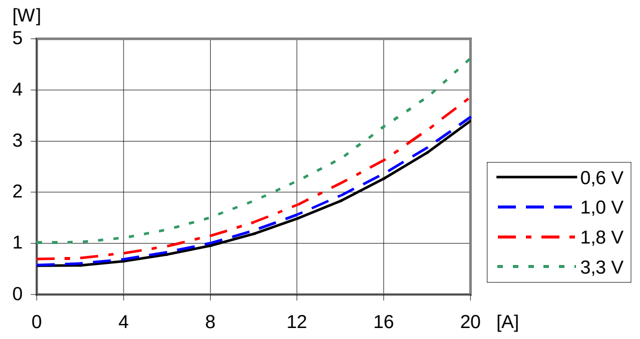
Dissipated power vs. load current and output voltage:
T_{P1} = +25 °C, V_I = 5 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Efficiency vs. Output Current, V_I = 12 V



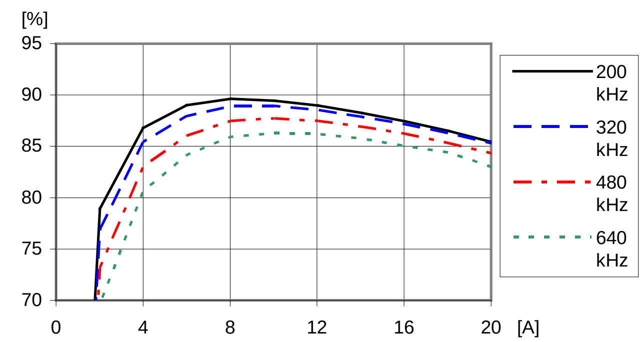
Efficiency vs. load current and output voltage at
T_{P1} = +25 °C, V_I = 12 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Power Dissipation vs. Output Current, V_I = 12 V



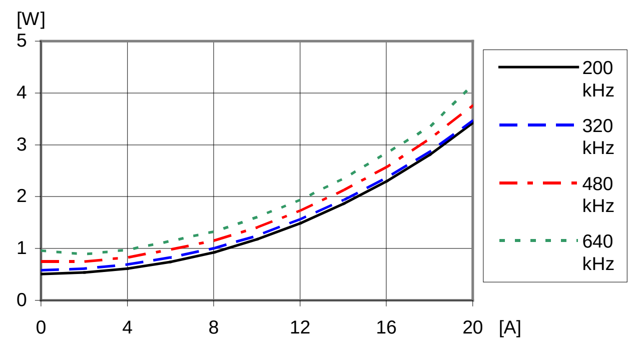
Dissipated power vs. load current and output voltage:
T_{P1} = +25 °C, V_I=12 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Efficiency vs. Output Current and Switching Frequency



Efficiency vs. load current and switch frequency at
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ
Default configuration except changed frequency

Power Dissipation vs. Output Current and Switching frequency



Dissipated power vs. load current and switch frequency at
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ
Default configuration except changed frequency

BMR 463 series POL Regulators Input 4.5-14 V, Output up to 25 A / 82.5 W	EN/LZT 146 434 R4B February 2014
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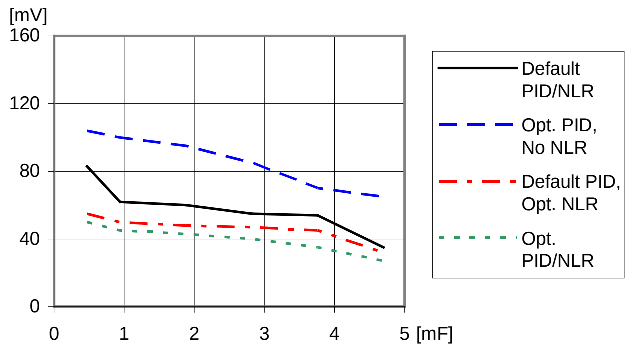
Typical Characteristics

Load Transient

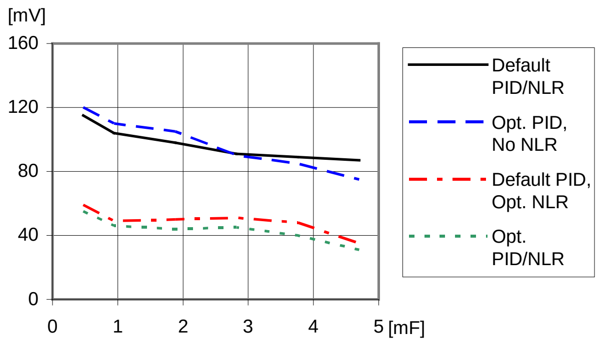
BMR 463 2002 (SIP)

Load Transient vs. External Capacitance, V_O = 1.0 V



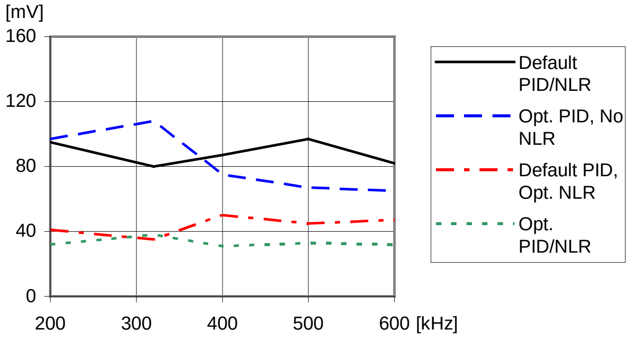
Load transient peak voltage deviation vs. external capacitance.
Step-change (5-15-5 A). Parallel coupling of capacitors with 470 µF/10 mΩ,
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, f_{sw} = 320 kHz, di/dt = 2 A/µs

Load Transient vs. External Capacitance, V_O = 3.3 V



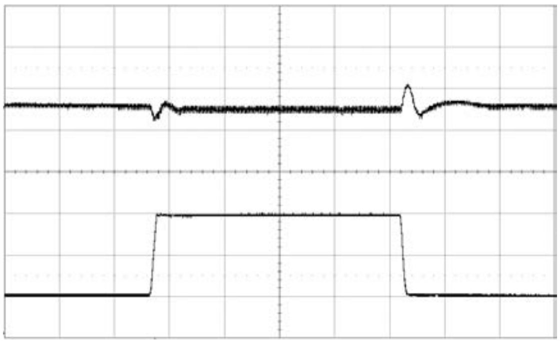
Load transient peak voltage deviation vs. external capacitance.
Step-change (5-15-5 A). Parallel coupling of capacitors with 470 µF/10 mΩ,
T_{P1} = +25 °C, V_I = 12 V, V_O = 3.3 V, f_{sw} = 320 kHz, di/dt = 2 A/µs

Load transient vs. Switch Frequency



Load transient peak voltage deviation vs. frequency.
Step-change (5-15-5 A).
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ

Output Load Transient Response, Default PID/NLR



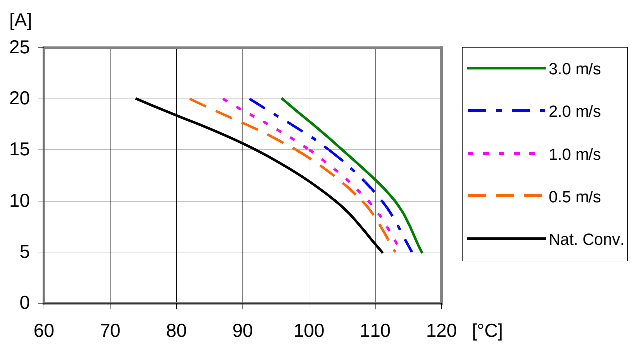
Output voltage response to load current step-change (5-15-5 A) at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
di/dt = 2 A/µs, f_{sw} = 320 kHz
C_O = 470 µF/10 mΩ

Top trace: output voltage (200 mV/div.).
Bottom trace: load current (5 A/div.).
Time scale: (0.1 ms/div.).

Typical Characteristics
Output Current Characteristic

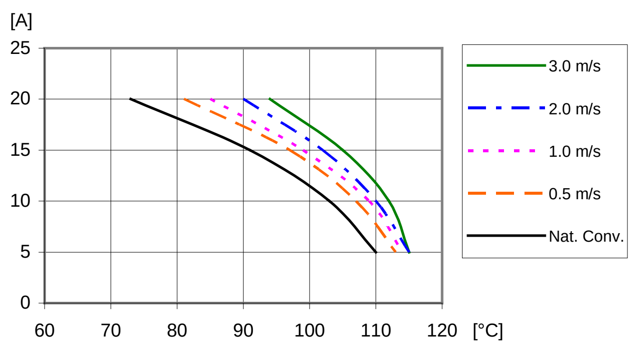
BMR 463 2002 (SIP)

Output Current Derating, V_O = 0.6 V



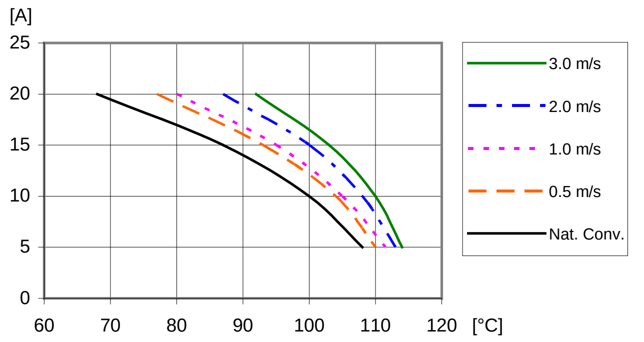
Available load current vs. ambient air temperature and airflow at V_O = 0.6 V, V_I = 12 V. See Thermal Consideration section.

Output Current Derating, V_O = 1.0 V



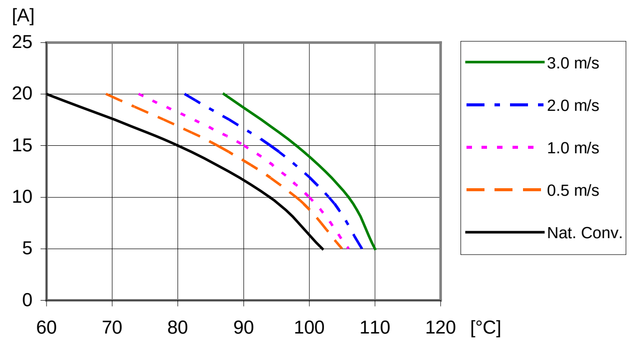
Available load current vs. ambient air temperature and airflow at V_O = 1.0 V, V_I = 12 V. See Thermal Consideration section.

Output Current Derating, V_O = 1.8 V



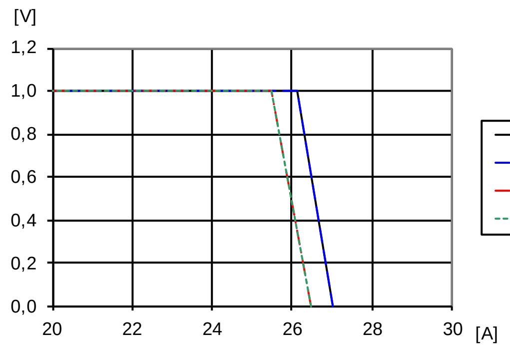
Available load current vs. ambient air temperature and airflow at V_O = 1.8 V, V_I = 12 V. See Thermal Consideration section.

Output Current Derating, V_O = 3.3 V



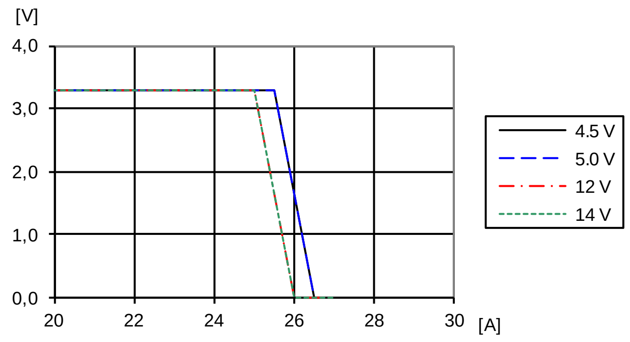
Available load current vs. ambient air temperature and airflow at V_O = 3.3 V, V_I = 12 V. See Thermal Consideration section.

Current Limit Characteristics, V_O = 1.0 V



Output voltage vs. load current at T_{P1} = +25 °C, V_O = 1.0 V
Note: Output enters hiccup mode at current limit.

Current Limit Characteristics, V_O = 3.3 V

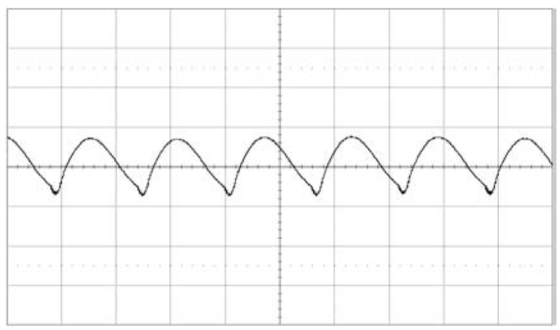


Output voltage vs. load current at T_{P1} = +25 °C, V_O = 3.3 V.
Note: Output enters hiccup mode at current limit.

Typical Characteristics
Output Voltage

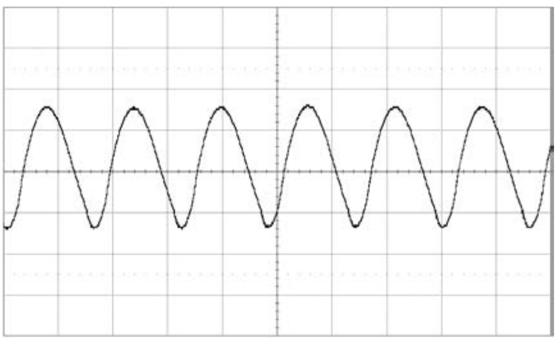
BMR 463 2002 (SIP)

Output Ripple & Noise, V_O = 1.0 V



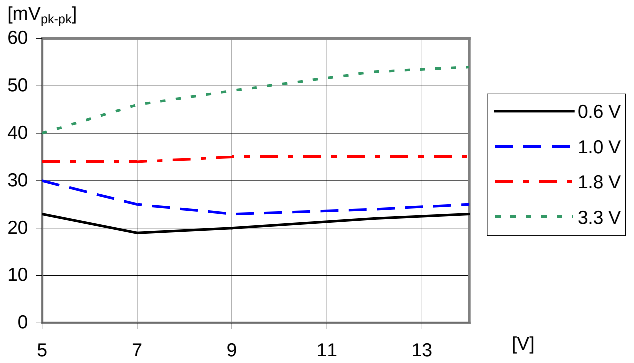
Output voltage ripple at: T_{P1} = +25 °C, V_I = 12 V, C_O = 470 µF/10 mΩ
I_O = 20 A
Trace: output voltage (10 mV/div.).
Time scale: (2 µs/div.).

Output Ripple & Noise, V_O = 3.3 V



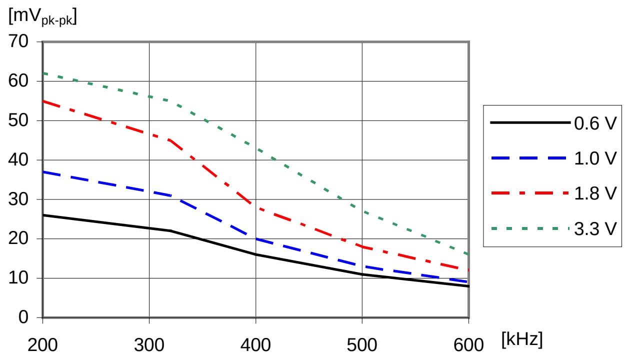
Output voltage ripple at: T_{P1} = +25 °C, V_I = 12 V, C_O = 470 µF/10 mΩ
I_O = 20 A
Trace: output voltage (10 mV/div.).
Time scale: (2 µs/div.).

Output Ripple vs. Input Voltage



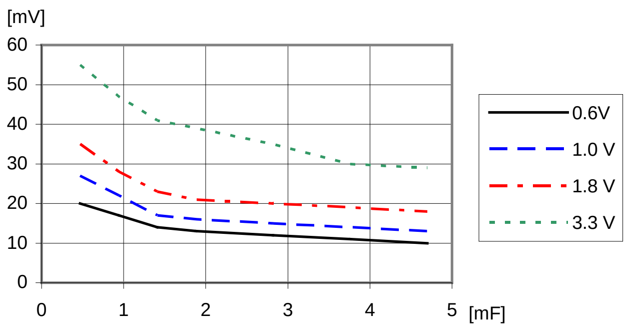
Output voltage ripple $V_{pk\text{-}pk}$ at: T_{P1} = +25 °C, C_O = 470 µF/10 mΩ, I_O = 20 A.

Output Ripple vs. Frequency



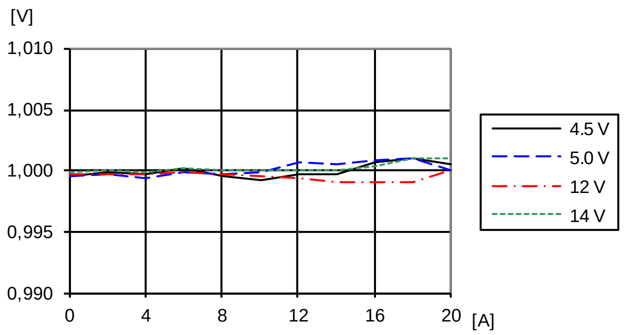
Output voltage ripple $V_{pk\text{-}pk}$ at: T_{P1} = +25 °C, V_I = 12 V, C_O = 470 µF/10 mΩ, I_O = 20 A. Default configuration except changed frequency.

Output Ripple vs. External Capacitance



Output voltage ripple $V_{pk\text{-}pk}$ at: T_{P1} = +25 °C, V_I = 12 V, I_O = 20 A.
Parallel coupling of capacitors with 470 µF/10 mΩ,

Load regulation, V_O=1.0V



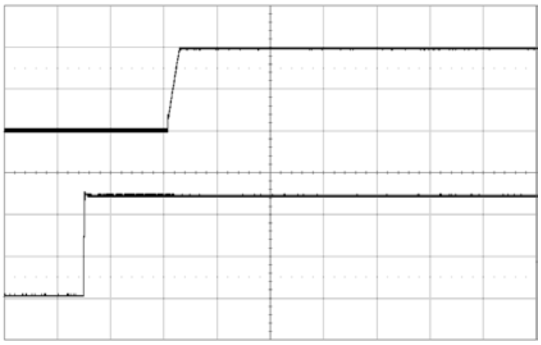
Load regulation at V_o=1.0 V, T_{P1} = +25 °C, C_O = 470 µF/10 mΩ

BMR 463 series POL Regulators Input 4.5-14 V, Output up to 25 A / 82.5 W	EN/LZT 146 434 R4B February 2014 © Ericsson AB

Typical Characteristics
Start-up and shut-down

BMR 463 2002 (SIP)

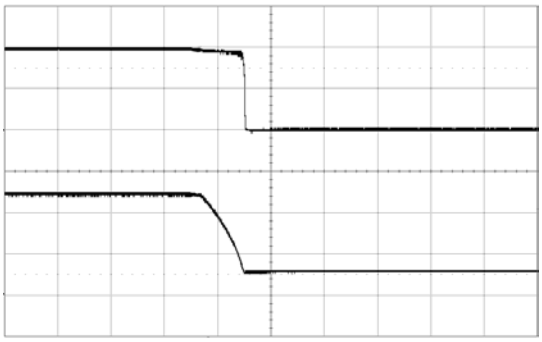
Start-up by input source



Start-up enabled by connecting V_I at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 20 A

Top trace: output voltage (0.5 V/div.).
Bottom trace: input voltage (5 V/div.).
Time scale: (20 ms/div.).

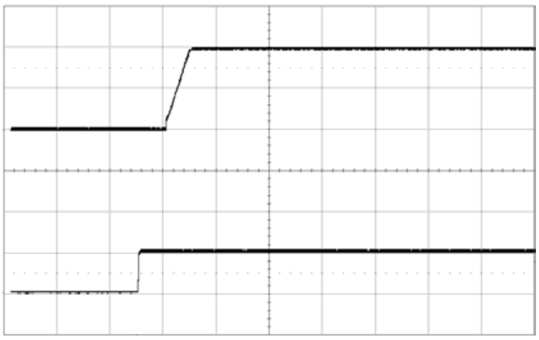
Shut-down by input source



Shut-down enabled by disconnecting V_I at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 20 A

Top trace: output voltage (0.5 V/div).
Bottom trace: input voltage (5 V/div.).
Time scale: (2 ms/div.).

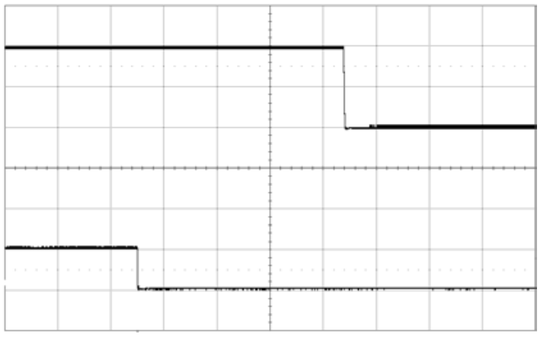
Start-up by CTRL signal



Start-up by enabling CTRL signal at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 20 A

Top trace: output voltage (0.5 V/div.).
Bottom trace: CTRL signal (5 V/div.).
Time scale: (20 ms/div.).

Shut-down by CTRL signal



Shut-down enabled by disconnecting V_I at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 20 A

Top trace: output voltage (0.5 V/div).
Bottom trace: CTRL signal (5 V/div.).
Time scale: (2 ms/div.).

Electrical Specification **BMR 463 0008, BMR 463 1008, BMR 463 0009, BMR 463 1009**

T_{P1} = -30 to +95 °C, V_I = 4.5 to 14 V, $V_I > V_O$ + 1.0 V
Typical values given at: T_{P1} = +25 °C, V_I = 12.0 V, max I_O, unless otherwise specified under Conditions.
Default configuration file, 190 10-CDA 102 0495/001.
External C_{IN} = 470 µF/10 mΩ, C_{OUT} = 470 µF/10 mΩ. See Operating Information section for selection of capacitor types.
Sense pins are connected to the output pins.

Characteristics			Conditions	min	typ	max	Unit
V_I	Input voltage rise time		monotonic			2.4	V/ms

V_O	Output voltage without pin strap				1.2		V
	Output voltage adjustment range			0.60		3.3	V
	Output voltage adjustment including margining		See Note 17	0.54		3.63	V
	Output voltage set-point resolution				±0.025		% V_O
	Output voltage accuracy		Including line, load, temp. See Note 14	-1		1	%
			Current sharing operation See Note 15	-2		2	%
	Internal resistance +S/-S to VOUT/GND				47		Ω
	Line regulation		V_O = 0.6 V		2		mV
			V_O = 1.0 V		2		
			V_O = 1.8 V		2		
			V_O = 3.3 V		3		
	Load regulation; I_O = 0 - 100%		V_O = 0.6 V		2		mV
			V_O = 1.0 V		2		
			V_O = 1.8 V		2		
			V_O = 3.3 V		3		
V_{Oac}	Output ripple & noise C_O = 470 µF (minimum external capacitance). See Note 11		V_O = 0.6 V		20		mVp-p
			V_O = 1.0 V		30		
			V_O = 1.8 V		40		
			V_O = 3.3 V		60		

I_O	Output current			0		25	A
I_S	Static input current at max I_O		V_O = 0.6 V		1.58		A
			V_O = 1.0 V		2.43		
			V_O = 1.8 V		4.13		
			V_O = 3.3 V		7.32		
I_{lim}	Current limit threshold			27		37.5	A
I_{sc}	Short circuit current	RMS, hiccup mode, See Note 3	V_O = 0.6 V		8		A
			V_O = 1.0 V		6		
			V_O = 1.8 V		5		
			V_O = 3.3 V		4		

η	Efficiency	50% of max I_O	V_O = 0.6 V		84.4		%
			V_O = 1.0 V		89.4		
			V_O = 1.8 V		93.1		
			V_O = 3.3 V		95.2		
		max I_O	V_O = 0.6 V		79.2		%
			V_O = 1.0 V		85.7		
			V_O = 1.8 V		90.8		
			V_O = 3.3 V		93.9		
P_d	Power dissipation at max I_O		V_O = 0.6 V		3.93		W
			V_O = 1.0 V		4.17		
			V_O = 1.8 V		4.55		
			V_O = 3.3 V		5.34		
P_{li}	Input idling power (no load)	Default configuration: Continues Conduction Mode, CCM	V_O = 0.6 V		0.56		W
			V_O = 1.0 V		0.57		
			V_O = 1.8 V		0.67		
			V_O = 3.3 V		0.92		

Characteristics			Conditions	min	typ	max	Unit
P_{CTRL}	Input standby power	Turned off with CTRL-pin	Default configuration: Monitoring enabled, Precise timing enabled		170		mW
C_i	Internal input capacitance				70		µF
C_o	Internal output capacitance				200		µF
C_{OUT}	Total external output capacitance		See Note 9	300		15 000	µF
C_{OUT}	ESR range of capacitors (per single capacitor)		See Note 9	5		30	mΩ

V_{tr1}	Load transient peak voltage deviation Load step 25-75-25% of max I_O	Default configuration di/dt = 2 A/µs C_O = 470 µF (minimum external capacitance) see Note 12	V_O = 0.6 V		95		mV
			V_O = 1.0 V		105		
			V_O = 1.8 V		115		
			V_O = 3.3 V		168		
t_{tr1}	Load transient recovery time, Note 5 Load step 25-75-25% of max I_O	Default configuration di/dt = 2 A/µs C_O = 470 µF (minimum external capacitance) see Note 12	V_O = 0.6 V		74		µs
			V_O = 1.0 V		85		
			V_O = 1.8 V		122		
			V_O = 3.3 V		140		

f_s	Switching frequency			320		kHz
f_s	Switching frequency range	PMBus configurable		200-640		kHz
f_s	Switching frequency set-point accuracy		-5		5	%
	Control Circuit PWM Duty Cycle		5		95	%
	Minimum Sync Pulse Width		150			ns
	Input Clock Frequency Drift Tolerance	External clock source	-13		13	%

Input Under Voltage Lockout, UVLO	UVLO threshold			3.85		V
	UVLO threshold range	PMBus configurable		3.85-14		V
	Set point accuracy		-150		150	mV
	UVLO hysteresis			0.35		V
	UVLO hysteresis range	PMBus configurable		0-10.15		V
	Delay			2.5		µs
	Fault response	See Note 3		Automatic restart, 70 ms		
Input Over Voltage Protection, IOVP	IOVP threshold			16		V
	IOVP threshold range	PMBus configurable		4.2-16		V
	Set point accuracy		-150		150	mV
	IOVP hysteresis			1		V
	IOVP hysteresis range	PMBus configurable		0-11.8		V
	Delay			2.5		µs
	Fault response	See Note 3		Automatic restart, 70 ms		
Power Good, PG, See Note 2	PG threshold			90		% V_O
	PG hysteresis			5		% V_O
	PG delay			Direct after DLC		
	PG delay range	PMBus configurable		0-500		s
Output voltage Over/Under Voltage Protection, OVP/UVP	UVP threshold			85		% V_O
	UVP threshold range	PMBus configurable		0-100		% V_O
	UVP hysteresis			5		% V_O
	OVP threshold			115		% V_O
	OVP threshold range	PMBus configurable		100-115		% V_O
	UVP/OVP response time			25		µs
	UVP/OVP response time range	PMBus configurable		5-60		µs
	Fault response	See Note 3		Automatic restart, 70 ms		

Characteristics		Conditions	min	typ	max	Unit
Over Current Protection, OCP	OCP threshold			32		A
	OCP threshold range	PMBus configurable		0-32		A
	Protection delay,	See Note 4		32		T_{sw}
	Protection delay range	PMBus configurable		1-32		T_{sw}
	Fault response	See Note 3		Automatic restart, 70 ms		
Over Temperature Protection, OTP at P2 See Note 8	OTP threshold			120		°C
	OTP threshold range	PMBus configurable		-40…+125		°C
	OTP hysteresis			25		°C
	OTP hysteresis range	PMBus configurable		0-165		°C
	Fault response	See Note 3		Automatic restart, 240 ms		

V_{IL}	Logic input low threshold	SYNC, SA0, SA1, SCL, SDA, GCB, CTRL, VSET			0.8	V
V_{IH}	Logic input high threshold		2			V
I_{IL}	Logic input low sink current	CTRL			0.6	mA
V_{OL}	Logic output low signal level	SYNC, SCL, SDA, SALERT, GCB, PG			0.4	V
V_{OH}	Logic output high signal level		2.25			V
I_{OL}	Logic output low sink current				4	mA
I_{OH}	Logic output high source current				2	mA
t_{set}	Setup time, SMBus	See Note 1	300			ns
t_{hold}	Hold time, SMBus	See Note 1	250			ns
t_{free}	Bus free time, SMBus	See Note 1	2			ms
C_p	Internal capacitance on logic pins			10		pF

Initialization time		See Note 10		40		ms
Output Voltage Delay Time See Note 6	Delay duration	See Note 16		10		ms
	Delay duration range	PMBus configurable		5-500000		
	Delay accuracy turn-on			-0.25/+4		ms
	Delay accuracy turn-off			-0.25/+4		ms
Output Voltage Ramp Time See Note 13	Ramp duration			10		ms
	Ramp duration range	PMBus configurable		0-200		
	Ramp time accuracy			100		µs
		Current sharing operation		20		%

VTRK Input Bias Current	V_{VTRK} = 5.5 V		110	200	µA
VTRK Tracking Ramp Accuracy (V_O - V_{VTRK})	100% tracking, see Note 7	-100		100	mV
	Current sharing operation 2 phases, 100% tracking V_O = 1.0 V, 10 ms ramp		±100		mV
VTRK Regulation Accuracy (V_O - V_{VTRK})	100% Tracking	-1		1	%
	Current sharing operation 100% Tracking	-2		2	%

Current difference between products in a current sharing group	Steady state operation		Max 2 x READ_IOUT monitoring accuracy		
	Ramp-up		2		A
Number of products in a current sharing group				7	

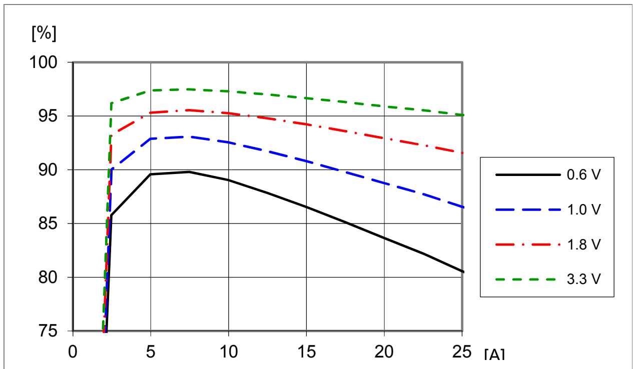
Monitoring accuracy	READ_VIN vs V_I			3		%
	READ_VOUT vs V_O			1		%
	READ_IOUT vs I_O	I_O = 0-25 A, T_{P1} = 0 to +95 °C V_I = 4.5-14 V, V_O = 1.0 V		±1.7		A
	READ_IOUT vs I_O	I_O = 0-25 A, T_{P1} = 0 to +95 °C V_I = 4.5-14 V, V_O = 0.6-3.3 V		±3.0		A

Note 1: See section I2C/SMBus Setup and Hold Times – Definitions.
Note 2: Monitorable over PMBus Interface.
Note 3: Automatic restart ~70 or 240 ms after fault if the fault is no longer present. Continuous restart attempts if the fault reappear after restart. See Operating Information and AN302 for other fault response options.
Note 4: T_{sw} is the switching period.
Note 5: Within +/-3% of V_O
Note 6: See section Soft-start Power Up.
Note 7: Tracking functionality is designed to follow a VTRK signal with slew rate < 2.4 V/ms. For faster VTRK signals accuracy will depend on the regulator bandwidth.
Note 8: See section Over Temperature Protection (OTP).
Note 9: See section External Capacitors.
Note 10: See section Initialization Procedure.
Note 11: See graph Output Ripple vs External Capacitance and Operating information section Output Ripple and Noise.
Note 12: See graph Load Transient vs. External Capacitance and Operating information section External Capacitors.
Note 13: Time for reaching 100% of nominal Vout.
Note 14: For Vout < 1.0 V accuracy is +/-10 mV. For further deviations see section Output Voltage Adjust using PMBus.
Note 15: Accuracy here means deviation from ideal output voltage level given by configured droop and actual load. Includes line, load and temperature variations.
Note 16: For current sharing the Output Voltage Delay Time must be reconfigured to minimum 15 ms, see AN307 for details.
Note 17: For steady state operation above 1.05 x 3.3 V, please contact your local Ericsson sales representative.

Typical Characteristics
Efficiency and Power Dissipation

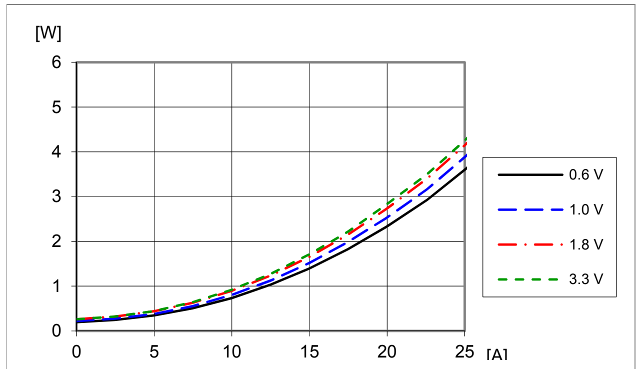
BMR 463 0008, BMR 463 1008
BMR 463 0009, BMR 463 1009

Efficiency vs. Output Current, $V_I = 5$ V



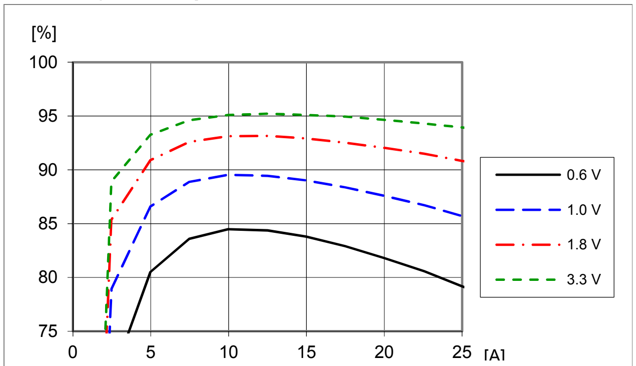
Efficiency vs. load current and output voltage:
T_{P1} = +25 °C, V_I = 5 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Power Dissipation vs. Output Current, $V_I = 5$ V



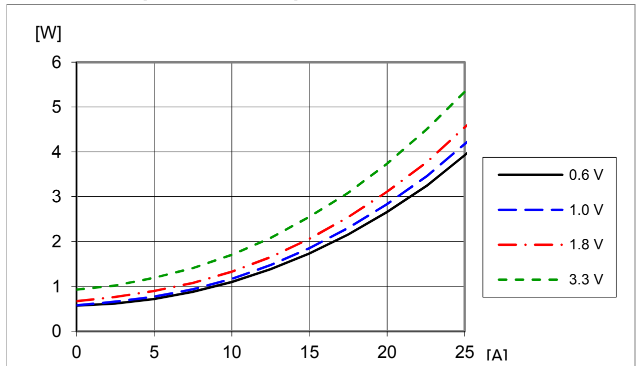
Dissipated power vs. load current and output voltage:
T_{P1} = +25 °C, V_I = 5 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Efficiency vs. Output Current, $V_I = 12$ V



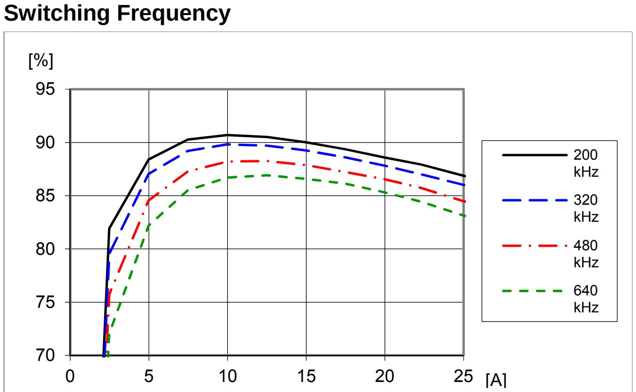
Efficiency vs. load current and output voltage at
T_{P1} = +25 °C, V_I = 12 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Power Dissipation vs. Output Current, $V_I = 12$ V



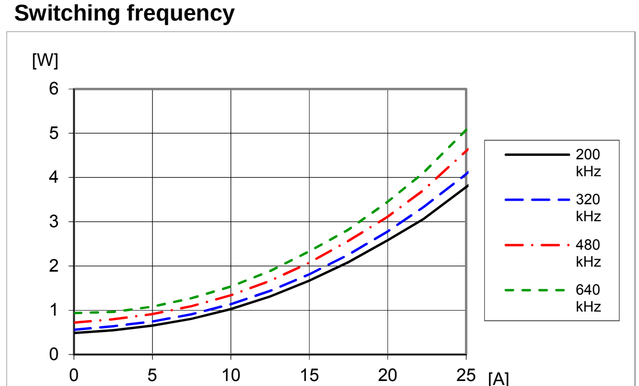
Dissipated power vs. load current and output voltage:
T_{P1} = +25 °C, V_I = 12 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Efficiency vs. Output Current and Switching Frequency



Efficiency vs. load current and switch frequency at
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ.
Default configuration except changed frequency

Power Dissipation vs. Output Current and Switching frequency

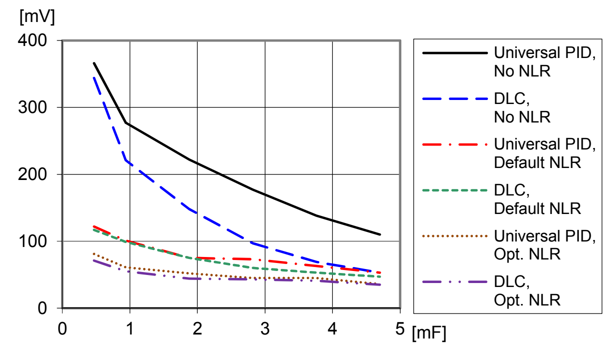


Dissipated power vs. load current and switch frequency at
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ.
Default configuration except changed frequency

Typical Characteristics
Load Transient

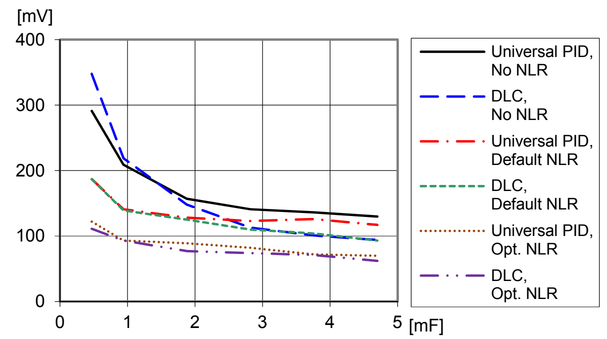
BMR 463 0008, BMR 463 1008
BMR 463 0009, BMR 463 1009

Load Transient vs. External Capacitance, $V_O = 1.0$ V



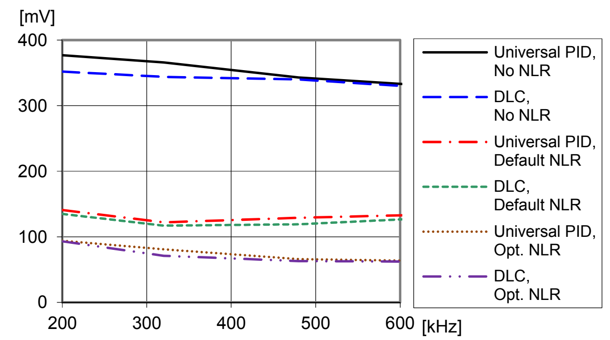
Load transient peak voltage deviation vs. external capacitance.
Step (6.25-18.75-6.25 A). Parallel coupling of capacitors with 470 µF/10 mΩ,
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, f_{sw} = 320 kHz, di/dt = 2 A/µs

Load Transient vs. External Capacitance, $V_O = 3.3$ V



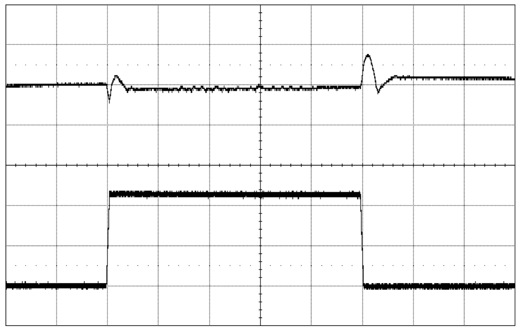
Load transient peak voltage deviation vs. external capacitance.
Step (6.25-18.75-6.25 A). Parallel coupling of capacitors with 470 µF/10 mΩ,
T_{P1} = +25 °C, V_I = 12 V, V_O = 3.3 V, f_{sw} = 320 kHz, di/dt = 2 A/µs

Load transient vs. Switch Frequency



Load transient peak voltage deviation vs. frequency.
Step-change (6.25-18.75-6.25 A).
T_{P1} = +25 °C. V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ

Output Load Transient Response, Default Configuration



Output voltage response to load current
Step-change (6.25-18.75-6.25 A) at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
di/dt = 2 A/µs, f_{sw} = 320 kHz
C_O = 470 µF/10 mΩ

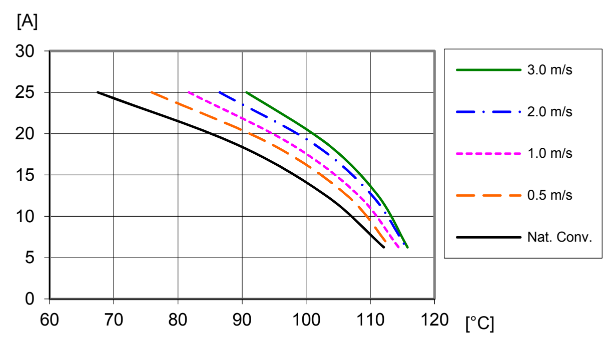
Top trace: output voltage (200 mV/div.).
Bottom trace: load current (5 A/div.).
Time scale: (0.1 ms/div.).

Note: For Universal PID, see section Dynamic Loop Compensation (DLC).

Typical Characteristics
Output Current Characteristic

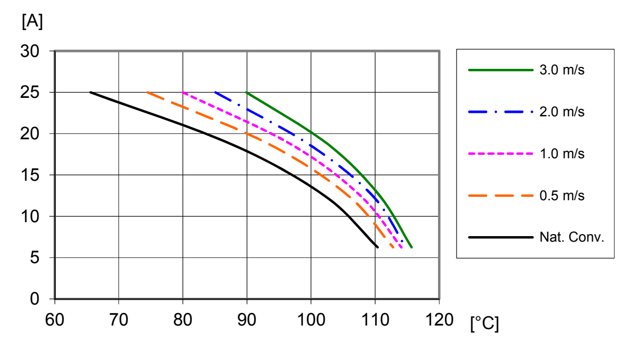
BMR 463 0008, BMR 463 1008
BMR 463 0009, BMR 463 1009

Output Current Derating, V_O = 0.6 V



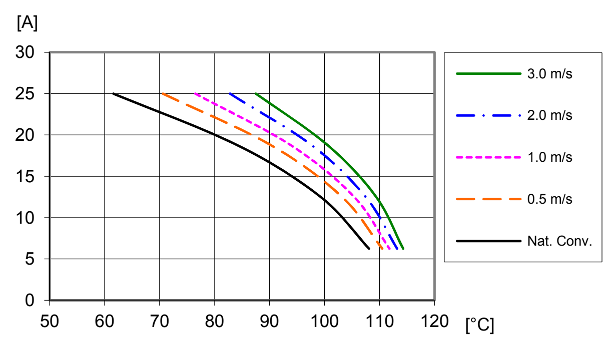
Available load current vs. ambient air temperature and airflow at V_O = 0.6 V, V_I = 12 V. See Thermal Consideration section.

Output Current Derating, V_O = 1.0 V



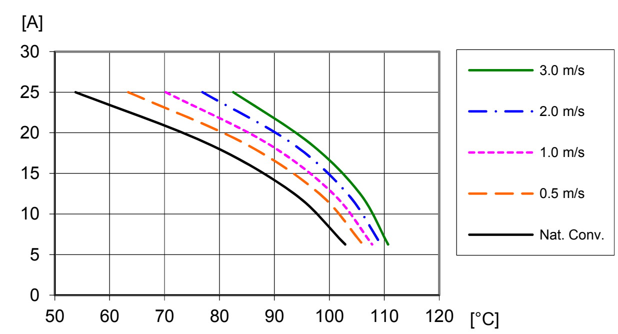
Available load current vs. ambient air temperature and airflow at V_O = 1.0 V, V_I = 12 V. See Thermal Consideration section.

Output Current Derating, V_O = 1.8 V



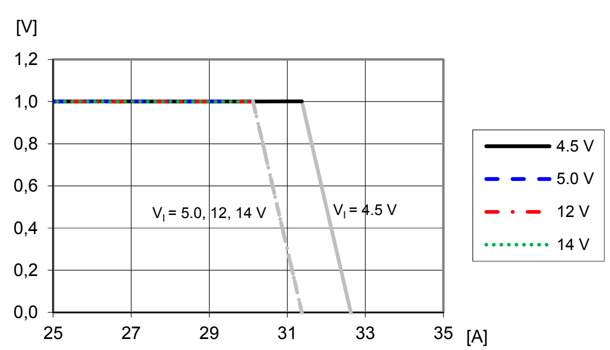
Available load current vs. ambient air temperature and airflow at V_O = 1.8 V, V_I = 12 V. See Thermal Consideration section.

Output Current Derating, V_O = 3.3 V



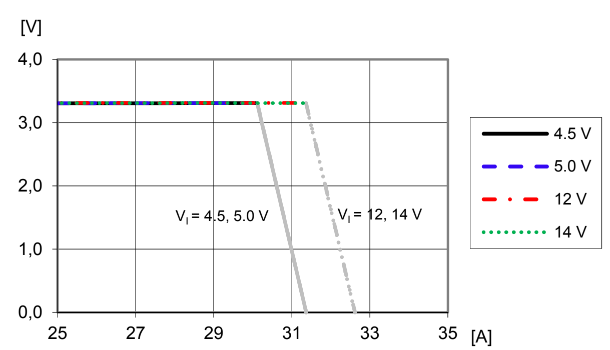
Available load current vs. ambient air temperature and airflow at V_O = 3.3 V, V_I = 12 V. See Thermal Consideration section.

Current Limit Characteristics, V_O = 1.0 V



Output voltage vs. load current at T_{P1} = +25 °C, V_O = 1.0 V.
Note: Output enters hiccup mode at current limit.

Current Limit Characteristics, V_O = 3.3 V

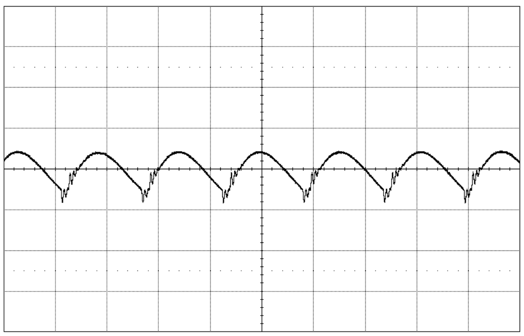


Output voltage vs. load current at T_{P1} = +25 °C, V_O = 3.3 V.
Note: Output enters hiccup mode at current limit.

Typical Characteristics
Output Voltage

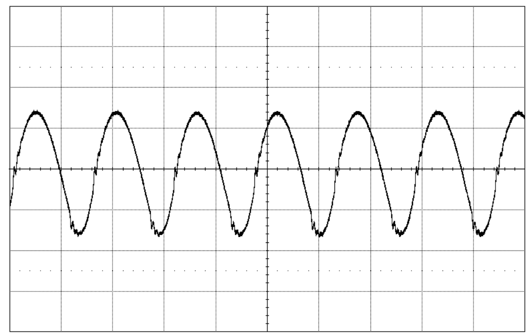
BMR 463 0008, BMR 463 1008
BMR 463 0009, BMR 463 1009

Output Ripple & Noise, V_O = 1.0 V



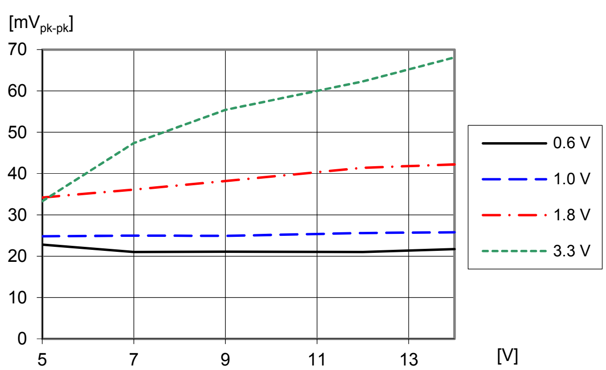
Output voltage ripple at: T_{P1} = +25 °C, V_I = 12 V, C_O = 470 µF/10 mΩ
I_O = 25 A
Trace: output voltage (20 mV/div.).
Time scale: (2 µs/div.).

Output Ripple & Noise, V_O = 3.3 V



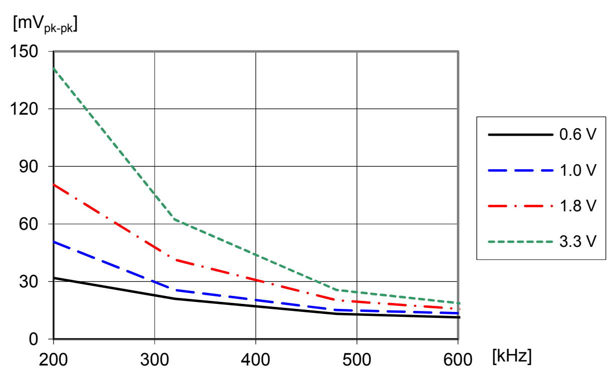
Output voltage ripple at: T_{P1} = +25 °C, V_I = 12 V, C_O = 470 µF/10 mΩ
I_O = 25 A
Trace: output voltage (20 mV/div.).
Time scale: (2 µs/div.).

Output Ripple vs. Input Voltage



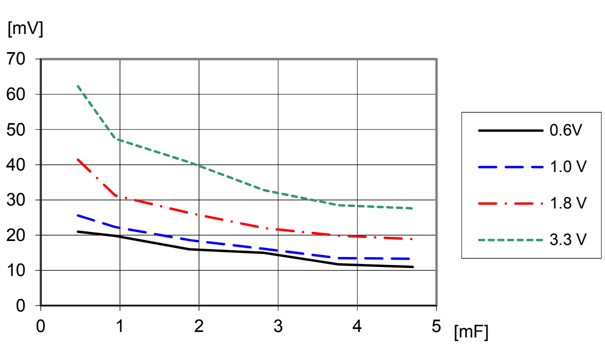
Output voltage ripple V_{pk-pk} at: T_{P1} = +25 °C, C_O = 470 µF/10 mΩ, I_O = 25 A

Output Ripple vs. Frequency



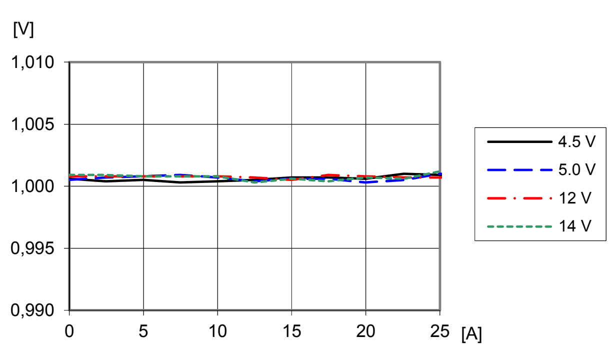
Output voltage ripple V_{pk-pk} at: T_{P1} = +25 °C, V_I = 12 V, C_O = 470 µF/10 mΩ, I_O = 25 A. Default configuration except changed frequency.

Output Ripple vs. External Capacitance



Output voltage ripple V_{pk-pk} at: T_{P1} = +25 °C, V_I = 12 V. I_O = 25 A.
Parallel coupling of capacitors with 470 µF/10 mΩ

Load regulation, V_O = 1.0 V

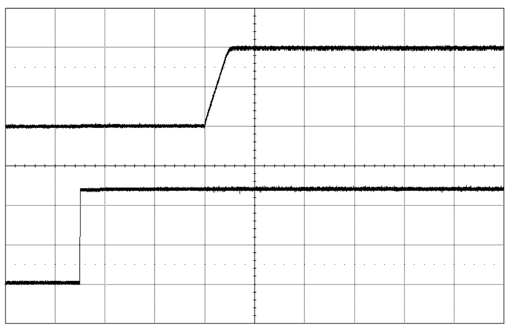


Load regulation at V_o = 1.0 V, T_{P1} = +25 °C, C_O = 470 µF/10 mΩ

Typical Characteristics
Start-up and shut-down

BMR 463 0008, BMR 463 1008
BMR 463 0009, BMR 463 1009

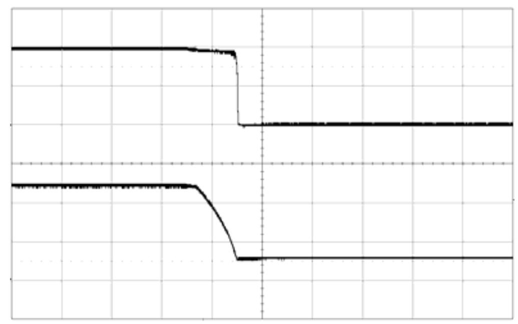
Start-up by input source



Start-up enabled by connecting V_I at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 25 A

Top trace: output voltage (0.5 V/div.).
Bottom trace: input voltage (5 V/div.).
Time scale: (20 ms/div.).

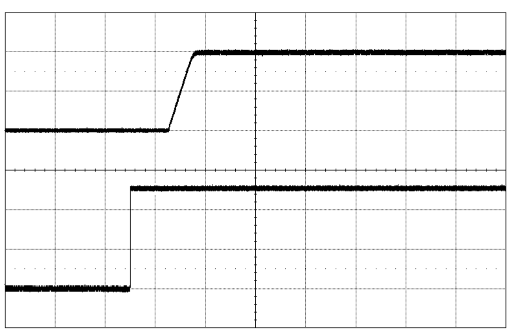
Shut-down by input source



Shut-down enabled by disconnecting V_I at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 25 A

Top trace: output voltage (0.5 V/div.).
Bottom trace: input voltage (5 V/div.).
Time scale: (2 ms/div.).

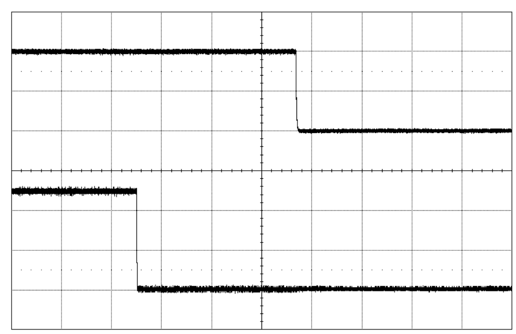
Start-up by CTRL signal



Start-up by enabling CTRL signal at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 25 A

Top trace: output voltage (0.5 V/div.).
Bottom trace: CTRL signal (2 V/div.).
Time scale: (20 ms/div.).

Shut-down by CTRL signal



Shut-down enabled by disconnecting V_I at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 25 A

Top trace: output voltage (0.5 V/div).
Bottom trace: CTRL signal (2 V/div.).
Time scale: (2 ms/div.).

Electrical Specification

BMR 463 2008 (SIP)

T_{P1} = -30 to +95 °C, V_I = 4.5 to 14 V, $V_I > V_O$ + 1.0 V
Typical values given at: T_{P1} = +25 °C, V_I = 12.0 V, max I_O, unless otherwise specified under Conditions.
Default configuration file, 190 10-CDA 102 0497/001.
External C_{IN} = 470 µF/10 mΩ, C_{OUT} = 470 µF/10 mΩ. See Operating Information section for selection of capacitor types.
Sense pins are connected to the output pins.

Characteristics		Conditions	min	typ	max	Unit
V_I	Input voltage rise time	monotonic			2.4	V/ms

V_O	Output voltage without pin strap			1.2		V
	Output voltage adjustment range		0.60		3.3	V
	Output voltage adjustment including margining	See Note 17	0.54		3.63	V
	Output voltage set-point resolution			±0.025		% V_O
	Output voltage accuracy	Including line, load, temp. See Note 14	-1		1	%
		Current sharing operation See Note 15	-2		2	%
	Internal resistance +S/-S to VOUT/GND			47		Ω
	Line regulation	V_O = 0.6 V		2		mV
		V_O = 1.0 V		2		
		V_O = 1.8 V		2		
		V_O = 3.3 V		3		
	Load regulation; I_O = 0 - 100%	V_O = 0.6 V		2		mV
		V_O = 1.0 V		2		
		V_O = 1.8 V		2		
		V_O = 3.3 V		3		
V_{Oac}	Output ripple & noise C_O = 470 µF (minimum external capacitance). See Note 11	V_O = 0.6 V		20		mVp-p
		V_O = 1.0 V		30		
		V_O = 1.8 V		40		
		V_O = 3.3 V		60		

I_O	Output current			0		25	A
I_S	Static input current at max I_O		V_O = 0.6 V		1.61		A
			V_O = 1.0 V		2.46		
			V_O = 1.8 V		4.17		
			V_O = 3.3 V		7.35		
I_{lim}	Current limit threshold			27		37.5	A
I_{sc}	Short circuit current	RMS, hiccup mode, See Note 3	V_O = 0.6 V		8		A
			V_O = 1.0 V		6		
			V_O = 1.8 V		5		
			V_O = 3.3 V		4		

η	Efficiency	50% of max I_O	V_O = 0.6 V		83.6		%
			V_O = 1.0 V		89.0		
			V_O = 1.8 V		92.8		
			V_O = 3.3 V		95.1		
		max I_O	V_O = 0.6 V		77.4		%
			V_O = 1.0 V		84.6		
			V_O = 1.8 V		90.0		
			V_O = 3.3 V		93.5		
P_d	Power dissipation at max I_O		V_O = 0.6 V		4.37		W
			V_O = 1.0 V		4.54		
			V_O = 1.8 V		5.01		
			V_O = 3.3 V		5.77		
P_{li}	Input idling power (no load)	Default configuration: Continues Conduction Mode, CCM	V_O = 0.6 V		0.56		W
			V_O = 1.0 V		0.57		
			V_O = 1.8 V		0.67		
			V_O = 3.3 V		0.92		

Characteristics			Conditions	min	typ	max	Unit
P_{CTRL}	Input standby power	Turned off with CTRL-pin	Default configuration: Monitoring enabled, Precise timing enabled		170		mW
C_i	Internal input capacitance				70		µF
C_o	Internal output capacitance				200		µF
C_{OUT}	Total external output capacitance		See Note 9	300		15 000	µF
C_{OUT}	ESR range of capacitors (per single capacitor)		See Note 9	5		30	mΩ
V_{tr1}	Load transient peak voltage deviation Load step 25-75-25% of max I_O	Default configuration di/dt = 2 A/µs C_O = 470 µF (minimum external capacitance) see Note 12	V_O = 0.6 V		115		mV
			V_O = 1.0 V		122		mV
			V_O = 1.8 V		143		mV
			V_O = 3.3 V		174		mV
t_{tr1}	Load transient recovery time, Note 5 Load step 25-75-25% of max I_O	Default configuration di/dt = 2 A/µs C_O = 470 µF (minimum external capacitance) see Note 12	V_O = 0.6 V		60		µs
			V_O = 1.0 V		65		µs
			V_O = 1.8 V		115		µs
			V_O = 3.3 V		130		µs
f_s	Switching frequency				320		kHz
f_s	Switching frequency range		PMBus configurable		200-640		kHz
f_s	Switching frequency set-point accuracy			-5		5	%
	Control Circuit PWM Duty Cycle			5		95	%
	Minimum Sync Pulse Width			150			ns
	Input Clock Frequency Drift Tolerance		External clock source	-13		13	%
Input Under Voltage Lockout, UVLO		UVLO threshold			3.85		V
		UVLO threshold range	PMBus configurable		3.85-14		V
		Set point accuracy		-150		150	mV
		UVLO hysteresis			0.35		V
		UVLO hysteresis range	PMBus configurable		0-10.15		V
		Delay			2.5		µs
		Fault response	See Note 3		Automatic restart, 70 ms		
Input Over Voltage Protection, IOVP		IOVP threshold			16		V
		IOVP threshold range	PMBus configurable		4.2-16		V
		Set point accuracy		-150		150	mV
		IOVP hysteresis			1		V
		IOVP hysteresis range	PMBus configurable		0-11.8		V
		Delay			2.5		µs
		Fault response	See Note 3		Automatic restart, 70 ms		
Power Good, PG, See Note 2		PG threshold			90		% V_O
		PG hysteresis			5		% V_O
		PG delay			Direct after DLC		ms
		PG delay range	PMBus configurable		0-500		s
Output voltage Over/Under Voltage Protection, OVP/UVP		UVP threshold			85		% V_O
		UVP threshold range	PMBus configurable		0-100		% V_O
		UVP hysteresis			5		% V_O
		OVP threshold			115		% V_O
		OVP threshold range	PMBus configurable		100-115		% V_O
		UVP/OVP response time			25		µs
		UVP/OVP response time range	PMBus configurable		5-60		µs
		Fault response	See Note 3		Automatic restart, 70 ms		

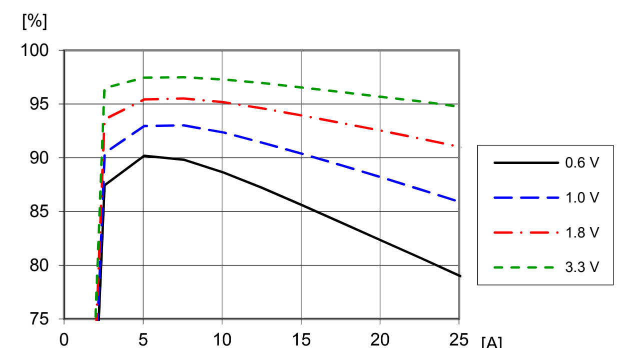
Characteristics		Conditions	min	typ	max	Unit
Over Current Protection, OCP	OCP threshold			32		A
	OCP threshold range	PMBus configurable		0-32		A
	Protection delay,	See Note 4		32		T_{sw}
	Protection delay range	PMBus configurable		1-32		T_{sw}
	Fault response	See Note 3		Automatic restart, 70 ms		
Over Temperature Protection, OTP at P2 See Note 8	OTP threshold			120		°C
	OTP threshold range	PMBus configurable		-40…+125		°C
	OTP hysteresis			25		°C
	OTP hysteresis range	PMBus configurable		0-165		°C
	Fault response	See Note 3		Automatic restart, 240 ms		
V_{IL}	Logic input low threshold	SYNC, SA0, SA1, SCL, SDA, GCB, CTRL, VSET			0.8	V
V_{IH}	Logic input high threshold		2			V
I_{IL}	Logic input low sink current	CTRL			0.6	mA
V_{OL}	Logic output low signal level	SYNC, SCL, SDA, SALERT, GCB, PG			0.4	V
V_{OH}	Logic output high signal level		2.25			V
I_{OL}	Logic output low sink current				4	mA
I_{OH}	Logic output high source current				2	mA
t_{set}	Setup time, SMBus	See Note 1	300			ns
t_{hold}	Hold time, SMBus	See Note 1	250			ns
t_{free}	Bus free time, SMBus	See Note 1	2			ms
C_p	Internal capacitance on logic pins			10		pF
Initialization time		See Note 10		40		ms
Output Voltage Delay Time See Note 6	Delay duration	See Note 16		10		ms
	Delay duration range	PMBus configurable		5-500000		
	Delay accuracy turn-on			-0.25/+4		ms
	Delay accuracy turn-off			-0.25/+4		ms
Output Voltage Ramp Time See Note 13	Ramp duration			10		ms
	Ramp duration range	PMBus configurable		0-200		
	Ramp time accuracy			100		µs
		Current sharing operation		20		%
VTRK Input Bias Current		V_{VTRK} = 5.5 V		110	200	µA
VTRK Tracking Ramp Accuracy (V_O - V_{VTRK})		100% tracking, see Note 7	-100		100	mV
		Current sharing operation 2 phases, 100% tracking V_O = 1.0 V, 10 ms ramp		±100		mV
VTRK Regulation Accuracy (V_O - V_{VTRK})		100% Tracking	-1		1	%
		Current sharing operation 100% Tracking	-2		2	%
Current difference between products in a current sharing group		Steady state operation		Max 2 x READ_IOUT monitoring accuracy		
		Ramp-up		2		A
Number of products in a current sharing group					7	
Monitoring accuracy	READ_VIN vs V_I			3		%
	READ_VOUT vs V_O			1		%
	READ_IOUT vs I_O	I_O = 0-25 A, T_{P1} = 0 to +95 °C V_I = 4.5-14 V, V_O = 1.0 V		±1.7		A
	READ_IOUT vs I_O	I_O = 0-25 A, T_{P1} = 0 to +95 °C V_I = 4.5-14 V, V_O = 0.6-3.3 V		±3.0		A

Note 1: See section I2C/SMBus Setup and Hold Times – Definitions.
Note 2: Monitorable over PMBus Interface.
Note 3: Automatic restart ~70 or 240 ms after fault if the fault is no longer present. Continuous restart attempts if the fault reappear after restart. See Operating Information and AN302 for other fault response options.
Note 4: T_{sw} is the switching period.
Note 5: Within +/-3% of V_O
Note 6: See section Soft-start Power Up.
Note 7: Tracking functionality is designed to follow a VTRK signal with slew rate < 2.4 V/ms. For faster VTRK signals accuracy will depend on the regulator bandwidth.
Note 8: See section Over Temperature Protection (OTP).
Note 9: See section External Capacitors.
Note 10: See section Initialization Procedure.
Note 11: See graph Output Ripple vs External Capacitance and Operating information section Output Ripple and Noise.
Note 12: See graph Load Transient vs. External Capacitance and Operating information section External Capacitors.
Note 13: Time for reaching 100% of nominal Vout.
Note 14: For Vout < 1.0 V accuracy is +/-10 mV. For further deviations see section Output Voltage Adjust using PMBus.
Note 15: Accuracy here means deviation from ideal output voltage level given by configured droop and actual load. Includes line, load and temperature variations.
Note 16: For current sharing the Output Voltage Delay Time must be reconfigured to minimum 15 ms, see AN307 for details.
Note 17: For steady state operation above 1.05 x 3.3 V, please contact your local Ericsson sales representative.

Typical Characteristics
Efficiency and Power Dissipation

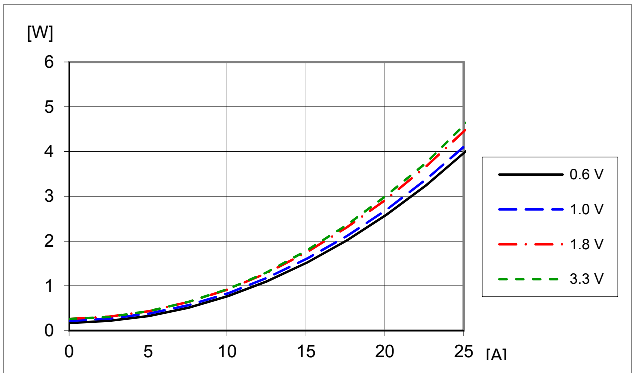
BMR 463 2008 (SIP)

Efficiency vs. Output Current, V_I = 5 V



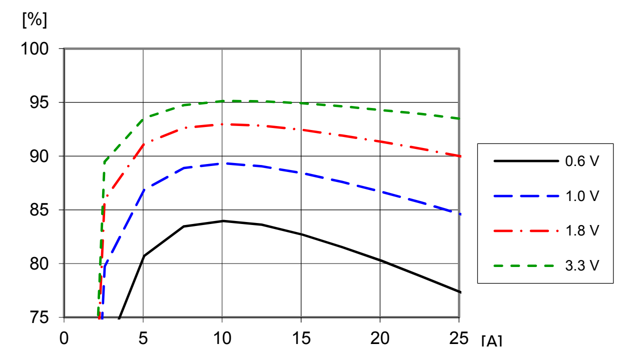
Efficiency vs. load current and output voltage:
T_{P1} = +25 °C, V_I = 5 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Power Dissipation vs. Output Current, V_I = 5 V



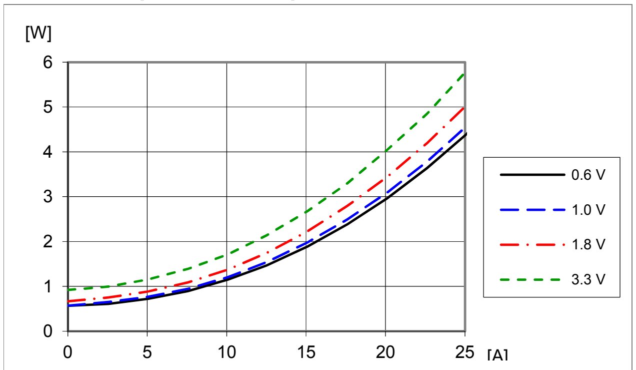
Dissipated power vs. load current and output voltage:
T_{P1} = +25 °C, V_I = 5 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Efficiency vs. Output Current, V_I = 12 V



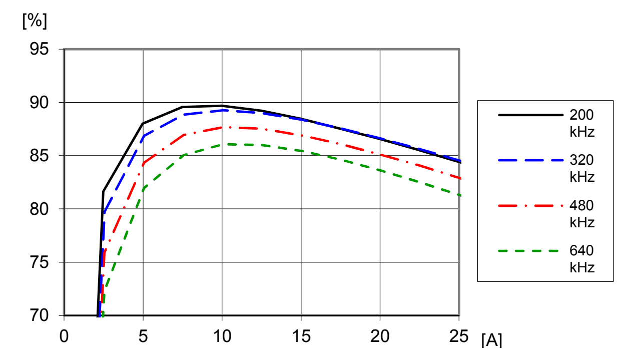
Efficiency vs. load current and output voltage at
T_{P1} = +25 °C, V_I=12 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Power Dissipation vs. Output Current, V_I = 12 V



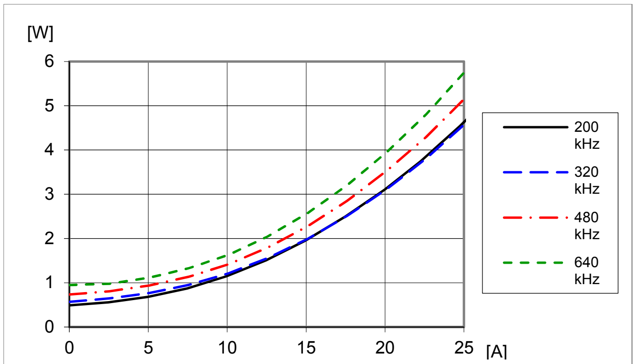
Dissipated power vs. load current and output voltage:
T_{P1} = +25 °C, V_I=12 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Efficiency vs. Output Current and Switching Frequency



Efficiency vs. load current and switch frequency at
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ.
Default configuration except changed frequency

Power Dissipation vs. Output Current and Switching frequency

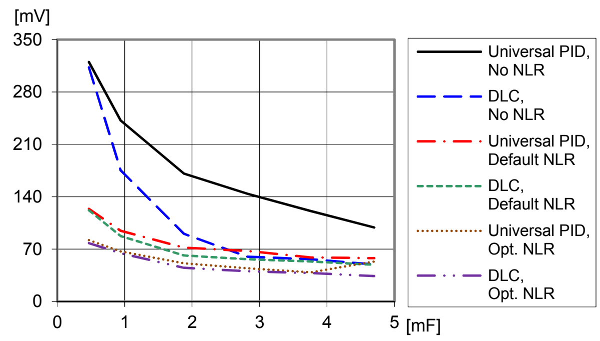


Dissipated power vs. load current and switch frequency at
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ.
Default configuration except changed frequency

Typical Characteristics
Load Transient

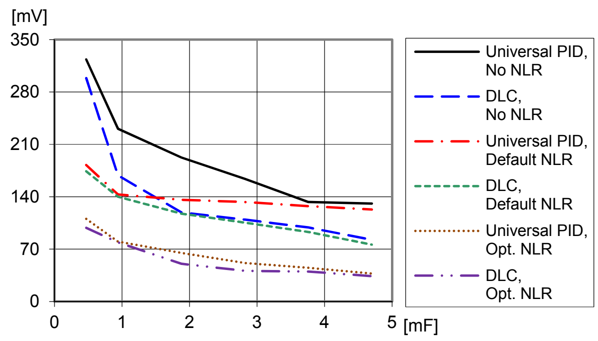
BMR 463 2008 (SIP)

Load Transient vs. External Capacitance, V_O = 1.0 V



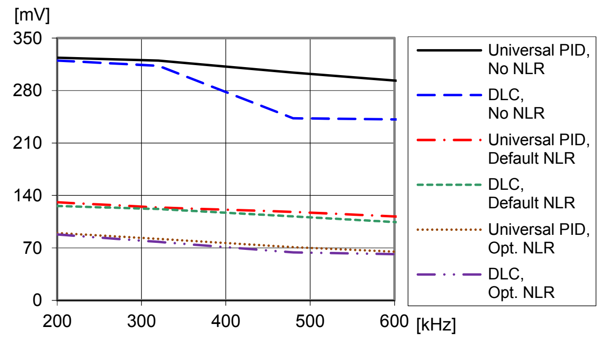
Load transient peak voltage deviation vs. external capacitance.
Step (6.25-18.75-6.25 A). Parallel coupling of capacitors with 470 µF/10 mΩ,
T_{P1} = +25 °C. V_I = 12 V, V_O = 1.0 V, f_{sw} = 320 kHz, di/dt = 2 A/µs

Load Transient vs. External Capacitance, V_O = 3.3 V



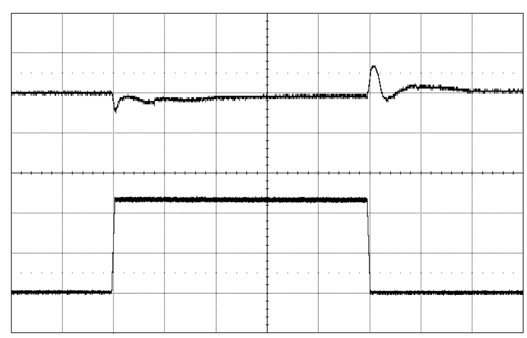
Load transient peak voltage deviation vs. external capacitance.
Step (6.25-18.75-6.25 A). Parallel coupling of capacitors with 470 µF/10 mΩ,
T_{P1} = +25 °C. V_I = 12 V, V_O = 3.3 V, f_{sw} = 320 kHz, di/dt = 2 A/µs

Load transient vs. Switch Frequency



Load transient peak voltage deviation vs. frequency.
Step-change (6.25-18.75-6.25 A).
T_{P1} = +25 °C. V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ

Output Load Transient Response, Default Configuration



Output voltage response to load Step-change (6.25-18.75-6.25 A) at: T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V di/dt = 2 A/µs, f_{sw} = 320 kHz C_O = 470 µF/10 mΩ

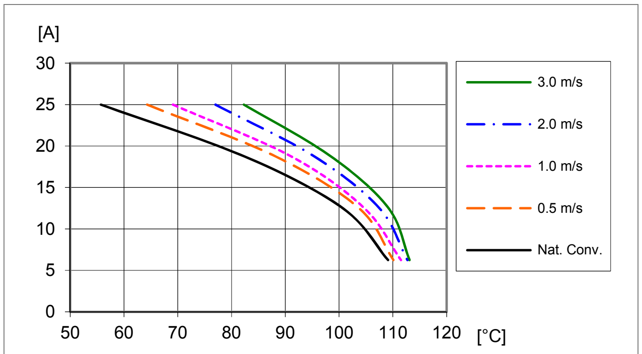
Top trace: output voltage (200 mV/div.).
Bottom trace: load current (5 A/div.).
Time scale: (0.1 ms/div.).

Note: For Universal PID, see section Dynamic Loop Compensation (DLC).

Typical Characteristics
Output Current Characteristic

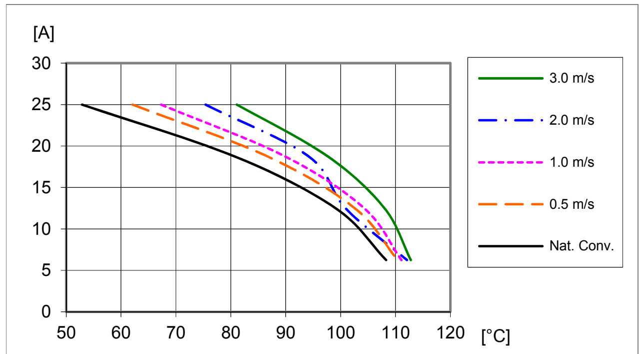
BMR 463 2008 (SIP)

Output Current Derating, V_O = 0.6 V



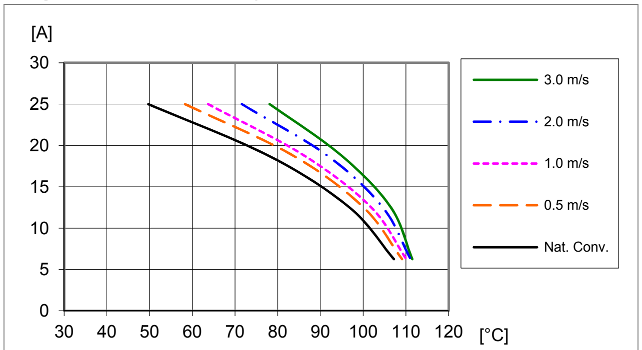
Available load current vs. ambient air temperature and airflow at V_O = 0.6 V, V_I = 12 V. See Thermal Consideration section.

Output Current Derating, V_O = 1.0 V



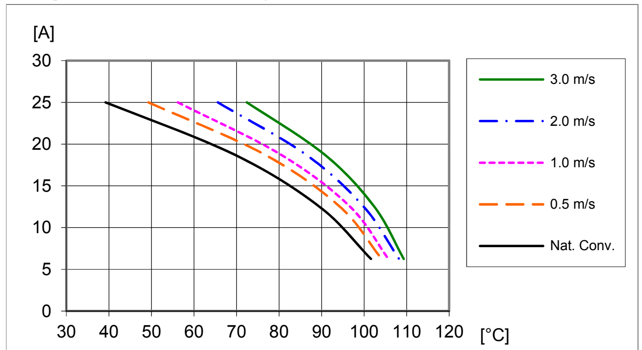
Available load current vs. ambient air temperature and airflow at V_O = 1.0 V, V_I = 12 V. See Thermal Consideration section.

Output Current Derating, V_O = 1.8 V



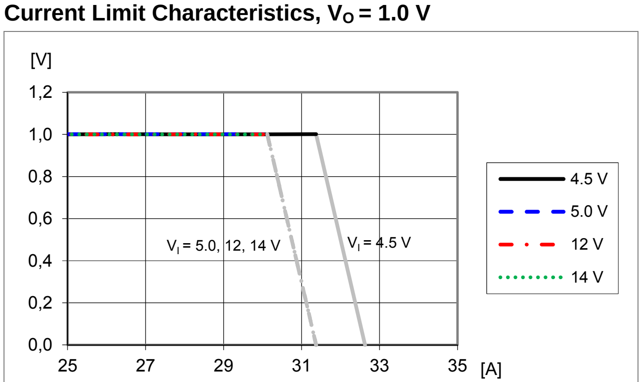
Available load current vs. ambient air temperature and airflow at V_O = 1.8 V, V_I = 12 V. See Thermal Consideration section.

Output Current Derating, V_O = 3.3 V



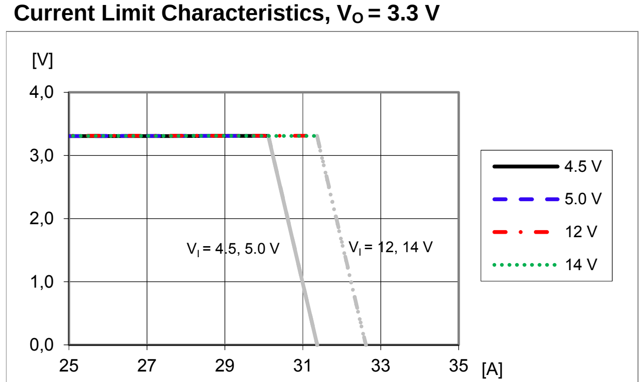
Available load current vs. ambient air temperature and airflow at V_O = 3.3 V, V_I = 12 V. See Thermal Consideration section.

Current Limit Characteristics, V_O = 1.0 V



Output voltage vs. load current at T_{P1} = +25 °C, V_O = 1.0 V.
Note: Output enters hiccup mode at current limit.

Current Limit Characteristics, V_O = 3.3 V

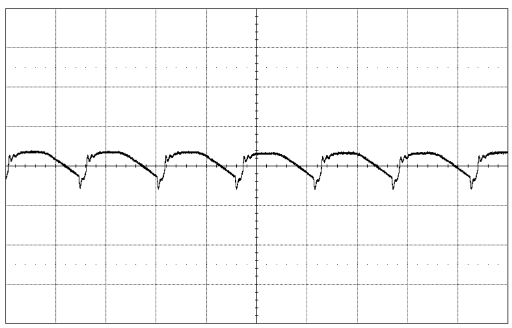


Output voltage vs. load current at T_{P1} = +25 °C, V_O = 3.3 V.
Note: Output enters hiccup mode at current limit.

Typical Characteristics
Output Voltage

BMR 463 2008 (SIP)

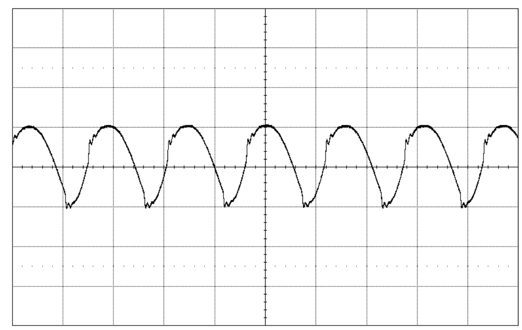
Output Ripple & Noise, V_O = 1.0 V



Output voltage ripple at: T_{P1} = +25 °C, V_I = 12 V, C_O = 470 µF/10 mΩ, I_O = 25 A

Trace: output voltage (20 mV/div.). Time scale: (2 µs/div.).

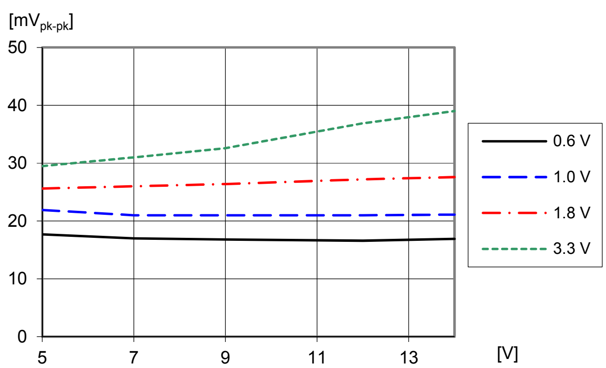
Output Ripple & Noise, V_O = 3.3 V



Output voltage ripple at: T_{P1} = +25 °C, V_I = 12 V, C_O = 470 µF/10 mΩ, I_O = 25 A

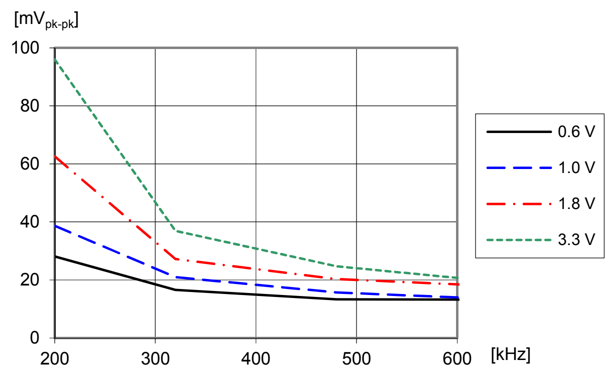
Trace: output voltage (20 mV/div.). Time scale: (2 µs/div.).

Output Ripple vs. Input Voltage



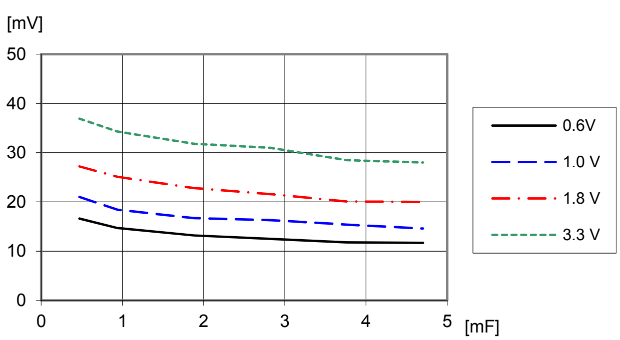
Output voltage ripple V_{pk-pk} at: T_{P1} = +25 °C, C_O = 470 µF/10 mΩ, I_O = 25 A.

Output Ripple vs. Frequency



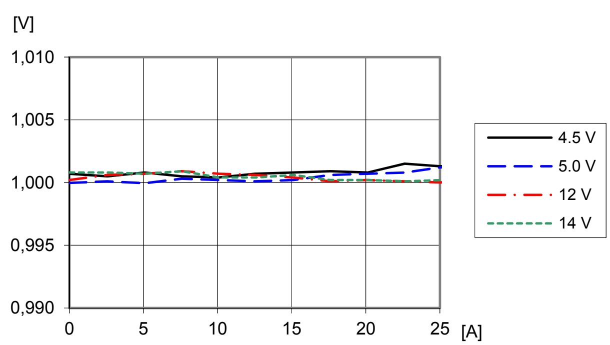
Output voltage ripple V_{pk-pk} at: T_{P1} = +25 °C, V_I = 12 V, C_O = 470 µF/10 mΩ, I_O = 25 A. Default configuration except changed frequency.

Output Ripple vs. External Capacitance



Output voltage ripple V_{pk-pk} at: T_{P1} = +25 °C, V_I = 12 V. I_O = 25 A.
Parallel coupling of capacitors with 470 µF/10 mΩ

Load regulation, V_O = 1.0 V

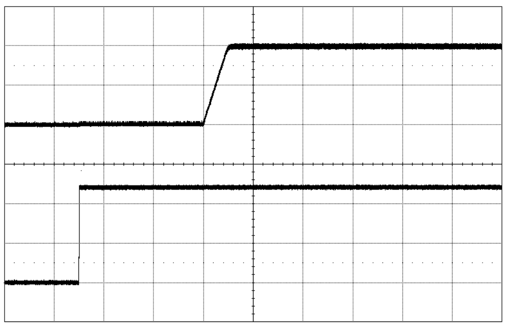


Load regulation at V_o=1.0 V, T_{P1} = +25 °C, C_O = 470 µF/10 mΩ

Typical Characteristics
Start-up and shut-down

BMR 463 2008 (SIP)

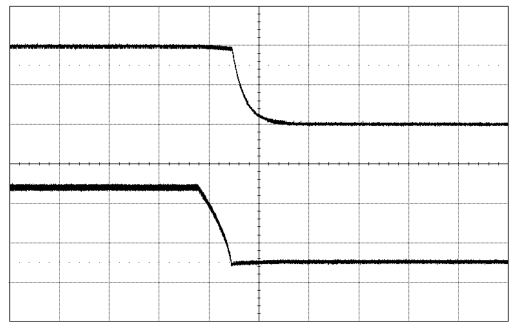
Start-up by input source



Start-up enabled by connecting V_I at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 25 A

Top trace: output voltage (0.5 V/div.).
Bottom trace: input voltage (5 V/div.).
Time scale: (20 ms/div.).

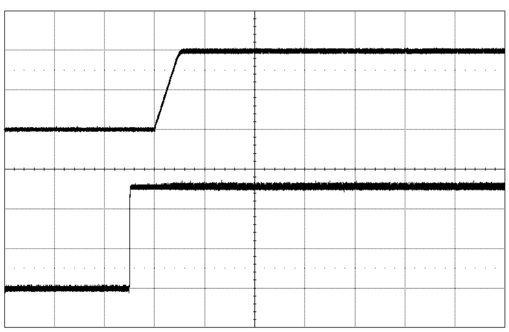
Shut-down by input source



Shut-down enabled by disconnecting V_I at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 25 A

Top trace: output voltage (0.5 V/div).
Bottom trace: input voltage (5 V/div.).
Time scale: (2 ms/div.).

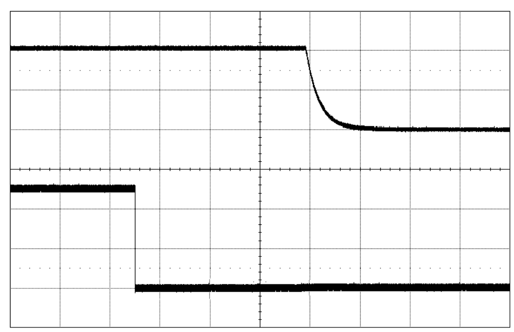
Start-up by CTRL signal



Start-up by enabling CTRL signal at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 25 A

Top trace: output voltage (0.5 V/div.).
Bottom trace: CTRL signal (2 V/div.).
Time scale: (20 ms/div.).

Shut-down by CTRL signal



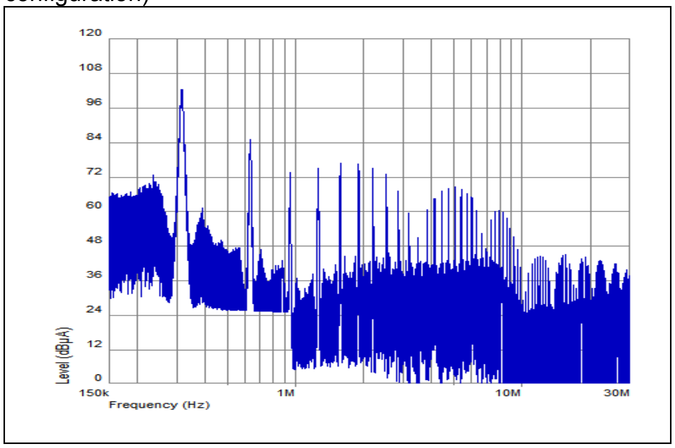
Shut-down enabled by disconnecting V_I at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 25 A

Top trace: output voltage (0.5 V/div).
Bottom trace: CTRL signal (2 V/div.).
Time scale: (2 ms/div.).

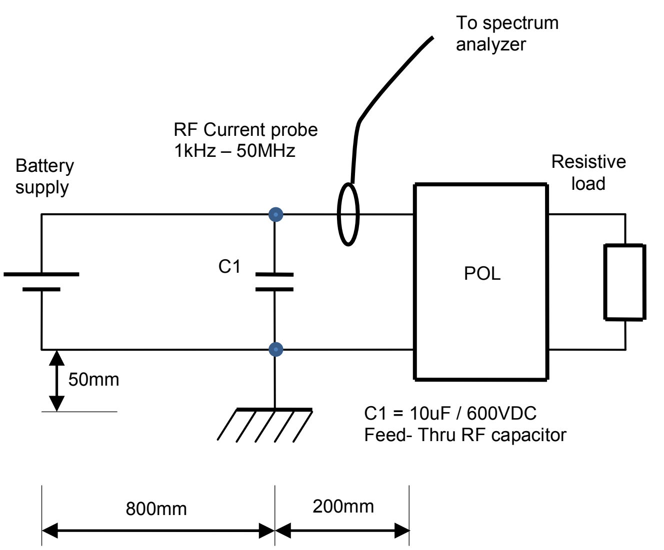
EMC Specification

Conducted EMI measured according to test set-up below. The fundamental switching frequency is 320 kHz at V_I = 12 V, max I_O.

Conducted EMI Input terminal value (typical for default configuration)



EMI without filter for BMR 463 0008



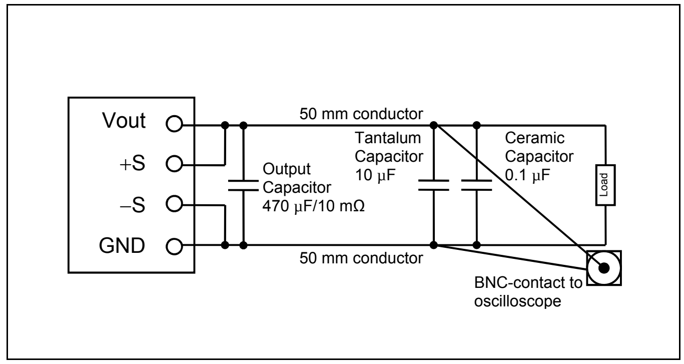
Conducted EMI test set-up

Layout Recommendations

The radiated EMI performance of the product will depend on the PWB layout and ground layer design. It is also important to consider the stand-off of the product. If a ground layer is used, it should be connected to the output of the product and the equipment ground or chassis.
A ground layer will increase the stray capacitance in the PWB and improve the high frequency EMC performance.

Output Ripple and Noise

Output ripple and noise is measured according to figure below. A 50 mm conductor works as a small inductor forming together with the two capacitors as a damped filter.



Output ripple and noise test set-up.

Operating information

Power Management Overview

This product is equipped with a PMBus interface. The product incorporates a wide range of readable and configurable power management features that are simple to implement with a minimum of external components. Additionally, the product includes protection features that continuously safeguard the load from damage due to unexpected system faults. A fault is also shown as an alert on the SALERT pin.
The following product parameters can continuously be monitored by a host: Input voltage, output voltage/current, and internal temperature. If the monitoring is not needed it can be disabled and the product enters a low power mode reducing the power consumption. The protection features are not affected.
The product is delivered with a default configuration suitable for a wide range operation in terms of input voltage, output voltage, and load. The configuration is stored in an internal Non-Volatile Memory (NVM). All power management functions can be reconfigured using the PMBus interface. Please contact your local Ericsson Power Modules representative for design support of custom configurations or appropriate SW tools for design and download of your own configurations.

Input Voltage

The input voltage range, 4.5 - 14 V, makes the product easy to use in intermediate bus applications when powered by a non-regulated bus converter or a regulated bus converter. See Ordering Information for input voltage range.

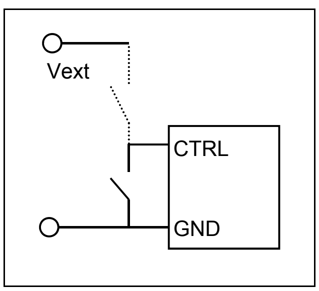
Input Under Voltage Lockout, UVLO

The product monitors the input voltage and will turn-on and turn-off at configured levels. The default turn-on input voltage level setting is 4.20 V, whereas the corresponding turn-off input voltage level is 3.85 V. Hence, the default hysteresis between turn-on and turn-off input voltage is 0.35 V. Once an input turn-off condition occurs, the device can respond in a number of ways as follows:

1. Continue operating without interruption. The unit will continue to operate as long as the input voltage can be supported. If the input voltage continues to fall, there will come a point where the unit will cease to operate.
2. Continue operating for a given delay period, followed by shutdown if the fault still exists. The device will remain in shutdown until instructed to restart.
3. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.

The default response from a turn-off is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition. If the fault condition is no longer present, the product will be re-enabled. The turn-on and turn-off levels and response can be reconfigured using the PMBus interface.

Remote Control



The product is equipped with a remote control function, i.e., the CTRL pin. The remote control can be connected to either the primary negative input connection (GND) or an external voltage (Vext), which is a 3 - 5 V positive supply voltage in accordance to the SMBus Specification version 2.0.

The CTRL function allows the product to be turned on/off by an external device like a semiconductor or mechanical switch. By default the product will turn on when the CTRL pin is left open and turn off when the CTRL pin is applied to GND. The CTRL pin has an internal pull-up resistor. When the CTRL pin is left open, the voltage generated on the CTRL pin is max 5.5 V.
If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to asserting the CTRL pin.
The product can also be configured using the PMBus interface to be "Always on", or turn on/off can be performed with PMBus commands.

Input and Output Impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. The performance in some applications can be enhanced by addition of external capacitance as described under External Decoupling Capacitors. If the input voltage source contains significant inductance, the addition a capacitor with low ESR at the input of the product will ensure stable operation.

External Capacitors

Input capacitors:
The input ripple RMS current in a buck converter is equal to

Eq. 1. $I_{inputRMS} = I_{load}\sqrt{D(1-D)}$,

where I_{load} is the output load current and D is the duty cycle. The maximum load ripple current becomes $I_{load}/2$. The ripple current is divided into three parts, i.e., currents in the input source, external input capacitor, and internal input capacitor. How the current is divided depends on the impedance of the input source, ESR and capacitance values in the capacitors. A minimum capacitance of 300 µF with low ESR is recommended. The ripple current rating of the capacitors must follow Eq. 1. For high-performance/transient applications or wherever the input source performance is degraded, additional low ESR ceramic type capacitors at the input is recommended. The additional input low ESR capacitance above the minimum level insures an optimized performance.

Output capacitors:
When powering loads with significant dynamic current requirements, the voltage regulation at the point of load can be improved by addition of decoupling capacitors at the load.
The most effective technique is to locate low ESR ceramic and electrolytic capacitors as close to the load as possible, using several capacitors in parallel to lower the effective ESR. The ceramic capacitors will handle high-frequency dynamic load changes while the electrolytic capacitors are used to handle low frequency dynamic load changes. Ceramic capacitors will also reduce high frequency noise at the load.
It is equally important to use low resistance and low inductance PWB layouts and cabling.
External decoupling capacitors are a part of the control loop of the product and may affect the stability margins.
Stable operation is guaranteed for the following total capacitance C_O in the output decoupling capacitor bank where

Eq. 2. $C_O = [C_{min}, C_{max}] = [300, 15000]$ µF.

The decoupling capacitor bank should consist of capacitors which has a capacitance value larger than $C \ge C_{min}$ and has an ESR range of

Eq. 3. $ESR = [ESR_{min}, ESR_{max}] = [5, 30]$ mΩ

The control loop stability margins are limited by the minimum time constant τ_{min} of the capacitors. Hence, the time constant of the capacitors should follow Eq. 4.

Eq. 4. $\tau \ge \tau_{min} = C_{min} ESR_{min} = 1.5\,\mu s$

This relation can be used if your preferred capacitors have parameters outside the above stated ranges in Eq. 2 and Eq.3.

- If the capacitors capacitance value is $C < C_{\min}$ one must use at least N capacitors where $N \geq \left\lceil \frac{C_{\min}}{C} \right\rceil$ and $ESR \geq ESR_{\min} \frac{C_{\min}}{C}$.
- If the ESR value is $ESR > ESR_{\max}$ one must use at least N capacitors of that type where $N \geq \left\lceil \frac{ESR}{ESR_{\max}} \right\rceil$ and $C \geq \frac{C_{\min}}{N}$.
- If the ESR value is $ESR < ESR_{\min}$ the capacitance value should be $C \geq C_{\min} \frac{ESR_{\min}}{ESR}$.

For a total capacitance outside the above stated range or capacitors that do not follow the stated above requirements above a re-design of the control loop parameters will be necessary for robust dynamic operation and stability.
See technical paper TP022 for further information.

Control Loop

The product uses a voltage-mode synchronous buck controller with a fixed frequency PWM scheme. Although the product uses a digital control loop, it operates much like a traditional analog PWM controller. As in the analog controller case, the control loop compares the output voltage to the desired voltage reference and compensation is added to keep the loop stable and fast. The resulting error signal is used to drive the PWM logic. Instead of using external resistors and capacitors required with traditional analog control loops, the product uses a digital Proportional-Integral-Derivative (PID) compensator in the control loop. The characteristics of the control loop is configured by setting PID compensation parameters. These PID settings can be reconfigured using the PMBus interface.

Control Loop Compensation Setting

The products without DLC are by default configured with a robust control loop compensation setting (PID setting) which allows for a wide range operation of input and output voltages and capacitive loads as defined in the section External Decoupling Capacitors. For an application with a specific input voltage, output voltage, and capacitive load, the control loop can be optimized for a robust and stable operation and with an improved load transient response. This optimization will minimize the amount of required output decoupling capacitors for a given load transient requirement yielding an optimized cost and minimized board space.

Dynamic Loop Compensation (DLC)

Only some of the products that this specification covers have this feature (see section Ordering Information).
The DLC feature might in some documents be referred to as “Auto Compensation” or “Auto Tuning” feature.
The DLC feature measures the characteristics of the power train and calculates the proper compensator PID coefficients. The default configuration is that once the output voltage ramp up has completed, the DLC algorithm will begin and a new optimized compensator solution (PID setting) will be found and implemented. The DLC algorithm typically takes between 50 ms and 200 ms to complete.
By the PMBus command AUTO_COMP_CONFIG the user may select between several different modes of operation:

- Disable
- Autocomp once, will run DLC algorithm each time the output is enabled (default configuration)
- Autocomp every second will initiate a new DLC algorithm each 1 second
- Autocomp every minute will initiate a new DLC algorithm every minute.

The DLC can also be configured to run once only after the first ramp up (after input power have been applied) and to use that temporary stored PID settings in all subsequent ramps. If input power is cycled a new DLC algorithm will be performed after the first ramp up. The default setting is however to run the DLC algorithm after every ramp up.
The DLC algorithm can also be initiated manually by sending the AUTO_COMP_CONTROL command.
The DLC can also be configured with Auto Comp Gain Control. This scales the DLC results to allow a trade-off between transient response and steady-state duty cycle jitter. A setting of 100% will provide the fastest transient response while a setting of 10% will produce the lowest jitter. The default is 50%.

Changing DLC and PID Setting

Some caution must be considered while DLC is enabled and when it is changed from enabled or disabled.
When operating, the controller IC uses the settings loaded in its (volatile) RAM memory. When the input power is applied the RAM settings are retrieved from the pin-strap resistors and the two non-volatile memories (DEFAULT and USER). The sequence is described in the “Initialization Procedure” section.

<u>When DLC is enabled:</u>
When DLC is enabled, the normal sequence (after input power has been applied) that a value stored in the user non-volatile memory overwrites any previously loaded value does not apply for the PID setting (stored in the PID_TAPS register). The PID setting in the user non-volatile memory is ignored and a non-configurable default PID setting is loaded to RAM to act as a safe starting value for the DLC. Once the output has been enabled and the DLC algorithm has found a new optimized PID setting it will be loaded in RAM and used by the control loop.

When saving changes to the user non-volatile memory, all changes made to the content of RAM will be saved. This also includes the default PID setting (loaded to RAM to act as a safe starting value) or the PID setting changed by the DLC algorithm after enabling output. The result is that as long as DLC is enabled the PID setting in the user non-volatile memory is ignored, but it might accidentally get overwritten.

<u>When changing DLC from disabled to enabled:</u>
A non-configurable default PID setting is loaded to RAM to act as a safe starting value for the DLC (same as above).

When changing DLC from enabled to disabled:
When changing DLC from enabled to disabled, the PID setting in the user non-volatile memory will be loaded to RAM. Any new optimized PID setting in RAM will be lost, if not first stored to the user non-volatile memory.

When DLC is disabled:
When DLC is disabled and input power has been applied, the PID setting in the user non-volatile memory will be loaded to RAM and used in the control loop.
The original PID setting in the user non-volatile memory is quite slow and not recommended for optimal performance. If DLC is disabled it is recommended to either:

1. Use the DLC to find optimized PID setting.
2. Use Loop Compensator Tool in Ericsson Power Designer to find appropriate PID setting.
3. Use Universal PID as defined below.

The Universal PID setting (taps) is:

A = 4580.75,
B = -8544.00,
C = 3972.81

Write 0x7CF84DFE85807D8F26 to PID_TAPS register and write command STORE_USER_ALL

Note that if DLC is enabled, for best results V_I must be stable before DLC algorithm begins.

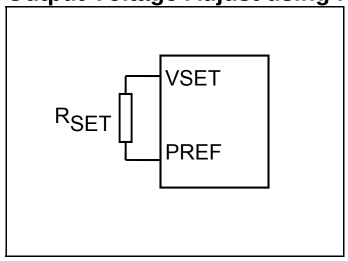
Load Transient Response Optimization

The product incorporates a Non-Linear transient Response, NLR, loop that decreases the response time and the output voltage deviation during a load transient. The NLR results in a higher equivalent loop bandwidth than is possible using a traditional linear control loop. The product is pre-configured with appropriate NLR settings for robust and stable operation for a wide range of input voltage and a capacitive load range as defined in the section External Decoupling Capacitors. For an application with a specific input voltage, output voltage, and capacitive load, the NLR configuration can be optimized for a robust and stable operation and with an improved load transient response. This will also reduce the amount of output decoupling capacitors and yield a reduced cost. However, the NLR slightly reduces the efficiency. In order to obtain maximal energy efficiency the load transient requirement has to be met by the standard control loop compensation and the decoupling capacitors. The NLR settings can be reconfigured using the PMBus interface.
See application note AN306 for further information.

Remote Sense

The product has remote sense that can be used to compensate for voltage drops between the output and the point of load. The sense traces should be located close to the PWB ground layer to reduce noise susceptibility. Due to derating of internal output capacitance the voltage drop should be kept below $V_{DROPMAX} = (5.5 - V_O)/2$. A large voltage drop will impact the electrical performance of the regulator. If the remote sense is not needed, +S should be connected to VOUT and −S should be connected to GND.

Output Voltage Adjust using Pin-strap Resistor



Using an external Pin-strap resistor, R_{SET}, the output voltage can be set in the range 0.6 V to 3.3 V at 28 different levels shown in the table below. The resistor should be applied between the VSET pin and the PREF pin.

R_{SET} also sets the maximum output voltage, see section "Output Voltage Range Limitation". The resistor is sensed only during product start-up. Changing the resistor value during normal operation will not change the output voltage. The input voltage must be at least 1 V larger than the output voltage in order to deliver the correct output voltage. See Ordering Information for output voltage range.

The following table shows recommended resistor values for R_{SET}. Maximum 1% tolerance resistors are required.

V_O [V]	R_{SET}[kΩ]	V_O [V]	R_{SET}[kΩ]
0.60	10	1.50	46.4
0.65	11	1.60	51.1
0.70	12.1	1.70	56.2
0.75	13.3	1.80	61.9
0.80	14.7	1.90	68.1
0.85	16.2	2.00	75
0.90	17.8	2.10	82.5
0.95	19.6	2.20	90.9
1.00	21.5	2.30	100
1.05	23.7	2.50	110
1.10	26.1	3.00	121
1.15	28.7	3.30	133
1.20	31.6		
1.25	34.8		
1.30	38.3		
1.40	42.2		

The output voltage and the maximum output voltage can be pin strapped to three fixed values by connecting the VSET pin according to the table below.

V_O [V]	VSET
0.60	Shorted to PREF
1.2	Open "high impedance"
2.5	Logic High, GND as reference

Output Voltage Adjust using PMBus
The output voltage set by pin-strap can be overridden by configuration file or by using a PMBus command. See Electrical Specification for adjustment range.

When setting the output voltage by configuration file or by a PMBus command, the specified output voltage accuracy is valid only when the set output voltage level falls within the same bin range as the voltage level defined by the pin-strap resistor R_{SET}. The applicable bin ranges are defined in the table below. Valid accuracy for voltage levels outside the applicable bin range is two times the specified.

Example:
Nominal V_O is set to 1.10 V by R_{SET} = 26.1 kΩ. 1.10 V falls within the bin range 0.988-1.383 V, thus specified accuracy is valid when adjusting V_O within 0.988-1.383V.

V_O bin ranges [V]
0.600 – 0.988
0.988 – 1.383
1.383 – 1.975
1.975 – 2.398
2.398 – 2.963
2.963 – 3.753

Output Voltage Range Limitation
The output voltage range that is possible to set by configuration or by the PMBus interface is limited by the pin-strap resistor R_{SET}. The maximum output voltage is set to 110% of the nominal output value defined by R_{SET}, $V_{O,MAX} = 1.1 \times V_{O,RSET}$. This protects the load from an over voltage due to an accidental wrong PMBus command.

Output Voltage Adjust Limitation using PMBus
In addition to the maximum output voltage limitation by the pin-strap resistor R_{SET}, there is also a limitation in how much the output voltage can be increased while the output is enabled. If output is disabled then R_{SET} resistor is the only limitation.

Example:
If the output is enabled with output voltage set to 1.0 V, then it is only possible to adjust/change the output voltage up to 1.7-V as long as the output is enabled.

V_O setting when enabled [V]	V_O set range while enabled [V]
0.000 – 0.988	~0.2 to >1.2
0.988 – 1.383	~0.2 to >1.7
1.383 – 1.975	~0.2 to >2.5
1.975 – 2.398	~0.2 to >2.97
2.398 – 2.963	~0.2 to >3.68
2.963 – 3.753	~0.2 to >4.65

Over Voltage Protection (OVP)
The product includes over voltage limiting circuitry for protection of the load. The default OVP limit is 15% above the nominal output voltage. If the output voltage exceeds the OVP limit, the product can respond in different ways:

1. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.
2. Turn off the high-side MOSFET and turn on the low-side MOSFET. The low-side MOSFET remains ON until the device attempts a restart, i.e. the output voltage is pulled to ground level (crowbar function).

The default response from an overvoltage fault is to immediately shut down as in 2. The device will continuously check for the presence of the fault condition, and when the fault condition no longer exists the device will be re-enabled. For continuous OVP when operating from an external clock for synchronization, the only allowed response is an immediate shutdown. The OVP limit and fault response can be reconfigured using the PMBus interface.

Under Voltage Protection (UVP)
The product includes output under voltage limiting circuitry for protection of the load. The default UVP limit is 15% below the nominal output voltage. The UVP limit can be reconfigured using the PMBus interface.

Power Good
The product provides a Power Good (PG) flag in the Status Word register that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. If specified in section Connections, the product also provides a PG signal output. The PG pin is active high and by default open-drain but may also be configured as push-pull via the PMBus interface.
By default, the PG signal will be asserted when the output reaches above 90% of the nominal voltage, and de-asserted when the output falls below 85% of the nominal voltage. These limits may be changed via the PMBus interface. A PG delay period is defined as the time from when all conditions within the product for asserting PG are met to when the PG signal is actually asserted. The default PG delay is set to 10 ms. This value can be reconfigured using the PMBus interface.
For products with DLC the PG signal is by default asserted directly after the DLC operation have been completed. If DLC is disabled the configured PG delay will be used. This can be reconfigured using the PMBus interface.

Switching Frequency
The fundamental switching frequency is 320 kHz, which yields optimal power efficiency. The switching frequency can be set to any value between 200 kHz and 640 kHz using the PMBus interface. The switching frequency will change the efficiency/power dissipation, load transient response and output ripple. For optimal control loop performance the control loop must be re-designed when changing the switching frequency.

Synchronization

Synchronization is a feature that allows multiple products to be synchronized to a common frequency. Synchronized products powered from the same bus eliminate beat frequencies reflected back to the input supply, and also reduces EMI filtering requirements. Eliminating the slow beat frequencies (usually <10 kHz) allows the EMI filter to be designed to attenuate only the synchronization frequency. Synchronization can also be utilized for phase spreading, described in section Phase Spreading.
The products can be synchronized with an external oscillator or one product can be configured with the SYNC pin as a SYNC Output working as a master driving the synchronization. All others on the same synchronization bus must be configured with SYNC Input. Default configuration is using the internal clock, independently of signal at the SYNC pin.
See application note AN309 for further information.

Phase Spreading

When multiple products share a common DC input supply, spreading of the switching clock phase between the products can be utilized. This dramatically reduces input capacitance requirements and efficiency losses, since the peak current drawn from the input supply is effectively spread out over the whole switch period. This requires that the products are synchronized. Up to 16 different phases can be used.
The phase spreading of the product can be configured using the PMBus interface.
See application note AN309 for further information.

Parallel Operation (Current Sharing)

Paralleling multiple products can be used to increase the output current capability of a single power rail. By connecting the GCB pins of each device and configuring the devices as a current sharing rail, the units will share the current equally, enabling up to 100% utilization of the current capability for each device in the current sharing rail. The product uses a low-bandwidth, first-order digital current sharing by aligning the output voltage of the slave devices to deliver the same current as the master device. Artificial droop resistance is added to the output voltage path to control the slope of the load line curve, calibrating out the physical parasitic mismatches due to power train components and PWB layout. Up to 7 devices can be configured in a given current sharing group.
See application note AN307 for further information.

Phase Adding and Shedding for Parallel Operation

During periods of light loading, it may be beneficial to disable one or more phases (modules) in order to eliminate the current drain and switching losses associated with those phases, resulting in higher efficiency. The product offers the ability to add and drop phases (modules) using a PMBus command in response to an observed load current change. All phases (modules) in a current share rail are considered active prior to the current sharing rail ramp to power-good. Phases can be dropped after power-good is reached. Any member of the current sharing rail can be dropped. If the reference module is dropped, the remaining active module with the lowest member position will become the new reference. Additionally, any change to the number of members of a current sharing rail will precipitate autonomous phase distribution within the rail where all active phases realign their phase position based on their order within the number of active members. If the members of a current sharing rail are forced to shut down due to an observed fault, all members of the rail will attempt to re-start simultaneously after the fault has cleared.
See application note AN307 for further information.

Efficiency Optimized Dead Time Control

The product utilizes a closed loop algorithm to optimize the dead-time applied between the gate drive signals for the switch and synch FETs. The algorithm constantly adjusts the deadtime non-overlap to minimize the duty cycle, thus maximizing efficiency. This algorithm will null out deadtime differences due to component variation, temperature and loading effects. The algorithm can be configured via the PMBus interface.

Over Current Protection (OCP)

The product includes current limiting circuitry for protection at continuous overload. The following OCP response options are available:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

The default response from an over current fault is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition, and if the fault condition no longer exists the device will be re-enabled. The load distribution should be designed for the maximum output short circuit current specified. The OCP limit and response of the product can be reconfigured using the PMBus interface.

Initialization Procedure

The product follows a specific internal initialization procedure after power is applied to the VIN pin:

1. Status of the address and output voltage pin-strap pins are checked and values associated with the pin settings are loaded to RAM.
2. Values stored in the Ericsson default non-volatile memory are loaded to RAM. This overwrites any previously loaded values.
3. Values stored in the user non-volatile memory are loaded to RAM. This overwrites any previously loaded values.

Once the initialization process is completed, the product is ready to be enabled using the CTRL pin. The product is also ready to accept commands via the PMBus interface, which will overwrite any values loaded during the initialization procedure.

Soft-start Power Up

The soft-start control introduces a time-delay before allowing the output voltage to rise. Once the initialization time has passed the device will wait for the configured delay period prior to starting to ramp its output. After the delay period has expired, the output will begin to ramp towards its target voltage according to the configured soft-start ramp time.
The default settings for the soft-start delay period and the soft-start ramp time is 10 ms. Hence, power-up is completed within 20 ms in default configuration using remote control. When the soft-start delay time is set to 0 ms, the module will begin its ramp-up after the internal circuitry has initialized (approximately 2 ms). It is generally recommended to set the soft-start ramp-up time to a value greater than 500 µs to prevent inadvertent fault conditions due to excessive inrush current. The acctual minimum ramp-up time will however normally be limited by the control loop settings and ramp-up times of internal interface voltages in the controller circuit to approximatley 2 ms. The soft-start power up of the product can be reconfigured using the PMBus interface.

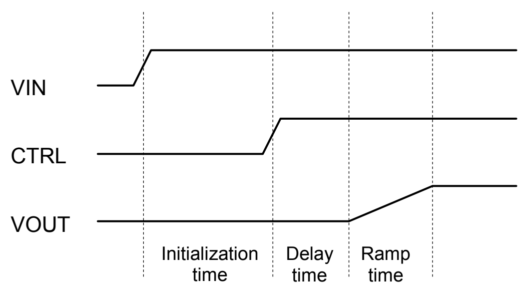


Illustration of Power Up Procedure.

Output Voltage Sequencing

A group of products may be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs, and ASICs that require one supply to reach its operating voltage prior to another. Multi-product sequencing can be achieved by configuring the start delay and rise time of each device through the PMBus interface and by using the CTRL start signal.
See application note AN310 for further information.

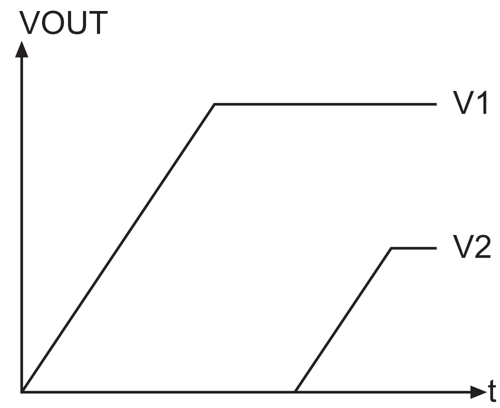


Illustration of Output Voltage Sequencing.

Voltage Tracking

The product integrates a lossless tracking scheme that allows its output to track a voltage that is applied to the VTRK pin with no external components required. During ramp-up, the output voltage follows the VTRK voltage until the preset output voltage level is met. The product offers two modes of tracking as follows:

1. Coincident. This mode configures the product to ramp its output voltage at the same rate as the voltage applied to the VTRK pin.

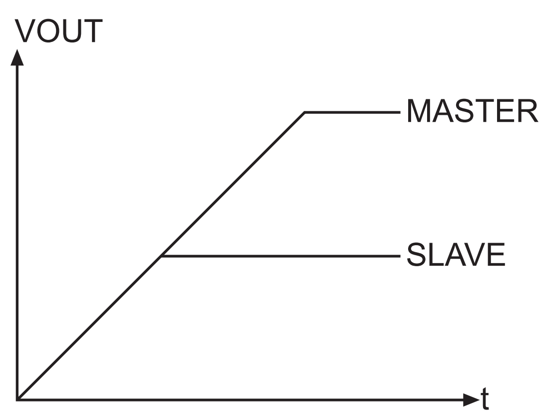


Illustration of Coincident Voltage Tracking.

2. Ratiometric. This mode configures the product to ramp its output voltage at a rate that is a percentage of the voltage applied to the VTRK pin. The default setting is 50%, but a different tracking ratio may be set by an external resistive voltage divider or through the PMBus interface.

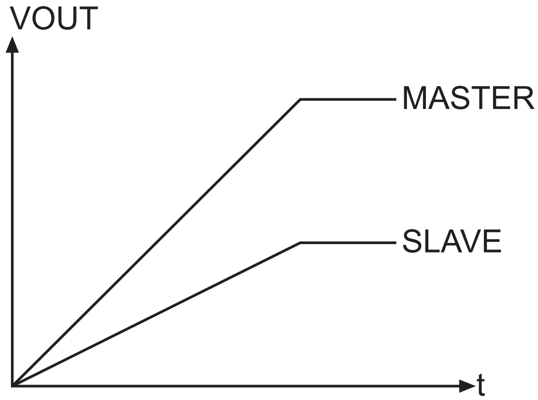


Illustration of Ratiometric Voltage Tracking

The master device in a tracking group is defined as the device that has the highest target output voltage within the group. This master device will control the ramp rate of all tracking devices and is not configured for tracking mode. All of the CTRL pins in the tracking group must be connected and driven by a single logic source. It should be noted that current sharing groups that are also configured to track another voltage do not offer pre-bias protection; a minimum load should therefore be enforced to avoid the output voltage from being held up by an outside force.
See application note AN310 for further information.

Voltage Margining Up/Down

The product can adjust its output higher or lower than its nominal voltage setting in order to determine whether the load device is capable of operating over its specified supply voltage range. This provides a convenient method for dynamically testing the operation of the load circuit over its supply margin or range. It can also be used to verify the function of supply voltage supervisors. Margin limits of the nominal output voltage ±5% are default, but the margin limits can be reconfigured using the PMBus interface.

Pre-Bias Startup Capability

Pre-bias startup often occurs in complex digital systems when current from another power source is fed back through a dual-supply logic component, such as FPGAs or ASICs. The BMR463 product family incorporates synchronous rectifiers, but will not sink current during startup, or turn off, or whenever a fault shuts down the product in a pre-bias condition. Pre-bias protection is not offered for current sharing groups that also have voltage tracking enabled.

Group Communication Bus

The Group Communication Bus, GCB, is used to communicate between products. This dedicated bus provides the communication channel between devices for features such as sequencing, fault spreading, and current sharing. The GCB solves the PMBus data rate limitation. The GCB pin on all devices in an application should be connected together. A pull-up resistor is required on the common GCB in order to guarantee the rise time as follows:

Eq. 5. $\tau = R_{GCB}\, C_{GCB} \le 1\,\mu\text{s}$,

where R_{GCB} is the pull up resistor value and C_{GCB} is the bus loading. The pull-up resistor should be tied to an external supply voltage in range from 3.3 to 5 V, which should be present prior to or during power-up.
If exploring untested compensation or deadtime configurations, it is recommended that 27 Ω series resistors are placed between the GCB pin of each product and the common GCB connection. This will avoid propagation of faults between products potentially caused by hazardous configuration settings. When the configurations of the products are settled the series resistors can be removed.
The GCB is an internal bus, such that it is only connected across the modules and not the PMBus system host. GCB addresses are assigned on a rail level, i.e. modules within the same current sharing group share the same GCB address. Addressing rails across the GCB is done with a 5 bit GCB ID, yielding a theoretical total of 32 rails that can be shared with a single GCB bus. See application note AN307 for further information.

Fault spreading

The product can be configured to broadcast a fault event over the GCB bus to the other devices in the group. When a non-destructive fault occurs and the device is configured to shut down on a fault, the device will shut down and broadcast the fault event over the GCB bus. The other devices on the GCB bus will shut down together if configured to do so, and will attempt to re-start in their prescribed order if configured to do so.

Over Temperature Protection (OTP)

The products are protected from thermal overload by an internal over temperature shutdown function in the controller circuit N1, located at position P2 (see section Thermal Consideration). Some of the products that this specification covers use the temperature at position P2 (T_{P2}) as a reference for OTP and some use position P1 (T_{P1}) as a reference for OTP. See the Over Temperature Protection section in the electrical specification for each product.

Products with P1 as reference for OTP:
When T_{P1} as defined in thermal consideration section exceeds approximately 120 °C the product will shut down. The specified OTP level and hysteresis are valid for worst case operation regarding cooling conditions, input voltage and output voltage. The actually configured default value in the controller circuit in position P2 is 110 °C, but at worst case operation the

temperature is approximately 10 °C higher at position P1. At light load the temperature is approximately the same in position P1 and P2. This means the OTP level and hysteresis will be lower at light load conditions when P1 is used as reference for OTP.

Products with P2 as reference OTP:
When T_{P2} as defined in thermal consideration section exceeds 120 °C the product will shut down. For products with P2 as a reference for OTP the configured default value in the controller circuit in position P2 is 120 °C.

The OTP level, hysteresis, and fault response of the product can be reconfigured using the PMBus interface. The fault response can be configured as follows:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts (default configuration).
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

Optimization examples

This product is designed with a digital control circuit. The control circuit uses a configuration file which determines the functionality and performance of the product. It is possible to change the configuration file to optimize certain performance characteristics. In the table below is a schematic view on how to change different configuration parameters in order to achieve an optimization towards a wanted performance.

↑	Increase
→	No change
↓	Decrease

Config. parameters	Switching frequency	Control loop bandwidth	NLR threshold	Diode emulation (DCM)	Min. pulse
Optimized performance					
Maximize efficiency	↓	→	↑	Enable	Disable
Minimize ripple ampl.	↑	→	↑	Enable or disable	Enable or disable
Improve load transient response	↑	↑	↓	Disable	Disable
Minimize idle power loss	↓	↑	→	Enable	Enable

Note: The following table, graphs and waveforms are only examples and valid for BMR 463 0008 and BMR 463 1008.

P_{li}	Input idling power (no load)	Default configuration: Continues Conduction Mode, CCM	V_O = 0.6 V	0.56	W
			V_O = 1.0 V	0.57	
			V_O = 1.8 V	0.67	
			V_O = 3.3 V	0.92	
		DCM, Discontinues Conduction Mode (diode emulation)	V_O = 0.6 V	0.20	W
			V_O = 1.0 V	0.20	
			V_O = 1.8 V	0.20	
			V_O = 3.3 V	0.20	
		DCM with Minimum Pulse Enabled	V_O = 0.6 V	0.32	W
			V_O = 1.0 V	0.33	
			V_O = 1.8 V	0.35	
			V_O = 3.3 V	0.43	
P_{CTRL}	Input standby power	Turned off with CTRL-pin	Default configuration: Monitoring enabled	170	mW
			Pulse monitor mode: Monitoring disabled	108	mW
			Low power mode: Monitoring disabled	84	mW
V_{tr1}	Load transient peak voltage deviation Load step 25-75-25% of max I_O	Default configuration di/dt = 2 A/µs C_O = 470 µF	V_O = 0.6 V	95	mV
			V_O = 1.0 V	105	
			V_O = 1.8 V	115	
			V_O = 3.3 V	168	
		DLC and Optimized NLR configuration di/dt = 2 A/µs C_O = 470 µF	V_O = 0.6 V	63	mV
			V_O = 1.0 V	71	
			V_O = 1.8 V	79	
			V_O = 3.3 V	108	
t_{tr1}	Load transient recovery time Load step 25-75-25% of max I_O	Default configuration di/dt = 2 A/µs C_O=470 µF	V_O = 0.6 V	74	µs
			V_O = 1.0 V	85	
			V_O = 1.8 V	122	
			V_O = 3.3 V	140	
		DLC and Optimized NLR configuration di/dt = 2 A/µs C_O = 470 µF	V_O = 0.6 V	40	
			V_O = 1.0 V	40	
			V_O = 1.8 V	50	
			V_O = 3.3 V	50	

BMR 463 series POL Regulators Input 4.5-14 V, Output up to 25 A / 82.5 W	EN/LZT 146 434 R4B February 2014
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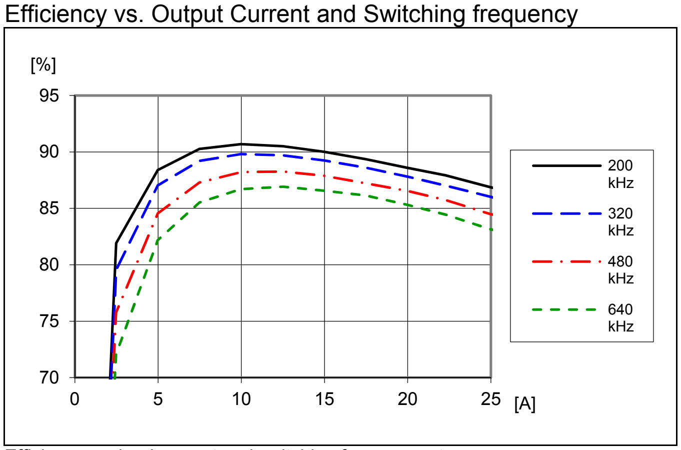
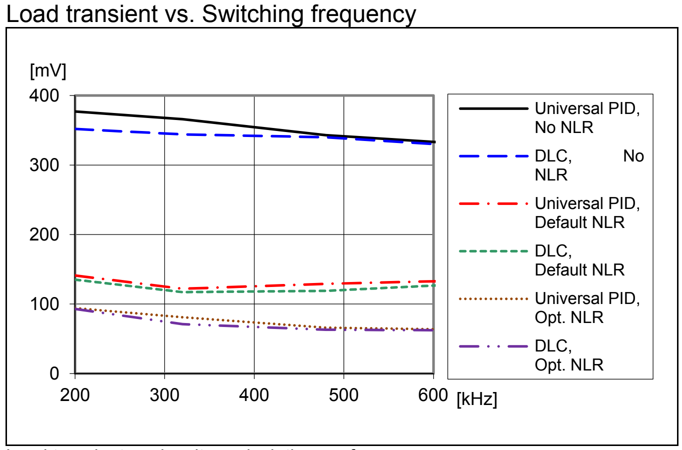
Efficiency vs. Output Current and Switching frequency



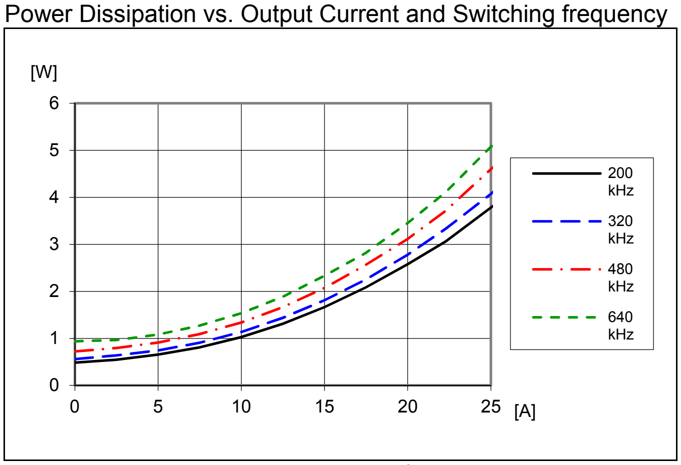
Efficiency vs. load current and switching frequency at
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ
Default configuration except changed frequency

Load transient vs. Switching frequency



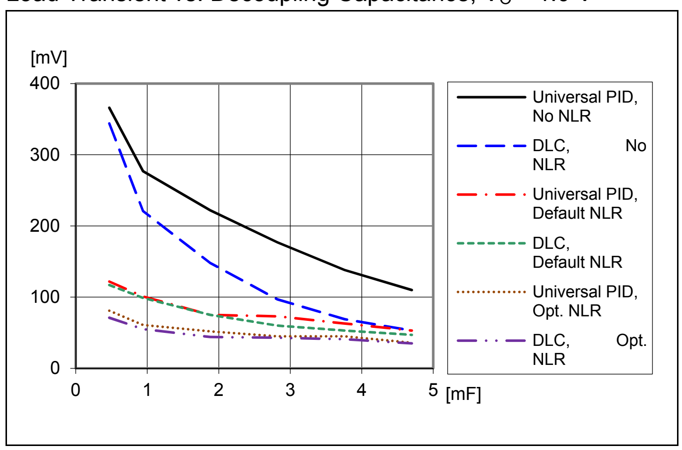
Load transient peak voltage deviation vs. frequency.
Step-change (6.25-18.75-6.25 A).
TP1 = +25 °C, V_I = 12 V, V_O =1.0 V, C_O = 470 µF/10 mΩ

Power Dissipation vs. Output Current and Switching frequency



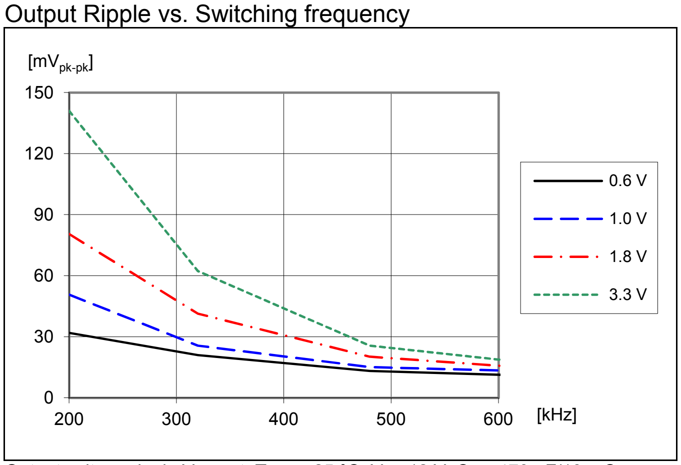
Dissipated power vs. load current and switching frequency at
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ
Default configuration except changed frequency

Load Transient vs. Decoupling Capacitance, V_O = 1.0 V



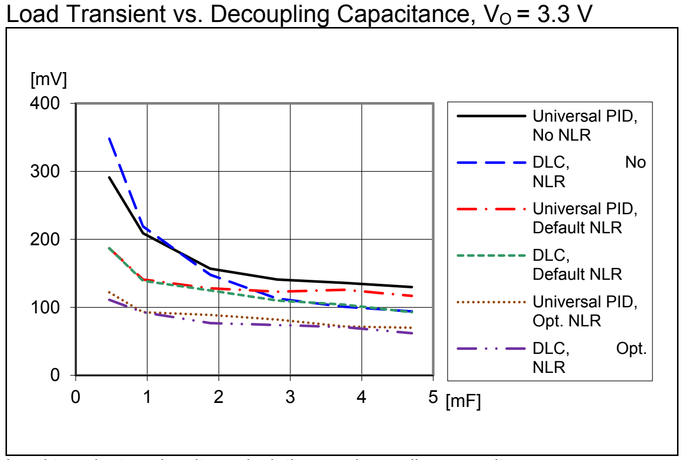
Load transient peak voltage deviation vs. decoupling capacitance.
Step (6.25-18.75-6.25 A). Parallel coupling of capacitors with 470 µF/10 mΩ,
T_{P1} = +25 °C. V_I = 12 V, V_O = 1.0 V, f_{sw} = 320 kHz, di/dt = 2 A/µs

Output Ripple vs. Switching frequency



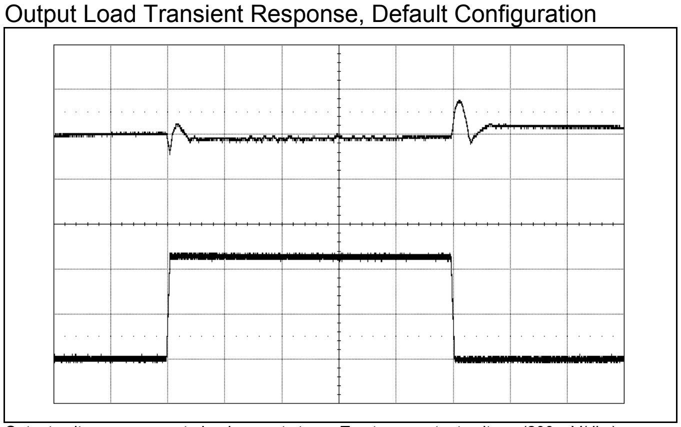
Output voltage ripple V_{pk-pk} at: T_{P1} = +25 °C, V_I = 12 V, C_O = 470 µF/10 mΩ,
I_O = 25 A resistive load. Default configuration except changed frequency.

Load Transient vs. Decoupling Capacitance, V_O = 3.3 V



Load transient peak voltage deviation vs. decoupling capacitance.
Step (6.25-18.75-6.25 A). Parallel coupling of capacitors with 470 µF/10 mΩ,
T_{P1} = +25 °C. V_I = 12 V, V_O = 3.3 V, f_{sw} = 320 kHz, di/dt = 2 A/µs

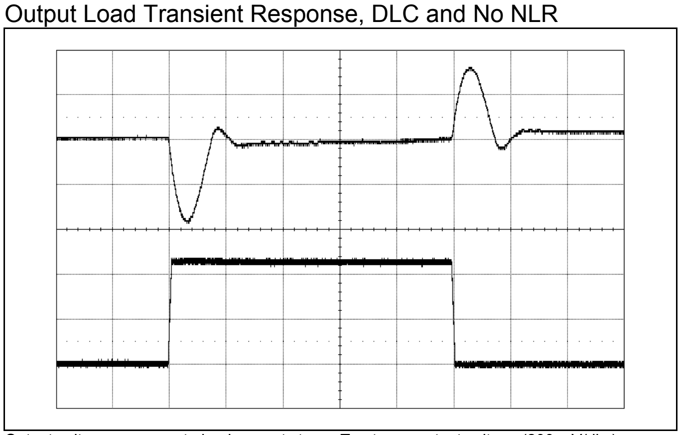
Output Load Transient Response, Default Configuration



Output voltage response to load current step-change (6.25-18.75-6.25 A) at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
di/dt=2 A/μs, f_{sw} = 320 kHz, C_O = 470 μF/10 mΩ
Default configuration (DLC and default NLR)

Top trace: output voltage (200 mV/div.).
Bottom trace: load current (5 A/div.).
Time scale: (0.1 ms/div.).

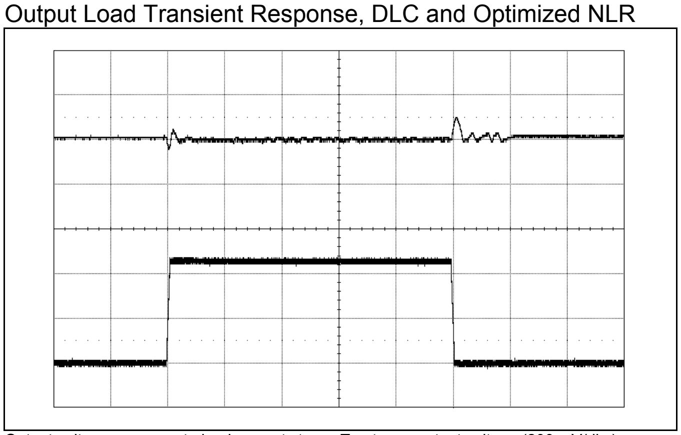
Output Load Transient Response, DLC and No NLR



Output voltage response to load current step-change (6.25-18.75-6.25 A) at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
di/dt=2 A/μs, f_{sw} = 320 kHz, C_O = 470 μF/10 mΩ
DLC and no NLR

Top trace: output voltage (200 mV/div.).
Bottom trace: load current (5 A/div.).
Time scale: (0.1 ms/div.).

Output Load Transient Response, DLC and Optimized NLR



Output voltage response to load current step-change (6.25-18.75-6.25 A) at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
di/dt=2 A/μs, f_{sw} = 320 kHz, C_O = 470 μF/10 mΩ
DLC and optimized NLR

Top trace: output voltage (200 mV/div.).
Bottom trace: load current (5 A/div.).
Time scale: (0.1 ms/div.).

BMR 463 series POL Regulators Input 4.5-14 V, Output up to 25 A / 82.5 W	EN/LZT 146 434 R4B February 2014
	© Ericsson AB

Thermal Consideration

General

The product is designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation.
Cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependent on the airflow across the product. Increased airflow enhances the cooling of the product.
The Output Current Derating graph found in the Output section for each model provides the available output current vs. ambient air temperature and air velocity at specified V_I.

The product is tested on a 254 x 254 mm, 35 µm (1 oz), test board mounted vertically in a wind tunnel with a cross-section of 608 x 203 mm. The test board has 8 layers.

Proper cooling of the product can be verified by measuring the temperature at positions P1 and P2. The temperature at these positions should not exceed the max values provided in the table below.
Note that the max value is the absolute maximum rating (non destruction) and that the electrical Output data is guaranteed up to T_{P1} +95 °C.

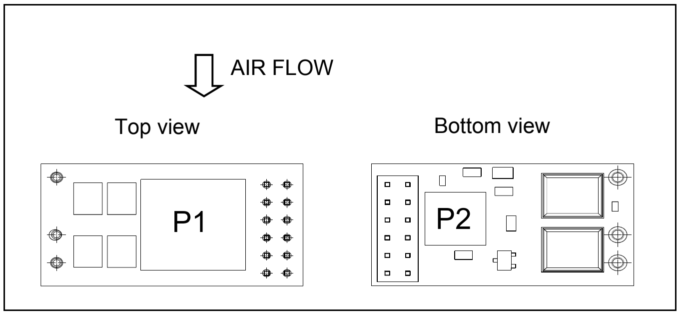
See Design Note 019 for further information.

Definition of product operating temperature

The product operating temperatures are used to monitor the temperature of the product, and proper thermal conditions can be verified by measuring the temperature at positions P1 and P2. The temperature at these positions (T_{P1}, T_{P2}) should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology. Temperatures above maximum T_{P1}, measured at the reference point P1 are not allowed and may cause permanent damage. It should also be noted that depending on setting of the over temperature protection (OTP) and operating conditions, the product may shut down before the maximum allowed temperature at T_{P1} is reached.

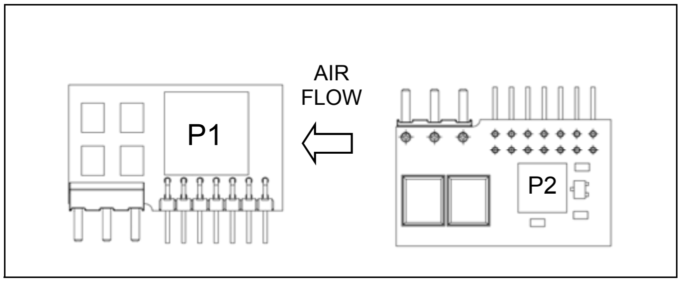
Position	Description	Max Temp.
P1	Reference point, L1, inductor	125 °C*
P2	N1, control circuit	125 °C*

* A guard band of 5 °C is applied to the maximum recorded component temperatures when calculating output current derating curves.



Temperature positions and air flow direction.

SIP version

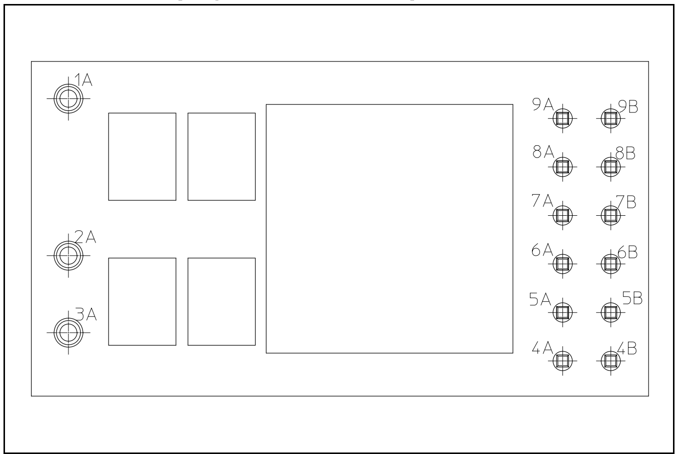


Temperature positions and air flow direction.

Definition of reference temperature T_{P1}

The reference temperature is used to monitor the temperature limits of the product. Temperature above maximum T_{P1}, measured at the reference point P1 is not allowed and may cause degradation or permanent damage to the product. T_{P1} is also used to define the temperature range for normal operating conditions. T_{P1} is defined by the design and used to guarantee safety margins, proper operation and high reliability of the product.

Connections (Lay Down version)



Pin layout, top view (component placement for illustration only).

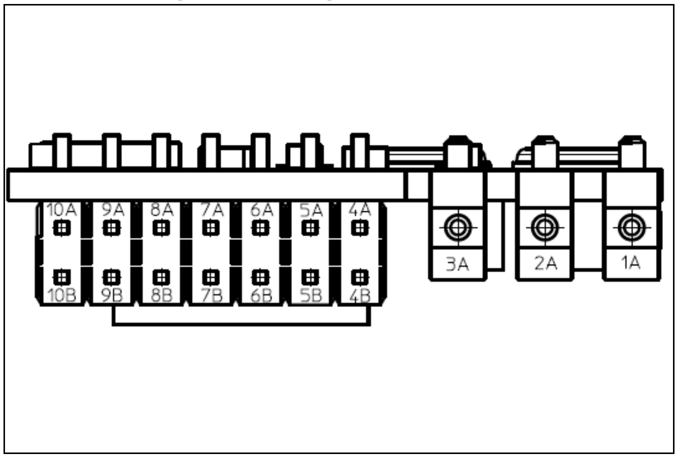
Pin	Designation	Function
1A	VIN	Input Voltage
2A	GND	Power Ground
3A	VOUT	Output Voltage
4A	VTRK or PG*	Voltage Tracking input or Power Good
4B	PREF	Pin-strap reference
5A	+S	Positive sense
5B	−S	Negative sense
6A	SA0	PMBus address pin-strap
6B	GCB	Group Communication Bus
7A	SCL	PMBus Clock
7B	SDA	PMBus Data
8A	VSET	Output voltage pin-strap
8B	SYNC	Synchronization I/O
9A	SALERT	PMBus Alert
9B	CTRL	Remote Control

*

BMR 463 0002, BMR 463 1002, BMR 463 0008, BMR 463 1008: Pin 4A = VTRK pin.

BMR 463 0006, BMR 463 1006, BMR 463 0009, BMR 463 1009: Pin 4A = PG pin.
For these products the PG pin is internally tied to the VTRK input of the products' controller. Typically the VTRK input bias current will be equivalent to a 50 kΩ pull-down resistor. This should be considered when choosing pull-up resistor for the PG signal.

Connections (SIP version)



Pin layout, bottom view (component placement for illustration only).

Pin	Designation	Function
1A	VIN	Input Voltage
2A	GND	Power Ground
3A	VOUT	Output Voltage
4A	+S	Positive sense
4B	−S	Negative sense
5A	VSET	Output voltage pin-strap
5B	VTRK	Voltage Tracking input
6A	SALERT	PMBus Alert
6B	SDA	PMBus Data
7A	SCL	PMBus Clock
7B	SA1	PMBus address pin-strap 1
8A	SA0	PMBus address pin-strap 0
8B	SYNC	Synchronization I/O
9A	PG	Power Good
9B	CTRL	Remote Control
10A	GCB	Group Communication Bus
10B	PREF	Pin-strap reference

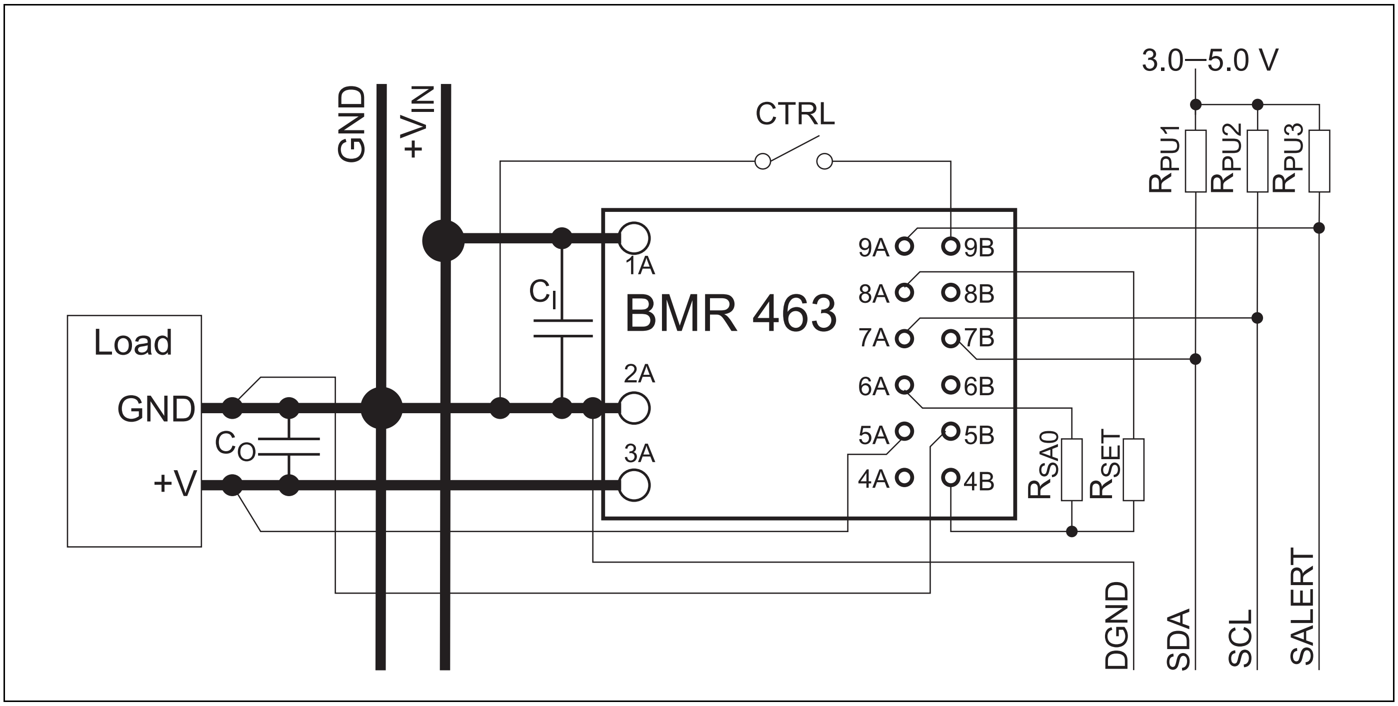
Unused input pins

Unused SDA, SCL and GCB pins should still have pull-up resistors as specified.
Unused VTRK or SYNC pins should be left unconnected or connected to the PREF pin.
Unused CTRL pin can be left open due to internal pull-up.
VSET and SA0/SA1 pins are never unused. These pins must have pin-strap resistors or strapping settings as specified.

PWB layout considerations

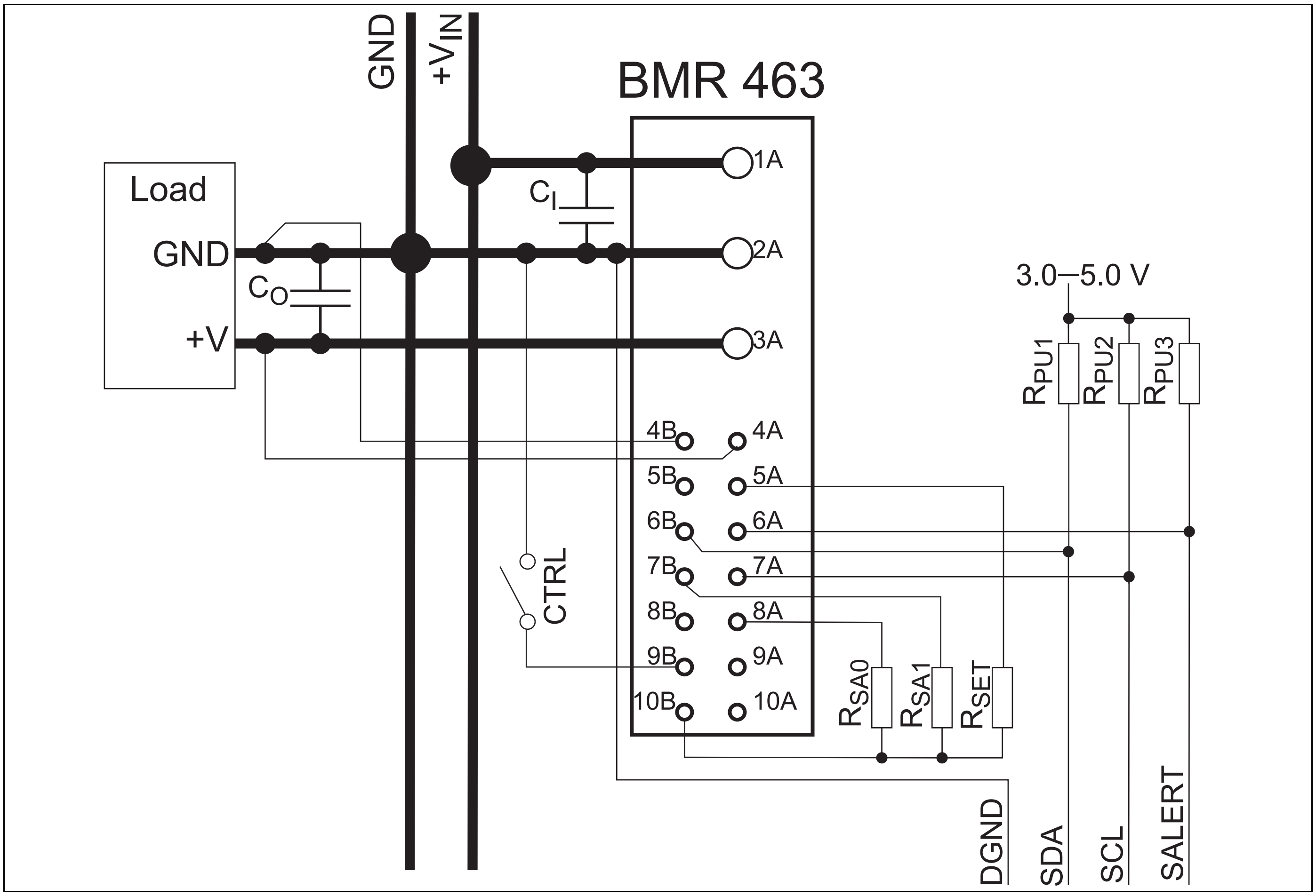
The pin-strap resistors, R_{SET}, and R_{SA0}/R_{SA1} should be placed as close to the product as possible to minimize loops that may pick up noise.
Avoid current carrying planes under the pin-strap resistors and the PMBus signals.
The capacitor C_I (or capacitors implementing it) should be placed as close to the input pins as possible.
Capacitor C_O (or capacitors implementing it) should be placed close to the load.
Care should be taken in the routing of the connections from the sensed output voltage to the S+ and S– terminals. These sensing connections should be routed as a differential pair, preferably between ground planes which are not carrying high currents. The routing should avoid areas of high electric or magnetic fields.

Typical Application Circuit (Lay Down version)



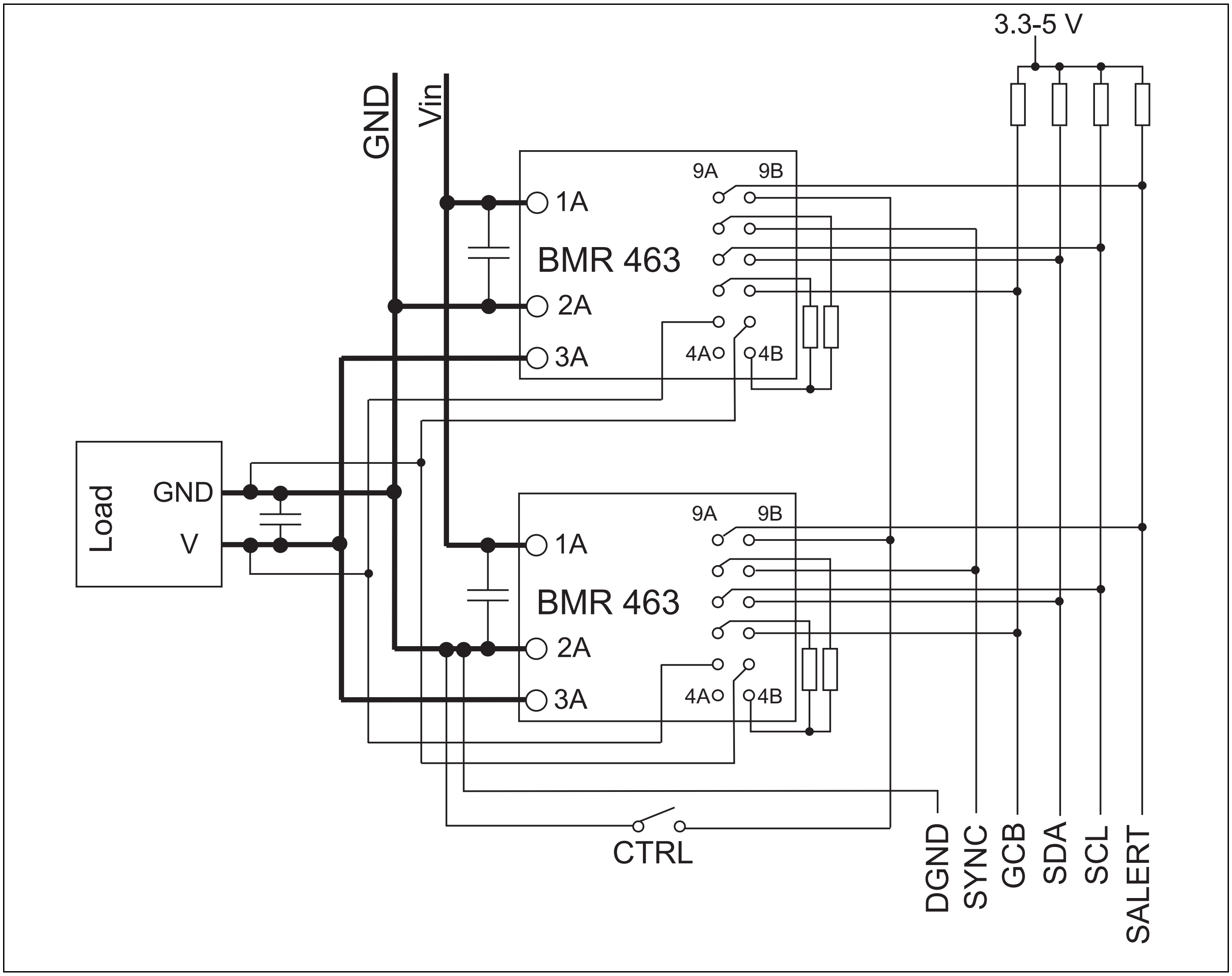
Standalone operation with PMBus communication. Top view of product footprint.

Typical Application Circuit (SIP version)



Standalone operation with PMBus communication. Top view of product footprint.

Typical Application Circuit – Parallel Operation



Parallel operation.

PMBus interface

This product provides a PMBus digital interface that enables the user to configure many aspects of the device operation as well as to monitor the input and output voltages, output current and device temperature. The product can be used with any standard two-wire I^2C or SMBus host device. In addition, the product is compatible with PMBus version 1.1 and includes an SALERT line to help mitigate bandwidth limitations related to continuous fault monitoring. The product supports 100 kHz bus clock frequency only. The PMBus signals, SCL, SDA and SALERT require passive pull-up resistors as stated in the SMBus Specification. Pull-up resistors are required to guarantee the rise time as follows:

Eq. 6 $$\tau = R_P C_p \leq 1\mu s$$

where R_p is the pull-up resistor value and C_p is the bus loading, the maximum allowed bus load is 400 pF. The pull-up resistor should be tied to an external supply voltage in range from 2.7 to 5.5 V, which should be present prior to or during power-up. If the proper power supply is not available, voltage dividers may be applied. Note that in this case, the resistance in the equation above corresponds to parallel connection of the resistors forming the voltage divider.
See application note AN304 for details on interfacing the product with a microcontroller.

Monitoring via PMBus

It is possible to monitor a wide variety of parameters through the PMBus interface. Fault conditions can be monitored using the SALERT pin, which will be asserted when any number of pre-configured fault or warning conditions occurs. It is also possible to continuously monitor one or more of the power conversion parameters including but not limited to the following:

- Input voltage (READ_VIN)
- Output voltage (READ_VOUT)
- Output current (READ_IOUT)
- Internal junction temperature (READ_TEMPERATURE_1)
- Switching frequency (READ_FREQUENCY)
- Duty cycle (READ_DUTY_CYCLE)

In the default configuration monitoring is enabled also when the output voltage is disabled. This can be changed in order to reduce standby power consumption.

Snap shot parameter capture

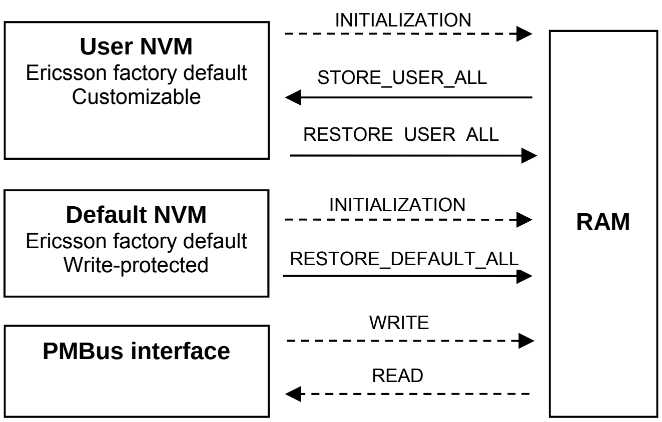
This product offers a special feature that enables the user to capture parametric data during normal operation or following a fault. The following parameters are stored:

- Input voltage
- Output voltage
- Output current
- Internal junction temperature
- Switching frequency
- Duty cycle
- Status registers

The Snapshot feature enables the user to read the parameters via the PMBus interface during normal operation, although it should be noted that reading the 22 bytes will occupy the bus for some time. The Snapshot enables the user to store the snapshot parameters to Flash memory in response to a pending fault as well as to read the stored data from Flash memory after a fault has occurred. Automatic store to Flash memory following a fault is triggered when any fault threshold level is exceeded, provided that the specific fault response is to shut down. Writing to Flash memory is not allowed if the device is configured to restart following the specific fault condition. It should also be noted that the device supply voltage must be maintained during the time the device is writing data to Flash memory; a process that requires between 700-1400 µs depending on whether the data is set up for a block write. Undesirable results may be observed if the input voltage of the product drops below 3.0 V during this process.

Non-Volatile Memory (NVM)

The product incorporates two Non-Volatile Memory areas for storage of the supported PMBus commands; the Default NVM and the User NVM.
The Default NVM is pre-loaded with Ericsson factory default values. The Default NVM is write-protected and can be used to restore the Ericsson factory default values through the command RESTORE_DEFAULT_ALL.
The User NVM is pre-loaded with Ericsson factory default values. The User NVM is writable and open for customization.
The values in NVM are loaded into operational RAM during initialization according to section "Initialization Procedure", where after commands can be changed through the PMBus Interface. The STORE_USER_ALL command will store the changed parameters to the User NVM.

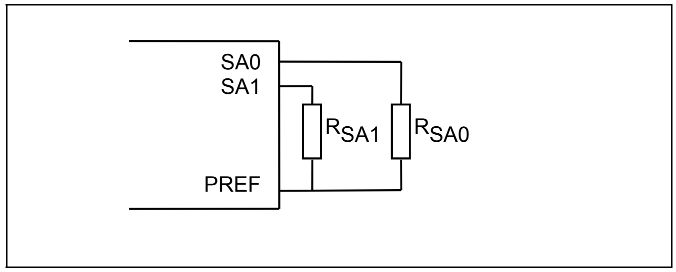


Software tools for design and production

Ericsson provides software tools for configuration and monitoring of this product via the PMBus interface.
For more information please contact your local Ericsson sales representative.

PMBus addressing

The PMBus address should be configured with resistors connected between the SA0/SA1 pins and the PREF pin, as shown in the figure below. Recommended resistor values for hard-wiring PMBus addresses are shown in the table. 1% tolerance resistors are required.



Schematic of connection of address resistor.

Index	R_{SA} [kΩ]	Index	R_{SA} [kΩ]
0	10	13	34.8
1	11	14	38.3
2	12.1	15	42.2
3	13.3	16	46.4
4	14.7	17	51.1
5	16.2	18	56.2
6	17.8	19	61.9
7	19.6	20	68.1
8	21.5	21	75
9	23.7	22	82.5
10	26.1	23	90.9
11	28.7	24	100
12	31.6		

The PMBus address follows the equation below:

Eq. 7 PMBus Address (decimal) = 25 x (SA1 index) + (SA0 index)

The user can theoretically configure up to 625 unique PMBus addresses, however the PMBus address range is inherently limited to 128. Therefore, the user should use index values 0 - 4 on the SA1 pin and the full range of index values on the SA0 pin, which will provide 125 device address combinations.

Products with no SA1 pin have an internally defined SA1 index as follows.

Product	SA1 index
BMR 463 (non SIP)	3

Optional PMBus Addressing

Alternatively the PMBus address can be defined by connecting the SA0/SA1 pins according to the table below. SA1 = open for products with no SA1 pin.

		SA0		
		low	open	high
SA1	low	20h	21h	22h
	open	23h	24h	25h
	high	26h	27h	Reserved

Low = Shorted to PREF
Open = High impedance
High = Logic high, GND as reference,
Logic High definitions see Electrical Specification

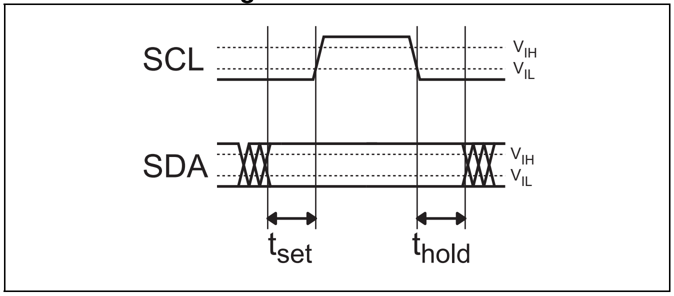
Reserved Addresses

Address 4Bh is allocated for production needs and cannot be used.

Addresses listed in the table below are reserved or assigned according to the SMBus specification and may not be usable. Refer to the SMBus specification for further information.

Address (decimal)	Comment
0	General Call Address / START byte
1	CBUS address
2	Address reserved for different bus format
3-7	Reserved for future use
8	SMBus Host
9-11	Assigned for Smart Battery
12	SMBus Alert Response Address
40	Reserved for ACCESS.bus host
44-45	Reserved by previous versions of the SMBus specification
55	Reserved for ACCESS.bus default address
64-68	Reserved by previous versions of the SMBus specification
72-75	Unrestricted addresses
97	SMBus Device Default Address
120-123	10-bit slave addressing
124-127	Reserved for future use

I²C/SMBus – Timing



Setup and hold times timing diagram

The setup time, t_{set}, is the time data, SDA, must be stable before the rising edge of the clock signal, SCL. The hold time t_{hold}, is the time data, SDA, must be stable after the rising edge of the clock signal, SCL. If these times are violated incorrect data may be captured or meta-stability may occur and the bus communication may fail. When configuring the product, all standard SMBus protocols must be followed, including clock stretching. Refer to the SMBus specification, for SMBus electrical and timing requirements.
This product does not support the BUSY flag in the status commands to indicate product being too busy for SMBus response. Instead a bus-free time delay according to this specification must occur between every SMBus transmission (between every stop & start condition). In case of storing the RAM content into the internal non-volatile memory (commands STORE_USER_ALL and STORE_DEFAULT_ALL) an additional delay of 100 ms has to be inserted. A 100 ms delay should be inserted after a restore from internal non-volatile memory (commands RESTORE_DEFAULT_ALL and RESTORE_USER_ALL).

PMBus Commands

The products are PMBus compliant. The following table lists the implemented PMBus read commands. For more detailed information see PMBus Power System Management Protocol Specification; Part I – General Requirements, Transport and Electrical Interface and PMBus Power System Management Protocol; Part II – Command Language.

Designation	Cmd	Impl
Standard PMBus Commands		
Control Commands		
PAGE	00h	No
OPERATION	01h	Yes
ON_OFF_CONFIG	02h	Yes
WRITE_PROTECT	10h	No
Output Commands		
VOUT_MODE (Read Only)	20h	Yes
VOUT_COMMAND	21h	Yes
VOUT_TRIM	22h	Yes
VOUT_CAL_OFFSET	23h	Yes
VOUT_MAX	24h	Yes
VOUT_MARGIN_HIGH	25h	Yes
VOUT_MARGIN_LOW	26h	Yes
VOUT_TRANSITION_RATE	27h	Yes
VOUT_DROOP	28h	Yes
MAX_DUTY	32h	Yes
FREQUENCY_SWITCH	33h	Yes
VIN_ON	35h	No
VIN_OFF	36h	No
IOUT_CAL_GAIN	38h	Yes
IOUT_CAL_OFFSET	39h	Yes
VOUT_SCALE_LOOP	29h	No
VOUT_SCALE_MONITOR	2Ah	No
COEFFICIENTS	30h	No
Fault Limit Commands		
POWER_GOOD_ON	5Eh	Yes
POWER_GOOD_OFF	5Fh	No
VOUT_OV_FAULT_LIMIT	40h	Yes
VOUT_OV_WARN_LIMIT	42h	No
VOUT_UV_WARN_LIMIT	43h	No
VOUT_UV_FAULT_LIMIT	44h	Yes
IOUT_OC_FAULT_LIMIT	46h	Yes
IOUT_OC_WARN_LIMIT	4Ah	No
IOUT_UC_FAULT_LIMIT	4Bh	Yes

Designation	Cmd	Impl
OT_FAULT_LIMIT	4Fh	Yes
OT_WARN_LIMIT	51h	Yes
UT_WARN_LIMIT	52h	Yes
UT_FAULT_LIMIT	53h	Yes
VIN_OV_FAULT_LIMIT	55h	Yes
VIN_OV_WARN_LIMIT	57h	Yes
VIN_UV_WARN_LIMIT	58h	Yes
VIN_UV_FAULT_LIMIT	59h	Yes
Fault Response Commands		
VOUT_OV_FAULT_RESPONSE	41h	Yes
VOUT_UV_FAULT_RESPONSE	45h	Yes
OT_FAULT_RESPONSE	50h	Yes
UT_FAULT_RESPONSE	54h	Yes
VIN_OV_FAULT_RESPONSE	56h	Yes
VIN_UV_FAULT_RESPONSE	5Ah	Yes
IOUT_OC_FAULT_RESPONSE	47h	No
IOUT_UC_FAULT_RESPONSE	4Ch	No
Time setting Commands		
TON_DELAY	60h	Yes
TON_RISE	61h	Yes
TOFF_DELAY	64h	Yes
TOFF_FALL	65h	Yes
TON_MAX_FAULT_LIMIT	62h	No
Status Commands (Read Only)		
CLEAR_FAULTS	03h	Yes
STATUS_BYTE	78h	Yes
STATUS_WORD	79h	Yes
STATUS_VOUT	7Ah	Yes
STATUS_IOUT	7Bh	Yes
STATUS_INPUT	7Ch	Yes
STATUS_TEMPERATURE	7Dh	Yes
STATUS_CML	7Eh	Yes
STATUS_MFR_SPECIFIC	80h	Yes
Monitor Commands (Read Only		
READ_VIN	88h	Yes
READ_VOUT	8Bh	Yes
READ_IOUT	8Ch	Yes
READ_TEMPERATURE_1	8Dh	Yes
READ_TEMPERATURE_2	8Eh	No
READ_FAN_SPEED_1	90h	No
READ_DUTY_CYCLE	94h	Yes
READ_FREQUENCY	95h	Yes

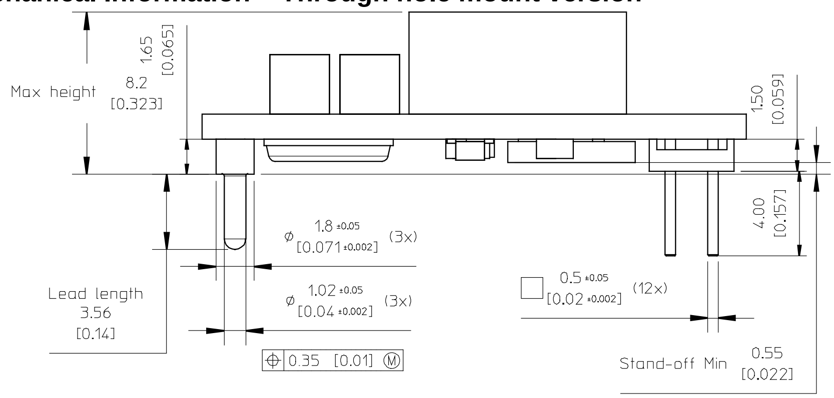
Designation	Cmd	Impl
Group Commands		
INTERLEAVE	37h	Yes
PHASE_CONTROL	F0h	Yes
Identification Commands		
PMBUS_REVISION	98h	Yes
MFR_ID	99h	Yes
MFR_MODEL	9Ah	Yes
MFR_REVISION	9Bh	Yes
MFR_LOCATION	9Ch	Yes
MFR_DATE	9Dh	Yes
MFR_SERIAL	9Eh	Yes
Supervisory Commands		
STORE_DEFAULT_ALL	11h	Yes
RESTORE_DEFAULT_ALL	12h	Yes
STORE_USER_ALL	15h	Yes
RESTORE_USER_ALL	16h	Yes
Product Specific Commands		
Output Commands		
XTEMP_SCALE	D9h	No
XTEMP_OFFSET	DAh	No
Time Setting Commands		
POWER_GOOD_DELAY	D4h	Yes
Fault limit Commands		
IOUT_AVG_OC_FAULT_LIMIT	E7h	Yes
IOUT_AVG_UC_FAULT_LIMIT	E8h	Yes
Fault Response Commands		
MFR_IOUT_OC_FAULT_RESPONSE	E5h	Yes
MFR_IOUT_UC_FAULT_RESPONSE	E6h	Yes
OVUV_CONFIG	D8h	Yes
Configuration and Control Commands		
MFR_CONFIG	D0h	Yes
USER_CONFIG	D1h	Yes
MISC_CONFIG	E9h	Yes
TRACK_CONFIG	E1h	Yes
PID_TAPS	D5h	Yes
PID_TAPS_CALC*	F2h	Yes
INDUCTOR	D6h	Yes
NLR_CONFIG	D7h	Yes
TEMPCO_CONFIG	DCh	Yes
IOUT_OMEGA_OFFSET*	BEh	Yes
AUTO_COMP_CONTROL**	BDh	Yes
AUTO_COMP_CONFIG**	BCh	Yes
DEADTIME	DDh	Yes
DEADTIME_CONFIG	DEh	Yes
DEADTIME_MAX	BFh	Yes
SNAPSHOT	EAh	Yes

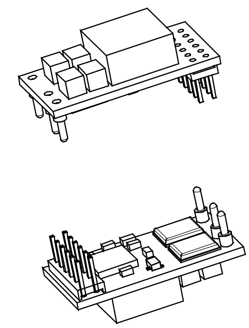
Designation	Cmd	Impl
SNAPSHOT_CONTROL	F3h	Yes
DEVICE_ID	E4h	Yes
USER_DATA_00	B0h	Yes
Group Commands		
SEQUENCE	E0h	Yes
GCB_CONFIG	D3h	Yes
GCB_GROUP	E2h	Yes
ISHARE_CONFIG	D2h	Yes
PHASE_CONTROL	F0h	Yes
Supervisory Commands		
PRIVATE_PASSWORD	FBh	Yes
PUBLIC_PASSWORD	FCh	Yes
UNPROTECT	FDh	Yes
SECURITY_LEVEL	FAh	Yes

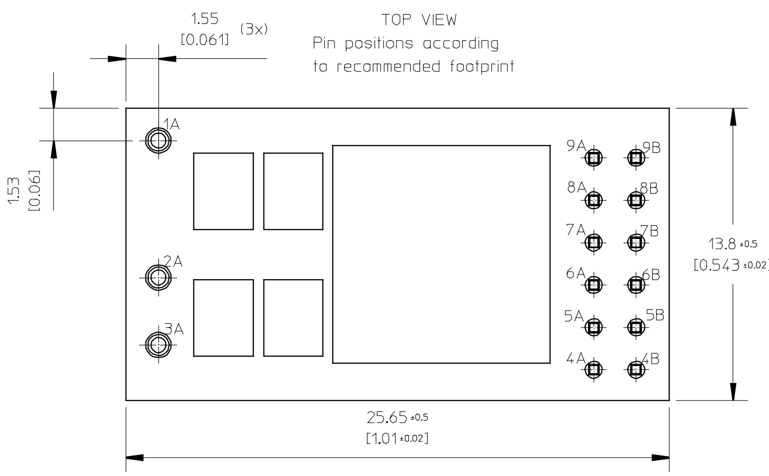
Notes:
Cmd is short for Command.
Impl is short for Implemented.

* These commands are available in products without DLC.
** These commands are available in products with DLC.

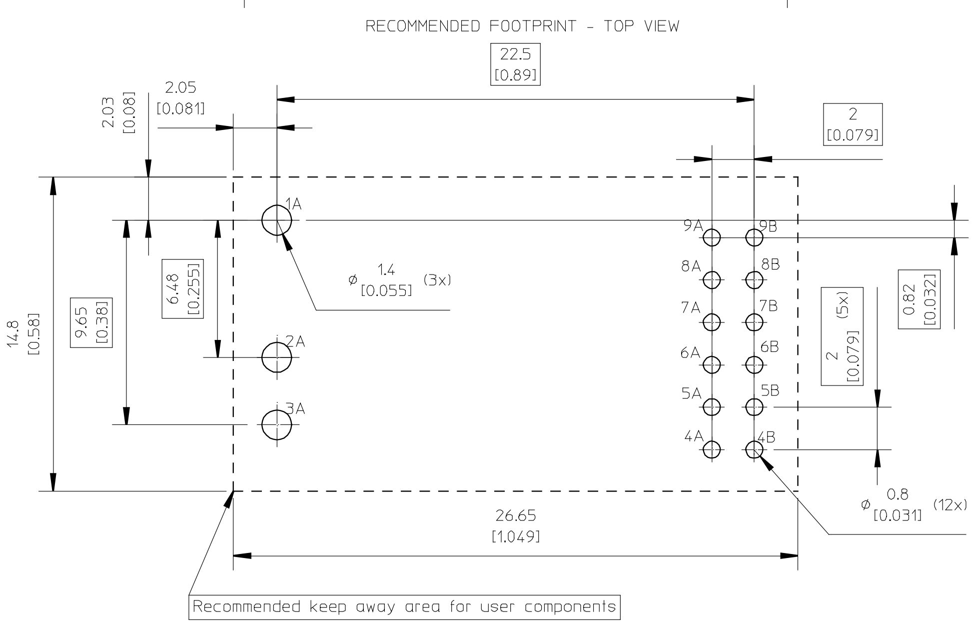
Mechanical Information – Through hole mount version



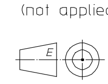




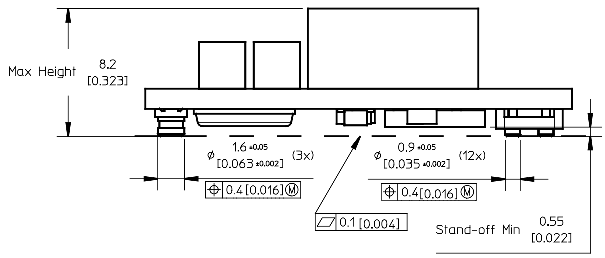
PIN SPECIFICATIONS
Pin 1A-3A Material: Copper alloy
Plating: Min Matte tin 8-13 µm over 2.5-5 µm Ni.
Pin 4A-9B Material: Brass
Plating: Min Au 0.2 µm over 1.27 µm Ni.

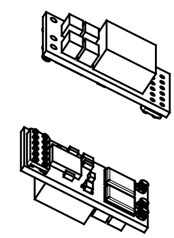


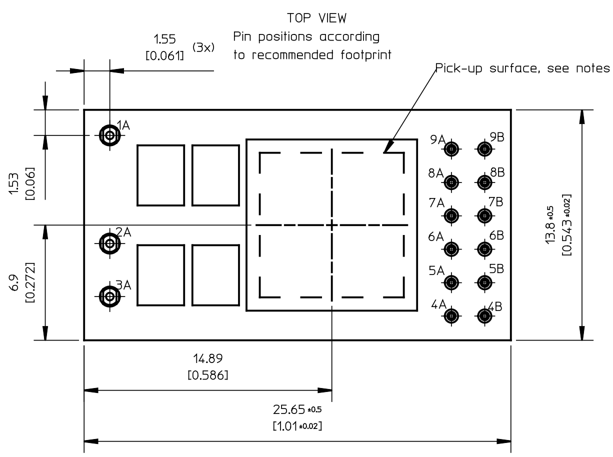
Weight: Typical 6.2 g
All dimensions in mm [inch].
Tolerances unless specified:
x.x ±0.50 mm [0.02],
x.xx ±0.25 mm [0.01]
(not applied on footprint or typical values)



Mechanical Information – Surface Mount Version





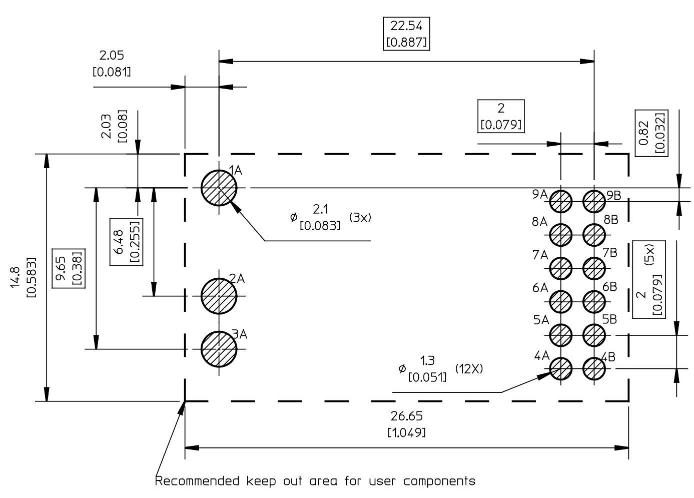


NOTES

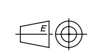
PIN SPECIFICATIONS
Pin 1A-3A Material: Copper alloy
Plating: Au 0.1 μm over 1-3 μm Ni.
Pin 4A-9B Material: Brass
Plating: Au 0.1 μm over 2 μm Ni.

PICK-UP SURFACE
Recommended pick-up nozzle size for assigned pick-up area is maximum Ø8 [0.315].

RECOMMENDED FOOTPRINT - TOP VIEW



Weight: Typical 5.8 g
All dimensions in mm [inch].
Tolerances unless specified:
x.x ±0.50 [0.02]
x.xx±0.25 [0.01]
(not applied on footprint or typical values)



All component placements – whether shown as physical components or symbolical outline – are for reference only and are subject to change throughout the product's life cycle, unless explicitly described and dimensioned in this drawing.

Mechanical Information – SIP

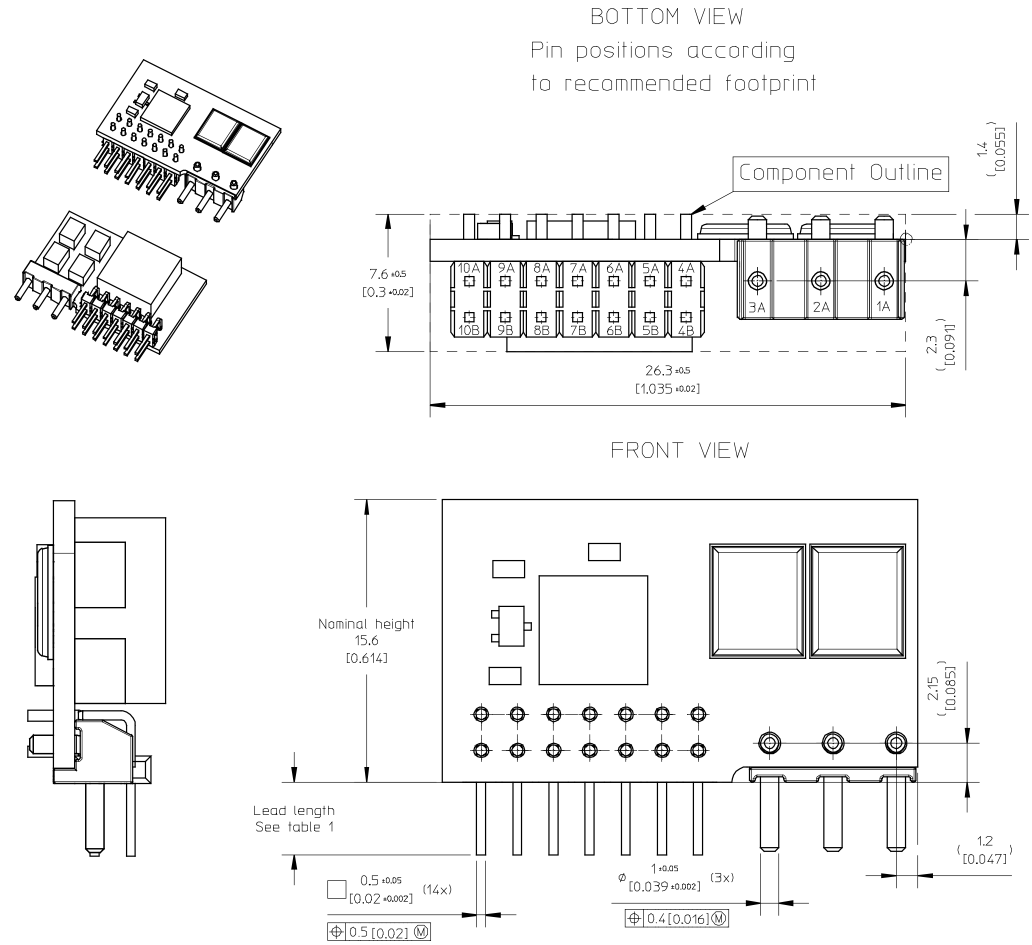
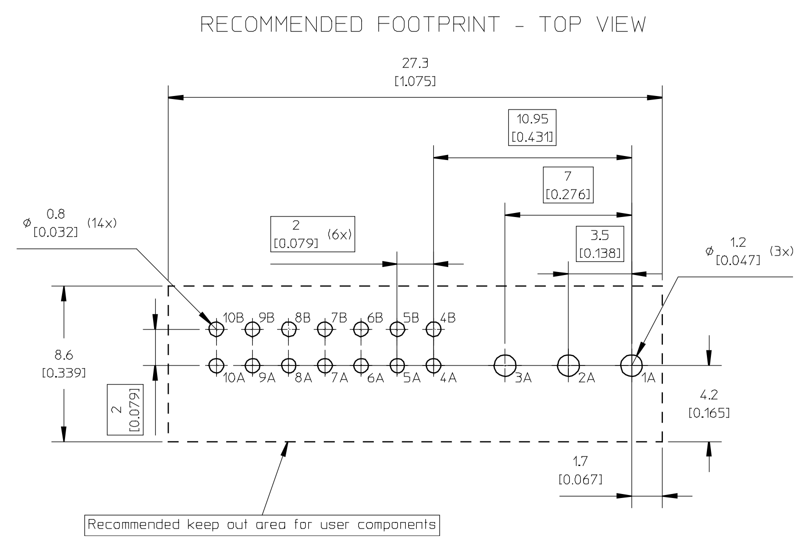


Table 1

Pin option	Lead Length
Standard	4±0.25 [0.157±0.01]
Long option	5.5±0.25[0.217±0.01]



PIN SPECIFICATIONS
Pin 1A-3A Material: Copper alloy (C11000)
Plating: Min Au 0.1 µm Au over 1-3 µm Ni.
Pin 4A-10B Material: Copper alloy
Plating: Min Au 0.1 µm over 1 µm Ni.

Weight: Typical 6.5 g
All dimensions in mm [inch].
Tolerances unless specified:
x.x ±0.50 mm [0.02]
x.xx±0.25 mm [0.01]
(not applied on footprint or typical values)

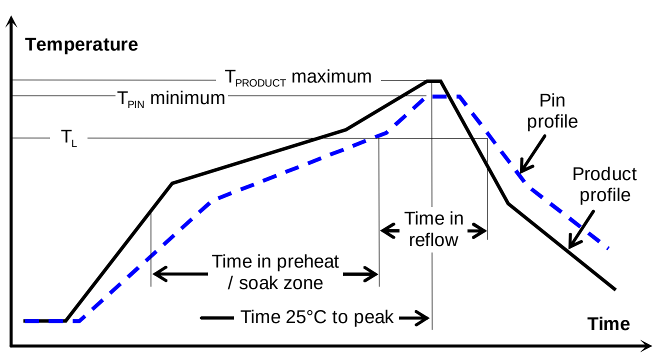
Soldering Information - Surface Mounting and Hole Mount through Pin in Paste Assembly

The product is intended for forced convection or vapor phase reflow soldering in SnPb or Pb-free processes.

The reflow profile should be optimised to avoid excessive heating of the product. It is recommended to have a sufficiently extended preheat time to ensure an even temperature across the host PWB and it is also recommended to minimize the time in reflow.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board, since cleaning residues may affect long time reliability and isolation voltage.

General reflow process specifications		SnPb eutectic	Pb-free
Average ramp-up ($T_{PRODUCT}$)		3°C/s max	3°C/s max
Typical solder melting (liquidus) temperature	T_L	183°C	221°C
Minimum reflow time above T_L		60 s	60 s
Minimum pin temperature	T_{PIN}	210°C	235°C
Peak product temperature	$T_{PRODUCT}$	225°C	260°C
Average ramp-down ($T_{PRODUCT}$)		6°C/s max	6°C/s max
Maximum time 25°C to peak		6 minutes	8 minutes



Minimum Pin Temperature Recommendations

Pin number 2A chosen as reference location for the minimum pin temperature recommendation since this will likely be the coolest solder joint during the reflow process.

SnPb solder processes

For SnPb solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature, (T_L, 183°C for Sn63Pb37) for more than 60 seconds and a peak temperature of 220°C is recommended to ensure a reliable solder joint.

For dry packed products only: depending on the type of solder paste and flux system used on the host board, up to a recommended maximum temperature of 245°C could be used, if the products are kept in a controlled environment (dry pack handling and storage) prior to assembly.

Lead-free (Pb-free) solder processes

For Pb-free solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature (T_L, 217 to 221°C for SnAgCu solder alloys) for more than 60 seconds and a peak temperature of 245°C on all solder joints is recommended to ensure a reliable solder joint.

Maximum Product Temperature Requirements

Top of the product PWB near pin 4B is chosen as reference location for the maximum (peak) allowed product temperature ($T_{PRODUCT}$) since this will likely be the warmest part of the product during the reflow process.

SnPb solder processes

For SnPb solder processes, the product is qualified for MSL 1 according to IPC/JEDEC standard J-STD-020C.

During reflow $T_{PRODUCT}$ must not exceed 225 °C at any time.

Pb-free solder processes

For Pb-free solder processes, the product is qualified for MSL 3 according to IPC/JEDEC standard J-STD-020C.

During reflow $T_{PRODUCT}$ must not exceed 260 °C at any time.

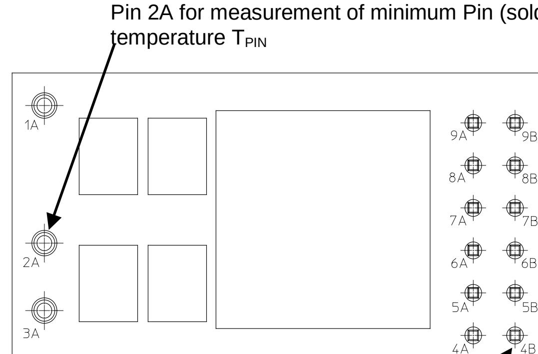
Dry Pack Information

Products intended for Pb-free reflow soldering processes are delivered in standard moisture barrier bags according to IPC/JEDEC standard J-STD-033 (Handling, packing, shipping and use of moisture/reflow sensitivity surface mount devices).

Using products in high temperature Pb-free soldering processes requires dry pack storage and handling. In case the products have been stored in an uncontrolled environment and no longer can be considered dry, the modules must be baked according to J-STD-033.

Thermocoupler Attachment

Pin 2A for measurement of minimum Pin (solder joint) temperature T_{PIN}



Pin 4B for measurement of maximum Product temperature $T_{PRODUCT}$

Soldering Information - Hole Mounting

The hole mounted product is intended for plated through hole mounting by wave or manual soldering. The pin temperature is specified to maximum to 270°C for maximum 10 seconds.

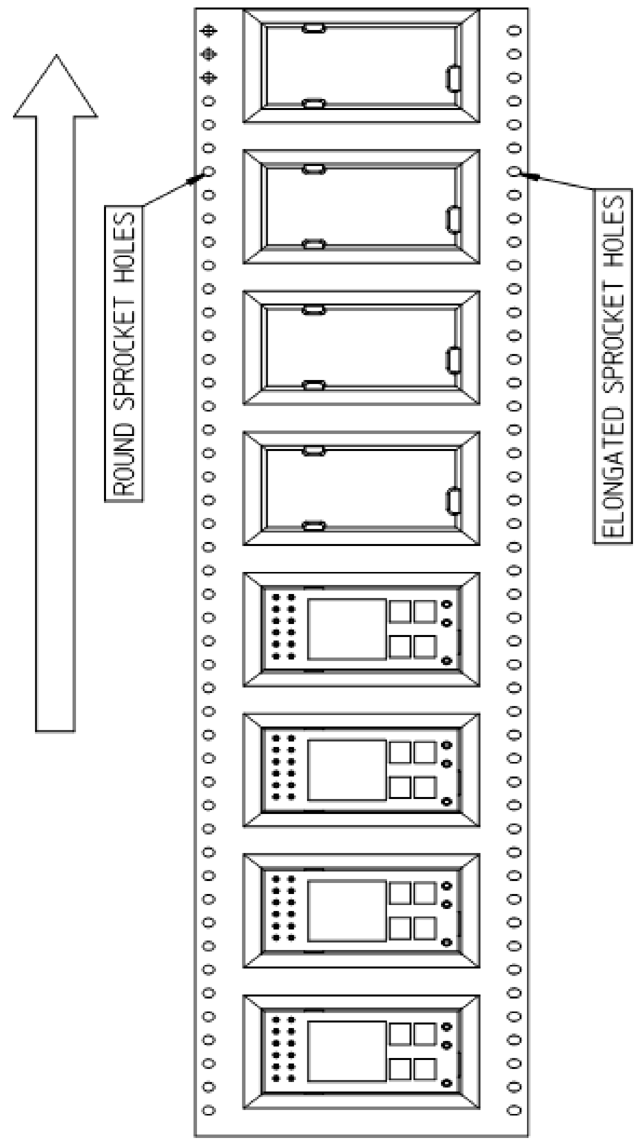
A maximum preheat rate of 4°C/s and maximum preheat temperature of 150°C is suggested. When soldering by hand, care should be taken to avoid direct contact between the hot soldering iron tip and the pins for more than a few seconds in order to prevent overheating.

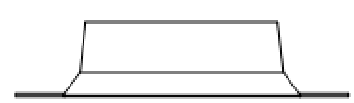
A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board. The cleaning residues may affect long time reliability and isolation voltage.

Delivery Package Information

The products are delivered in antistatic carrier tape (EIA 481 standard).

Carrier Tape Specifications	
Material	Antistatic PS
Surface resistance	$<10^7$ Ohm/square
Bakeability	The tape is not bakable
Tape width, W	44 mm [1.73 inch]
Pocket pitch, P_1	24 mm [0.95 inch]
Pocket depth, K_0	12.4 mm [0.488 inch]
Reel diameter	381 mm [15 inch]
Reel capacity	200 products /reel
Reel weight	1.7 kg/full reel





Soldering Information - Hole Mounting (SIP version)

The product is intended for plated through hole mounting by wave or manual soldering. The pin temperature is specified to maximum to 270°C for maximum 10 seconds.

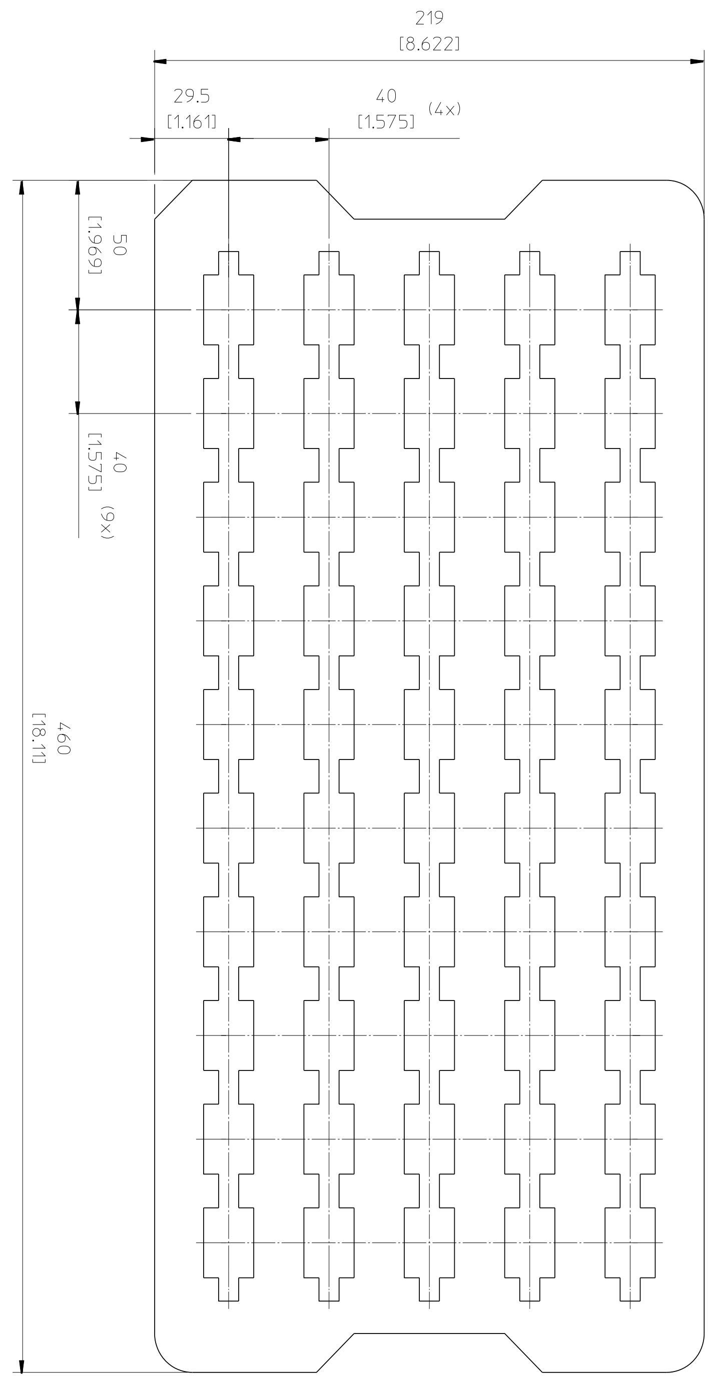
A maximum preheat rate of 4°C/s and maximum preheat temperature of 150°C is suggested. When soldering by hand, care should be taken to avoid direct contact between the hot soldering iron tip and the pins for more than a few seconds in order to prevent overheating.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board. The cleaning residues may affect long time reliability and isolation voltage.

Delivery Package Information (SIP version)

The products are delivered in antistatic trays

Tray Specifications	
Material	Antistatic Polyethylene foam
Surface resistance	10^5< Ohms/square <10^{11}
Bakability	The trays are not bakeable
Tray thickness	15 mm [0.709 inch]
Box capacity	100 products, 2 full trays/box)
Tray weight	35 g empty tray, 357 g full tray



Product Qualification Specification

Characteristics			
External visual inspection	IPC-A-610		
Change of temperature (Temperature cycling)	IEC 60068-2-14 Na	Temperature range Number of cycles Dwell/transfer time	-40 to 100°C 1000 15 min/0-1 min
Cold (in operation)	IEC 60068-2-1 Ad	Temperature T_A Duration	-45°C 72 h
Damp heat	IEC 60068-2-67 Cy	Temperature Humidity Duration	85°C 85 % RH 1000 hours
Dry heat	IEC 60068-2-2 Bd	Temperature Duration	125°C 1000 h
Electrostatic discharge susceptibility	IEC 61340-3-1, JESD 22-A114 IEC 61340-3-2, JESD 22-A115	Human body model (HBM) Machine Model (MM)	Class 2, 2000 V Class 3, 200 V
Immersion in cleaning solvents	IEC 60068-2-45 XA, method 2	Water Glycol ether	55°C 35°C
Mechanical shock	IEC 60068-2-27 Ea	Peak acceleration Duration	100 g 6 ms
Moisture reflow sensitivity [1]	J-STD-020C	Level 1 (SnPb-eutectic) Level 3 (Pb Free)	225°C 260°C
Operational life test	MIL-STD-202G, method 108A	Duration	1000 h
Resistance to soldering heat [2]	IEC 60068-2-20 Tb, method 1A	Solder temperature Duration	270°C 10-13 s
Robustness of terminations	IEC 60068-2-21 Test Ua1 IEC 60068-2-21 Test Ue1	Through hole mount products Surface mount products	All leads All leads
Solderability	IEC 60068-2-58 test Td [1] IEC 60068-2-20 test Ta [2]	Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free	150°C dry bake 16 h 215°C 235°C Steam ageing 235°C 245°C
Vibration, broad band random	IEC 60068-2-64 Fh, method 1	Frequency Spectral density Duration	10 to 500 Hz 0.07 g^2/Hz 10 min in each direction

Notes
[1] Only for products intended for reflow soldering (surface mount products)
[2] Only for products intended for wave soldering (plated through hole products)