# KSZ9031MNX

## Gigabit Ethernet Transceiver with GMII/MII Support

### Target Applications

- Laser/Network Printer
- Network Attached Storage (NAS)
- Network Server
- Broadband Gateway
- Gigabit SOHO/SMB Router
- IPTV
- IP Set-Top Box
- Game Console
- IP Camera
- Triple-Play (Data, Voice, Video) Media Center
- Media Converter

### Features

- Single-Chip 10/100/1000 Mbps Ethernet Transceiver Suitable for IEEE 802.3 Applications
- GMII/MII Standard Interface with 3.3V/2.5V/1.8V Tolerant I/Os
- Auto-Negotiation to Automatically Select the Highest Link-Up Speed (10/100/1000 Mbps) and Duplex (Half/Full)
- On-Chip Termination Resistors for the Differential Pairs
- On-Chip LDO Controller to Support Single 3.3V Supply Operation
- Jumbo Frame Support Up to 16 KB
- 125 MHz Reference Clock Output
- Energy-Detect Power-Down Mode for Reduced Power Consumption When the Cable is Not Attached
- Wake-On-LAN (WOL) Support with Robust Custom-Packet Detection
- Programmable LED Outputs for Link, Activity, and Speed
- Baseline Wander Correction
- LinkMD TDR-based Cable Diagnostic to Identify Faulty Copper Cabling
- Parametric NAND Tree Support to Detect Faults Between Chip I/Os and Board
- Loopback Modes for Diagnostics
- Automatic MDI/MDI-X Crossover to Detect and Correct Pair Swap at All Speeds of Operation
- Automatic Detection and Correction of Pair Swaps, Pair Skew, and Pair Polarity
- MDC/MDIO Management Interface for PHY Register Configuration
- Interrupt Pin Option
- Power-Down and Power-Saving Modes
- Operating Voltages
  - Core (DVDDL, AVDDL, AVDDL_PLL): 1.2V (External FET or Regulator)
  - VDD I/O (DVDDH): 3.3V, 2.5V, or 1.8V
  - Transceiver (AVDDH): 3.3V or 2.5V (Commercial Temp.)
- 64-pin QFN (8 mm × 8 mm) Package

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# 1.0 INTRODUCTION

## 1.1 General Description

The KSZ9031MNX is a completely integrated triple-speed (10BASE-T/100BASE-TX/1000BASE-T) Ethernet physical-layer transceiver for transmission and reception of data on standard CAT-5 unshielded twisted pair (UTP) cable.

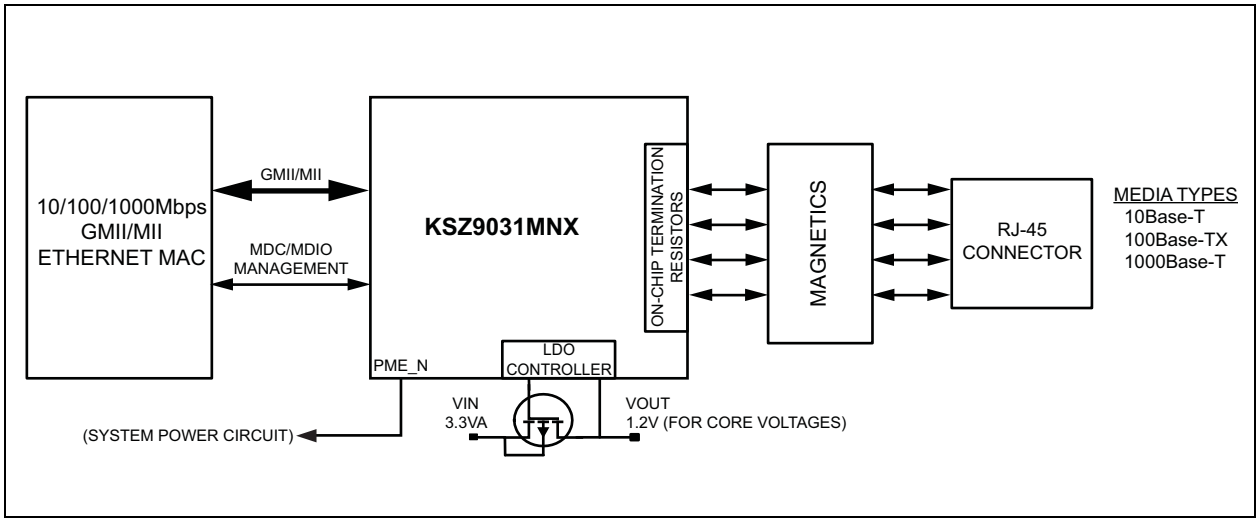
The KSZ9031MNX offers the industry-standard GMII/MII (Gigabit Media Independent Interface/Media Independent Interface) for connection to GMII/MII MACs in Gigabit Ethernet processors and switches for data transfer at 1000 Mbps or 10/100 Mbps.

The KSZ9031MNX reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating an LDO controller to drive a low-cost MOSFET to supply the 1.2V core.

The KSZ9031MNX offers diagnostic features to facilitate system bring-up and debugging in production testing and in product deployment. Parametric NAND tree support enables fault detection between KSZ9031MNX I/Os and the board. The LinkMD® TDR-based cable diagnostic identifies faulty copper cabling. Remote and local loopback functions verify analog and digital data paths.

The KSZ9031MNX is available in a 64-pin, lead-free QFN package.

**FIGURE 1-1: SYSTEM BLOCK DIAGRAM**



## 2.0 PIN DESCRIPTION AND CONFIGURATION

**FIGURE 2-1: 64-QFN PIN ASSIGNMENT (TOP VIEW)**

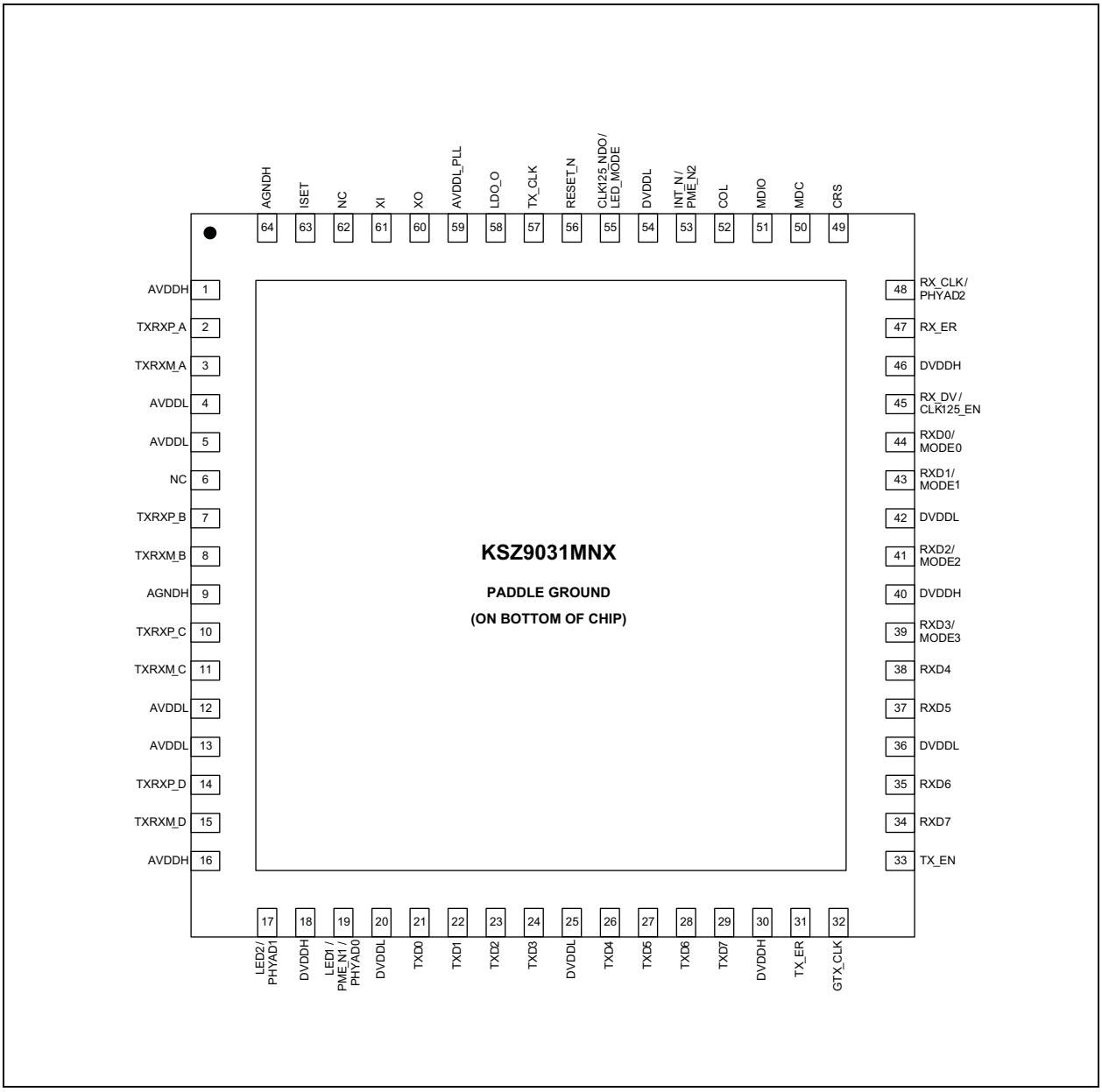


**TABLE 2-1: SIGNALS - KSZ9031MNX**

| Pin Number | Pin Name | Type Note 2-1 | Description |
|---|---|---|---|
| 1 | AVDDH | P | 3.3V/2.5V (commercial temperature only) analog $V_{DD}$ |
| 2 | TXRXP_A | I/O | Media Dependent Interface[0], positive signal of differential pair<br>1000BASE-T mode: TXRXP_A corresponds to BI_DA+ for MDI configuration and BI_DB+ for MDI-X configuration, respectively.<br>10BASE-T/100BASE-TX mode: TXRXP_A is the positive transmit signal (TX+) for MDI configuration and the positive receive signal (RX+) for MDI-X configuration, respectively. |
| 3 | TXRXM_A | I/O | Media Dependent Interface[0], negative signal of differential pair<br>1000BASE-T mode: TXRXM_A corresponds to BI_DA– for MDI configuration and BI_DB– for MDI-X configuration, respectively.<br>10BASE-T/100BASE-TX mode: TXRXM_A is the negative transmit signal (TX–) for MDI configuration and the negative receive signal (RX–) for MDI-X configuration, respectively. |
| 4 | AVDDL | P | 1.2V analog $V_{DD}$ |
| 5 | AVDDL | P | 1.2V analog $V_{DD}$ |
| 6 | NC | — | No connect |
| 7 | TXRXP_B | I/O | Media Dependent Interface[1], positive signal of differential pair<br>1000BASE-T mode: TXRXP_B corresponds to BI_DB+ for MDI configuration and BI_DA+ for MDI-X configuration, respectively.<br>10BASE-T/100BASE-TX mode: TXRXP_B is the positive receive signal (RX+) for MDI configuration and the positive transmit signal (TX+) for MDI-X configuration, respectively. |
| 8 | TXRXM_B | I/O | Media Dependent Interface[1], negative signal of differential pair<br>1000BASE-T mode: TXRXM_B corresponds to BI_DB– for MDI configuration and BI_DA– for MDI-X configuration, respectively.<br>10BASE-T/100BASE-TX mode: TXRXM_B is the negative receive signal (RX–) for MDI configuration and the negative transmit signal (TX–) for MDI-X configuration, respectively. |
| 9 | AGNDH | GND | Analog ground |
| 10 | TXRXP_C | I/O | Media Dependent Interface[2], positive signal of differential pair<br>1000BASE-T mode: TXRXP_C corresponds to BI_DC+ for MDI configuration and BI_DD+ for MDI-X configuration, respectively.<br>10BASE-T/100BASE-TX mode: TXRXP_C is not used. |
| 11 | TXRXM_C | I/O | Media Dependent Interface[2], negative signal of differential pair<br>1000BASE-T mode: TXRXM_C corresponds to BI_DC– for MDI configuration and BI_DD– for MDI-X configuration, respectively.<br>10BASE-T/100BASE-TX mode: TXRXM_C is not used. |
| 12 | AVDDL | P | 1.2V analog $V_{DD}$ |
| 13 | AVDDL | P | 1.2V analog $V_{DD}$ |

**TABLE 2-1: SIGNALS - KSZ9031MNX (CONTINUED)**

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-1</th><th>Description</th></tr>
<tr><td>14</td><td>TXRXP_D</td><td>I/O</td><td>Media Dependent Interface[3], positive signal of differential pair<br>1000BASE-T mode: TXRXP_D corresponds to BI_DD+ for MDI configuration and BI_DC+ for MDI-X configuration, respectively.<br>10BASE-T/100BASE-TX mode: TXRXP_D is not used.</td></tr>
<tr><td>15</td><td>TXRXM_D</td><td>I/O</td><td>Media Dependent Interface[3], negative signal of differential pair<br>1000BASE-T mode: TXRXM_D corresponds to BI_DD– for MDI configuration and BI_DC– for MDI-X configuration, respectively.<br>10BASE-T/100BASE-TX mode: TXRXM_D is not used.</td></tr>
<tr><td>16</td><td>AVDDH</td><td>P</td><td>3.3V/2.5V (commercial temperature only) analog $V_{DD}$</td></tr>
<tr><td>17</td><td>LED2/<br>PHYAD1</td><td>I/O</td><td>LED2 output: Programmable LED2 output<br>Config mode: The voltage on this pin is sampled and latched during the power-up/reset process to determine the value of PHYAD[1]. See the Strapping Options - KSZ9031MNX section for details.<br>The LED2 pin is programmed by the LED_MODE strapping option (Pin 55), and is defined as follows:<br>Single-LED Mode
<table>
<tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>Link Off</td><td>H</td><td>OFF</td></tr>
<tr><td>Link On (any speed)</td><td>L</td><td>ON</td></tr>
</table>
Tri-Color Dual-LED Mode
<table>
<tr><th rowspan="2">Link/Activity</th><th colspan="2">Pin State</th><th colspan="2">LED Definition</th></tr>
<tr><th>LED2</th><th>LED1</th><th>LED2</th><th>LED1</th></tr>
<tr><td>Link Off</td><td>H</td><td>H</td><td>OFF</td><td>OFF</td></tr>
<tr><td>1000 Link/No Activity</td><td>L</td><td>H</td><td>ON</td><td>OFF</td></tr>
<tr><td>1000 Link/Activity (RX, TX)</td><td>Toggle</td><td>H</td><td>Blinking</td><td>OFF</td></tr>
<tr><td>100 Link/No Activity</td><td>H</td><td>L</td><td>OFF</td><td>ON</td></tr>
<tr><td>100 Link/Activity (RX, TX)</td><td>H</td><td>Toggle</td><td>OFF</td><td>Blinking</td></tr>
<tr><td>10 Link/No Activity</td><td>L</td><td>L</td><td>ON</td><td>ON</td></tr>
<tr><td>10 Link/Activity (RX, TX)</td><td>Toggle</td><td>Toggle</td><td>Blinking</td><td>Blinking</td></tr>
</table>
For tri-color dual-LED mode, LED2 works in conjunction with LED1 (Pin 19) to indicate 10 Mbps link and activity.</td></tr>
<tr><td>18</td><td>DVDDH</td><td>P</td><td>3.3V, 2.5V, or 1.8V digital $V_{DD\_IO}$</td></tr>
</table>

**TABLE 2-1: SIGNALS - KSZ9031MNX (CONTINUED)**

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type Note 2-1</th><th>Description</th></tr>
<tr><td rowspan="20">19</td><td rowspan="20">LED1/<br>PHYAD0/<br>PME_N1</td><td rowspan="20">I/O</td><td>LED1 output: Programmable LED1 output<br>Config mode: The voltage on this pin is sampled and latched during the power-up/reset process to determine the value of PHYAD[0]. See the Strapping Options - KSZ9031MNX section for details.<br>PME_N output: Programmable PME_N output (pin option 1). This pin function requires an external pull-up resistor to DVDDH (digital $V_{DD\_I/O}$) in a range from 1.0 kΩ to 4.7 kΩ. When asserted low, this pin signals that a WOL event has occurred.<br>This pin is not an open-drain for all operating modes.<br>The LED1 pin is programmed by the LED_MODE strapping option (Pin 55), and is defined as follows:</td></tr>
<tr><td>Single-LED Mode</td></tr>
<tr><td><table>
<tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Activity</td><td>H</td><td>OFF</td></tr>
<tr><td>Activity (RX, TX)</td><td>Toggle</td><td>Blinking</td></tr>
</table></td></tr>
<tr><td>Tri-Color Dual-LED Mode</td></tr>
<tr><td><table>
<tr><th rowspan="2">Link/Activity</th><th colspan="2">Pin State</th><th colspan="2">LED Definition</th></tr>
<tr><th>LED2</th><th>LED1</th><th>LED2</th><th>LED1</th></tr>
<tr><td>Link Off</td><td>H</td><td>H</td><td>OFF</td><td>OFF</td></tr>
<tr><td>1000 Link/No Activity</td><td>L</td><td>H</td><td>ON</td><td>OFF</td></tr>
<tr><td>1000 Link/Activity (RX, TX)</td><td>Toggle</td><td>H</td><td>Blinking</td><td>OFF</td></tr>
<tr><td>100 Link/No Activity</td><td>H</td><td>L</td><td>OFF</td><td>ON</td></tr>
<tr><td>100 Link/Activity (RX, TX)</td><td>H</td><td>Toggle</td><td>OFF</td><td>Blinking</td></tr>
<tr><td>10 Link/No Activity</td><td>L</td><td>L</td><td>ON</td><td>ON</td></tr>
<tr><td>10 Link/Activity (RX, TX)</td><td>Toggle</td><td>Toggle</td><td>Blinking</td><td>Blinking</td></tr>
</table></td></tr>
<tr><td>For tri-color dual-LED mode, LED1 works in conjunction with LED2 (Pin 17) to indicate 10 Mbps link and activity.</td></tr>
<tr><td>20</td><td>DVDDL</td><td>P</td><td>1.2V digital $V_{DD}$</td></tr>
<tr><td>21</td><td>TXD0</td><td>I</td><td>GMII mode: GMII TXD0 (Transmit Data 0) input<br>MII mode: MII TXD0 (Transmit Data 0) input</td></tr>
<tr><td>22</td><td>TXD1</td><td>I</td><td>GMII mode: GMII TXD1 (Transmit Data 1) input<br>MII mode: MII TXD1 (Transmit Data 1) input</td></tr>
<tr><td>23</td><td>TXD2</td><td>I</td><td>GMII mode: GMII TXD2 (Transmit Data 2) input<br>MII mode: MII TXD2 (Transmit Data 2) Input</td></tr>
</table>

**TABLE 2-1: SIGNALS - KSZ9031MNX (CONTINUED)**

| Pin Number | Pin Name | Type Note 2-1 | Description |
|---|---|---|---|
| 24 | TXD3 | I | GMII mode: GMII TXD3 (Transmit Data 3) input<br>MII mode: MII TXD3 (Transmit Data 3) input |
| 25 | DVDDL | P | 1.2V digital $V_{DD}$ |
| 26 | TXD4 | I | GMII mode: GMII TXD4 (Transmit Data 4) input<br>MII mode: This pin is not used and can be driven high or low. |
| 27 | TXD5 | I | GMII mode: GMII TXD5 (Transmit Data 5) input<br>MII mode: This pin is not used and can be driven high or low. |
| 28 | TXD6 | I | GMII mode: GMII TXD6 (Transmit Data 6) input<br>MII Mode: This pin is not used and can be driven high or low. |
| 29 | TXD7 | I | GMII mode: GMII TXD7 (Transmit Data 7) input<br>MII mode: This pin is not used and can be driven high or low. |
| 30 | DVDDH | P | 3.3V, 2.5V, or 1.8V digital $V_{DD\_IO}$ |
| 31 | TX_ER | I | GMII mode: GMII TX_ER (Transmit Error) input<br>MII mode: MII TX_ER (Transmit Error) input<br>If the GMII/MII MAC does not provide the TX_ER output signal, this pin should be tied low. |
| 32 | GTX_CLK | I | GMII mode: GMII GTX_CLK (Transmit Reference Clock) input |
| 33 | TX_EN | I | GMII mode: GMII TX_EN (Transmit Enable) input<br>MII mode: MII TX_EN (Transmit Enable) input |
| 34 | RXD7 | O | GMII mode: GMII RXD7 (Receive Data 7) output<br>MII mode: This pin is not used and is driven low. |
| 35 | RXD6 | O | GMII mode: GMII RXD6 (Receive Data 6) output<br>MII mode: This pin is not used and is driven low. |
| 36 | DVDDL | P | 1.2V digital $V_{DD}$ |
| 37 | RXD5 | O | GMII mode: GMII RXD5 (Receive Data 5) output<br>MII mode: This pin is not used and is driven low. |
| 38 | RXD4 | O | GMII mode: GMII RXD4 (Receive Data 4) output<br>MII mode: This pin is not used and is driven low. |
| 39 | RXD3/<br>MODE3 | I/O | GMII mode: GMII RXD3 (Receive Data 3) output<br>MII mode: MII RXD3 (Receive Data 3) output<br>Config mode: The voltage on this pin is sampled and latched during the power-up/reset process to determine the value of MODE3. See the Strapping Options - KSZ9031MNX section for details. |
| 40 | DVDDH | P | 3.3V, 2.5V, or 1.8V digital $V_{DD\_IO}$ |
| 41 | RXD2/<br>MODE2 | I/O | GMII mode: GMII RXD2 (Receive Data 2) output<br>MII mode: MII RXD2 (Receive Data 2) output<br>Config mode: The voltage on this pin is sampled and latched during the power-up/reset process to determine the value of MODE2. See the Strapping Options - KSZ9031MNX section for details. |
| 42 | DVDDL | P | 1.2V digital $V_{DD}$ |

**TABLE 2-1: SIGNALS - KSZ9031MNX (CONTINUED)**

| Pin Number | Pin Name | Type Note 2-1 | Description |
|---|---|---|---|
| 43 | RXD1/ MODE1 | I/O | GMII mode: GMII RXD1 (Receive Data 1) output<br>MII mode: MII RXD1 (Receive Data 1) output<br>Config mode: The voltage on this pin is sampled and latched during the power-up/reset process to determine the value of MODE1. See the Strapping Options - KSZ9031MNX section for details. |
| 44 | RXD0/ MODE0 | I/O | GMII mode: GMII RXD0 (Receive Data 0) output<br>MII mode: MII RXD0 (Receive Data 0) output<br>Config mode: The voltage on this pin is sampled and latched during the power-up/reset process to determine the value of MODE0. See the Strapping Options - KSZ9031MNX section for details. |
| 45 | RX_DV/ CLK125_EN | I/O | GMII mode: GMII RX_DV (Receive Data Valid) output<br>MII mode: MII RX_DV (Receive Data Valid) output<br>Config mode: The voltage on this pin is sampled and latched during the power-up/reset process to determine the value of CLK125_EN. See the Strapping Options - KSZ9031MNX section for details. |
| 46 | DVDDH | P | 3.3V, 2.5V, or 1.8V digital $V_{DD\_IO}$ |
| 47 | RX_ER | O | GMII mode: GMII RX_ER (Receive Error) output<br>MII mode: MII RX_ER (Receive Error) output |
| 48 | RX_CLK/ PHYAD2 | I/O | GMII mode: GMII RX_CLK (Receive Reference Clock) output<br>MII mode: MII RX_CLK (Receive Reference Clock) output<br>Config mode: The voltage on this pin is sampled and latched during the power up/reset process to determine the value of PHYAD[2]. See the Strapping Options - KSZ9031MNX section for details. |
| 49 | CRS | O | GMII mode: GMII CRS (Carrier Sense) output<br>MII mode: MII CRS (Carrier Sense) output |
| 50 | MDC | Ipu | Management data clock input<br>This pin is the input reference clock for MDIO (Pin 51). |
| 51 | MDIO | Ipu/O | Management data input/output<br>This pin is synchronous to MDC (Pin 50) and requires an external pull-up resistor to DVDDH (digital $V_{DD\_IO}$) in a range from 1.0 kΩ to 4.7 kΩ. |
| 52 | COL | O | GMII mode: GMII COL (Collision Detected) output<br>MII mode: MII COL (Collision Detected) output |
| 53 | INT_N/ PME_N2 | O | Interrupt output: Programmable interrupt output, with Register 1Bh as the Interrupt Control/Status Register, for programming the interrupt conditions and reading the interrupt status. Register 1Fh, Bit [14] sets the interrupt output to active low (default) or active high.<br>PME_N output: Programmable PME_N output (pin option 2). When asserted low, this pin signals that a WOL event has occurred.<br>For Interrupt (when active low) and PME functions, this pin requires an external pull-up resistor to DVDDH (digital $V_{DD\_I/O}$) in a range from 1.0 kΩ to 4.7 kΩ.<br>This pin is not an open-drain for all operating modes. |
| 54 | DVDDL | P | 1.2V digital $V_{DD}$ |

**TABLE 2-1: SIGNALS - KSZ9031MNX (CONTINUED)**

| Pin Number | Pin Name | Type Note 2-1 | Description |
|---|---|---|---|
| 55 | CLK125_NDO/ LED_MODE | I/O | 125 MHz clock output<br>This pin provides a 125 MHz reference clock output option for use by the MAC.<br>Config mode: The voltage on this pin is sampled during the power-up/reset process to determine the value of LED_MODE. See the Strapping Options - KSZ9031MNX section for details. |
| 56 | RESET_N | Ipu | Chip reset (active low)<br>Hardware pin configurations are strapped-in (sampled and latched) at the de-assertion (rising edge) of RESET_N. See the Strapping Options - KSZ9031MNX section for details. |
| 57 | TX_CLK | O | MII mode: MII TX_CLK (Transmit Reference Clock) output |
| 58 | LDO_O | O | On-chip 1.2V LDO controller output<br>This pin drives the input gate of a P-channel MOSFET to generate 1.2V for the chip's core voltages. If the system provides 1.2V and this pin is not used, it can be left floating. |
| 59 | AVDDL_PLL | P | 1.2V analog $V_{DD}$ for PLL |
| 60 | XO | O | 25 MHz crystal feedback<br>This pin connects to one end of an external 25 MHz crystal.<br>This pin is a no connect if an oscillator or other external (non-crystal) clock source is used. |
| 61 | XI | I | Crystal/Oscillator/External Clock input<br>This pin connects to one end of an external 25 MHz crystal or to the output of an oscillator or other external (non-crystal) clock source.<br>25 MHz ±50 ppm tolerance |
| 62 | NC | — | No connect<br>This pin is not bonded and can be connected to AVDDH power for footprint compatibility with the KSZ9021GN Gigabit PHY. |
| 63 | ISET | I/O | Set the transmit output level.<br>Connect a 12.1 kΩ 1% resistor to ground on this pin. |
| 64 | AGNDH | GND | Analog ground. |
| Paddle | P_GND | GND | Exposed paddle on bottom of chip.<br>Connect P_GND to ground. |

**Note 2-1** P = power supply
GND = ground
I = input
O = output
I/O = bi-directional
Ipu = Input with internal pull-up (see Electrical Characteristics for value).
Ipu/O = Input with internal pull-up (see Electrical Characteristics for value) during power-up/reset; output pin otherwise.

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may be driven during the power-up or reset process, and consequently cause the PHY strap-in pins on the GMII/MII signals to be latched to the incorrect configuration. In this case, external pull-up or pull-down resistors should be added on the PHY strap-in pins to ensure the PHY is configured to the correct pin strap-in mode.

**TABLE 2-2: STRAPPING OPTIONS - KSZ9031MNX**

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type<br>Note 2-1</th><th>Description</th></tr>
<tr><td>48<br>17<br>19</td><td>PHYAD2<br>PHYAD1<br>PHYAD0</td><td>I/O<br>I/O<br>I/O</td><td>The PHY address, PHYAD[2:0], is sampled and latched at power-up/reset and is configurable to any value from 0 to 7. Each PHY address bit is configured as follows:<br>Pull-up = 1<br>Pull-down = 0<br>PHY Address Bits [4:3] are always set to ‘00’.</td></tr>
<tr><td rowspan="18">39<br>41<br>43<br>44</td><td rowspan="18">MODE3<br>MODE2<br>MODE1<br>MODE0</td><td rowspan="18">I/O<br>I/O<br>I/O<br>I/O</td><td>The MODE[3:0] strap-in pins are sampled and latched at power-up/reset and are defined as follows:</td></tr>
<tr><td>
<table>
<tr><th>MODE[3:0]</th><th>Mode</th></tr>
<tr><td>0000</td><td>Reserved - not used</td></tr>
<tr><td>0001</td><td>GMII/MII mode</td></tr>
<tr><td>0010</td><td>Reserved - not used</td></tr>
<tr><td>0011</td><td>Reserved - not used</td></tr>
<tr><td>0100</td><td>NAND tree mode</td></tr>
<tr><td>0101</td><td>Reserved - not used</td></tr>
<tr><td>0110</td><td>Reserved - not used</td></tr>
<tr><td>0111</td><td>Chip power-down mode</td></tr>
<tr><td>1000</td><td>Reserved - not used</td></tr>
<tr><td>1001</td><td>Reserved - not used</td></tr>
<tr><td>1010</td><td>Reserved - not used</td></tr>
<tr><td>1011</td><td>Reserved - not used</td></tr>
<tr><td>1100</td><td>Reserved - not used</td></tr>
<tr><td>1101</td><td>Reserved - not used</td></tr>
<tr><td>1110</td><td>Reserved - not used</td></tr>
<tr><td>1111</td><td>Reserved - not used</td></tr>
</table>
</td></tr>
<tr><td>45</td><td>CLK125_EN</td><td>I/O</td><td>CLK125_EN is sampled and latched at power-up/reset and is defined as follows:<br>Pull-up (1) = Enable 125 MHz clock output<br>Pull-down (0) = Disable 125 MHz clock output<br>Pin 55 (CLK125_NDO) provides the 125 MHz reference clock output option for use by the MAC.</td></tr>
<tr><td>55</td><td>LED_MODE</td><td>I/O</td><td>LED_MODE is sampled and latched at power-up/reset and is defined as follows:<br>Pull-up (1) = Single-LED mode<br>Pull-down (0) = Tri-color dual-LED mode</td></tr>
</table>

**Note 2-1** I/O = Bi-directional.

## 3.0 FUNCTIONAL DESCRIPTION

The KSZ9031MNX is a completely integrated triple-speed (10BASE-T/100BASE-TX/1000BASE-T) Ethernet physical layer transceiver solution for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable.

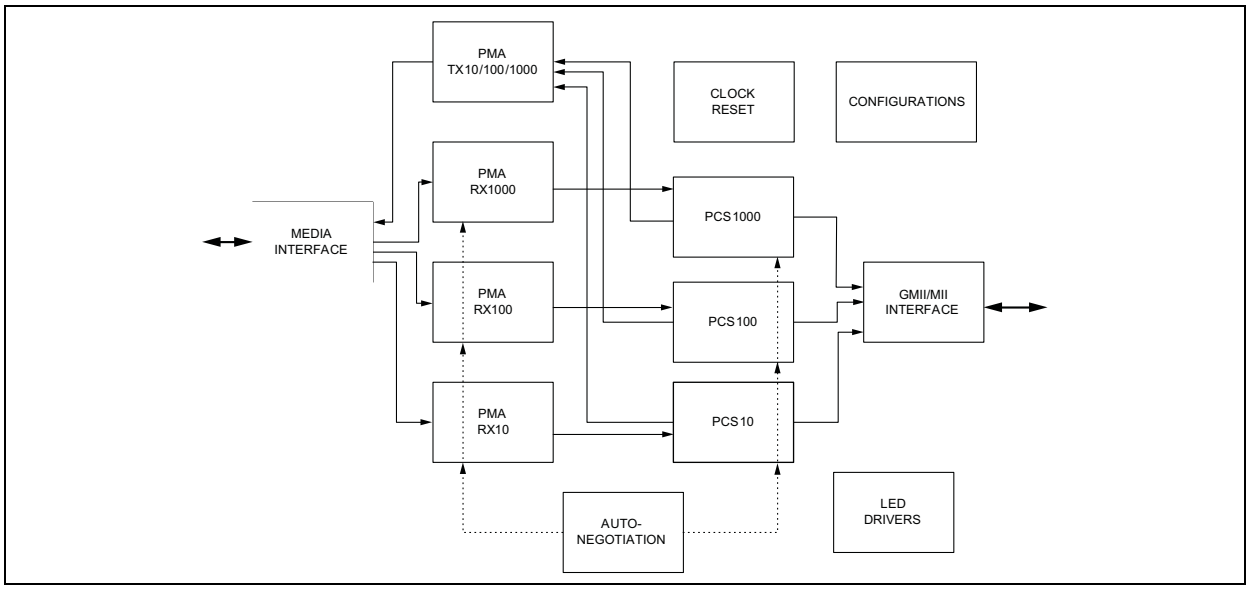
The KSZ9031MNX reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating an LDO controller to drive a low-cost MOSFET to supply the 1.2V core.

On the copper media interface, the KSZ9031MNX can automatically detect and correct for differential pair misplacements and polarity reversals, and correct propagation delays and re-sync timing between the four differential pairs, as specified in the IEEE 802.3 standard for 1000BASE-T operation.

The KSZ9031MNX provides the GMII/MII interface for connection to GMACs in Gigabit Ethernet processors and switches for data transfer at 10/100/1000Mbps.

Figure 3-1 shows a high-level block diagram of the KSZ9031MNX.

**FIGURE 3-1: KSZ9031MNX BLOCK DIAGRAM**




## 3.1 10BASE-T/100BASE-TX Transceiver

### 3.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT-3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT-3 current output. The output current is set by an external 12.1 kΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, and overshoot. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

### 3.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT-3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion are a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC-restoration and data-conversion block. The DC-restoration circuit compensates for the effect of baseline wander and improves the dynamic range. The differential data conversion circuit converts the MLT-3 format back to NRZI. The slicing threshold is also adaptive.

The clock-recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the GMII/MII format and provided as the input data to the MAC.

### 3.1.3 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled using an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, then the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

### 3.1.4 10BASE-T TRANSMIT

The 10BASE-T output drivers are incorporated into the 100BASE-TX drivers to allow for transmission with the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output signals with typical amplitude of 2.5V peak for standard 10BASE-T mode and 1.75V peak for energy-efficient 10BASE-Te mode. The 10BASE-T/10BASE-Te signals have harmonic contents that are at least 31 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

### 3.1.5 10BASE-T RECEIVE

On the receive side, input buffer and level-detecting squelch circuits are used. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 300 mV or with short pulse widths to prevent noises at the receive inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ9031MNX decodes a data frame. The receiver clock is maintained active during idle periods between receiving data frames.

The KSZ9031MNX removes all 7 bytes of the preamble and presents the received frame starting with the SFD (start of frame delimiter) to the MAC.

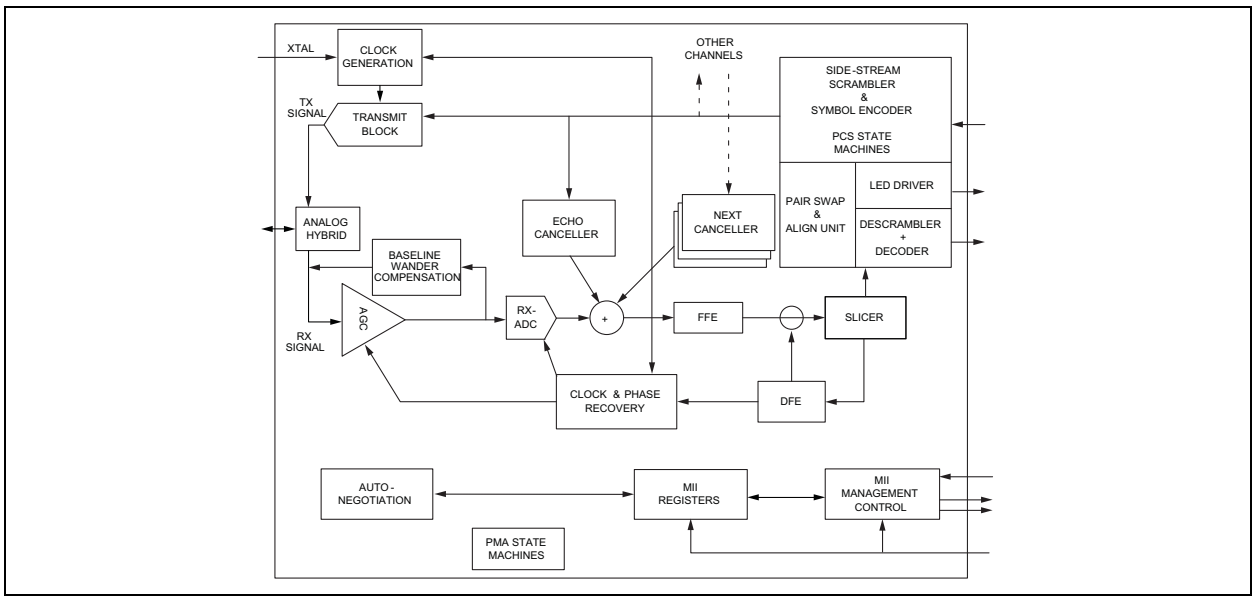
Auto-polarity correction is provided for the receiving differential pair to automatically swap and fix the incorrect +/– polarity wiring in the cabling.

## 3.2 1000BASE-T Transceiver

The 1000BASE-T transceiver is based-on a mixed-signal/digital-signal processing (DSP) architecture, which includes the analog front-end, digital channel equalizers, trellis encoders/decoders, echo cancelers, cross-talk cancelers, precision clock recovery scheme, and power-efficient line drivers.

Figure 3-2 shows a high-level block diagram of a single channel of the 1000BASE-T transceiver for one of the four differential pairs.

**FIGURE 3-2: KSZ9031MNX 1000BASE-T BLOCK DIAGRAM - SINGLE CHANNEL**




### 3.2.1 ANALOG ECHO-CANCELLATION CIRCUIT

In 1000BASE-T mode, the analog echo-cancellation circuit helps to reduce the near-end echo. This analog hybrid circuit relieves the burden of the ADC and the adaptive equalizer.

This circuit is disabled in 10BASE-T/100BASE-TX mode.

### 3.2.2 AUTOMATIC GAIN CONTROL (AGC)

In 1000BASE-T mode, the automatic gain control (AGC) circuit provides initial gain adjustment to boost up the signal level. This pre-conditioning circuit is used to improve the signal-to-noise ratio of the receive signal.

### 3.2.3 ANALOG-TO-DIGITAL CONVERTER (ADC)

In 1000BASE-T mode, the analog-to-digital converter (ADC) digitizes the incoming signal. ADC performance is essential to the overall performance of the transceiver.

This circuit is disabled in 10BASE-T/100BASE-TX mode.

### 3.2.4 TIMING RECOVERY CIRCUIT

In 1000BASE-T mode, the mixed-signal clock recovery circuit together with the digital phase-locked loop is used to recover and track the incoming timing information from the received data. The digital phase-locked loop has very low long-term jitter to maximize the signal-to-noise ratio of the receive signal.

The 1000BASE-T slave PHY must transmit the exact receive clock frequency recovered from the received data back to the 1000BASE-T master PHY. Otherwise, the master and slave will not be synchronized after long transmission. This also helps to facilitate echo cancellation and NEXT removal.

### 3.2.5 ADAPTIVE EQUALIZER

In 1000BASE-T mode, the adaptive equalizer provides the following functions:

- Detection for partial response signaling
- Removal of NEXT and ECHO noise
- Channel equalization

Signal quality is degraded by residual echo that is not removed by the analog hybrid because of impedance mismatch. The KSZ9031MNX uses a digital echo canceler to further reduce echo components on the receive signal.

In 1000BASE-T mode, data transmission and reception occurs simultaneously on all four pairs of wires (four channels). This results in high-frequency cross-talk coming from adjacent wires. The KSZ9031MNX uses three NEXT cancelers on each receive channel to minimize the cross-talk induced by the other three channels.

In 10BASE-T/100BASE-TX mode, the adaptive equalizer needs only to remove the inter-symbol interference and recover the channel loss from the incoming data.

### 3.2.6 TRELLIS ENCODER AND DECODER

In 1000BASE-T mode, the transmitted 8-bit data is scrambled into 9-bit symbols and further encoded into 4D-PAM5 symbols. The initial scrambler seed is determined by the specific PHY address to reduce EMI when more than one KSZ9031MNX is used on the same board. On the receiving side, the idle stream is examined first. The scrambler seed, pair skew, pair order, and polarity must be resolved through the logic. The incoming 4D-PAM5 data is then converted into 9-bit symbols and de-scrambled into 8-bit data.

## 3.3 Auto MDI/MDI-X

The Automatic MDI/MDI-X feature eliminates the need to determine whether to use a straight cable or a crossover cable between the KSZ9031MNX and its link partner. This auto-sense function detects the MDI/MDI-X pair mapping from the link partner, and assigns the MDI/MDI-X pair mapping of the KSZ9031MNX accordingly.

Table 3-1 shows the KSZ9031MNX 10/100/1000 pin configuration assignments for MDI/MDI-X pin mapping.

**TABLE 3-1: MDI/MDI-X PIN MAPPING**

| Pin (RJ-45 Pair) | MDI | | | MDI-X | | |
|---|---|---|---|---|---|---|
| | 1000BASE-T | 100BASE-T | 10BASE-T | 1000BASE-T | 100BASE-T | 10BASE-T |
| TXRXP/M_A (1, 2) | A+/– | TX+/– | TX+/– | B+/– | RX+/– | RX+/– |
| TXRXP/M_B (3, 6) | B+/– | RX+/– | RX+/– | A+/– | TX+/– | TX+/– |
| TXRXP/M_C (4, 5) | C+/– | Not Used | Not Used | D+/– | Not Used | Not Used |
| TXRXP/M_D (7, 8) | D+/– | Not Used | Not Used | C+/– | Not Used | Not Used |

Auto MDI/MDI-X is enabled by default. It is disabled by writing a one to Register 1Ch, Bit [6]. MDI and MDI-X mode is set by Register 1Ch, Bit [7] if Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

## 3.4 Pair-Swap, Alignment, and Polarity Check

In 1000BASE-T mode, the KSZ9031MNX

- Detects incorrect channel order and automatically restores the pair order for the A, B, C, D pairs (four channels).
- Supports 50 ns ±10 ns difference in propagation delay between pairs of channels in accordance with the IEEE 802.3 standard, and automatically corrects the data skew so the corrected four pairs of data symbols are synchronized.

Incorrect pair polarities of the differential signals are automatically corrected for all speeds.

## 3.5 Wave Shaping, Slew-Rate Control, and Partial Response

In communication systems, signal transmission encoding methods are used to provide the noise-shaping feature and to minimize distortion and error in the transmission channel.

- For 1000BASE-T, a special partial-response signaling method is used to provide the band-limiting feature for the transmission path.
- For 100BASE-TX, a simple slew-rate control method is used to minimize EMI.
- For 10BASE-T, pre-emphasis is used to extend the signal quality through the cable.

## 3.6 PLL Clock Synthesizer

The KSZ9031MNX generates 125 MHz, 25 MHz, and 10 MHz clocks for system timing. Internal clocks are generated from the external 25 MHz crystal or reference clock.

## 3.7 Auto-Negotiation

The KSZ9031MNX conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-negotiation allows UTP (unshielded twisted pair) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the operating mode.

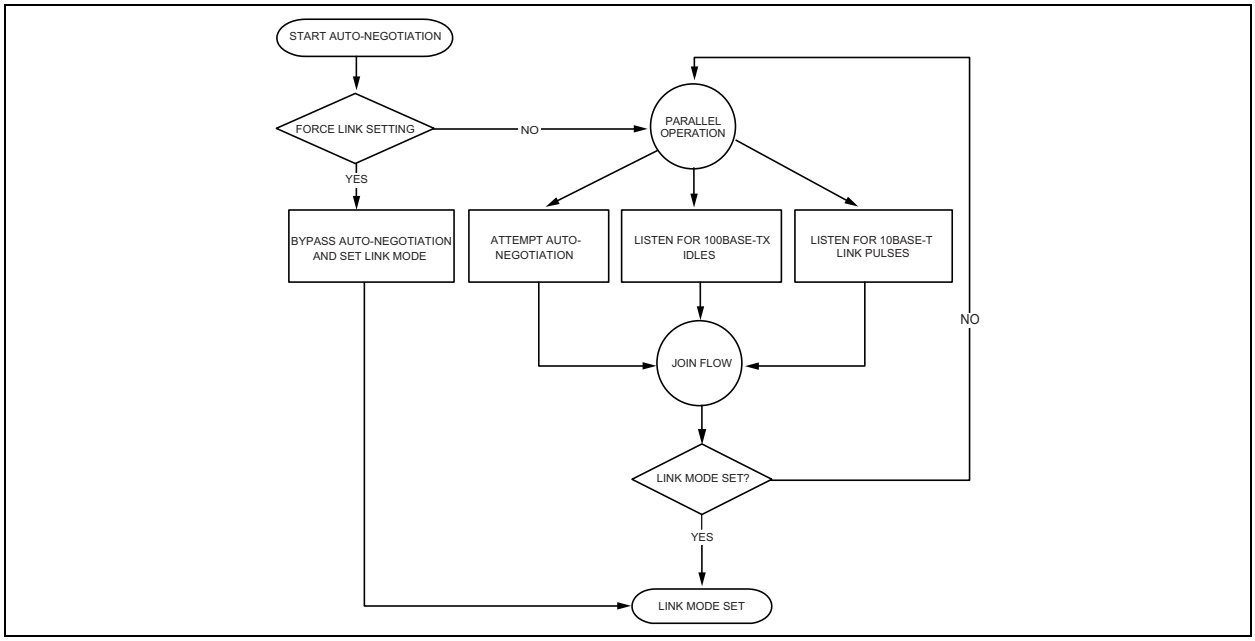
The following list shows the speed and duplex operation mode from highest-to-lowest:

- Priority 1: 1000BASE-T, full-duplex
- Priority 2: 1000BASE-T, half-duplex
- Priority 3: 100BASE-TX, full-duplex
- Priority 4: 100BASE-TX, half-duplex
- Priority 5: 10BASE-T, full-duplex
- Priority 6: 10BASE-T, half-duplex

If auto-negotiation is not supported or the KSZ9031MNX link partner is forced to bypass auto-negotiation for 10BASE-T and 100BASE-TX modes, the KSZ9031MNX sets its operating mode by observing the input signal at its receiver. This is known as parallel detection, and allows the KSZ9031MNX to establish a link by listening for a fixed signal protocol in the absence of the auto-negotiation advertisement protocol.

The auto-negotiation link-up process is shown in Figure 3-3.

**FIGURE 3-3: AUTO-NEGOTIATION FLOW CHART**




For 1000BASE-T mode, auto-negotiation is required and always used to establish a link. During 1000BASE-T auto-negotiation, the master and slave configuration is first resolved between link partners. Then the link is established with the highest common capabilities between link partners.

Auto-negotiation is enabled by default after power-up or hardware reset. After that, auto-negotiation can be enabled or disabled through Register 0h, Bit [12]. If auto-negotiation is disabled, the speed is set by Register 0h, Bits [6, 13] and the duplex is set by Register 0h, Bit [8].

If the speed is changed on the fly, the link goes down and either auto-negotiation or parallel detection initiates until a common speed between KSZ9031MNX and its link partner is re-established for a link.

If the link is already established and there is no change of speed on the fly, the changes (for example, duplex and pause capabilities) will not take effect unless either auto-negotiation is restarted through Register 0h, Bit [9], or a link-down to link-up transition occurs (that is, disconnecting and reconnecting the cable).

After auto-negotiation is completed, the link status is updated in Register 1h, Bit [2], and the link partner capabilities are updated in Registers 5h, 6h, and Ah.

The auto-negotiation finite state machines use interval timers to manage the auto-negotiation process. The duration of these timers under normal operating conditions is summarized in Table 3-2.

**TABLE 3-2: AUTO-NEGOTIATION TIMERS**

| Auto-Negotiation Interval Timers | Time Duration |
|---|---|
| Transmit Burst Interval | 16 ms |
| Transmit Pulse Interval | 68 µs |
| FLP Detect Minimum Time | 17.2 µs |
| FLP Detect Maximum Time | 185 µs |
| Receive Minimum Burst Interval | 6.8 ms |
| Receive Maximum Burst Interval | 112 ms |
| Data Detect Minimum Interval | 35.4 µs |
| Data Detect Maximum Interval | 95 µs |
| NLP Test Minimum Interval | 4.5 ms |
| NLP Test Maximum Interval | 30 ms |
| Link Loss Time | 52 ms |
| Break Link Time | 1480 ms |
| Parallel Detection Wait Time | 830 ms |
| Link Enable Wait Time | 1000 ms |

## 3.8 10/100 Mbps Speeds Only

Some applications require link-up to be limited to 10/100 Mbps speeds only.

After power-up/reset, the KSZ9031MNX can be restricted to auto-negotiate and link-up to 10/100 Mbps speeds only by programming the following register settings:

1. Set Register 0h, Bit [6] = ‘0’ to remove 1000 Mbps speed.
2. Set Register 9h, Bits [9:8] = ‘00’ to remove Auto-Negotiation advertisements for 1000 Mbps full/half duplex.
3. Write a ‘1’ to Register 0h, Bit [9], a self-clearing bit, to force a restart of Auto-Negotiation.

Auto-Negotiation and 10BASE-T/100BASE-TX speeds use only differential pairs A (pins 2, 3) and B (pins 7, 8). Differential pairs C (pins 10, 11) and D (pins 14, 15) can be left as no connects.

## 3.9 GMII Interface

The Gigabit Media Independent Interface (GMII) is compliant to the IEEE 802.3 Specification. It provides a common interface between GMII PHYs and MACs, and has the following key characteristics:

- Pin count is 24 pins (11 pins for data transmission, 11 pins for data reception, and 2 pins for carrier and collision indication).
- 1000 Mbps is supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 8 bits wide, a byte.

In GMII operation, the GMII pins function as follows:

- The MAC sources the transmit reference clock, GTX_CLK, at 125 MHz for 1000 Mbps.
- The PHY recovers and sources the receive reference clock, RX_CLK, at 125 MHz for 1000 Mbps.
- TX_EN, TXD[7:0], and TX_ER are sampled by the KSZ9031MNX on the rising edge of GTX_CLK.
- RX_DV, RXD[7:0], and RX_ER are sampled by the MAC on the rising edge of RX_CLK.
- CRS and COL are driven by the KSZ9031MNX and do not have to transition synchronously with respect to either GTX_CLK or RX_CLK.

The KSZ9031MNX combines GMII mode with MII mode to form GMII/MII mode to support data transfer at 10/100/1000 Mbps. After power-up or reset, the KSZ9031MNX is configured to GMII/MII mode if the MODE[3:0] strap-in pins are set to '0001'. See the Strapping Options - KSZ9031MNX section.

The KSZ9031MNX has the option to output a 125 MHz reference clock on CLK125_NDO (Pin 55). This clock provides a lower-cost reference clock alternative for GMII/MII MACs that require a 125 MHz crystal or oscillator. The 125 MHz clock output is enabled after power-up or reset if the CLK125_EN strap-in pin is pulled high.

The KSZ9031MNX provides a dedicated transmit clock input pin (GTX_CLK, Pin 32) for GMII mode, which is sourced by the MAC for 1000 Mbps speed.

### 3.9.1 GMII SIGNAL DEFINITION

Table 3-3 describes the GMII signals. Refer to Clause 35 of the IEEE 802.3 Specification for more detailed information.

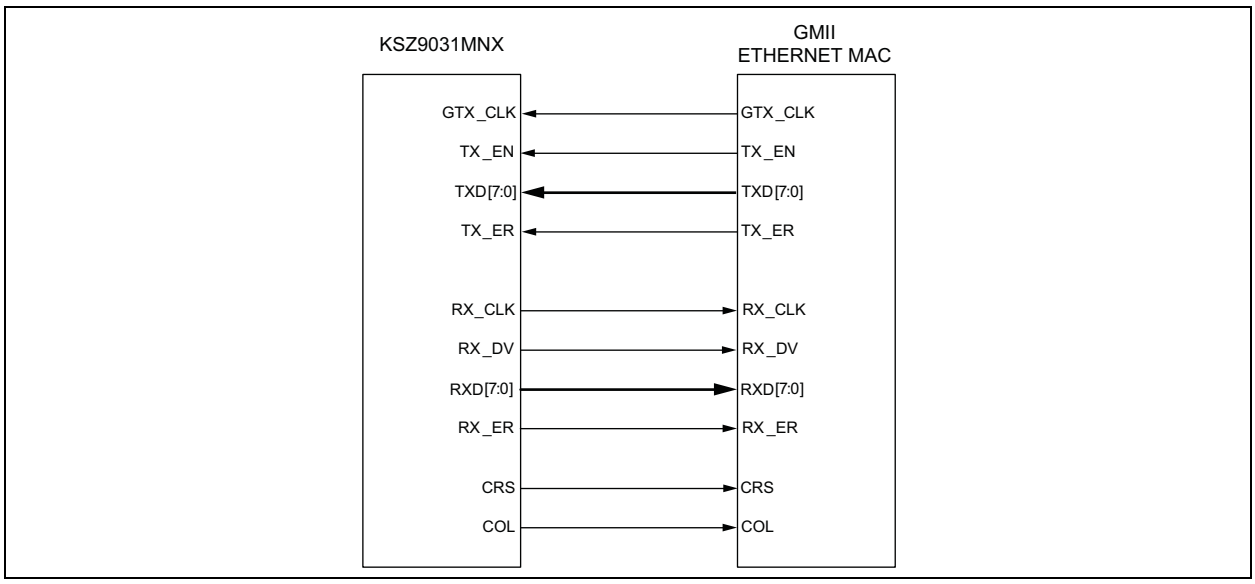
**TABLE 3-3: GMII SIGNAL DEFINITION**

| GMII Signal Name (per spec) | GMII Signal Name (per KSZ9031MNX) | Pin Type (with respect to PHY) | Pin Type (with respect to MAC) | Description |
|---|---|---|---|---|
| GTX_CLK | GTX_CLK | Input | Output | Transmit Reference Clock (125 MHz for 1000 Mbps) |
| TX_EN | TX_EN | Input | Output | Transmit Enable |
| TXD[7:0] | TXD[7:0] | Input | Output | Transmit Data[7:0] |
| TX_ER | TX_ER | Input | Output | Transmit Error |
| RX_CLK | RX_CLK | Output | Input | Receive Reference Clock (125 MHz for 1000 Mbps) |
| RX_DV | RX_DV | Output | Input | Receive Data Valid |
| RXD[7:0] | RXD[7:0] | Output | Input | Receive Data[7:0] |
| RX_ER | RX_ER | Output | Input | Receive Error |
| CRS | CRS | Output | Input | Carrier Sense |
| COL | COL | Output | Input | Collision Detected |

### 3.9.2 GMII SIGNAL DIAGRAM

The KSZ9031MNX GMII pin connections to the MAC are shown in Figure 3-4.

**FIGURE 3-4: KSZ9031MNX GMII INTERFACE**



## 3.10 MII Interface

The Media Independent Interface (MII) is compliant with the IEEE 802.3 Specification. It provides a common interface between MII PHYs and MACs, and has the following key characteristics:

- Pin count is 16 pins (7 pins for data transmission, 7 pins for data reception, and 2 pins for carrier and collision indication).
- 10 Mbps and 100 Mbps are supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 4 bits wide, a nibble.

In MII operation, the MII pins function as follows:

- The PHY sources the transmit reference clock, TX_CLK, at 25 MHz for 100 Mbps and 2.5 MHz for 10 Mbps.
- The PHY recovers and sources the receive reference clock, RX_CLK, at 25 MHz for 100 Mbps and 2.5 MHz for 10 Mbps.
- TX_EN, TXD[3:0], and TX_ER are driven by the MAC and transition synchronously with respect to TX_CLK.
- RX_DV, RXD[3:0], and RX_ER are driven by the KSZ9031MNX and transition synchronously with respect to RX_CLK.
- CRS and COL are driven by the KSZ9031MNX and do not have to transition synchronously with respect to either TX_CLK or RX_CLK.

The KSZ9031MNX combines GMII mode with MII mode to form GMII/MII mode to support data transfer at 10/100/1000 Mbps. After power-up or reset, the KSZ9031MNX is configured to GMII/MII mode if the MODE[3:0] strap-in pins are set to ‘0001’. See the Strapping Options - KSZ9031MNX section.

The KSZ9031MNX has the option to output a 125 MHz reference clock on CLK125_NDO (Pin 55). This clock provides a lower-cost reference clock alternative for GMII/MII MACs that require a 125 MHz crystal or oscillator. The 125 MHz clock output is enabled after power-up or reset if the CLK125_EN strap-in pin is pulled high.

The KSZ9031MNX provides a dedicated transmit clock output pin (TX_CLK, Pin 57) for MII mode, which is sourced by the KSZ9031MNX for 10/100 Mbps speed.

### 3.10.1 MII SIGNAL DEFINITION

Table 3-4 describes the MII signals. Refer to Clause 22 of the IEEE 802.3 Specification for detailed information.

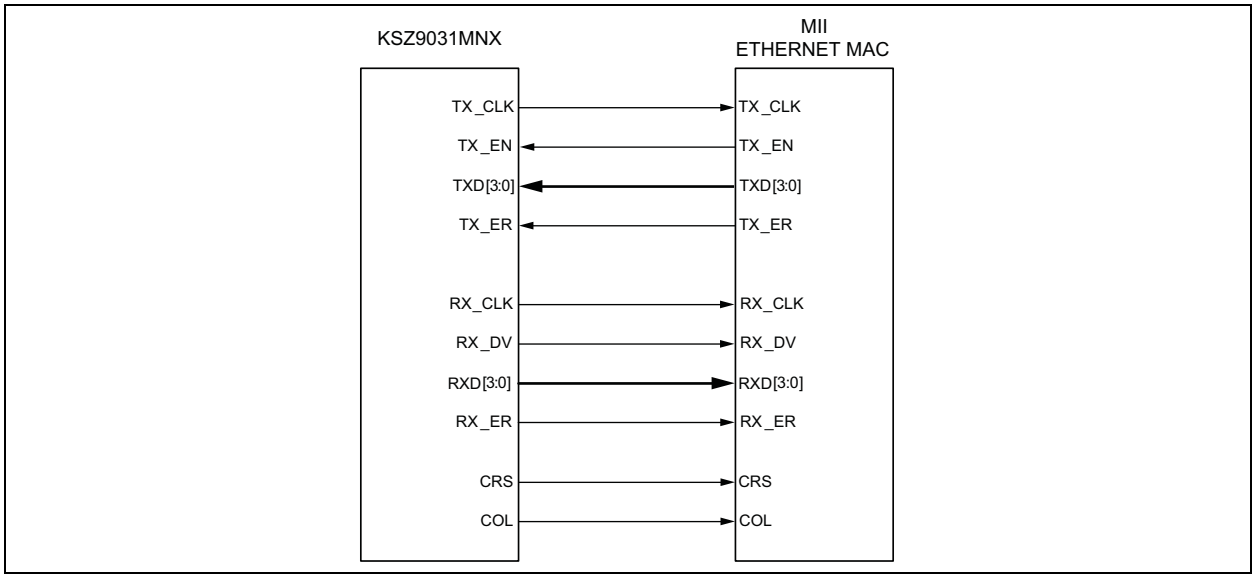
**TABLE 3-4: MII SIGNAL DEFINITION**

| MII Signal Name (per spec) | MII Signal Name (per KSZ9031MNX) | Pin Type (with respect to PHY) | Pin Type (with respect to MAC) | Description |
|---|---|---|---|---|
| TX_CLK | TX_CLK | Output | Input | Transmit Reference Clock (25 MHz for 100 Mbps, 2.5 MHz for 10 Mbps) |
| TX_EN | TX_EN | Input | Output | Transmit Enable |
| TXD[3:0] | TXD[3:0] | Input | Output | Transmit Data[3:0] |
| TX_ER | TX_ER | Input | Output | Transmit Error |
| RX_CLK | RX_CLK | Output | Input | Receive Reference Clock (25 MHz for 100 Mbps, 2.5 MHz for 10 Mbps) |
| RX_DV | RX_DV | Output | Input | Receive Data Valid |
| RXD[3:0] | RXD[3:0] | Output | Input | Receive Data[3:0] |
| RX_ER | RX_ER | Output | Input | Receive Error |
| CRS | CRS | Output | Input | Carrier Sense |
| COL | COL | Output | Input | Collision Detection |

### 3.10.2 MII SIGNAL DIAGRAM

The KSZ9031MNX MII pin connections to the MAC are shown in Figure 3-5.

**FIGURE 3-5: KSZ9031MNX MII INTERFACE**




## 3.11 MII Management (MIIM) Interface

The KSZ9031MNX supports the IEEE 802.3 MII management interface, also known as the Management Data Input/Output (MDIO) interface. This interface allows upper-layer devices to monitor and control the state of the KSZ9031MNX. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. More details about the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the physical connection mentioned earlier, which allows an external controller to communicate with one or more KSZ9031MNX devices. Each KSZ9031MNX device is assigned a unique PHY address between 0h and 7h by the PHYAD[2:0] strapping pins.
- A 32-register address space for direct access to IEEE-defined registers and vendor-specific registers, and for indirect access to MMD addresses and registers. See the Register Map section.

PHY Address 0h is supported as the unique PHY address only; it is not supported as the broadcast PHY address, which allows for a single write command to simultaneously program an identical PHY register for two or more PHY devices (for example, using PHY Address 0h to set Register 0h to a value of 0x1940 to set Bit [11] to a value of one to enable software power-down). Instead, separate write commands are used to program each PHY device.

Table 3-5 shows the MII management frame format for the KSZ9031MNX.

**TABLE 3-5: MII MANAGEMENT FRAME FORMAT FOR THE KSZ9031MNX**

| | Preamble | Start of Frame | Read/Write OP Code | PHY Address Bits [4:0] | REG Address Bits [4:0] | TA | Data Bits [15:0] | Idle |
|---|---|---|---|---|---|---|---|---|
| **Read** | 32 1's | 01 | 10 | 00AAA | RRRRR | Z0 | DDDDDDDD_DDDDDDDD | Z |
| **Write** | 32 1's | 01 | 01 | 00AAA | RRRRR | 10 | DDDDDDDD_DDDDDDDD | Z |

## 3.12 Interrupt (INT_N)

The INT_N pin is an optional interrupt signal that is used to inform the external controller that there has been a status update in the KSZ9031MNX PHY register. Bits [15:8] of Register 1Bh are the interrupt control bits that enable and disable the conditions for asserting the INT_N signal. Bits [7:0] of Register 1Bh are the interrupt status bits that indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading Register 1Bh.

Bit [14] of Register 1Fh sets the interrupt level to active high or active low. The default is active low.

The MII management bus option gives the MAC processor complete access to the KSZ9031MNX control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll the PHY for status change.

## 3.13 LED Mode

The KSZ9031MNX provides two programmable LED output pins, LED2 and LED1, which are configurable to support two LED modes. The LED mode is configured by the LED_MODE strap-in (Pin 55). It is latched at power-up/reset and is defined as follows:

- Pull-Up: Single-LED Mode
- Pull-Down: Tri-Color Dual-LED Mode

Each LED output pin can directly drive an LED with a series resistor (typically 220Ω to 470Ω).

### 3.13.1 SINGLE-LED MODE

In single-LED mode, the LED2 pin indicates the link status while the LED1 pin indicates the activity status, as shown in Table 3-6.

**TABLE 3-6: SINGLE-LED MODE - PIN DEFINITION**

| LED Pin | Pin State | LED Definition | Link/Activity |
|---|---|---|---|
| LED2 | H | OFF | Link Off |
| | L | ON | Link On (any speed) |
| LED1 | H | OFF | No Activity |
| | Toggle | Blinking | Activity (RX, TX) |

### 3.13.2 TRI-COLOR DUAL-LED MODE

In tri-color dual-LED mode, the link and activity status are indicated by the LED2 pin for 1000BASE-T; by the LED1 pin for 100BASE-TX; and by both LED2 and LED1 pins, working in conjunction, for 10BASE-T. This is summarized in Table 3-7.

**TABLE 3-7: TRI-COLOR DUAL-LED MODE - PIN DEFINITION**

| LED Pin (State) | | LED Pin (Definition) | | Link/Activity |
|---|---|---|---|---|
| LED2 | LED1 | LED2 | LED1 | |
| H | H | OFF | OFF | Link Off |
| L | H | ON | OFF | 1000 Link/No Activity |
| Toggle | H | Blinking | OFF | 1000 Link/Activity (RX, TX) |
| H | L | OFF | ON | 100 Link/No Activity |
| H | Toggle | OFF | Blinking | 100 Link/Activity (RX, TX) |
| L | L | ON | ON | 10 Link/No Activity |
| Toggle | Toggle | Blinking | Blinking | 10 Link/Activity (RX, TX) |

## 3.14 Loopback Mode

The KSZ9031MNX supports the following loopback operations to verify analog and/or digital data paths.

- Local (digital) loopback
- Remote (analog) loopback

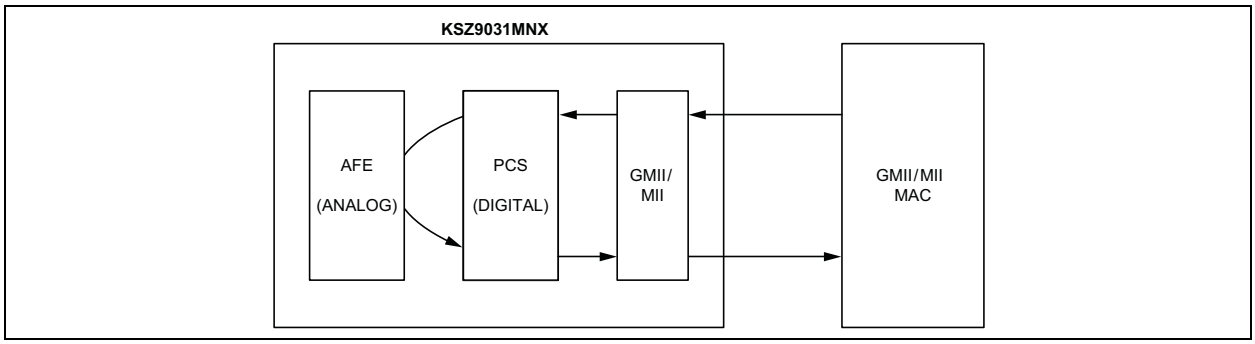
### 3.14.1 LOCAL (DIGITAL) LOOPBACK

This loopback mode checks the GMII/MII transmit and receive data paths between KSZ9031MNX and external MAC, and is supported for all three speeds (10/100/1000 Mbps) at full-duplex.

The loopback data path is shown in Figure 3-6.

1. GMII/MII MAC transmits frames to KSZ9031MNX.
2. Frames are wrapped around inside KSZ9031MNX.
3. KSZ9031MNX transmits frames back to GMII/MII MAC.

**FIGURE 3-6: LOCAL (DIGITAL) LOOPBACK**




The following programming steps and register settings are used for local loopback mode.

For 1000 Mbps loopback,

1. Set Register 0h,
   - Bit [14] = 1 // Enable local loopback mode
   - Bits [6, 13] = 10 // Select 1000 Mbps speed
   - Bit [12] = 0 // Disable auto-negotiation
   - Bit [8] = 1 // Select full-duplex mode
2. Set Register 9h,
   - Bit [12] = 1 // Enable master-slave manual configuration
   - Bit [11] = 0 // Select slave configuration (required for loopback mode)

For 10/100 Mbps loopback,

1. Set Register 0h,
   - Bit [14] = 1 // Enable local loopback mode
   - Bits [6, 13] = 00 / 01 // Select 10 Mbps/100 Mbps speed
   - Bit [12] = 0 // Disable auto-negotiation
   - Bit [8] = 1 // Select full-duplex mode

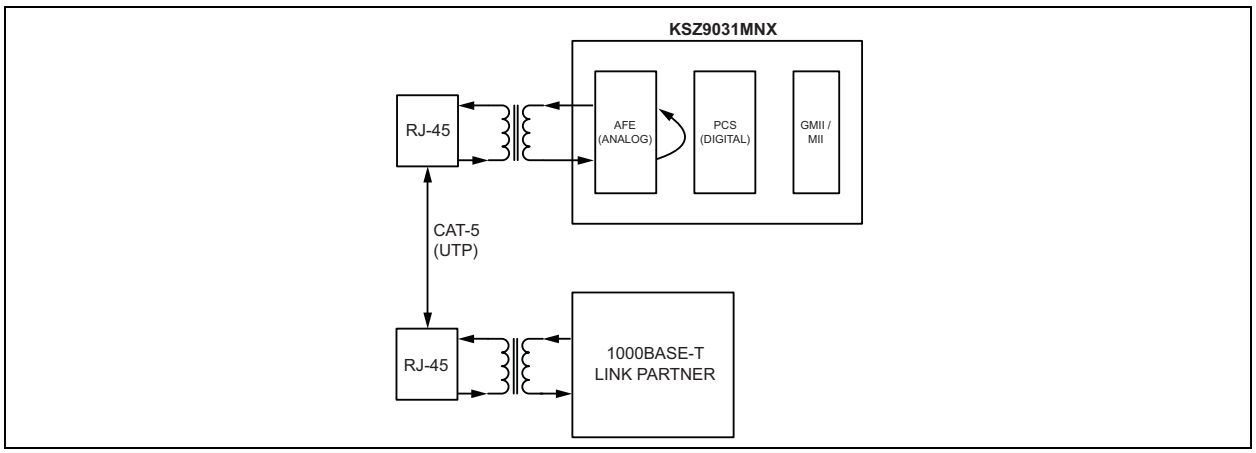
### 3.14.2 REMOTE (ANALOG) LOOPBACK

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between KSZ9031MNX and its link partner, and is supported for 1000BASE-T full-duplex mode only.

The loopback data path is shown in Figure 3-7.

1. The Gigabit PHY link partner transmits frames to KSZ9031MNX.
2. Frames are wrapped around inside KSZ9031MNX.
3. KSZ9031MNX transmits frames back to the Gigabit PHY link partner.

**FIGURE 3-7: REMOTE (ANALOG) LOOPBACK**




The following programming steps and register settings are used for remote loopback mode.

1. Set Register 0h,
   - Bits [6, 13] = 10 // Select 1000 Mbps speed
   - Bit [12] = 0 // Disable auto-negotiation
   - Bit [8] = 1 // Select full-duplex mode

   Or just auto-negotiate and link up at 1000BASE-T full-duplex mode with the link partner.
2. Set Register 11h,
   - Bit [8] = 1 // Enable remote loopback mode

## 3.15 LinkMD® Cable Diagnostic

The LinkMD function uses time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems, such as open circuits, short circuits, and impedance mismatches.

LinkMD operates by sending a pulse of known amplitude and duration down the selected differential pair, then analyzing the polarity and shape of the reflected signal to determine the type of fault: open circuit for a positive/non-inverted amplitude reflection and short circuit for a negative/inverted amplitude reflection. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

LinkMD is initiated by accessing Register 12h, the LinkMD – Cable Diagnostic register, in conjunction with Register 1Ch, the Auto MDI/MDI-X register. The latter register is needed to disable the Auto MDI/MDI-X function before running the LinkMD test. Additionally, a software reset (Reg. 0h, Bit [15] = 1) should be performed before and after running the LinkMD test. The reset helps to ensure the KSZ9031MNX is in the normal operating state before and after the test.

## 3.16 NAND Tree Support

The KSZ9031MNX provides parametric NAND tree support for fault detection between chip I/Os and board. NAND tree mode is enabled at power-up/reset with the MODE[3:0] strap-in pins set to ‘0100’. Table 3-8 lists the NAND tree pin order.

**TABLE 3-8: NAND TREE TEST PIN ORDER FOR KSZ9031MNX**

| Pin | Description |
|---|---|
| LED2 | Input |
| LED1/PME_N1 | Input |
| TXD0 | Input |
| TXD1 | Input |
| TXD2 | Input |
| TXD3 | Input |

**TABLE 3-8: NAND TREE TEST PIN ORDER FOR KSZ9031MNX (CONTINUED)**

| Pin | Description |
|---|---|
| TX_ER | Input |
| GTX_CLK | Input |
| TX_EN | Input |
| RX_DV | Input |
| RX_ER | Input |
| RX_CLK | Input |
| CRS | Input |
| COL | Input |
| INT_/PME_N2 | Input |
| MDC | Input |
| MDIO | Input |
| CLK125_NDO | Output |

## 3.17 Power Management

The KSZ9031MNX incorporates a number of power-management modes and features that provide methods to consume less energy. These are discussed in the following sections.

### 3.17.1 ENERGY-DETECT POWER-DOWN MODE

Energy-detect power-down (EDPD) mode is used to further reduce the transceiver power consumption when the cable is unplugged. It is enabled by writing a one to MMD Address 1Ch, Register 23h, Bit [0], and is in effect when auto-negotiation mode is enabled and the cable is disconnected (no link).

In EDPD Mode, the KSZ9031MNX shuts down all transceiver blocks, except for the transmitter and energy detect circuits. Power can be reduced further by extending the time interval between the transmissions of link pulses to check for the presence of a link partner. The periodic transmission of link pulses is needed to ensure the KSZ9031MNX and its link partner, when operating in the same low-power state and with Auto MDI/MDI-X disabled, can wake up when the cable is connected between them. By default, EDPD mode is disabled after power-up.

### 3.17.2 SOFTWARE POWER-DOWN MODE

This mode is used to power down the KSZ9031MNX device when it is not in use after power-up. Software power-down (SPD) mode is enabled by writing a one to Register 0h, Bit [11]. In the SPD state, the KSZ9031MNX disables all internal functions, except for the MII management interface. The KSZ9031MNX exits the SPD state after a zero is written to Register 0h, Bit [11].

### 3.17.3 CHIP POWER-DOWN MODE

This mode provides the lowest power state for the KSZ9031MNX device when it is mounted on the board but not in use. Chip power-down (CPD) mode is enabled after power-up/reset with the MODE[3:0] strap-in pins set to ‘0111’. The KSZ9031MNX exits CPD mode after a hardware reset is applied to the RESET_N pin (Pin 56) with the MODE[3:0] strap-in pins set to an operating mode other than CPD.

## 3.18 Wake-On-LAN

Wake-On-LAN (WOL) is normally a MAC-based function to wake up a host system (for example, an Ethernet end device, such as a PC) that is in standby power mode. Wake-up is triggered by receiving and detecting a special packet (commonly referred to as the “magic packet”) that is sent by the remote link partner. The KSZ9031MNX can perform the same WOL function if the MAC address of its associated MAC device is entered into the KSZ9031MNX PHY registers for magic-packet detection. When the KSZ9031MNX detects the magic packet, it wakes up the host by driving its power management event (PME) output pin low.

By default, the WOL function is disabled. It is enabled by setting the enabling bit and configuring the associated registers for the selected PME wake-up detection method.

The KSZ9031MNX provides three methods to trigger a PME wake-up:

- Magic-packet detection

- Customized-packet detection
- Link status change detection

### 3.18.1 MAGIC-PACKET DETECTION

The magic packet's frame format starts with 6 bytes of 0xFFh and is followed by 16 repetitions of the MAC address of its associated MAC device (local MAC device).

When the magic packet is detected from its link partner, the KSZ9031MNX asserts its PME output pin low.

The following MMD Address 2h registers are provided for magic-packet detection:

- Magic-packet detection is enabled by writing a '1' to MMD Address 2h, Register 10h, Bit [6]
- The MAC address (for the local MAC device) is written to and stored in MMD Address 2h, Registers 11h – 13h

The KSZ9031MNX does not generate the magic packet. The magic packet must be provided by the external system.

### 3.18.2 CUSTOMIZED-PACKET DETECTION

The customized packet has associated register/bit masks to select which byte, or bytes, of the first 64 bytes of the packet to use in the CRC calculation. After the KSZ9031MNX receives the packet from its link partner, the selected bytes for the received packet are used to calculate the CRC. The calculated CRC is compared to the expected CRC value that was previously written to and stored in the KSZ9031MNX PHY registers. If there is a match, the KSZ9031MNX asserts its PME output pin low.

Four customized packets are provided to support four types of wake-up scenarios. A dedicated set of registers is used to configure and enable each customized packet.

The following MMD registers are provided for customized-packet detection:

- Each of the four customized packets is enabled via MMD Address 2h, Register 10h,
  - Bit [2] // For customized packets, type 0
  - Bit [3] // For customized packets, type 1
  - Bit [4] // For customized packets, type 2
  - Bit [5] // For customized packets, type 3
- 32-bit expected CRCs are written to and stored in:
  - MMD Address 2h, Registers 14h – 15h // For customized packets, type 0
  - MMD Address 2h, Registers 16h – 17h // For customized packets, type 1
  - MMD Address 2h, Registers 18h – 19h // For customized packets, type 2
  - MMD Address 2h, Registers 1Ah – 1Bh // For customized packets, type 3
- Masks to indicate which of the first 64-bytes to use in the CRC calculation are set in:
  - MMD Address 2h, Registers 1Ch – 1Fh // For customized packets, type 0
  - MMD Address 2h, Registers 20h – 23h // For customized packets, type 1
  - MMD Address 2h, Registers 24h – 27h // For customized packets, type 2
  - MMD Address 2h, Registers 28h – 2Bh // For customized packets, type 3

### 3.18.3 LINK STATUS CHANGE DETECTION

If link status change detection is enabled, the KSZ9031MNX asserts its PME output pin low whenever there is a link status change using the following MMD Address 2h registers bits and their enabled (1) or disabled (0) settings:

- MMD Address 2h, Register 10h, Bit [0] // For link-up detection
- MMD Address 2h, Register 10h, Bit [1] // For link-down detection

The PME output signal is available on either LED1/PME_N1 (Pin 19) or INT_N/PME_N2 (Pin 53), and is selected and enabled using MMD Address 2h, Register 2h, Bits [8] and [10], respectively. Additionally, MMD Address 2h, Register 10h, Bits [15:14] defines the output functions for Pins 19 and 53.

The PME output is active low and requires a 1 kΩ pull-up to the VDDIO supply. When asserted, the PME output is cleared by disabling the register bit that enabled the PME trigger source (magic packet, customized packet, link status change).

## 3.19 Typical Current/Power Consumption

Table 3-9, Table 3-10, Table 3-11, and Table 3-12 show the typical current consumption by the core (DVDDL, AVDDL, AVDDL_PLL), transceiver (AVDDH) and digital I/O (DVDDH) supply pins, and the total typical power for the entire KSZ9031MNX device for various nominal operating voltage combinations.

**TABLE 3-9: TYPICAL CURRENT/POWER CONSUMPTION TRANSCEIVER (3.3V), DIGITAL I/O (3.3V)**

| Condition | 1.2V Core (DVDDL, AVDDL, AVDDL_PLL) | 3.3V Transceiver (AVDDH) | 3.3V Digital I/O (DVDDH) | Total Chip Power |
|---|---|---|---|---|
| 1000BASE-T Link-Up (no traffic) | 211 mA | 66.6 mA | 26.0 mA | 560 mW |
| 1000BASE-T Full-Duplex at 100% Utilization | 221 mA | 65.6 mA | 53.8 mA | 660 mW |
| 100BASE-TX Link-Up (no traffic) | 60.6 mA | 28.7 mA | 13.3 mA | 211 mW |
| 100BASE-TX Full-Duplex at 100% Utilization | 61.2 mA | 28.7 mA | 18.0 mA | 228 mW |
| 10BASE-T Link-Up (no traffic) | 7.0 mA | 17.0 mA | 5.7 mA | 83 mW |
| 10BASE-T Full-Duplex at 100% Utilization | 7.7 mA | 29.3 mA | 11.1 mA | 143 mW |
| Software Power-Down Mode (Reg. 0h.11 = 1) | 0.9 mA | 4.1 mA | 7.1 mA | 38 mW |

**TABLE 3-10: TYPICAL CURRENT/POWER CONSUMPTION TRANSCEIVER (3.3V), DIGITAL I/O (1.8V)**

| Condition | 1.2V Core (DVDDL, AVDDL, AVDDL_PLL) | 3.3V Transceiver (AVDDH) | 1.8V Digital I/O (DVDDH) | Total Chip Power |
|---|---|---|---|---|
| 1000BASE-T Link-Up (no traffic) | 211 mA | 66.6 mA | 14.2 mA | 498 mW |
| 1000BASE-T Full-Duplex at 100% Utilization | 221 mA | 65.6 mA | 29.3 mA | 534 mW |
| 100BASE-TX Link-Up (no traffic) | 60.6 mA | 28.7 mA | 7.3 mA | 181 mW |
| 100BASE-TX Full-Duplex at 100% Utilization | 61.2 mA | 28.7 mA | 10.0 mA | 186 mW |
| 10BASE-T Link-Up (no traffic) | 7.0 mA | 17.0 mA | 3.1 mA | 70 mW |
| 10BASE-T Full-Duplex at 100% Utilization | 7.7 mA | 29.3 mA | 6.0 mA | 117 mW |
| Software Power-Down Mode (Reg. 0h.11 = 1) | 0.9 mA | 4.1 mA | 3.7 mA | 21 mW |

**TABLE 3-11: TYPICAL CURRENT/POWER CONSUMPTION TRANSCEIVER (2.5V; Note 1), DIGITAL I/O (2.5V)**

| Condition | 1.2V Core (DVDDL, AVDDL, AVDDL_PLL) | 2.5V Transceiver (AVDDH) | 2.5V Digital I/O (DVDDH) | Total Chip Power |
|---|---|---|---|---|
| 1000BASE-T Link-Up (no traffic) | 211 mA | 58.6 mA | 19.3 mA | 448 mW |
| 1000BASE-T Full-Duplex at 100% Utilization | 221 mA | 57.6 mA | 40.5 mA | 510 mW |
| 100BASE-TX Link-Up (no traffic) | 60.6 mA | 24.8 mA | 10.0 mA | 160 mW |
| 100BASE-TX Full-Duplex at 100% Utilization | 61.2 mA | 24.8 mA | 13.7 mA | 170 mW |
| 10BASE-T Link-Up (no traffic) | 7.0 mA | 12.5 mA | 4.3 mA | 50 mW |
| 10BASE-T Full-Duplex at 100% Utilization | 7.7 mA | 25.8 mA | 8.3 mA | 94 mW |
| Software Power-Down Mode (Reg. 0h.11 = 1) | 0.9 mA | 3.0 mA | 5.3 mA | 22 mW |

**Note 1:** 2.5V AVDDH is recommended for commercial temperature range (0°C to +70°C) operation only.

**TABLE 3-12: TYPICAL CURRENT/POWER CONSUMPTION TRANSCEIVER (2.5V; Note 1), DIGITAL I/O (1.8V)**

| Condition | 1.2V Core (DVDDL, AVDDL, AVDDL_PLL) | 2.5V Transceiver (AVDDH) | 1.8V Digital I/O (DVDDH) | Total Chip Power |
|---|---|---|---|---|
| 1000BASE-T Link-Up (no traffic) | 211 mA | 58.6 mA | 14.2 mA | 425 mW |
| 1000BASE-T Full-Duplex at 100% Utilization | 221 mA | 57.6 mA | 29.3 mA | 462 mW |
| 100BASE-TX Link-Up (no traffic) | 60.6 mA | 24.8 mA | 7.3 mA | 148 mW |
| 100BASE-TX Full-Duplex at 100% Utilization | 61.2 mA | 24.8 mA | 10.0 mA | 153 mW |
| 10BASE-T Link-Up (no traffic) | 7.0 mA | 12.5 mA | 3.1 mA | 45 mW |
| 10BASE-T Full-Duplex at 100% Utilization | 7.7 mA | 25.8 mA | 6.0 mA | 85 mW |
| Software Power-Down Mode (Reg. 0h.11 = 1) | 0.9 mA | 3.0 mA | 3.7 mA | 15 mW |

**Note 1:** 2.5V AVDDH is recommended for commercial temperature range (0°C to +70°C) operation only.

# 4.0 REGISTER DESCRIPTIONS

This chapter describes the various control and status registers (CSRs).

## 4.1 Register Map

The register space within the KSZ9031MNX consists of two distinct areas.

- Standard registers // Direct register access
- MDIO Manageable device (MMD) registers // Indirect register access

The KSZ9031MNX supports the following standard registers.

**TABLE 4-1: STANDARD REGISTERS SUPPORTED BY KSZ9031MNX**

| Register Number (hex) | Description |
|---|---|
| **IEEE-Defined Registers** | |
| 0h | Basic Control |
| 1h | Basic Status |
| 2h | PHY Identifier 1 |
| 3h | PHY Identifier 2 |
| 4h | Auto-Negotiation Advertisement |
| 5h | Auto-Negotiation Link Partner Ability |
| 6h | Auto-Negotiation Expansion |
| 7h | Auto-Negotiation Next Page |
| 8h | Auto-Negotiation Link Partner Next Page Ability |
| 9h | 1000BASE-T Control |
| Ah | 1000BASE-T Status |
| Bh - Ch | Reserved |
| Dh | MMD Access – Control |
| Eh | MMD Access – Register/Data |
| Fh | Extended Status |
| **Vendor-Specific Registers** | |
| 10h | Reserved |
| 11h | Remote Loopback |
| 12h | LinkMD Cable Diagnostic |
| 13h | Digital PMA/PCS Status |
| 14h | Reserved |
| 15h | RXER Counter |
| 16h - 1Ah | Reserved |
| 1Bh | Interrupt Control/Status |
| 1Ch | Auto MDI/MDI-X |
| 1Dh - 1Eh | Reserved |
| 1Fh | PHY Control |

The KSZ9031MNX supports the following MMD device addresses and their associated register addresses, which make up the indirect MMD registers. These can be seen in Table 4-2.

**TABLE 4-2: MMD REGISTERS SUPPORTED BY KSZ9031MNX**

| Device Address (hex) | Register Address (hex) | Description |
|---|---|---|
| 0h | 3h | AN FLP Burst Transmit – LO |
| | 4h | AN FLP Burst Transmit – HI |
| 1h | 5Ah | 1000BASE-T Link-Up Time Control |
| 2h | 0h | Common Control |
| | 1h | Strap Status |
| | 2h | Operation Mode Strap Override |
| | 3h | Operation Mode Strap Status |
| | 4h | GMII Control Signal Pad Skew |
| | 8h | GMII Clock Pad Skew |
| | 10h | Wake-On-LAN – Control |
| | 11h | Wake-On-LAN – Magic Packet, MAC-DA-0 |
| | 12h | Wake-On-LAN – Magic Packet, MAC-DA-1 |
| | 13h | Wake-On-LAN – Magic Packet, MAC-DA-2 |
| | 14h | Wake-On-LAN – Customized Packet, Type 0, Expected CRC 0 |
| | 15h | Wake-On-LAN – Customized Packet, Type 0, Expected CRC 1 |
| | 16h | Wake-On-LAN – Customized Packet, Type 1, Expected CRC 0 |
| | 17h | Wake-On-LAN – Customized Packet, Type 1, Expected CRC 1 |
| | 18h | Wake-On-LAN – Customized Packet, Type 2, Expected CRC 0 |
| | 19h | Wake-On-LAN – Customized Packet, Type 2, Expected CRC 1 |
| | 1Ah | Wake-On-LAN – Customized Packet, Type 3, Expected CRC 0 |
| | 1Bh | Wake-On-LAN – Customized Packet, Type 3, Expected CRC 1 |
| | 1Ch | Wake-On-LAN – Customized Packet, Type 0, Mask 0 |
| | 1Dh | Wake-On-LAN – Customized Packet, Type 0, Mask 1 |
| | 1Eh | Wake-On-LAN – Customized Packet, Type 0, Mask 2 |
| | 1Fh | Wake-On-LAN – Customized Packet, Type 0, Mask 3 |
| | 20h | Wake-On-LAN – Customized Packet, Type 1, Mask 0 |
| | 21h | Wake-On-LAN – Customized Packet, Type 1, Mask 1 |
| | 22h | Wake-On-LAN – Customized Packet, Type 1, Mask 2 |
| | 23h | Wake-On-LAN – Customized Packet, Type 1, Mask 3 |

**TABLE 4-2: MMD REGISTERS SUPPORTED BY KSZ9031MNX (CONTINUED)**

| Device Address (hex) | Register Address (hex) | Description |
|---|---|---|
| 2h | 24h | Wake-On-LAN – Customized Packet, Type 2, Mask 0 |
| | 25h | Wake-On-LAN – Customized Packet, Type 2, Mask 1 |
| | 26h | Wake-On-LAN – Customized Packet, Type 2, Mask 2 |
| | 27h | Wake-On-LAN – Customized Packet, Type 2, Mask 3 |
| | 28h | Wake-On-LAN – Customized Packet, Type 3, Mask 0 |
| | 29h | Wake-On-LAN – Customized Packet, Type 3, Mask 1 |
| | 2Ah | Wake-On-LAN – Customized Packet, Type 3, Mask 2 |
| | 2Bh | Wake-On-LAN – Customized Packet, Type 3, Mask 3 |
| 1Ch | 4h | Analog Control 4 |
| | 23h | EDPD Control |

## 4.2 Standard Registers

Standard registers provide direct read/write access to a 32-register address space, as defined in Clause 22 of the IEEE 802.3 Specification. Within this address space, the first 16 registers (Registers 0h to Fh) are defined according to the IEEE specification, while the remaining 16 registers (Registers 10h to 1Fh) are defined specific to the PHY vendor.

**TABLE 4-3: IEEE-DEFINED REGISTER DESCRIPTIONS**

| Address | Name | Description | Mode (Note 4-1) | Default |
|---|---|---|---|---|
| **Register 0h – Basic Control** | | | | |
| 0.15 | Reset | 1 = Software PHY reset<br>0 = Normal operation<br>This bit is self-cleared after a '1' is written to it. | RW/SC | 0 |
| 0.14 | Loopback | 1 = Loopback mode<br>0 = Normal operation | RW | 0 |
| 0.13 | Speed Select (LSB) | [0.6, 0.13]<br>[1,1] = Reserved<br>[1,0] = 1000 Mbps<br>[0,1] = 100 Mbps<br>[0,0] = 10 Mbps<br>This bit is ignored if auto-negotiation is enabled (Reg. 0.12 = 1). | RW | 0 |
| 0.12 | Auto-Negotiation Enable | 1 = Enable auto-negotiation process<br>0 = Disable auto-negotiation process<br>If enabled, auto-negotiation result overrides settings in Reg. 0.13, 0.8 and 0.6.<br>If disabled, Auto MDI-X is also automatically disabled. Use Register 1Ch to set MDI/MDI-X. | RW | 1 |

**TABLE 4-3: IEEE-DEFINED REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode (Note 4-1) | Default |
|---|---|---|---|---|
| 0.11 | Power-Down | 1 = Power-down mode<br>0 = Normal operation<br>When this bit is set to '1', the link-down status might not get updated in the PHY register. Software should note link is down and should not rely on the PHY register link status.<br>After this bit is changed from '1' to '0', an internal global reset is automatically generated. Wait a minimum of 1 ms before read/write access to the PHY registers. | RW | 0 |
| 0.10 | Isolate | 1 = Electrical isolation of PHY from GMII/MII<br>0 = Normal operation | RW | 0 |
| 0.9 | Restart Auto-Negotiation | 1 = Restart auto-negotiation process<br>0 = Normal operation<br>This bit is self-cleared after a '1' is written to it. | RW/SC | 0 |
| 0.8 | Duplex Mode | 1 = Full-duplex<br>0 = Half-duplex | RW | 1 |
| 0.7 | Collision Test | 1 = Enable COL test<br>0 = Disable COL test | RW | 0 |
| 0.6 | Speed Select (MSB) | [0.6, 0.13]<br>[1,1] = Reserved<br>[1,0] = 1000 Mbps<br>[0,1] = 100 Mbps<br>[0,0] = 10 Mbps<br>This bit is ignored if auto-negotiation is enabled (Reg. 0.12 = 1). | RW | Set by MODE[3:0] strapping pins.<br>See the Strapping Options - KSZ9031MNX section for details. |
| 0.5:0 | Reserved | Reserved | RO | 00_0000 |
| **Register 1h - Basic Status** | | | | |
| 1.15 | 100BASE-T4 | 1 = T4 capable<br>0 = Not T4 capable | RO | 0 |
| 1.14 | 100BASE-TX Full-Duplex | 1 = Capable of 100 Mbps full-duplex<br>0 = Not capable of 100 Mbps full-duplex | RO | 1 |
| 1.13 | 100BASE-TX Half-Duplex | 1 = Capable of 100 Mbps half-duplex<br>0 = Not capable of 100 Mbps half-duplex | RO | 1 |
| 1.12 | 10BASE-T Full-Duplex | 1 = Capable of 10 Mbps full-duplex<br>0 = Not capable of 10 Mbps full-duplex | RO | 1 |
| 1.11 | 10BASE-T Half-Duplex | 1 = Capable of 10 Mbps half-duplex<br>0 = Not capable of 10 Mbps half-duplex | RO | 1 |
| 1.10:9 | Reserved | Reserved | RO | 00 |
| 1.8 | Extended Status | 1 = Extended status info in Reg. 15h.<br>0 = No extended status info in Reg. 15h. | RO | 1 |
| 1.7 | Reserved | Reserved | RO | 0 |
| 1.6 | No Preamble | 1 = Preamble suppression<br>0 = Normal preamble | RO | 1 |
| 1.5 | Auto-Negotiation Complete | 1 = Auto-negotiation process completed<br>0 = Auto-negotiation process not completed | RO | 0 |
| 1.4 | Remote Fault | 1 = Remote fault<br>0 = No remote fault | RO/LH | 0 |

**TABLE 4-3: IEEE-DEFINED REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode (Note 4-1) | Default |
|---|---|---|---|---|
| 1.3 | Auto-Negotiation Ability | 1 = Can perform auto-negotiation<br>0 = Cannot perform auto-negotiation | RO | 1 |
| 1.2 | Link Status | 1 = Link is up<br>0 = Link is down | RO/LL | 0 |
| 1.1 | Jabber Detect | 1 = Jabber detected<br>0 = Jabber not detected (default is low) | RO/LH | 0 |
| 1.0 | Extended Capability | 1 = Supports extended capability registers | RO | 1 |
| **Register 2h - PHY Identifier 1** | | | | |
| 2.15:0 | PHY ID Number | Assigned to the 3rd through 18th bits of the organizationally unique identifier (OUI). KENDIN Communication's OUI is 0010A1h. | RO | 0022h |
| **Register 3h - PHY Identifier 2** | | | | |
| 3.15:10 | PHY ID Number | Assigned to the 19th through 24th bits of the organizationally unique identifier (OUI). KENDIN Communication's OUI is 0010A1h. | RO | 0001_01 |
| 3.9:4 | Model Number | Six-bit manufacturer's model number | RO | 10_0010 |
| 3.3:0 | Revision Number | Four-bit manufacturer's revision number | RO | Indicates silicon revision |
| **Register 4h - Auto-Negotiation Advertisement** | | | | |
| 4.15 | Next Page | 1 = Next page capable<br>0 = No next page capability | RW | 0 |
| 4.14 | Reserved | Reserved | RO | 0 |
| 4.13 | Remote Fault | 1 = Remote fault supported<br>0 = No remote fault | RW | 0 |
| 4.12 | Reserved | Reserved | RO | 0 |
| 4.11:10 | Pause | [4.11, 4.10]<br>[0,0] = No pause<br>[1,0] = Asymmetric pause (link partner)<br>[0,1] = Symmetric pause<br>[1,1] = Symmetric and asymmetric pause (local device) | RW | 00 |
| 4.9 | 100BASE-T4 | 1 = T4 capable<br>0 = No T4 capability | RO | 0 |
| 4.8 | 100BASE-TX Full-Duplex | 1 = 100 Mbps full-duplex capable<br>0 = No 100 Mbps full-duplex capability | RW | 1 |
| 4.7 | 100BASE-TX Half-Duplex | 1 = 100 Mbps half-duplex capable<br>0 = No 100 Mbps half-duplex capability | RW | 1 |
| 4.6 | 10BASE-T Full-Duplex | 1 = 10 Mbps full-duplex capable<br>0 = No 10 Mbps full-duplex capability | RW | 1 |
| 4.5 | 10BASE-T Half-Duplex | 1 = 10 Mbps half-duplex capable<br>0 = No 10 Mbps half-duplex capability | RW | 1 |
| 4.4:0 | Selector Field | [00001] = IEEE 802.3 | RW | 0_0001 |
| **Register 5h - Auto-Negotiation Link Partner Ability** | | | | |
| 5.15 | Next Page | 1 = Next page capable<br>0 = No next page capability | RO | 0 |

**TABLE 4-3: IEEE-DEFINED REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode (Note 4-1) | Default |
|---|---|---|---|---|
| 5.14 | Acknowledge | 1 = Link code word received from partner<br>0 = Link code word not yet received | RO | 0 |
| 5.13 | Remote Fault | 1 = Remote fault detected<br>0 = No remote fault | RO | 0 |
| 5.12 | Reserved | Reserved | RO | 0 |
| 5.11:10 | Pause | [5.11, 5.10]<br>[0,0] = No pause<br>[1,0] = Asymmetric Pause (link partner)<br>[0,1] = Symmetric pause<br>[1,1] = Symmetric and asymmetric pause (local device) | RW | 00 |
| 5.9 | 100BASE-T4 | 1 = T4 capable<br>0 = No T4 capability | RO | 0 |
| 5.8 | 100BASE-TX Full-Duplex | 1 = 100 Mbps full-duplex capable<br>0 = No 100 Mbps full-duplex capability | RO | 0 |
| 5.7 | 100BASE-TX Half-Duplex | 1 = 100 Mbps half-duplex capable<br>0 = No 100 Mbps half-duplex capability | RO | 0 |
| 5.6 | 10BASE-T Full-Duplex | 1 = 10 Mbps full-duplex capable<br>0 = No 10 Mbps full-duplex capability | RO | 0 |
| 5.5 | 10BASE-T Half-Duplex | 1 = 10 Mbps half-duplex capable<br>0 = No 10 Mbps half-duplex capability | RO | 0 |
| 5.4:0 | Selector Field | [00001] = IEEE 802.3 | RO | 0_0000 |
| **Register 6h - Auto-Negotiation Expansion** | | | | |
| 6.15:5 | Reserved | Reserved | RO | 0000_0000_000 |
| 6.4 | Parallel Detection Fault | 1 = Fault detected by parallel detection<br>0 = No fault detected by parallel detection | RO/LH | 0 |
| 6.3 | Link Partner Next Page Able | 1 = Link partner has next page capability<br>0 = Link partner does not have next page capability | RO | 0 |
| 6.2 | Next Page Able | 1 = Local device has next page capability<br>0 = Local device does not have next page capability | RO | 1 |
| 6.1 | Page Received | 1 = New page received<br>0 = New page not received | RO/LH | 0 |
| 6.0 | Link Partner Auto-Negotiation Able | 1 = Link partner has auto-negotiation capability<br>0 = Link partner does not have auto-negotiation capability | RO | 0 |
| **Register 7h - Auto-Negotiation Next Page** | | | | |
| 7.15 | Next Page | 1 = Additional next pages will follow<br>0 = Last page | RW | 0 |
| 7.14 | Reserved | Reserved | RO | 0 |
| 7.13 | Message Page | 1 = Message page<br>0 = Unformatted page | RW | 1 |
| 7.12 | Acknowledge2 | 1 = Will comply with message<br>0 = Cannot comply with message | RW | 0 |

**TABLE 4-3: IEEE-DEFINED REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode (Note 4-1) | Default |
|---|---|---|---|---|
| 7.11 | Toggle | 1 = Previous value of the transmitted link code word equal to logic one<br>0 = Previous value of the transmitted link code word equal to logic zero | RO | 0 |
| 7.10:0 | Message Field | 11-bit wide field to encode 2048 messages | RW | 000_0000_0001 |
| **Register 8h - Link Partner Next Page Ability** | | | | |
| 8.15 | Next Page | 1 = Additional next pages will follow<br>0 = Last page | RO | 0 |
| 8.14 | Acknowledge | 1 = Successful receipt of link word<br>0 = No successful receipt of link word | RO | 0 |
| 8.13 | Message Page | 1 = Message page<br>0 = Unformatted page | RO | 0 |
| 8.12 | Acknowl-edge2 | 1 = Able to act on the information<br>0 = Not able to act on the information | RO | 0 |
| 8.11 | Toggle | 1 = Previous value of transmitted link code word equal to logic zero<br>0 = Previous value of transmitted link code word equal to logic one | RO | 0 |
| 8.10:0 | Message Field | — | RO | 000_0000_0000 |
| **Register 9h – 1000BASE-T Control** | | | | |
| 9.15:13 | Test Mode Bits | Transmitter test mode operations<br>[9.15:13] Mode<br>[000] Normal operation<br>[001] Test mode 1 –Transmit waveform test<br>[010] Test mode 2 –Transmit jitter test in master mode<br>[011] Test mode 3 –Transmit jitter test in slave mode<br>[100] Test mode 4 –Transmitter distortion test<br>[101] Reserved, operations not identified<br>[110] Reserved, operations not identified<br>[111] Reserved, operations not identified<br>To enable 1000BASE-T Test Mode:<br>1) Set Register 0h = 0x0140 to disable auto-negotiation and select 1000Mbps speed.<br>2) Set Register 9h, bits [15:13] = 001, 010, 011, or 100 to select one of the 1000BASE-T Test Modes.<br>After the above settings, the test waveform for the selected test mode is transmitted onto each of the 4 differential pairs. No link partner is needed. | RW | 000 |
| 9.12 | Master-Slave Manual Con-figuration Enable | 1 = Enable master-slave manual configuration value<br>0 = Disable master-slave manual configuration value | RW | 0 |
| 9.11 | Master-Slave Manual Con-figuration Value | 1 = Configure PHY as master during master-slave negotiation<br>0 = Configure PHY as slave during master-slave negotiation<br>This bit is ignored if master-slave manual configuration is disabled (Reg. 9.12 = 0). | RW | 0 |

**TABLE 4-3: IEEE-DEFINED REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode (Note 4-1) | Default |
|---|---|---|---|---|
| 9.10 | Port Type | 1 = Indicate the preference to operate as multi-port device (master)<br>0 = Indicate the preference to operate as single-port device (slave)<br>This bit is valid only if master-slave manual configuration is disabled (Reg. 9.12 = 0). | RW | 0 |
| 9.9 | 1000BASE-T Full-Duplex | 1 = Advertise PHY is 1000BASE-T full-duplex capable<br>0 = Advertise PHY is not 1000BASE-T full-duplex capable | RW | 1 |
| 9.8 | 1000BASE-T Half-Duplex | 1 = Advertise PHY is 1000BASE-T half-duplex capable<br>0 = Advertise PHY is not 1000BASE-T half-duplex capable | RW | Set by MODE[3:0] strapping pins.<br>See the Strapping Options - KSZ9031MNX section for details. |
| 9.7:0 | Reserved | Write as 0, ignore on read | RO | |
| **Register Ah – 1000BASE-T Status** | | | | |
| A.15 | Master-Slave Configuration Fault | 1 = Master-slave configuration fault detected<br>0 = No master-slave configuration fault detected | RO/LH/SC | 0 |
| A.14 | Master-Slave Configuration Resolution | 1 = Local PHY configuration resolved to master<br>0 = Local PHY configuration resolved to slave | RO | 0 |
| A.13 | Local Receiver Status | 1 = Local receiver OK (loc_rcvr_status = 1)<br>0 = Local receiver not OK (loc_rcvr_status = 0) | RO | 0 |
| A.12 | Remote Receiver Status | 1 = Remote receiver OK (rem_rcvr_status = 1)<br>0 = Remote receiver not OK (rem_rcvr_status = 0) | RO | 0 |
| A.11 | Link Partner 1000BASE-T Full-Duplex Capability | 1 = Link partner is capable of 1000BASE-T full-duplex<br>0 = Link partner is not capable of 1000BASE-T full-duplex | RO | 0 |
| A.10 | Link Partner 1000BASE-T Half-Duplex Capability | 1 = Link partner is capable of 1000BASE-T half-duplex<br>0 = Link Partner is not capable of 1000BASE-T half-duplex | RO | 0 |
| A.9:8 | Reserved | Reserved | RO | 00 |
| A.7:0 | Idle Error Count | Cumulative count of errors detected when receiver is receiving idles and PMA_TXMODE.indicate = SEND_N.<br>The counter is incremented every symbol period that rxerror_status = ERROR. | RO/SC | 0000_0000 |

**TABLE 4-3: IEEE-DEFINED REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode (Note 4-1) | Default |
|---|---|---|---|---|
| **Register Dh - MMD Access – Control** | | | | |
| D.15:14 | MMD – Operation Mode | For the selected MMD device address (Bits [4:0] of this register), these two bits select one of the following register or data operations and the usage for MMD Access – Register/Data (Reg. Eh).<br>00 = Register<br>01 = Data, no post increment<br>10 = Data, post increment on reads and writes<br>11 = Data, post increment on writes only | RW | 00 |
| D.13:5 | Reserved | Reserved | RW | 00_0000_000 |
| D.4:0 | MMD – Device Address | These five bits set the MMD device address. | RW | 0_0000 |
| **Register Eh - MMD Access – Register/Data** | | | | |
| E.15:0 | MMD – Register/ Data | For the selected MMD device address (Reg. Dh, Bits [4:0]),<br>When Reg. Dh, Bits [15:14] = 00, this register contains the read/write register address for the MMD device address.<br>Otherwise, this register contains the read/write data value for the MMD device address and its selected register address.<br>See also Reg. Dh, Bits [15:14], for descriptions of post increment reads and writes of this register for data operation. | RW | 0000_0000_0000_0000 |
| **Register Fh – Extended Status** | | | | |
| F.15 | 1000BASE-X Full-Duplex | 1 = PHY can perform 1000BASE-X full-duplex<br>0 = PHY cannot perform 1000BASE-X full-duplex | RO | 0 |
| F.14 | 1000BASE-X Half-Duplex | 1 = PHY can perform 1000BASE-X half-duplex<br>0 = PHY cannot perform 1000BASE-X half-duplex | RO | 0 |
| F.13 | 1000BASE-T Full-Duplex | 1 = PHY can perform 1000BASE-T full-duplex<br>0 = PHY cannot perform 1000BASE-T full-duplex | RO | 1 |
| F.12 | 1000BASE-T Half-Duplex | 1 = PHY can perform 1000BASE-T half-duplex<br>0 = PHY cannot perform 1000BASE-T half-duplex | RO | 1 |
| F.11:0 | Reserved | Ignore when read | RO | — |

**Note 4-1** RW = Read/Write; RO = Read Only; SC = Self-Cleared; LH = Latch High; LL = Latch Low.

**TABLE 4-4: VENDOR-SPECIFIC REGISTER DESCRIPTIONS**

| Address | Name | Description | Mode (Note 4-1) | Default |
|---|---|---|---|---|
| **Register 11h – Remote Loopback** | | | | |
| 11.15:9 | Reserved | Reserved | RW | 0000_000 |
| 11.8 | Remote Loopback | 1 = Enable remote loopback<br>0 = Disable remote loopback | RW | 0 |
| 11.7:1 | Reserved | Reserved | RW | 1111_010 |
| 11.0 | Reserved | Reserved | RO | 0 |

**TABLE 4-4: VENDOR-SPECIFIC REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode (Note 4-1) | Default |
|---|---|---|---|---|
| **Register 12h – LinkMD – Cable Diagnostic** | | | | |
| 12.15 | Cable Diagnostic Test Enable | Write value:<br>1 = Enable cable diagnostic test. After test has completed, this bit is self-cleared.<br>0 = Disable cable diagnostic test.<br>Read value:<br>1 = Cable diagnostic test is in progress.<br>0 = Indicates cable diagnostic test (if enabled) has completed and the status information is valid for read. | RW/SC | 0 |
| 12.14 | Reserved | This bit should always be set to '0'. | RW | 0 |
| 12.13:12 | Cable Diagnostic Test Pair | These two bits select the differential pair for testing:<br>00 = Differential pair A (Pins 2, 3)<br>01 = Differential pair B (Pins 7, 8)<br>10 = Differential pair C (Pins 10, 11)<br>11 = Differential pair D (Pins 14, 15) | RW | 00 |
| 12.11:10 | Reserved | These two bits should always be set to '00'. | RW | 00 |
| 12.9:8 | Cable Diagnostic Status | These two bits represent the test result for the selected differential pair in Bits [13:12] of this register.<br>00 = Normal cable condition (no fault detected)<br>01 = Open cable fault detected<br>10 = Short cable fault detected<br>11 = Reserved | RO | 00 |
| 12.7:0 | Cable Diagnostic Fault Data | For the open or short cable fault detected in Bits [9:8] of this register, this 8-bit value represents the distance to the cable fault. | RO | 0000_0000 |
| **Register 13h – Digital PMA/PCS Status** | | | | |
| 13.15:3 | Reserved | Reserved | RO/LH | 0000_0000_0000_0 |
| 13.2 | 1000BASE-T Link Status | 1000BASE-T link status<br>1 = Link status is OK<br>0 = Link status is not OK | RO | 0 |
| 13.1 | 100BASE-TX Link Status | 100BASE-TX link status<br>1 = Link status is OK<br>0 = Link status is not OK | RO | 0 |
| 13.0 | Reserved | Reserved | RO | 0 |
| **Register 15h – RXER Counter** | | | | |
| 15.15:0 | RXER Counter | Receive error counter for symbol error frames | RO/RC | 0000_0000_0000_0000 |
| **Register 1Bh – Interrupt Control/Status** | | | | |
| 1B.15 | Jabber Interrupt Enable | 1 = Enable jabber interrupt<br>0 = Disable jabber interrupt | RW | 0 |
| 1B.14 | Receive Error Interrupt Enable | 1 = Enable receive error interrupt<br>0 = Disable receive error interrupt | RW | 0 |
| 1B.13 | Page Received Interrupt Enable | 1 = Enable page received interrupt<br>0 = Disable page received interrupt | RW | 0 |

**TABLE 4-4: VENDOR-SPECIFIC REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode (Note 4-1) | Default |
|---|---|---|---|---|
| 1B.12 | Parallel Detect Fault Interrupt Enable | 1 = Enable parallel detect fault interrupt<br>0 = Disable parallel detect fault interrupt | RW | 0 |
| 1B.11 | Link Partner Acknowl-edge Inter-rupt Enable | 1 = Enable link partner acknowledge interrupt<br>0 = Disable link partner acknowledge interrupt | RW | 0 |
| 1B.10 | Link-Down Interrupt Enable | 1 = Enable link-down interrupt<br>0 = Disable link-down interrupt | RW | 0 |
| 1B.9 | Remote Fault Interrupt Enable | 1 = Enable remote fault interrupt<br>0 = Disable remote fault interrupt | RW | 0 |
| 1B.8 | Link-Up Interrupt Enable | 1 = Enable link-up interrupt<br>0 = Disable link-up interrupt | RW | 0 |
| 1B.7 | Jabber Inter-rupt | 1 = Jabber occurred<br>0 = Jabber did not occur | RO/RC | 0 |
| 1B.6 | Receive Error Inter-rupt | 1 = Receive error occurred<br>0 = Receive error did not occur | RO/RC | 0 |
| 1B.5 | Page Receive Interrupt | 1 = Page receive occurred<br>0 = Page receive did not occur | RO/RC | 0 |
| 1B.4 | Parallel Detect Fault Interrupt | 1 = Parallel detect fault occurred<br>0 = Parallel detect fault did not occur | RO/RC | 0 |
| 1B.3 | Link Partner Acknowl-edge Inter-rupt | 1 = Link partner acknowledge occurred<br>0 = Link partner acknowledge did not occur | RO/RC | 0 |
| 1B.2 | Link-Down Interrupt | 1 = Link-down occurred<br>0 = Link-down did not occur | RO/RC | 0 |
| 1B.1 | Remote Fault Interrupt | 1 = Remote fault occurred<br>0 = Remote fault did not occur | RO/RC | 0 |
| 1B.0 | Link-Up Interrupt | 1 = Link-up occurred<br>0 = Link-up did not occur | RO/RC | 0 |
| **Register 1Ch – Auto MDI/MDI-X** | | | | |
| 1C.15:8 | Reserved | Reserved | RW | 0000_0000 |
| 1C.7 | MDI Set | When Swap-Off (Bit [6] of this register) is asserted (1),<br>1 = PHY is set to operate as MDI mode<br>0 = PHY is set to operate as MDI-X mode<br>This bit has no function when Swap-Off is de-asserted (0). | RW | 0 |
| 1C.6 | Swap-Off | 1 = Disable Auto MDI/MDI-X function<br>0 = Enable Auto MDI/MDI-X function | RW | 0 |
| 1C.5:0 | Reserved | Reserved | RW | 00_0000 |

**TABLE 4-4: VENDOR-SPECIFIC REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode (Note 4-1) | Default |
|---|---|---|---|---|
| **Register 1Fh – PHY Control** | | | | |
| 1F.15 | Reserved | Reserved | RW | 0 |
| 1F.14 | Interrupt Level | 1 = Interrupt pin active high<br>0 = Interrupt pin active low | RW | 0 |
| 1F.13:12 | Reserved | Reserved | RW | 00 |
| 1F.11:10 | Reserved | Reserved | RO/LH/RC | 00 |
| 1F.9 | Enable Jabber | 1 = Enable jabber counter<br>0 = Disable jabber counter | RW | 1 |
| 1F.8:7 | Reserved | Reserved | RW | 00 |
| 1F.6 | Speed Status 1000BASE-T | 1 = Indicate chip final speed status at 1000BASE-T | RO | 0 |
| 1F.5 | Speed Status 100BASE-TX | 1 = Indicate chip final speed status at 100BASE-TX | RO | 0 |
| 1F.4 | Speed Status 10BASE-T | 1 = Indicate chip final speed status at 10BASE-T | RO | 0 |
| 1F.3 | Duplex Status | Indicate chip duplex status<br>1 = Full-duplex<br>0 = Half-duplex | RO | 0 |
| 1F.2 | 1000BASE-T Master/Slave Status | Indicate chip master/slave status<br>1 = 1000BASE-T master mode<br>0 = 1000BASE-T slave mode | RO | 0 |
| 1F.1 | Reserved | Reserved | RW | 0 |
| 1F.0 | Link Status Check Fail | 1 = Fail<br>0 = Not failing | RO | 0 |

**Note 4-1** RW = Read/Write; RO = Read Only; SC = Self-Cleared; LH = Latch High; LL = Latch Low.

## 4.3 MMD Registers

MMD registers provide indirect read/write access to up to 32 MMD device addresses with each device supporting up to 65,536 16-bit registers, as defined in Clause 22 of the IEEE 802.3 Specification. The KSZ9031MNX, however, uses only a small fraction of the available registers. See the Register Map section for a list of supported MMD device addresses and their associated register addresses.

The following two standard registers serve as the portal registers to access the indirect MMD registers.

- Standard register Dh – MMD Access – Control
- Standard register Eh – MMD Access – Register/Data

**TABLE 4-5: MMD PORTAL REGISTERS**

| Address | Name | Description | Mode (Note 4-1) | Default |
|---|---|---|---|---|
| **Register Dh - MMD Access – Control** | | | | |
| D.15:14 | MMD - Operation Mode | For the selected MMD device address (Bits [4:0] of this register), these two bits select one of the following register or data operations and the usage for MMD Access – Register/Data (Reg. Eh).<br>00 = Register<br>01 = Data, no post increment<br>10 = Data, post increment on reads and writes<br>11 = Data, post increment on writes only | RW | 00 |
| D.13:5 | Reserved | Reserved | RW | 00_0000_000 |
| D.4:0 | MMD – Device Address | These five bits set the MMD device address | RW | 0_0000 |
| **Register Eh - MMD Access – Register/Data** | | | | |
| E.15:0 | MMD – Register/ Data | For the selected MMD device address (Reg. Dh, Bits [4:0]),<br>When Reg. Dh, Bits [15:14] = 00, this register contains the read/write register address for the MMD device address.<br>Otherwise, this register contains the read/write data value for the MMD device address and its selected register address.<br>See also Register Dh, Bits [15:14] descriptions for post increment reads and writes of this register for data operation. | RW | 0000_0000_ 0000_0000 |

**Note 4-1** RW = Read/Write

**Example: MMD Register Write**

Write MMD - Device Address 2h, Register 10h = 0001h to enable link-up detection to trigger PME for WOL.

1. Write Register Dh with 0002h // Set up register address for MMD – Device Address 2h.
2. Write Register Eh with 0010h // Select Register 10h of MMD – Device Address 2h.
3. Write Register Dh with 4002h // Select register data for MMD – Device Address 2h, Register 10h.
4. Write Register Eh with 0001h // Write value 0001h to MMD – Device Address 2h, Register 10h.

**Example: MMD Register Read**

Read MMD - Device Address 2h, Register 11h – 13h for the magic packet's MAC address.

1. Write Register Dh with 0002h // Set up register address for MMD – Device Address 2h.
2. Write Register Eh with 0011h // Select Register 11h of MMD – Device Address 2h.
3. Write Register Dh with 8002h // Select register data for MMD – Device Address 2h, Register 11h.
4. Read Register Eh // Read data in MMD – Device Address 2h, Register 11h.
5. Read Register Eh // Read data in MMD – Device Address 2h, Register 12h.
6. Read Register Eh // Read data in MMD – Device Address 2h, Register 13h.

**TABLE 4-6: MMD REGISTER DESCRIPTIONS**

| Address | Name | Description | Mode (Note 4-1) | Default |
|---|---|---|---|---|
| **MMD Address 0h, Register 3h – AN FLP Burst Transmit – LO** | | | | |
| 0.3.15:0 | AN FLP Burst Transmit – LO | This register and the following register set the Auto-Negotiation FLP burst transmit timing. The same timing must be set for both registers.<br>0x4000 = Select 8 ms interval timing (default)<br>0x1A80 = Select 16 ms interval timing<br>All other values are reserved. | RW | 0x4000 |
| **MMD Address 0h, Register 4h – AN FLP Burst Transmit – HI** | | | | |
| 0.4.15:0 | AN FLP Burst Transmit – HI | This register and the previous register set the Auto-Negotiation FLP burst transmit timing. The same timing must be set for both registers.<br>0x0003 = Select 8 ms interval timing (default)<br>0x0006 = Select 16 ms interval timing<br>All other values are reserved. | RW | 0x0003 |
| **MMD Address 1h, Register 5Ah – 1000BASE-T Link-Up Time Control** | | | | |
| 1.5A.15:9 | Reserved | Reserved | RO | 0000_000 |
| 1.5A.8:4 | Reserved | Reserved | RW | 1_0000 |
| 1.5A.3:1 | 1000BASE-T Link-Up Time | When the link partner is another KSZ9031 device, the 1000BASE-T link-up time can be long. These three bits provide an optional setting to reduce the 1000BASE-T link-up time.<br>100 = Default power-up setting<br>011 = Optional setting to reduce link-up time when the link partner is a KSZ9031 device.<br>All other settings are reserved and should not be used.<br>The optional setting is safe to use with any link partner.<br>**Note:** Read/Write access to this register bit is available only when Reg. 0h is set to 0x2100 to disable auto-negotiation and force 100BASE-TX mode. | RW | 100 |
| 1.5A.0 | Reserved | Reserved | RW | 0 |
| **MMD Address 2h, Register 0h – Common Control** | | | | |
| 2.0.15:5 | Reserved | Reserved | RW | 0000_0000_000 |
| 2.0.4 | LED Mode Override | Override strap-in for LED_MODE<br>1 = Single-LED mode<br>0 = Tri-color dual-LED mode<br>This bit is write-only and always reads back a value of '0'. The updated value is reflected in Bit [3] of this register. | WO | 0 |
| 2.0.3 | LED Mode | LED_MODE Status<br>1 = Single-LED mode<br>0 = Tri-color dual-LED mode | RO | Set by LED_MODE strapping pin.<br>See the Strapping Options - KSZ9031MNX section for details.<br>Can be updated by Bit [4] of this register after reset. |
| 2.0.2 | Reserved | Reserved | RW | 0 |

**TABLE 4-6: MMD REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode (Note 4-1) | Default |
|---|---|---|---|---|
| 2.0.1 | CLK125_EN Status | Override strap-in for CLK125_EN<br>1 = CLK125_EN strap-in is enabled<br>0 = CLK125_EN strap-in is disabled | RW | Set by CLK125_EN strapping pin.<br>See the Strapping Options - KSZ9031MNX section for details. |
| 2.0.0 | Reserved | Reserved | RW | 0 |
| **MMD Address 2h, Register 1h – Strap Status** | | | | |
| 2.1.15:8 | Reserved | Reserved | RO | 0000_0000 |
| 2.1.7 | LED_MODE Strap-In Status | Strap to<br>1 = Single-LED mode<br>0 = Tri-color dual-LED mode | RO | Set by LED_MODE strapping pin.<br>See the Strapping Options - KSZ9031MNX section for details. |
| 2.1.6 | Reserved | Reserved | RO | 0 |
| 2.1.5 | CLK125_EN Strap-In Status | Strap to<br>1 = CLK125_EN strap-in is enabled<br>0 = CLK125_EN strap-in is disabled | RO | Set by CLK125_EN strapping pin.<br>See the Strapping Options - KSZ9031MNX section for details. |
| 2.1.4:3 | Reserved | Reserved | RO | 00 |
| 2.1.2:0 | PHYAD[2:0] Strap-In Value | Strap-in value for PHY address<br>Bits [4:3] of PHY address are always set to '00'. | RO | Set by PHYAD[2:0] strapping pin.<br>See the Strapping Options - KSZ9031MNX section for details. |
| **MMD Address 2h, Register 2h – Operation Mode Strap Override** | | | | |
| 2.2.15:11 | Reserved | Reserved | RW | 0000_0 |
| 2.2.10 | PME_N2 Output Enable | For INT_N/PME_N2 (Pin 53),<br>1 = Enable PME output<br>0 = Disable PME output<br>This bit works in conjunction with MMD Address 2h, Reg. 10h, Bits [15:14] to define the output for Pin 53. | RW | 0 |
| 2.2.9 | Reserved | Reserved | RW | 0 |
| 2.2.8 | PME_N1 Output Enable | For LED1/PME_N1 (Pin 19),<br>1 = Enable PME output<br>0 = Disable PME output<br>This bit works in conjunction with MMD Address 2h, Reg. 10h, Bits [15:14] to define the output for Pin 19. | RW | 0 |
| 2.2.7 | Chip Power-Down Over-ride | 1 = Override strap-in for chip power-down mode | RW | Set by MODE[3:0] strapping pin.<br>See the Strapping Options - KSZ9031MNX section for details. |
| 2.2.6:5 | Reserved | Reserved | RW | 00 |

**TABLE 4-6: MMD REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode (Note 4-1) | Default |
|---|---|---|---|---|
| 2.2.4 | NAND Tree Override | 1 = Override strap-in for NAND Tree mode | RW | Set by MODE[3:0] strapping pin. See the Strapping Options - KSZ9031MNX section for details. |
| 2.2.3:2 | Reserved | Reserved | RW | 00 |
| 2.2.1 | GMII/MII override | 1 = Override strap-in for GMII/MII mode | RW | Set by MODE[3:0] strapping pin. See the Strapping Options - KSZ9031MNX section for details. |
| 2.2.0 | Reserved | Reserved | RW | 0 |
| **MMD Address 2h, Register 3h – Operation Mode Strap Status** | | | | |
| 2.3.15:8 | Reserved | Reserved | RO | 0000_0000 |
| 2.3.7 | Chip Power-Down Strap-In Status | 1 = Strap to chip power-down mode | RO | Set by MODE[3:0] strapping pin. See the Strapping Options - KSZ9031MNX section for details. |
| 2.3.6:5 | Reserved | Reserved | RO | 00 |
| 2.3.4 | NAND Tree Strap-In Status | 1 = Strap to NAND Tree mode | RO | Set by MODE[3:0] strapping pin. See the Strapping Options - KSZ9031MNX section for details. |
| 2.3.3:2 | Reserved | Reserved | RO | 00 |
| 2.3.1 | GMII/MII Strap-In Status | 1 = Strap to GMII/MII mode | RO | Set by MODE[3:0] strapping pin. See the Strapping Options - KSZ9031MNX section for details. |
| 2.3.0 | Reserved | Reserved | RO | 0 |
| **MMD Address 2h, Register 4h – GMII Control Signal Pad Skew** | | | | |
| 2.4.15:8 | Reserved | Reserved | RW | 0000_0000 |
| 2.4.7:4 | RX_DV Pad Skew | GMII RX_DV output pad skew control (0.06 ns/step) | RW | 0111 |
| 2.4.3:0 | TX_EN Pad Skew | GMII TX_EN input pad skew control (0.06 ns/step) | RW | 0111 |
| **MMD Address 2h, Register 8h – GMII Clock Pad Skew** | | | | |
| 2.8.15:10 | Reserved | Reserved | RW | 0000_00 |
| 2.8.9:5 | GTX_CLK Pad Skew | GMII GTX_CLK input pad skew control (0.06 ns/step) | RW | 01_111 |
| 2.8.4:0 | RX_CLK Pad Skew | GMII RX_CLK output pad skew control (0.06 ns/step) | RW | 0_1111 |

**TABLE 4-6: MMD REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode (Note 4-1) | Default |
|---|---|---|---|---|
| **MMD Address 2h, Register 10h – Wake-On-LAN – Control** | | | | |
| 2.10.15:14 | PME Output Select | These two bits work in conjunction with MMD Address 2h, Reg. 2h, Bits [8] and [10] for PME_N1 and PME_N2 enable, to define the output for Pins 19 and 53, respectively.<br>LED1/PME_N1 (Pin 19)<br>00 = PME_N1 output only<br>01 = LED1 output only<br>10 = LED1 and PME_N1 output<br>11 = Reserved<br>INT_N/PME_N2 (Pin 53)<br>00 = PME_N2 output only<br>01 = INT_N output only<br>10 = INT_N and PME_N2 output<br>11 = Reserved | RW | 00 |
| 2.10.13:7 | Reserved | Reserved | RW | 00_0000_0 |
| 2.10.6 | Magic Packet Detect Enable | 1 = Enable magic-packet detection<br>0 = Disable magic-packet detection | RW | 0 |
| 2.10.5 | Custom-Packet Type 3 Detect Enable | 1 = Enable custom-packet, Type 3 detection<br>0 = Disable custom-packet, Type 3 detection | RW | 0 |
| 2.10.4 | Custom-Packet Type 2 Detect Enable | 1 = Enable custom-packet, Type 2 detection<br>0 = Disable custom-packet, Type 2 detection | RW | 0 |
| 2.10.3 | Custom-Packet Type 1 Detect Enable | 1 = Enable custom-packet, Type 1 detection<br>0 = Disable custom-packet, Type 1 detection | RW | 0 |
| 2.10.2 | Custom-Packet Type 0 Detect Enable | 1 = Enable custom-packet, Type 0 detection<br>0 = Disable custom-packet, Type 0 detection | RW | 0 |
| 2.10.1 | Link-Down Detect Enable | 1 = Enable link-down detection<br>0 = Disable link-down detection | RW | 0 |
| 2.10.0 | Link-Up Detect Enable | 1 = Enable link-up detection<br>0 = Disable link-up detection | RW | 0 |
| **MMD Address 2h, Register 11h – Wake-On-LAN – Magic Packet, MAC-DA-0** | | | | |
| 2.11.15:0 | Magic Packet MAC-DA-0 | This register stores the lower two bytes of the destination MAC address for the magic packet.<br>Bit [15:8] = Byte 2 (MAC Address [15:8])<br>Bit [7:0] = Byte 1 (MAC Address [7:0])<br>The upper four bytes of the destination MAC address are stored in the following two registers. | RW | 0000_0000_0000_0000 |

**TABLE 4-6: MMD REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode (Note 4-1) | Default |
|---|---|---|---|---|
| **MMD Address 2h, Register 12h – Wake-On-LAN – Magic Packet, MAC-DA-1** | | | | |
| 2.12.15:0 | Magic Packet MAC-DA-1 | This register stores the middle two bytes of the destination MAC address for the magic packet.<br>Bit [15:8] = Byte 4 (MAC Address [31:24])<br>Bit [7:0] = Byte 3 (MAC Address [23:16])<br>The lower two bytes and upper two bytes of the destination MAC address are stored in the previous and following registers, respectively. | RW | 0000_0000_0000_0000 |
| **MMD Address 2h, Register 13h – Wake-On-LAN – Magic Packet, MAC-DA-2** | | | | |
| 2.13.15:0 | Magic Packet MAC-DA-2 | This register stores the upper two bytes of the destination MAC address for the magic packet.<br>Bit [15:8] = Byte 6 (MAC Address [47:40])<br>Bit [7:0] = Byte 5 (MAC Address [39:32])<br>The lower four bytes of the destination MAC address are stored in the previous two registers. | RW | 0000_0000_0000_0000 |
| **MMD Address 2h, Register 14h – Wake-On-LAN – Customized Packet, Type 0, Expected CRC 0**<br>**MMD Address 2h, Register 16h – Wake-On-LAN – Customized Packet, Type 1, Expected CRC 0**<br>**MMD Address 2h, Register 18h – Wake-On-LAN – Customized Packet, Type 2, Expected CRC 0**<br>**MMD Address 2h, Register 1Ah – Wake-On-LAN – Customized Packet, Type 3, Expected CRC 0** | | | | |
| 2.14.15:0<br>2.16.15:0<br>2.18.15:0<br>2.1A.15:0 | Custom Packet Type X CRC 0 | This register stores the upper two bytes for the expected CRC.<br>Bit [15:8] = Byte 2 (CRC [15:8])<br>Bit [7:0] = Byte 1 (CRC [7:0])<br>The lower two bytes for the expected CRC are stored in the following register. | RW | 0000_0000_0000_0000 |
| **MMD Address 2h, Register 15h – Wake-On-LAN – Customized Packet, Type 0, Expected CRC 1**<br>**MMD Address 2h, Register 17h – Wake-On-LAN – Customized Packet, Type 1, Expected CRC 1**<br>**MMD Address 2h, Register 19h – Wake-On-LAN – Customized Packet, Type 2, Expected CRC 1**<br>**MMD Address 2h, Register 1Bh – Wake-On-LAN – Customized Packet, Type 3, Expected CRC 1** | | | | |
| 2.15.15:0<br>2.17.15:0<br>2.19.15:0<br>2.1B.15:0 | Custom Packet Type X CRC 1 | This register stores the lower two bytes for the expected CRC.<br>Bit [15:8] = Byte 4 (CRC [31:24])<br>Bit [7:0] = Byte 3 (CRC [23:16])<br>The upper two bytes for the expected CRC are stored in the previous register. | RW | 0000_0000_0000_0000 |
| **MMD Address 2h, Register 1Ch – Wake-On-LAN – Customized Packet, Type 0, Mask 0**<br>**MMD Address 2h, Register 20h – Wake-On-LAN – Customized Packet, Type 1, Mask 0**<br>**MMD Address 2h, Register 24h – Wake-On-LAN – Customized Packet, Type 2, Mask 0**<br>**MMD Address 2h, Register 28h – Wake-On-LAN – Customized Packet, Type 3, Mask 0** | | | | |
| 2.1C.15:0<br>2.20.15:0<br>2.24.15:0<br>2.28.15:0 | Custom Packet Type X Mask 0 | This register selects the bytes in the first 16 bytes of the packet (bytes 1 through 16) that will be used for CRC calculation.<br>For each bit in this register,<br>1 = Byte is selected for CRC calculation<br>0 = Byte is not selected for CRC calculation<br>The register-bit to packet-byte mapping is as follows:<br>Bit [15]: Byte 16<br>……<br>Bit [2]: Byte 2<br>Bit [0]: Byte 1 | RW | 0000_0000_0000_0000 |

**TABLE 4-6: MMD REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode (Note 4-1) | Default |
|---|---|---|---|---|
| **MMD Address 2h, Register 1Dh – Wake-On-LAN – Customized Packet, Type 0, Mask 1<br>MMD Address 2h, Register 21h – Wake-On-LAN – Customized Packet, Type 1, Mask 1<br>MMD Address 2h, Register 25h – Wake-On-LAN – Customized Packet, Type 2, Mask 1<br>MMD Address 2h, Register 29h – Wake-On-LAN – Customized Packet, Type 3, Mask 1** | | | | |
| 2.1D.15:0<br>2.21.15:0<br>2.25.15:0<br>2.29.15:0 | Custom Packet Type X Mask 1 | This register selects the bytes in the second 16 bytes of the packet (bytes 17 thru 32) that will be used for CRC calculation.<br>For each bit in this register,<br>1 = Byte is selected for CRC calculation<br>0 = Byte is not selected for CRC calculation<br>The register-bit to packet-byte mapping is as follows:<br>Bit [15]: Byte 32<br>……<br>Bit [2]: Byte 18<br>Bit [0]: Byte 17 | RW | 0000_0000_0000_0000 |
| **MMD Address 2h, Register 1Eh – Wake-On-LAN – Customized Packet, Type 0, Mask 2<br>MMD Address 2h, Register 22h – Wake-On-LAN – Customized Packet, Type 1, Mask 2<br>MMD Address 2h, Register 26h – Wake-On-LAN – Customized Packet, Type 2, Mask 2<br>MMD Address 2h, Register 2Ah – Wake-On-LAN – Customized Packet, Type 3, Mask 2** | | | | |
| 2.1E.15:0<br>2.22.15:0<br>2.26.15:0<br>2.2A.15:0 | Custom Packet Type X Mask 2 | This register selects the bytes in the third 16 bytes of the packet (bytes 33 through 48) that will be used for CRC calculation.<br>For each bit in this register,<br>1 = Byte is selected for CRC calculation<br>0 = Byte is not selected for CRC calculation<br>The register-bit to packet-byte mapping is as follows:<br>Bit [15]: Byte 48<br>……<br>Bit [2]: Byte 34<br>Bit [0]: Byte 33 | RW | 0000_0000_0000_0000 |
| **MMD Address 2h, Register 1Fh – Wake-On-LAN – Customized Packet, Type 0, Mask 3<br>MMD Address 2h, Register 23h – Wake-On-LAN – Customized Packet, Type 1, Mask 3<br>MMD Address 2h, Register 27h – Wake-On-LAN – Customized Packet, Type 2, Mask 3<br>MMD Address 2h, Register 2Bh – Wake-On-LAN – Customized Packet, Type 3, Mask 3** | | | | |
| 2.1F.15:0<br>2.23.15:0<br>2.27.15:0<br>2.2B.15:0 | Custom Packet Type X Mask 3 | This register selects the bytes in the fourth 16 bytes of the packet (bytes 49 through 64) that will be used for CRC calculation.<br>For each bit in this register,<br>1 = Byte is selected for CRC calculation<br>0 = Byte is not selected for CRC calculation<br>The register-bit to packet-byte mapping is as follows:<br>Bit [15]: Byte 64<br>……<br>Bit [2]: Byte 50<br>Bit [0]: Byte 49 | RW | 0000_0000_0000_0000 |
| **MMD Address 1Ch, Register 4h – Analog Control 4** | | | | |
| 1C.4.15:11 | Reserved | Reserved | RW | 0000_0 |
| 1C.4.10 | 10BASE-Te Mode | 1 = 10BASE-Te (1.75V TX amplitude)<br>0 = Standard 10BASE-T (2.5V TX amplitude) | RW | 0 |
| 1C.4.9:0 | Reserved | Reserved | RW | 00_1111_1111 |

**TABLE 4-6: MMD REGISTER DESCRIPTIONS (CONTINUED)**

| Address | Name | Description | Mode (Note 4-1) | Default |
|---|---|---|---|---|
| **MMD Address 1Ch, Register 23h – EDPD Control** | | | | |
| 1C.23.15:1 | Reserved | Reserved | RW | 0000_0000_0000_000 |
| 1C.23.0 | EDPD Mode Enable | Energy-detect power-down mode<br>1 = Enable<br>0 = Disable | RW | 0 |

**Note 4-1** RW = Read/Write;
RO = Read Only;
WO = Write Only;
LH = Latch High.

# 5.0 OPERATIONAL CHARACTERISTICS

## 5.1 Absolute Maximum Ratings*

Supply Voltage ($V_{IN}$)
(DVDDL, AVDDL, AVDDL_PLL) ..... –0.5V to +1.8V
(AVDDH) ..... –0.5V to +5.0V
(DVDDH) ..... –0.5V to +5.0V
Input Voltage (all inputs) ..... –0.5V to +5.0V
Output Voltage (all outputs) ..... –0.5V to +5.0V
Lead Temperature (soldering, 10s) ..... +260°C
Storage Temperature ($T_S$) ..... –55°C to +150°C

*Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

## 5.2 Operating Ratings**

Supply Voltage
(DVDDL, AVDDL, AVDDL_PLL) ..... +1.140V to +1.260V
(AVDDH @ 3.3V) ..... +3.135V to +3.465V
(AVDDH @ 2.5V; Commercial temp. only) ..... +2.375V to +2.625V
(DVDDH @ 3.3V) ..... +3.135V to +3.465V
(DVDDH @ 2.5V) ..... +2.375V to +2.625V
(DVDDH @ 1.8V) ..... +1.710V to +1.890V
Ambient Temperature
($T_A$ Commercial: KSZ9031MNXC) ..... 0°C to +70°C
($T_A$ Industrial: KSZ9031MNXI) ..... –40°C to +85°C
Maximum Junction Temperature ($T_J$ max.) ..... +125°C
Thermal Resistance ($\Theta_{JA}$) ..... +32.27°C/W
Thermal Resistance ($\Theta_{JC}$) ..... +6.76°C/W

**The device is not guaranteed to function outside its operating ratings.

| **Note:** | Do not drive input signals without power supplied to the device. |
|---|---|

## 6.0 ELECTRICAL CHARACTERISTICS

$T_A$ = 25°C. Specification is for packaged product only.

**TABLE 6-1: SUPPLY CURRENT - CORE/DIGITAL I/O**

| Parameters | Symbol | Min. | Typ. | Max. | Units | Note |
|---|---|---|---|---|---|---|
| 1.2V Total of: DVDDL (digital core) + AVDDL (analog core) + AVDDL_PLL (PLL) | $I_{CORE}$ | — | 211 | — | mA | 1000Base-T link-up (no traffic) |
| | | — | 221 | — | | 1000Base-T full-duplex @ 100% utilization |
| | | — | 60.6 | — | | 100Base-TX link-up (no traffic) |
| | | — | 61.2 | — | | 100Base-TX full-duplex @ 100% utilization |
| | | — | 7.0 | — | | 10Base-T link-up (no traffic) |
| | | — | 7.7 | — | | 10Base-T full-duplex @ 100% utilization |
| | | — | 0.9 | — | | Software power-down mode (Reg. 0.11 = 1) |
| | | — | 0.8 | — | | Chip power-down mode (strap-in pins MODE[3:0] = 0111) |
| 1.8V for Digital I/O (GMII/MII operating @ 1.8V) | $I_{DVDDH\_1.8}$ | — | 14.2 | — | mA | 1000Base-T link-up (no traffic) |
| | | — | 29.3 | — | | 1000Base-T full-duplex @ 100% utilization |
| | | — | 7.3 | — | | 100Base-TX link-up (no traffic) |
| | | — | 10.0 | — | | 100Base-TX full-duplex @ 100% utilization |
| | | — | 3.1 | — | | 10Base-T link-up (no traffic) |
| | | — | 6.0 | — | | 10Base-T full-duplex @ 100% utilization |
| | | — | 3.7 | — | | Software power-down mode (Reg. 0.11 = 1) |
| | | — | 0.2 | — | | Chip power-down mode (strap-in pins MODE[3:0] = 0111) |
| 2.5V for Digital I/O (GMII/MII operating @ 2.5V) | $I_{DVDDH\_2.5}$ | — | 19.3 | — | mA | 1000Base-T link-up (no traffic) |
| | | — | 40.5 | — | | 1000Base-T full-duplex @ 100% utilization |
| | | — | 10.0 | — | | 100Base-TX link-up (no traffic) |
| | | — | 13.7 | — | | 100Base-TX full-duplex @ 100% utilization |
| | | — | 4.3 | — | | 10Base-T link-up (no traffic) |
| | | — | 8.3 | — | | 10Base-T full-duplex @ 100% utilization |
| | | — | 5.3 | — | | Software power-down mode (Reg. 0.11 = 1) |
| | | — | 0.9 | — | | Chip power-down mode (strap-in pins MODE[3:0] = 0111) |

**TABLE 6-1: SUPPLY CURRENT - CORE/DIGITAL I/O (CONTINUED)**

| Parameters | Symbol | Min. | Typ. | Max. | Units | Note |
|---|---|---|---|---|---|---|
| 3.3V for Digital I/O (GMII/MII operating @ 3.3V) | $I_{DVDDH\_3.3}$ | — | 26.0 | — | mA | 1000Base-T link-up (no traffic) |
| | | — | 53.8 | — | | 1000Base-T full-duplex @ 100% utilization |
| | | — | 13.3 | — | | 100Base-TX link-up (no traffic) |
| | | — | 18.0 | — | | 100Base-TX full-duplex @ 100% utilization |
| | | — | 5.7 | — | | 10Base-T link-up (no traffic) |
| | | — | 11.1 | — | | 10Base-T full-duplex @ 100% utilization |
| | | — | 7.1 | — | | Software power-down mode (Reg. 0.11 = 1) |
| | | — | 2.1 | — | | Chip power-down mode (strap-in pins MODE[3:0] = 0111) |

**TABLE 6-2: SUPPLY CURRENT - TRANSCEIVER (Note 6-1)**

| Parameters | Symbol | Min. | Typ. | Max. | Units | Note |
|---|---|---|---|---|---|---|
| 2.5V for Transceiver (Recommended for commercial temperature range operation only) | $I_{AVDDH\_2.5}$ | — | 58.6 | — | mA | 1000Base-T link-up (no traffic) |
| | | — | 57.6 | — | | 1000Base-T full-duplex @ 100% utilization |
| | | — | 24.8 | — | | 100Base-TX link-up (no traffic) |
| | | — | 24.8 | — | | 100Base-TX full-duplex @ 100% utilization |
| | | — | 12.5 | — | | 10Base-T link-up (no traffic) |
| | | — | 25.8 | — | | 10Base-T full-duplex @ 100% utilization |
| | | — | 3.0 | — | | Software power-down mode (Reg. 0.11 = 1) |
| | | — | 0.02 | — | | Chip power-down mode (strap-in pins MODE[3:0] = 0111) |
| 3.3V for Transceiver Parameter | $I_{AVDDH\_3.3}$ | — | 66.6 | — | mA | 1000Base-T link-up (no traffic) |
| | | — | 65.6 | — | | 1000Base-T full-duplex @ 100% utilization |
| | | — | 28.7 | — | | 100Base-TX link-up (no traffic) |
| | | — | 28.7 | — | | 100Base-TX full-duplex @ 100% utilization |
| | | — | 17.0 | — | | 10Base-T link-up (no traffic) |
| | | — | 29.3 | — | | 10Base-T full-duplex @ 100% utilization |
| | | — | 4.1 | — | | Software power-down mode (Reg. 0.11 = 1) |
| | | — | 0.02 | — | | Chip power-down mode (strap-in pins MODE[3:0] = 0111) |

**Note 6-1** Equivalent to current draw through external transformer center taps for PHY transceivers with current-mode transmit drivers.

**TABLE 6-3: CMOS INPUTS**

| Parameters | Symbol | Min. | Typ. | Max. | Units | Note |
|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | 2.0 | — | — | V | DVDDH (digital I/O) = 3.3V |
| | | 1.5 | — | — | | DVDDH (digital I/O) = 2.5V |
| | | 1.1 | — | — | | DVDDH (digital I/O) = 1.8V |
| Input Low Voltage | $V_{IL}$ | — | — | 1.3 | V | DVDDH (digital I/O) = 3.3V |
| | | — | — | 1.0 | | DVDDH (digital I/O) = 2.5V |
| | | — | — | 0.7 | | DVDDH (digital I/O) = 1.8V |
| Input High Leakage Current | $I_{IHL}$ | –2.0 | — | 2.0 | µA | DVDDH = 3.3V and $V_{IH}$ = 3.3V<br>All digital input pins |
| Input Low Leakage Current | $I_{ILL}$ | –2.0 | — | 2.0 | µA | DVDDH = 3.3V and $V_{IL}$ = 0.0V<br>All digital input pins, except MDC, MDIO, RESET_N. |
| | | –120 | — | –40 | | DVDDH = 3.3V and $V_{IL}$ = 0.0V<br>MDC, MDIO, RESET_N pins with internal pull-ups |

**TABLE 6-4: CMOS OUTPUTS**

| Parameter | Symbol | Min. | Typ. | Max. | Units | Note |
|---|---|---|---|---|---|---|
| Output High Voltage | $V_{OH}$ | 2.7 | — | — | V | DVDDH (digital I/O) = 3.3V,<br>$I_{OH}$ (min) = 10mA<br>All digital output pins |
| | | 2.0 | — | — | | DVDDH (digital I/O) = 2.5V,<br>$I_{OH}$ (min) = 10mA<br>All digital output pins |
| | | 1.5 | — | — | | DVDDH (digital I/O) = 1.8V,<br>$I_{OH}$ (min) = 13mA<br>All digital output pins, except LED1, LED2 |
| Output Low Voltage | $V_{OL}$ | — | — | 0.3 | V | DVDDH (digital I/O) = 3.3V,<br>$I_{OL}$ (min) = 10mA<br>All digital output pins |
| | | — | — | 0.3 | | DVDDH (digital I/O) = 2.5V,<br>$I_{OL}$ (min) = 10mA<br>All digital output pins |
| | | — | — | 0.3 | | DVDDH (digital I/O) = 1.8V,<br>$I_{OL}$ (min) = 13mA<br>All digital output pins, except LED1, LED2 |
| Output Tri-State Leakage | $\|I_{oz}\|$ | — | — | 10 | µA | — |

**TABLE 6-5: LED OUTPUTS**

| Parameters | Symbol | Min. | Typ. | Max. | Units | Note |
|---|---|---|---|---|---|---|
| Output Drive Current | $I_{LED}$ | 10 | — | — | mA | DVDDH (digital I/O) = 3.3V or 2.5V,<br>and $V_{OL}$ at 0.3V<br>Each LED pin (LED1, LED2) |

**TABLE 6-6: PULL-UP PINS**

| Parameters | Symbol | Min. | Typ. | Max. | Units | Note |
|---|---|---|---|---|---|---|
| Internal Pull-Up Resistance (MDC, MDIO, RESET_N pins) | pu | 13 | 22 | 31 | kΩ | DVDDH (digital I/O) = 3.3V |
| | | 16 | 28 | 39 | | DVDDH (digital I/O) = 2.5V |
| | | 26 | 44 | 62 | | DVDDH (digital I/O) = 1.8V |

**TABLE 6-7: 100BASE-TX TRANSMIT (Note 6-1)**

| Parameters | Symbol | Min. | Typ. | Max. | Units | Note |
|---|---|---|---|---|---|---|
| Peak Differential Output Voltage | $V_O$ | 0.95 | — | 1.05 | V | 100Ω termination across differential output |
| Output Voltage Imbalance | $V_{IMB}$ | — | — | 2 | % | 100Ω termination across differential output |
| Rise/Fall Time | $t_r$, $t_f$ | 3 | — | 5 | ns | — |
| Rise/Fall Time Imbalance | — | 0 | — | 0.5 | ns | — |
| Duty Cycle Distortion | — | — | — | ±0.25 | ns | — |
| Overshoot | — | — | — | 5 | % | — |
| Output Jitter | — | — | 0.7 | — | ns | Peak-to-peak |

**Note 6-1** Measured differentially after 1:1 transformer.

**TABLE 6-8: 10BASE-T TRANSMIT (Note 6-1)**

| Parameters | Symbol | Min. | Typ. | Max. | Units | Note |
|---|---|---|---|---|---|---|
| Peak Differential Output Voltage | $V_P$ | 2.2 | — | 2.8 | V | 100Ω termination across differential output |
| Jitter Added | — | — | — | 3.5 | ns | Peak-to-peak |
| Harmonic Rejection | — | — | –31 | — | dB | Transmit all-one signal sequence |

**Note 6-1** Measured differentially after 1:1 transformer.

**TABLE 6-9: 10BASE-T RECEIVE**

| Parameters | Symbol | Min. | Typ. | Max. | Units | Note |
|---|---|---|---|---|---|---|
| Squelch Threshold | $V_{SQ}$ | 300 | 400 | — | mV | 5 MHz square wave |

**TABLE 6-10: TRANSMITTER - DRIVE SETTING**

| Parameters | Symbol | Min. | Typ. | Max. | Units | Note |
|---|---|---|---|---|---|---|
| Reference Voltage of $I_{SET}$ | $V_{SET}$ | — | 1.2 | — | V | R($I_{SET}$) = 12.1 kΩ |

**TABLE 6-11: LDO CONTROLLER - DRIVE RANGE**

| Parameters | Symbol | Min. | Typ. | Max. | Units | Note |
|---|---|---|---|---|---|---|
| Output drive range for LDO_O (Pin 58) to gate input of P-channel MOSFET | $V_{LDO\_O}$ | 0.85 | — | 2.8 | V | AVDDH = 3.3V for MOSFET source voltage |
| | | 0.85 | — | 2.0 | | AVDDH = 2.5V for MOSFET source voltage (recommended for commercial temperature range operation only) |

## 7.0 TIMING DIAGRAMS

**FIGURE 7-1: GMII TRANSMIT TIMING - DATA INPUT TO PHY**

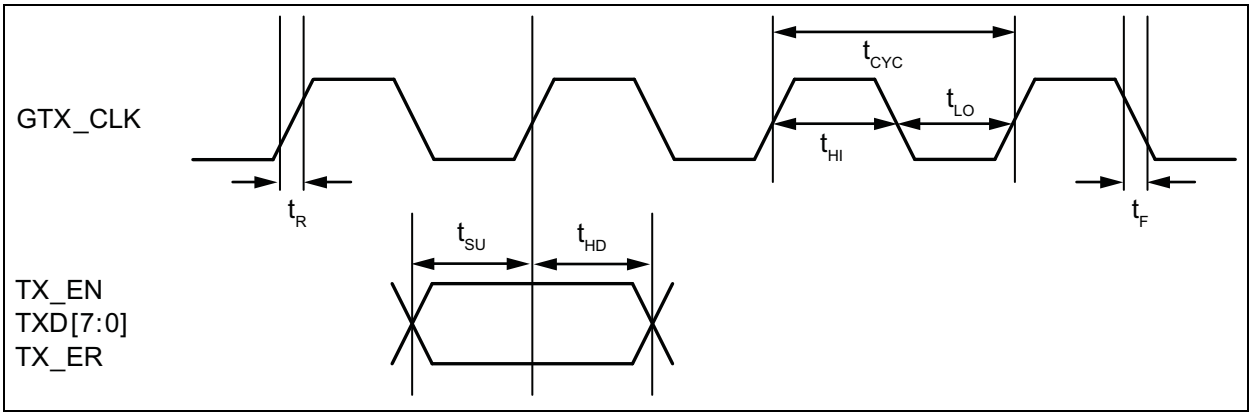



**TABLE 7-1: GMII TRANSMIT TIMING PARAMETERS**

| Timing Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **1000BASE-T** | | | | | |
| $t_{CYC}$ | GTX_CLK period | 7.5 | 8.0 | 8.5 | ns |
| $t_{SU}$ | TX_EN, TXD[7:0], TX_ER setup time to rising edge of GTX_CLK | 2.0 | — | — | |
| $t_{HD}$ | TX_EN, TXD[7:0], TX_ER hold time from rising edge of GTX_CLK | 0 | — | — | |
| $t_{HI}$ | GTX_CLK high pulse width | 2.5 | — | — | |
| $t_{LO}$ | GTX_CLK low pulse width | 2.5 | — | — | |
| $t_R$ | GTX_CLK rise time | — | — | 1.0 | |
| $t_F$ | GTX_CLK fall time | — | — | 1.0 | |

**FIGURE 7-2: GMII RECEIVE TIMING - DATA INPUT TO MAC**

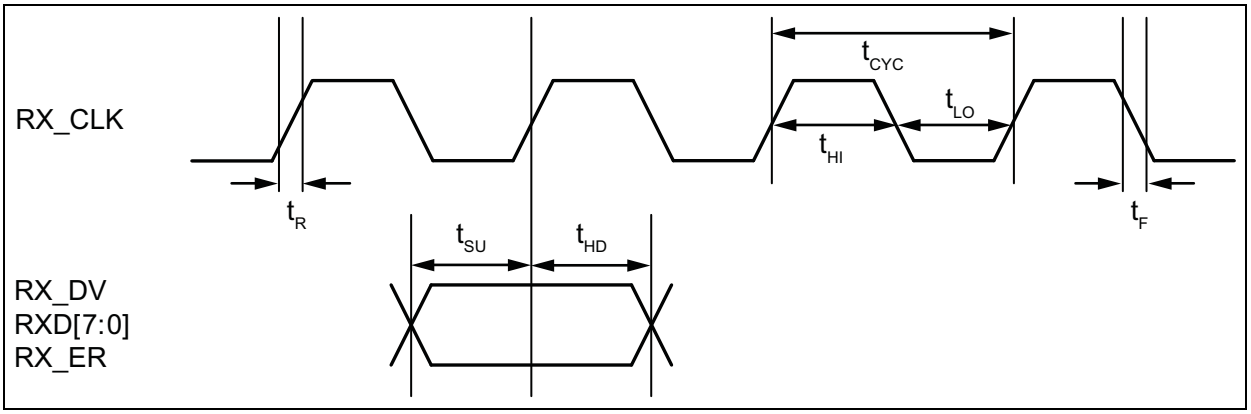



**TABLE 7-2: GMII RECEIVE TIMING PARAMETERS**

| Timing Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **1000BASE-T** | | | | | |
| $t_{CYC}$ | RX_CLK period | 7.5 | 8.0 | 8.5 | ns |
| $t_{SU}$ | RX_EN, RXD[7:0], RX_ER setup time to rising edge of RX_CLK | 2.5 | — | — | |
| $t_{HD}$ | RX_EN, RXD[7:0], RX_ER hold time from rising edge of RX_CLK | 0.5 | — | — | |
| $t_{HI}$ | RX_CLK high pulse width | 2.5 | — | — | |
| $t_{LO}$ | RX_CLK low pulse width | 2.5 | — | — | |
| $t_R$ | RX_CLK rise time | — | — | 1.0 | |
| $t_F$ | RX_CLK fall time | — | — | 1.0 | |

**FIGURE 7-3: MII TRANSMIT TIMING - DATA INPUT TO PHY**

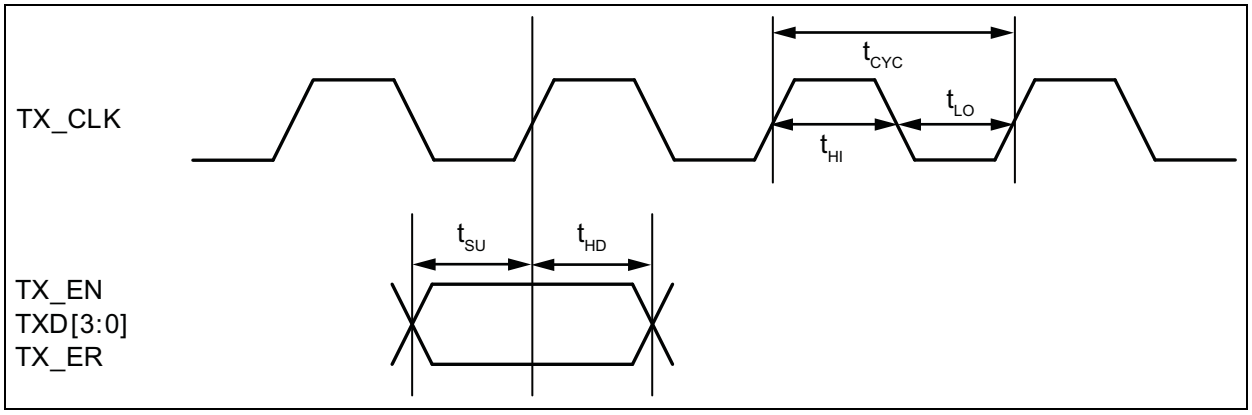



**TABLE 7-3: MII TRANSMIT TIMING PARAMETERS**

| Timing Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **10BASE-T** | | | | | |
| $t_{CYC}$ | TX_CLK period | — | 400 | — | ns |
| $t_{SU}$ | TX_EN, TXD[3:0], TX_ER setup time to rising edge of TX_CLK | 15 | — | — | |
| $t_{HD}$ | TX_EN, TXD[3:0], TX_ER hold time from rising edge of TX_CLK | 0 | — | — | |
| $t_{HI}$ | TX_CLK high pulse width | 140 | — | 260 | |
| $t_{LO}$ | TX_CLK low pulse width | 140 | — | 260 | |
| **100BASE-TX** | | | | | |
| $t_{CYC}$ | TX_CLK period | — | 40 | — | ns |
| $t_{SU}$ | TX_EN, TXD[3:0], TX_ER setup time to rising edge of TX_CLK | 15 | — | — | |
| $t_{HD}$ | TX_EN, TXD[3:0], TX_ER hold time from rising edge of TX_CLK | 0 | — | — | |
| $t_{HI}$ | TX_CLK high pulse width | 14 | — | 26 | |
| $t_{LO}$ | TX_CLK low pulse width | 14 | — | 26 | |

**FIGURE 7-4: MII RECEIVE TIMING - DATA INPUT TO MAC**

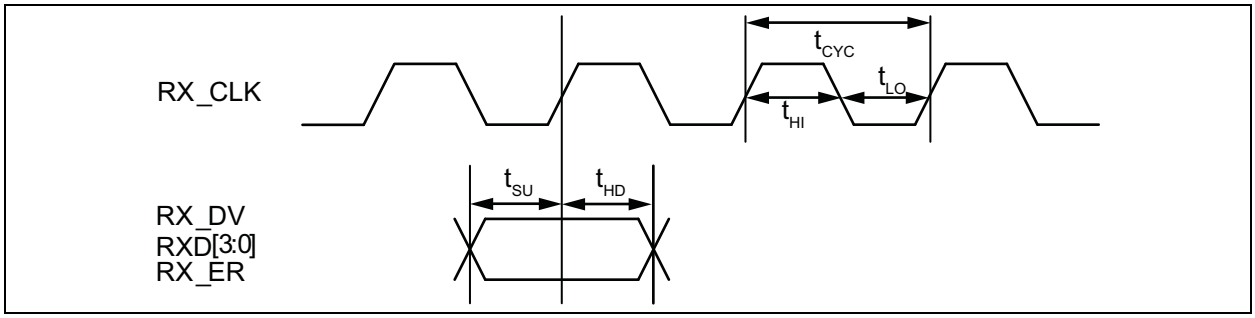



**TABLE 7-4: MII RECEIVE TIMING PARAMETERS**

| Timing Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **10BASE-T** | | | | | |
| $t_{CYC}$ | RX_CLK period | — | 400 | — | ns |
| $t_{SU}$ | RX_DV, RXD[3:0], RX_ER setup time to rising edge of RX_CLK | 10 | — | — | |
| $t_{HD}$ | RX_DV, RXD[3:0], RX_ER hold time from rising edge of RX_CLK | 10 | — | — | |
| $t_{HI}$ | RX_CLK high pulse width | 140 | — | 260 | |
| $t_{LO}$ | RX_CLK low pulse width | 140 | — | 260 | |
| **100BASE-TX** | | | | | |
| $t_{CYC}$ | RX_CLK period | — | 40 | — | ns |
| $t_{SU}$ | RX_DV, RXD[3:0], RX_ER setup time to rising edge of RX_CLK | 10 | — | — | |
| $t_{HD}$ | RX_DV, RXD[3:0], RX_ER hold time from rising edge of RX_CLK | 10 | — | — | |
| $t_{HI}$ | RX_CLK high pulse width | 14 | — | 26 | |
| $t_{LO}$ | RX_CLK low pulse width | 14 | — | 26 | |

**FIGURE 7-5: AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING**

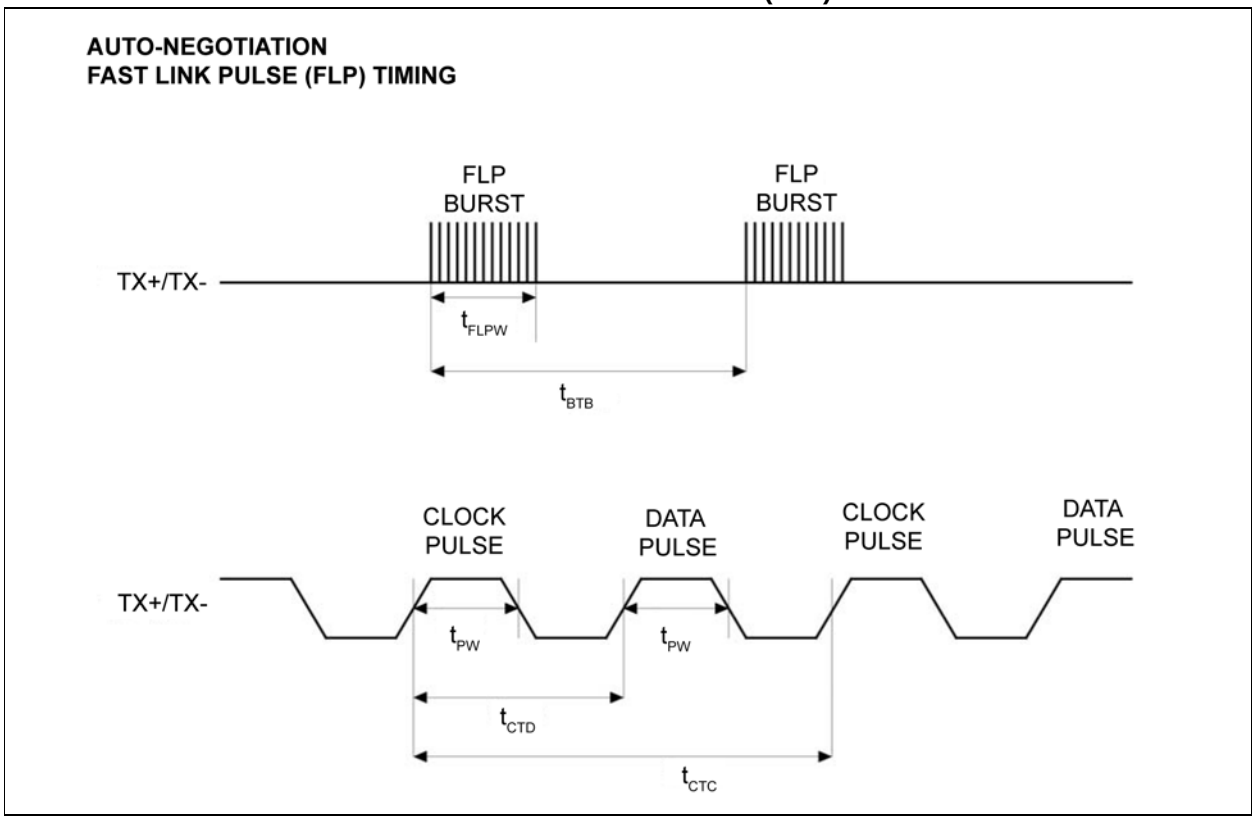



**TABLE 7-5: AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING PARAMETERS**

| Timing Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{BTB}$ | FLP burst to FLP burst | 8 | 16 | 24 | ms |
| $t_{FLPW}$ | FLP burst width | — | 2 | — | |
| $t_{PW}$ | Clock/Data pulse width | — | 100 | — | ns |
| $t_{CTD}$ | Clock pulse to data pulse | 55.5 | 64 | 69.5 | µs |
| $t_{CTC}$ | Clock pulse to clock pulse | 111 | 128 | 139 | |
| — | Number of clock/data pulses per FLP burst | 17 | — | 33 | — |

The KSZ9031MNX Fast Link Pulse (FLP) burst-to-burst transmit timing for Auto-Negotiation defaults to 8 ms. IEEE 802.3 Standard specifies this timing to be 16 ms ±8 ms. Some PHY link partners need to receive the FLP with 16 ms centered timing; otherwise, there can be intermittent link failures and long link-up times.

After KSZ9031MNX power-up/reset, program the following register sequence to set the FLP timing to 16 ms:

1. Write Register Dh = 0x0000 // Set up register address for MMD – Device Address 0h
2. Write Register Eh = 0x0004 // Select Register 4h of MMD – Device Address 0h
3. Write Register Dh = 0x4000 // Select register data for MMD – Device Address 0h, Register 4h
4. Write Register Eh = 0x0006 // Write value 0x0006 to MMD – Device Address 0h, Register 4h
5. Write Register Dh = 0x0000 // Set up register address for MMD – Device Address 0h
6. Write Register Eh = 0x0003 // Select Register 3h of MMD – Device Address 0h
7. Write Register Dh = 0x4000 // Select register data for MMD – Device Address 0h, Register 3h
8. Write Register Eh = 0x1A80 // Write value 0x1A80 to MMD – Device Address 0h, Register 3h
9. Write Register 0h, Bit [9] = 1 // Restart Auto-Negotiation

The above setting for 16 ms FLP transmit timing is compatible with all PHY link partners.

**FIGURE 7-6: MDC/MDIO TIMING**

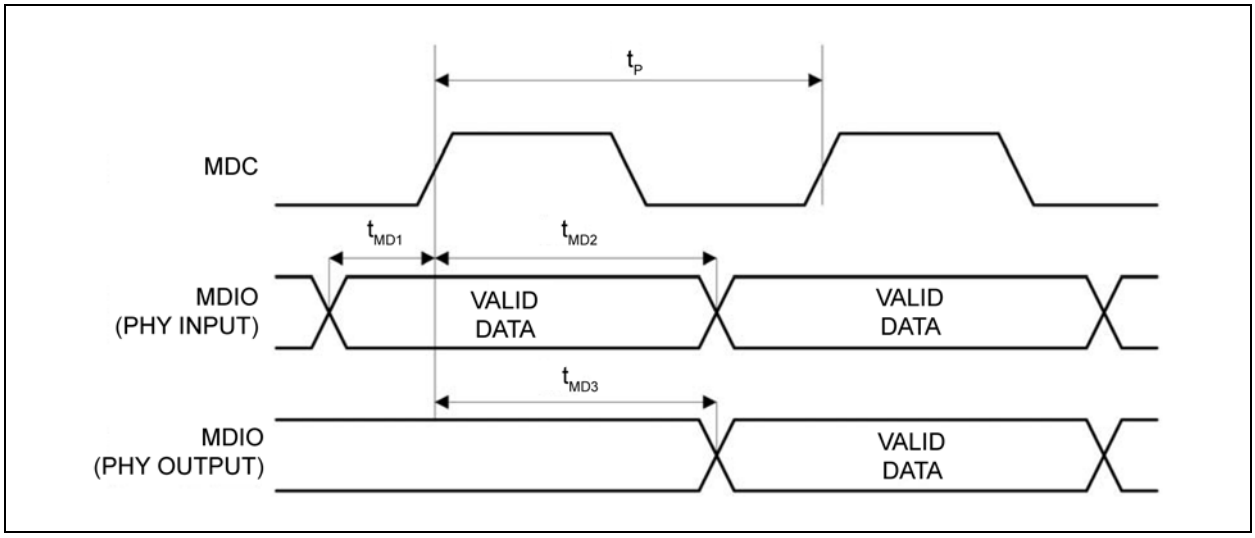


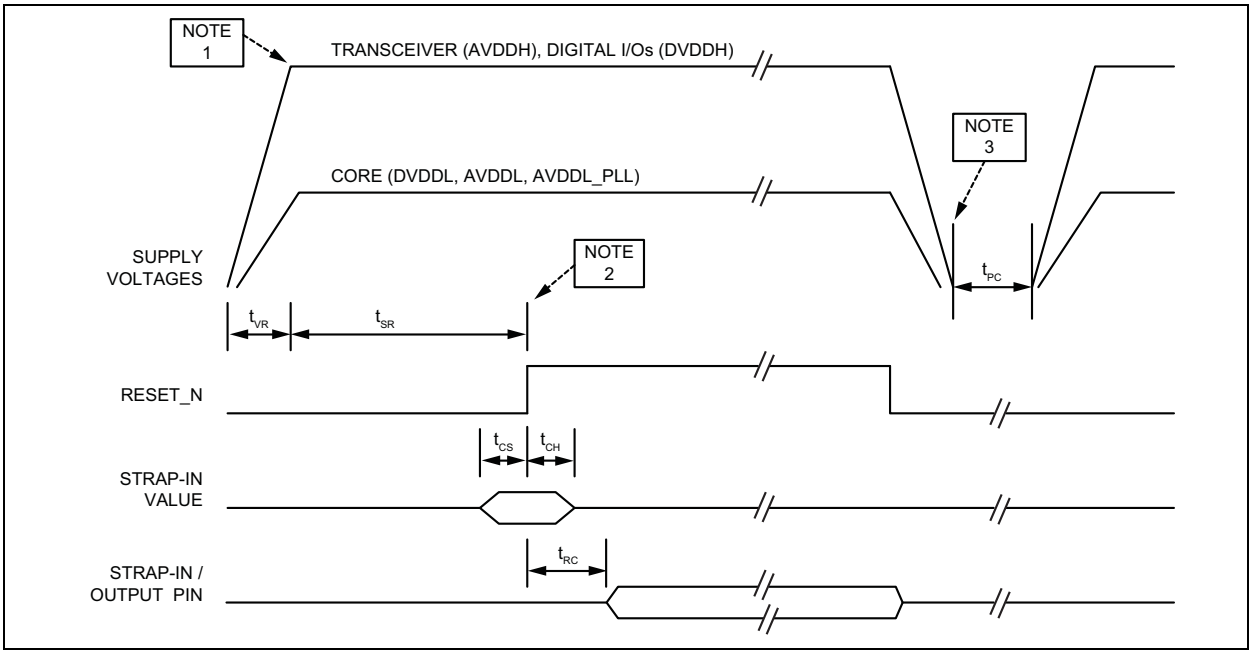

**TABLE 7-6: MDC/MDIO TIMING PARAMETERS**

| Timing Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_P$ | MDC period | 120 | 400 | — | ns |
| $t_{MD1}$ | MDIO (PHY input) setup to rising edge of MDC | 10 | — | — | |
| $t_{MD2}$ | MDIO (PHY input) hold from rising edge of MDC | 10 | — | — | |
| $t_{MD3}$ | MDIO (PHY output) delay from rising edge of MDC | 0 | — | — | |

The typical MDC clock frequency is 2.5 MHz (400 ns clock period).

The KSZ9031MNX can operate with MDC clock frequencies generated from bit banging with GPIO pin in the 10s/100s of Hertz and have been tested up to a MDC clock frequency of 8.33 MHz (120 ns clock period). Test condition for 8.33 MHz is for one KSZ9031MNX PHY on the MDIO line with a 1.0 kΩ pull-up to the DVDDH supply rail.

**FIGURE 7-7: POWER-UP/POWER-DOWN/RESET TIMING**




**Note 1:** The recommended power-up sequence is to have the transceiver (AVDDH) and digital I/O (DVDDH) voltages power up before the 1.2V core (DVDDL, AVDDL, AVDDL_PLL) voltage. If the 1.2V core must power up first, the maximum lead time for the 1.2V core voltage with respect to the transceiver and digital I/O voltages should be 200 µs.

There is no power sequence requirement between transceiver (AVDDH) and digital I/O (DVDDH) power rails.

The power-up waveforms should be monotonic for all supply voltages to the KSZ9031MNX.

**Note 2:** After the de-assertion of reset, wait a minimum of 100 µs before starting programming on the MIIM (MDC/MDIO) interface.

**Note 3:** The recommended power-down sequence is to have the 1.2V core voltage power-down before powering down the transceiver and digital I/O voltages.

Before the next power-up cycle, all supply voltages to the KSZ9031MNX should reach less than 0.4V and there should be a minimum wait time of 150 ms from power-off to power-on.

**TABLE 7-7: POWER-UP/POWER-DOWN/RESET TIMING PARAMETERS**

| Timing Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{VR}$ | Supply voltages rise time (must be monotonic) | 200 | — | — | µs |
| $t_{SR}$ | Stable supply voltages to de-assertion of reset | 10 | — | — | ms |
| $t_{CS}$ | Strap-in pin configuration setup time | 5 | — | — | ns |
| $t_{CH}$ | Strap-in pin configuration hold time | 5 | — | — | |
| $t_{RC}$ | De-assertion of reset to strap-in pin output | 6 | — | — | |
| $t_{PC}$ | Supply voltages cycle off-to-on time | 150 | — | — | ms |

## 8.0 RESET CIRCUIT

The following are some reset circuit suggestions.

Figure 8-1 illustrates the reset circuit for powering up the KSZ9031MNX if reset is triggered by the power supply.

**FIGURE 8-1: RESET CIRCUIT IF TRIGGERED BY THE POWER SUPPLY**

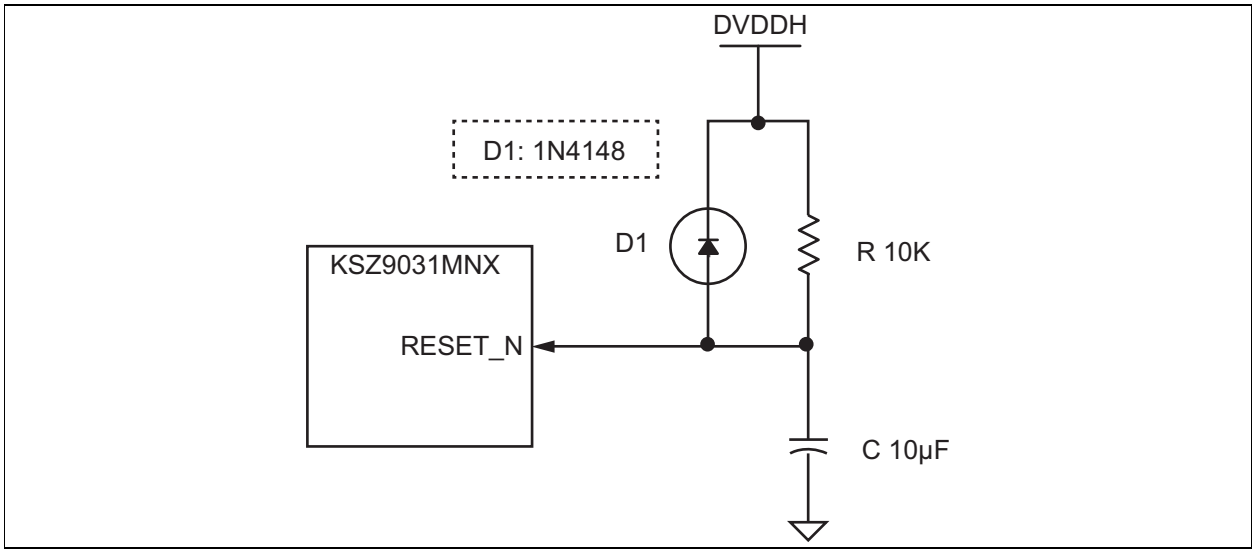



Figure 8-2 illustrates the reset circuit for applications where reset is driven by another device (for example, the CPU or an FPGA). At power-on-reset, R, C, and D1 provide the monotonic rise time to reset the KSZ9031MNX device. The RST_OUT_N from the CPU/FPGA provides the warm reset after power-up.

The KSZ9031MNX and CPU/FPGA references the same digital I/O voltage (DVDDH).

**FIGURE 8-2: RECOMMENDED RESET CIRCUIT FOR CPU/FPGA RESET OUTPUT**

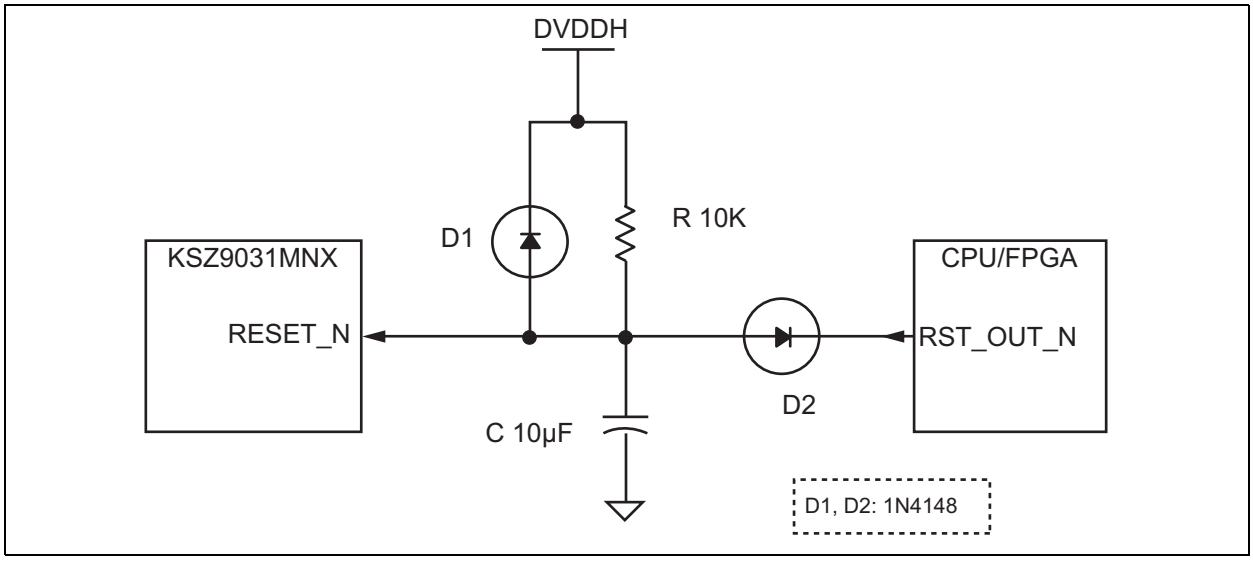
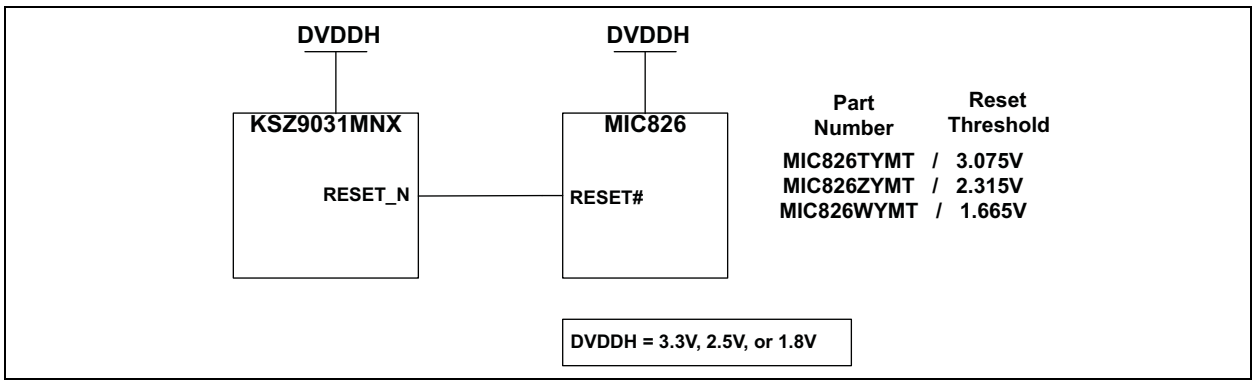



Figure 8-3 illustrates the reset circuit with an MIC826 voltage supervisor driving the KSZ9031MNX reset input.

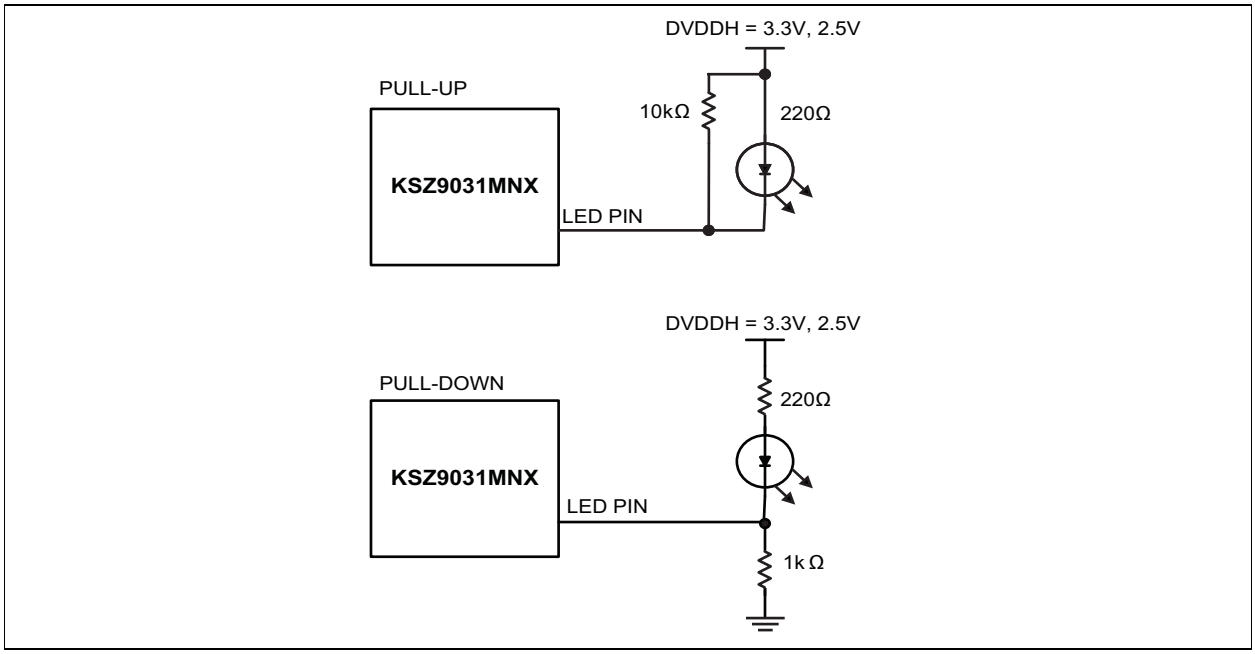
**FIGURE 8-3: RESET CIRCUIT WITH MIC826 VOLTAGE SUPERVISOR**



## 9.0 REFERENCE CIRCUITS — LED STRAP-IN PINS

The pull-up and pull-down reference circuits for the LED2/PHYAD1 and LED1/PHYAD0 strapping pins are shown in Figure 9-1 for 3.3V and 2.5V DVDDH.

**FIGURE 9-1: REFERENCE CIRCUITS FOR LED STRAPPING PINS**




For 1.8V DVDDH, LED indication support requires voltage level shifters between LED[2:1] pins and LED indicator diodes to ensure the multiplexed PHYAD[1:0] strapping pins are latched in high/low correctly. If LED indicator diodes are not implemented, the PHYAD[1:0] strapping pins just need 10 kΩ pull-up to 1.8V DVDDH for a value of 1, and 1.0 kΩ pull-down to ground for a value of 0.

## 10.0 REFERENCE CLOCK - CONNECTION AND SELECTION

A crystal or external clock source, such as an oscillator, is used to provide the reference clock for the KSZ9031MNX. The reference clock is 25 MHz for all operating modes of the KSZ9031MNX.

The KSZ9031MNX uses the AVDDH supply, analog 3.3V (or analog 2.5V option for commercial temperature only), for the crystal/ clock pins (XI, XO). If the 25 MHz reference clock is provided externally, the XI input pin should have a minimum clock voltage peak-to-peak ($V_{PP}$) swing of 2.5V reference to ground. If $V_{PP}$ is less than 2.5V, series capacitive coupling is recommended. With capacitive coupling, the $V_{PP}$ swing can be down to 1.5V. Maximum $V_{PP}$ swing is 3.3V +5%.

Figure 10-1 and Table 10-1 show the reference clock connection to XI (Pin 61) and XO (Pin 60) of the KSZ9031MNX, and the reference clock selection criteria.

**FIGURE 10-1: 25 MHZ CRYSTAL/OSCILLATOR REFERENCE CLOCK CONNECTION**

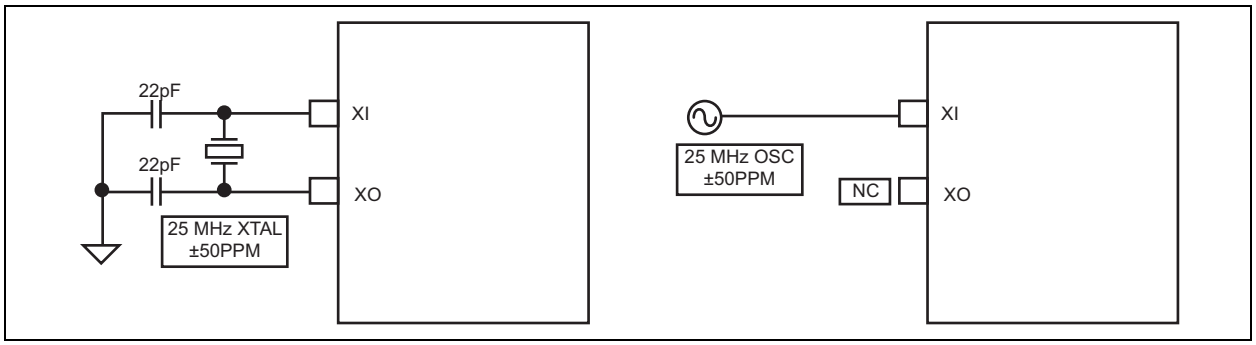



**TABLE 10-1: 25 MHZ CRYSTAL/REFERENCE CLOCK SELECTION CRITERIA**

| Characteristics | Value |
|---|---|
| Frequency | 25 MHz |
| Frequency Tolerance (max.) | ±50 ppm |
| Crystal Series Resistance (typ.) | 40Ω |
| Total Period Jitter (peak-to-peak) | <100 ps |

## 11.0 ON-CHIP LDO CONTROLLER - MOSFET SELECTION

If the optional LDO controller is used to generate 1.2V for the core voltage, the selected MOSFET should exceed the following minimum requirements:

- P-channel
- 500 mA (continuous current)
- 3.3V or 2.5V (source – input voltage)
- 1.2V (drain – output voltage)
- $V_{GS}$ in the range of:
  - (–1.2V to –1.5V) @ 500 mA for 3.3V source voltage
  - (–1.0V to –1.1V) @ 500 mA for 2.5V source voltage

The $V_{GS}$ for the MOSFET needs to be operating in the constant current saturated region, and not towards the $V_{GS(th)}$, the threshold voltage for the cut-off region of the MOSFET.

See Table 6-11 for LDO controller output driving range to the gate input of the MOSFET.

Refer to application note ANLAN206 – KSZ9031 Gigabit PHY Optimized Power Scheme for High Efficiency, Low-Power Consumption and Dissipation as a design reference.

## 12.0 MAGNETIC - CONNECTION AND SELECTION

A 1:1 isolation transformer is required at the line interface. Use one with integrated common-mode chokes for designs exceeding FCC requirements. An optional auto-transformer stage following the chokes provides additional common-mode noise and signal attenuation.

The KSZ9031MNX design incorporates voltage-mode transmit drivers and on-chip terminations.

With the voltage-mode implementation, the transmit drivers supply the common-mode voltages to the four differential pairs. Therefore, the four transformer center tap pins on the KSZ9031MNX side should not be connected to any power supply source on the board; rather, the center tap pins should be separated from one another and connected through separate 0.1 µF common-mode capacitors to ground. Separation is required because the common-mode voltage could be different between the four differential pairs, depending on the connected speed mode.

Figure 12-1 shows the typical gigabit magnetic interface circuit for the KSZ9031MNX.

**FIGURE 12-1: TYPICAL GIGABIT MAGNETIC INTERFACE CIRCUIT**

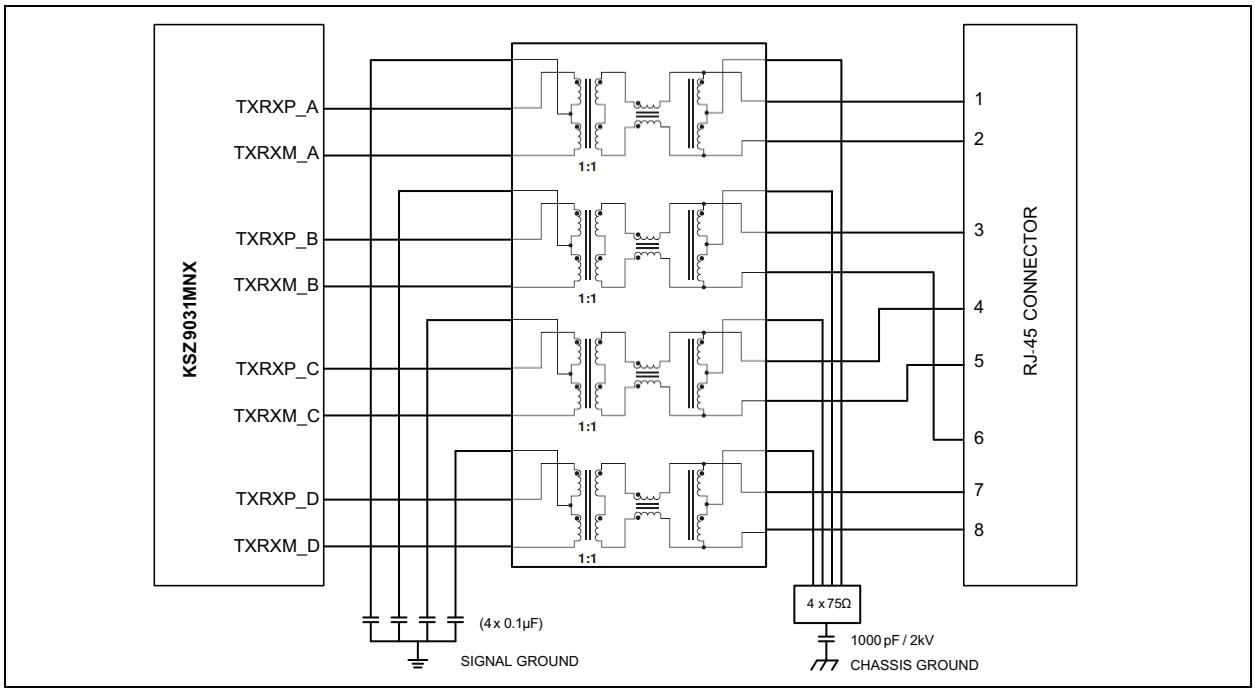



Table 12-1 lists recommended magnetic characteristics.

**TABLE 12-1: MAGNETICS SELECTION CRITERIA**

| Parameter | Value | Test Conditions |
|---|---|---|
| Turns Ratio | 1 CT : 1 CT | — |
| Open-Circuit Inductance (min.) | 350 µH | 100 mV, 100 kHz, 8 mA |
| Insertion Loss (max.) | 1.0 dB | 0 MHz to 100 MHz |
| HIPOT (min.) | 1500 $V_{RMS}$ | — |

Table 12-2 is a list of compatible single-port magnetics with separated transformer center tap pins on the G-PHY chip side that can be used with the KSZ9031MNX.

**TABLE 12-2: COMPATIBLE SINGLE-PORT 10/100/1000 MAGNETICS**

| Manufacturer | Part Number | Auto-Transformer | Temperature Range | Magnetic + RJ-45 |
|---|---|---|---|---|
| Bel Fuse | 0826-1G1T-23-F | Yes | 0°C to 70°C | Yes |
| HALO | TG1G-E001NZRL | No | –40°C to 85°C | No |

**TABLE 12-2: COMPATIBLE SINGLE-PORT 10/100/1000 MAGNETICS (CONTINUED)**

| Manufacturer | Part Number | Auto-Transformer | Temperature Range | Magnetic + RJ-45 |
|---|---|---|---|---|
| HALO | TG1G-S001NZRL | No | 0°C to 70°C | No |
| HALO | TG1G-S002NZRL | Yes | 0°C to 70°C | No |
| Pulse | H5007NL | Yes | 0°C to 70°C | No |
| Pulse | H5062NL | Yes | 0°C to 70°C | No |
| Pulse | HX5008NL | Yes | –40°C to 85°C | No |
| Pulse | JK0654219NL | Yes | 0°C to 70°C | Yes |
| Pulse | JK0-0136NL | No | 0°C to 70°C | Yes |
| TDK | TLA-7T101LF | No | 0°C to 70°C | No |
| Wurth/Midcom | 000-7093-37R-LF1 | Yes | 0°C to 70°C | No |

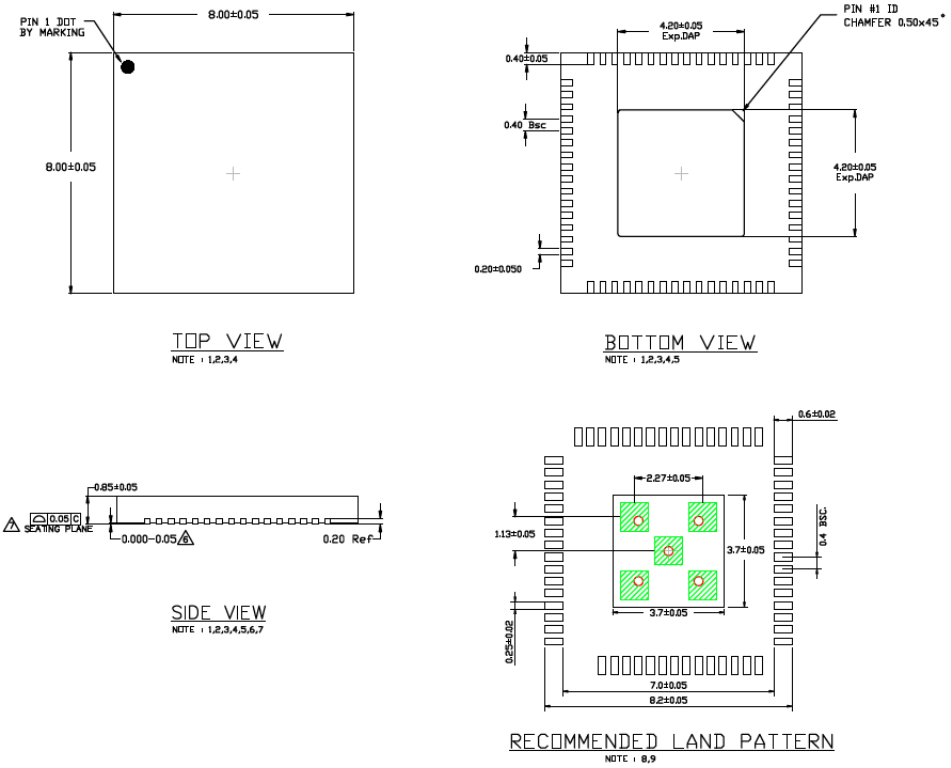
## 13.0 PACKAGE OUTLINES

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

**FIGURE 13-1: 64-LEAD QFN 8 MM X 8 MM PACKAGE WITH 4.2 MM X 4.2 MM EXPOSED PAD AREA**

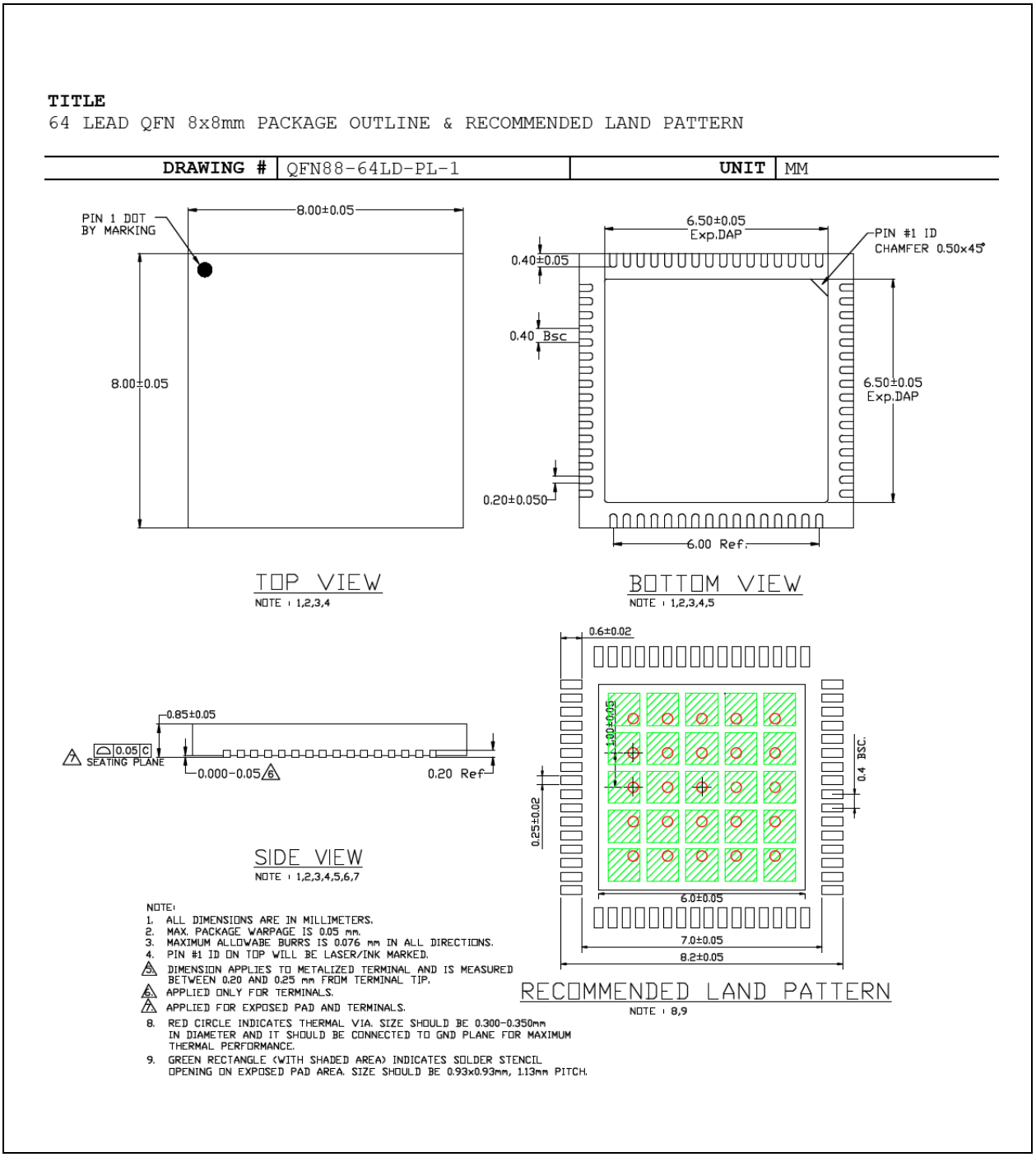
**TITLE**
64 LEAD QFN 8x8mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

| DRAWING # | QFN88-64LD-PL-2 | UNIT | MM |
|---|---|---|---|




1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP (PACKAGE) WILL BE LASER MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.
8. RED CIRCLE INDICATES THERMAL VIA. SIZE SHOULD BE 0.300-0.350mm IN DIAMETER AND IT SHOULD BE CONNECTED TO GND PLANE FOR MAXIMUM THERMAL PERFORMANCE.
9. GREEN RECTANGLE (WITH SHADED AREA) INDICATES SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.93x0.93mm.

**FIGURE 13-2: 64-LEAD QFN 8 MM X 8 MM PACKAGE WITH 6.5 MM X 6.5 MM EXPOSED PAD AREA**



## APPENDIX A: DATA SHEET REVISION HISTORY

**TABLE A-1: REVISION HISTORY**

| Revision | Section/Figure/Entry | Correction |
|---|---|---|
| DS00002096C (07-26-16) | All | Removed Energy Efficient Ethernet functionality. |
| DS00002096B (05-24-16) | 10.0 Reference Clock - Connection and Selection | Specified jitter for 25 MHz reference crystal/clock. |
| DS00002096A (02-19-16) | — | Converted Micrel data sheet KSZ9031MNX to Microchip DS00002096A. Minor text changes throughout. |
| | Wake-On-LAN – Customized Packet, Expected CRC 1 and CRC 2 Registers. | The “lower” and “upper” denotations for the two bytes of expected CRC are swapped in the previous revision. |
| | Product Identification System | Specified exposed pad size area for packages. |
| | Package Information | Corrected information for copper wire part numbers (KSZ9031MNXCC, KSZ9031MNXIC) to 64-pin (8 mm x 8 mm) QFN with (6.5 mm x 6.5 mm) exposed pad area. This is a data sheet correction. There is no change to the copper wire package. |

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- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | XX | X | X |
|---|---|---|---|---|
| Device | Interface | Package | Temperature | Bond Wire |

| | |
|---|---|
| **Device:** | KSZ9031 |
| **Interface:** | M = MII, GMII |
| **Package:** | NX = 64-pin QFN |
| **Temperature:** | C = 0°C to +70°C (Commercial)<br>I = –40°C to +85°C (Industrial) |
| **Bond Wire:** | A = Gold<br>C = Copper |

**Examples:**

a) KSZ9031MNXCA
MII, GMII Interface
64-pin QFN (Pb-Free, 4.2 mm x 4.2 mm ePad)
Commercial Temperature
Gold Wire Bonding

b) KSZ9031MNXCC
MII, GMII Interface
64-pin QFN (Pb-Free, 6.5 mm x 6.5 mm ePad)
Commercial Temperature
Copper Wire Bonding

c) KSZ9031MNXIA
MII, GMII Interface
64-pin QFN (Pb-Free, 4.2 mm x 4.2 mm ePad)
Industrial Temperature
Gold Wire Bonding

d) KSZ9031MNXIC
MII, GMII Interface
64-pin QFN (Pb-Free, 6.5 mm x 6.5 mm ePad)
Industrial Temperature
Copper Wire Bonding

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.



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**QUALITY MANAGEMENT SYSTEM**
**CERTIFIED BY DNV**
**═ ISO/TS 16949 ═**

*Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

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