GS9020

2A Sink/Source Bus Termination Regulator

Product Description

The GS9020 is a simple, cost-effective and high-speed linear regulator designed to generate termination voltage in double data rate (DDR) memory system to comply with the JEDEC SSTL_2 and SSTL_18 or other specific interfaces such as HSTL, SCSI-2 and SCSI-3 etc. devices requirements. The regulator is capable of actively sinking or sourcing up to 2A while regulating an output voltage to within 40mV.The output termination voltage cab be tightly regulated to track 1/2VDDQ by two external voltage divider resistors or the desired output voltage can be pro-grammed by externally forcing the REFEN pin voltage.

The GS9020 also incorporates a high-speed differential amplifier to provide ultra-fast response in line/load transient. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in bi-directions and on-chip thermal shut-down protection.

The GS9020 are available in the PSOP-8 (Exposed Pad) surface mount packages.

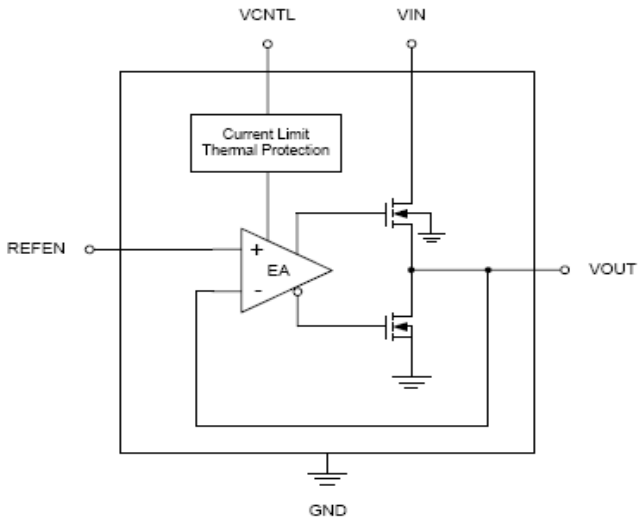
Features

- Ideal for DDR-I, DDR-II and DDR-III V_{TT} Applications
- Sink and Source 2A Continuous Current
- Integrated Power MOSFETs
- Generates Termination Voltage for SSTL_2, SSTL_18, HSTL, SCSI-2 and SCSI-3 Interfaces.
- High Accuracy Output Voltage at Full-Load
- Output Adjustment by Two External Resistors
- Low External Component Count
- Shutdown for Suspend to RAM (STR) Functionality with High-Impedance Output
- Current Limiting Protection
- On-Chip Thermal Protection
- Available in PSOP-8 (Exposed Pad) Packages
- V_{IN} and V_{CNTL} No Power Sequence Issue
- 100% Lead (Pb)-Free
- Stable with Ceramic Output Capacitor
- RoHS Compliant, 100%Pb & Halogen Free

Applications

- Desktop PCs, Notebooks, and Workstations
- Graphics Card Memory Termination
- Set Top Boxes, Digital TVs, Printers
- Embedded Systems
- Active Termination Buses
- DDR-I, DDR-II and DDR-III Memory Systems

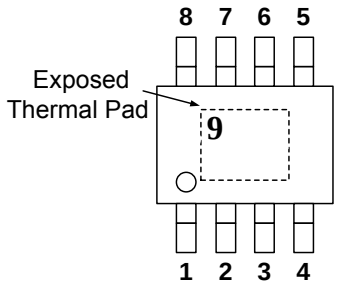
Block Diagram



GLOBALTECH SEMICONDUCTOR

Packages & Pin Assignments

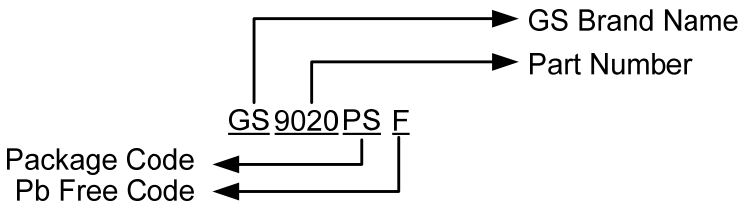
GS9020PSF (PSOP- 8)



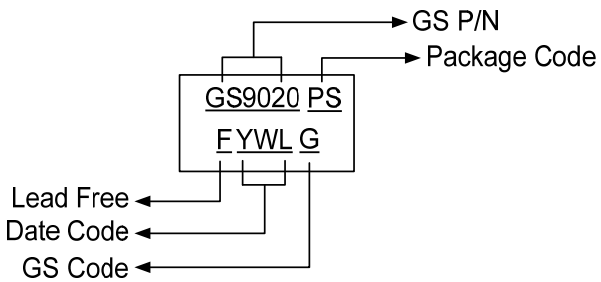
1	V_{IN}	5	NC
2	GND	6	V_{CNTL}
3	REFEN	7	NC
4	V_{OUT}	8	NC

Pin Name	Pin function
V_{IN}	Power input
GND	Ground
V_{CNTL}	Gate drive voltage
V_{OUT}	Output voltage
REFEN	Reference voltage input and chip enable

Ordering Information



Marking Information



Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input Voltage	6	V
V_{CNTL}	Control Voltage	6	V
V_{OUT}	V_{OUT} Output Voltage (V_{OUT} to GND)	-0.3 ~ V_{IN}+0.3V	V
P_D	Power Dissipation	Internally Limited	--
--	ESD Rating	3	KV
T_S	Storage Temperature Range	-65 to +150	ºC
T_{LEAD}	Lead Temperature(Soldering,5 sec.)	260	ºC
Θ_{JC}	Package Thermal Resistance	28	ºC/W

Operating Rating

Symbol	Parameter	Value	Unit
V_{IN}	Input Voltage	5.5 to 1.5 ±3%	V
V_{CNTL}	Control Voltage	5.0 to 3.3 ±5%	V
T_A	Ambient Temperature	-40 to +85	ºC
T_J	Junction Temperature	-40 to +125	ºC

Electrical Characteristics

V_{IN} =2.5V/1.8V/1.5V, V_{CNTL} =3.3V, V_{REFEN} =1.25V/0.9V/0.75V, C_{OUT} =10μF (Ceramic) , T_A =25° C, unless otherwise specified

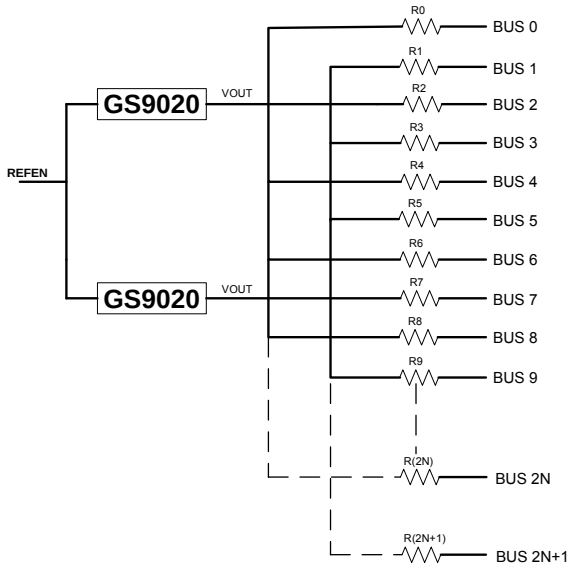
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
I_{CNTL}	V_{CNTL} Operation Current	I_{OUT}=0A	--	1	2.5	mA
I_{STBY}	Standby Current	V_{REFEN}<0.2V(Shutdown), R_{LOAD}=180 Ω	--	50	90	μA
Output (DDR / DDR II / DDR III)						
V_{OS}	Output Offset Voltage(3)	I_{OUT}= 0A	-20	--	+20	mV
ΔV_{LOAD}	Load Regulation(4)	I_{OUT}= +2A	-20	--	+20	mV
ΔV_{LOAD}	Load Regulation(4)	I_{OUT}= -2A	-20	--	+20	mV
Protection						
I_{LIM}	Current limit		2.2	--	--	A
T_{SD}	Thermal Shutdown Temperature	3.3V ≤ V_{CNTL} ≤ 5V	--	170	--	ºC
ΔT_{SD}	Thermal Shutdown Hysteresis	3.3V ≤ V_{CNTL} ≤ 5V	--	35	--	ºC
REFEN Shutdown						
V_{IH}	Shutdown Threshold	Enable	0.6	--	--	V
V_{IL}		Shutdown	--	--	0.2	
Tss	Soft Start interval	R1=R2=100K, Css=1uF		0.2		ms

Note 1: Exceeding the absolute maximum rating may damage the device.
Note 2: V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}.
Note 3: V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}.
Note 4: Regulation is measured at constant junction temperature by using a 5ms current pulse. Devices are tested for load regulation in the load range from 0A to 2A.

Application Information

Input Capacitor and Layout Consideration

Place the input bypass capacitor as close as possible to the GS9020. A low ESR capacitor larger than 470uF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance. Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between GS9020 and the preceding power converter.



Consideration while designs the resistance of voltage divider

Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on V_{REFEN} is below 0.2V. In addition, the capacitor and voltage divider form the low-pass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.

Thermal Consideration

GS9020 regulators have internal thermal limiting circuitry designed to protect the device during overload conditions. For continued operation, do not exceed maximum operation junction temperature 125℃. The power dissipation definition in device is:

$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula:

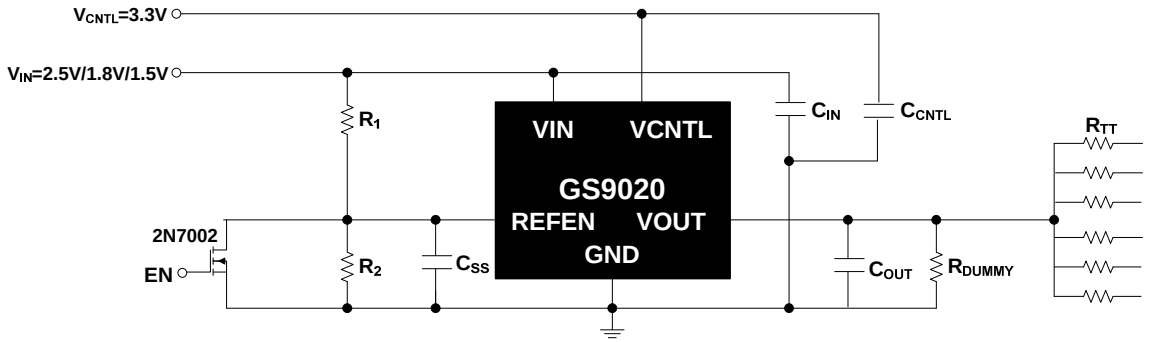
$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \Theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125ºC, T_A is the ambient temperature and the Θ_{JA} is the junction to ambient thermal resistance. The junction to ambient thermal resistance (Θ_{JA} is layout dependent) for PSOP-8 package (Exposed Pad) is 75 ºC/W on standard JEDEC 51-7 (4layers, 2S2P) thermal test board. The maximum power dissipation at T_A = 25ºC can be calculated by following formula:

$P_{D(MAX)}$ = (125ºC - 25ºC) / 75℃/W = 1.33W

The thermal resistance Θ_{JA} of PSOP-8 (Exposed Pad) is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding copper under the expose pad of PSOP-8 package. We have to consider the copper couldn't stretch infinitely and avoid the tin overflow.

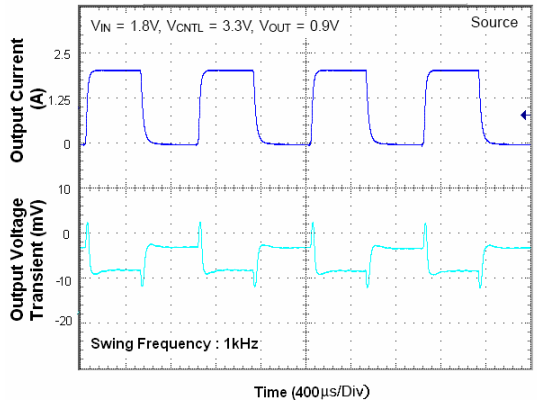
Typical Application Circuit



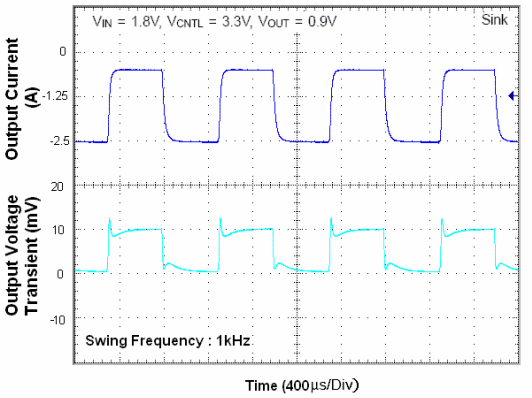
R_1=R_2=100KΩ,R_{TT}=50Ω/33Ω/25Ω
$C_{OUT, min}$=10μF(Ceramic)+1000μF under the worst case testing condition
R_{DUMMY}=1kΩ as for VOUT discharge when VIN is not present but VCNTL is present
C_{SS}=1μF,C_{IN}=470μF(ESR), C_{CNTL}= 1μF

Typical Operating Characteristics

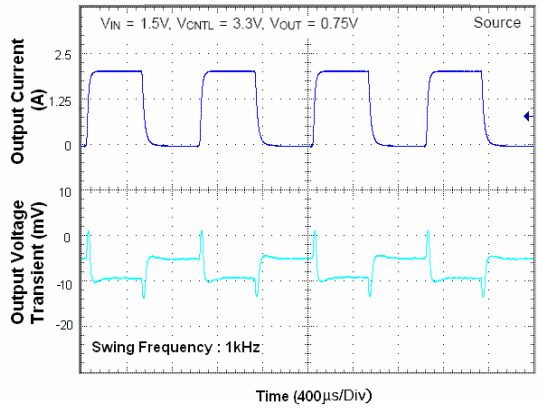
0.9V_{TT} @ 2A Transient Response



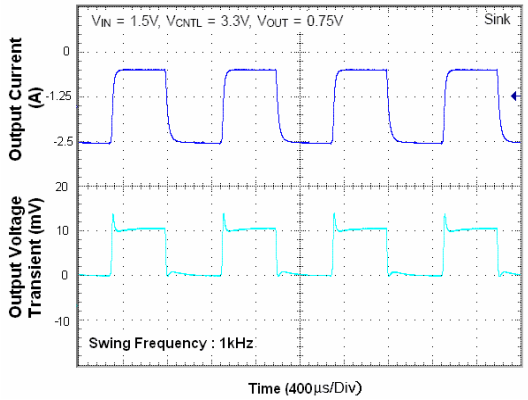
0.9V_{TT} @ 2A Transient Response



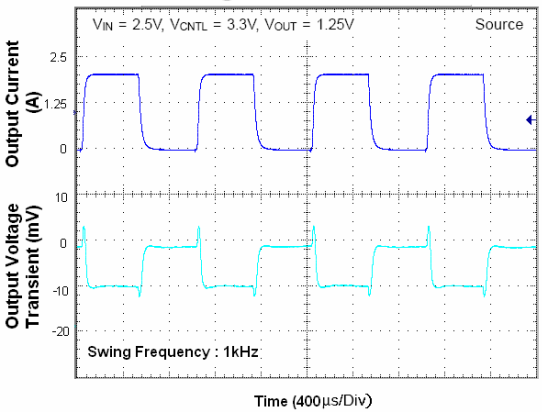
0.75V_{TT} @ 2A Transient Response



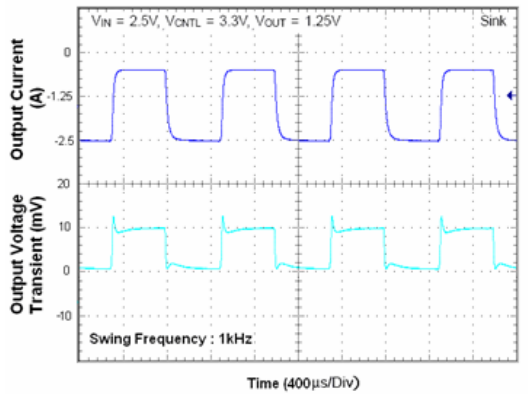
0.75V_{TT} @ 2A Transient Response



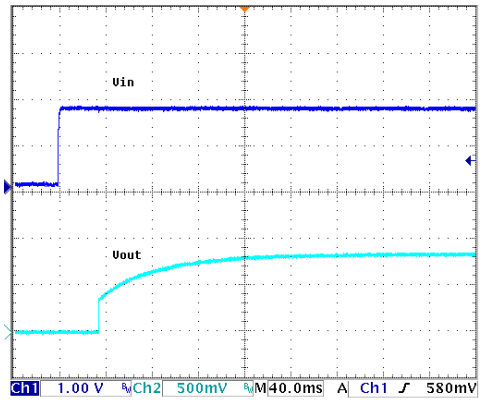
1.25V_{TT} @ 2A Transient Response



1.25V_{TT} @ 2A Transient Response

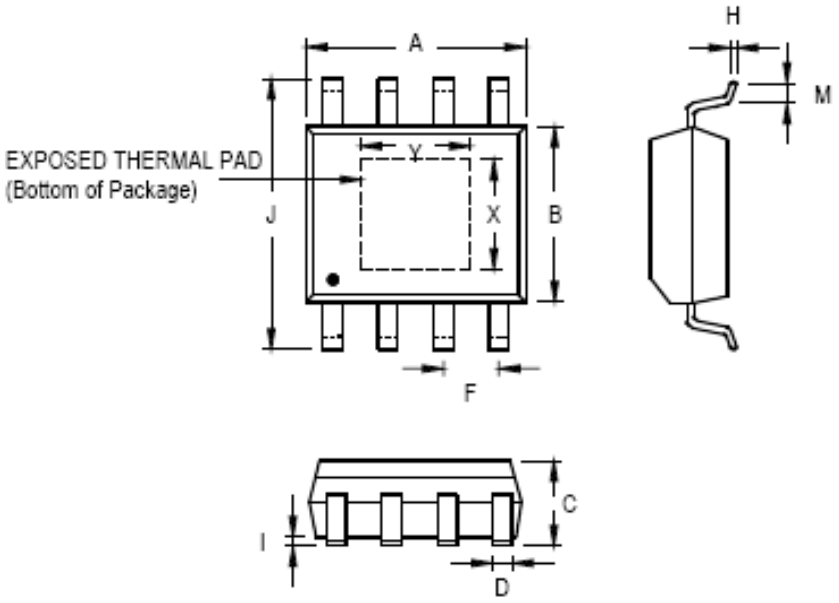


Power On Soft Start （Vin =1.8V）



Package Dimension

PSOP-8 PLASTIC PACKAGE



Dimensions				
SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.191	0.254	0.008	0.010
I	0.000	0.152	0.000	0.006
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
X	2.057	2.515	0.081	0.099
Y	2.057	3.404	0.081	0.134

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