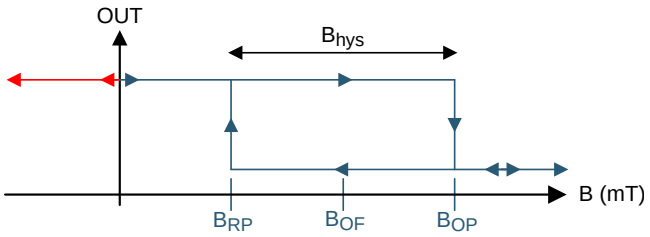
DRV5023-Q1 Automotive Digital-Switch Hall Effect Sensor

1 Features

- Digital Unipolar-Switch Hall Sensor
- AEC-Q100 Qualified for Automotive Applications
  - Grade 1: T_A = –40 to 125°C (Q, See Figure 23)
  - Grade 0: T_A = –40 to 150°C (E, See Figure 23)
- Inverse Output Option (FI)
- Superior Temperature Stability
  - Sensitivity ±10% Over Temperature
- Multiple Sensitivity Options (B_{OP} / B_{RP}):
  - 3.5 / 2 mT (FA, FI, see Figure 23)
  - 6.9 / 3.2 mT (AJ, see Figure 23)
  - 14.5 / 6 mT (BI, see Figure 23)
- Supports a Wide Voltage Range
  - 2.7 to 38 V
  - No External Regulator Required
- Open Drain Output (30-mA Sink)
- Fast 35-µs Power-On Time
- Small Package and Footprint
  - Surface Mount 3-Pin SOT-23 (DBZ)
    - 2.92 mm × 2.37 mm
  - Through-Hole 3-Pin TO-92 (LPG)
    - 4.00 mm × 3.15 mm
- **Protection Features**
  - Reverse Supply Protection (up to –22 V)
  - Supports up to 40-V Load Dump
  - Output Short-Circuit Protection
  - Output Current Limitation
  - OUT Short to Battery Protection

Output State



2 Applications

- Docking Detection
- Door Open and Close Detection
- Proximity Sensing
- Valve Positioning
- Pulse Counting

3 Description

The DRV5023-Q1 device is a chopper-stabilized Hall Effect Sensor that offers a magnetic sensing solution with superior sensitivity stability over temperature and integrated protection features.

When the applied magnetic flux density exceeds the B_{OP} threshold, the DRV5023-Q1 open-drain output goes low. The output stays low until the field decreases to less than B_{RP}, and then the output goes to high impedance. The output current sink capability is 30 mA. A wide operating voltage range from 2.7 to 38 V with reverse polarity protection up to –22 V makes the device suitable for a wide range of automotive applications.

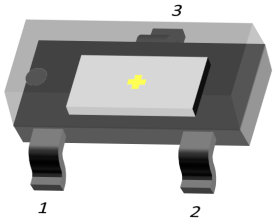
Internal protection functions are provided for reverse supply conditions, load dump, and output short circuit or over current.

Device Information(1)

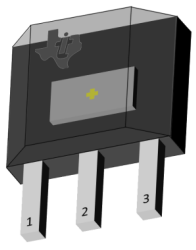
PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV5023-Q1	SOT-23 (3)	2.92 mm × 1.30 mm
	TO-92 (3)	4.00 mm × 3.15 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

SOT-23



TO-92



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2016) to Revision D — **Page**

- Revised preliminary limits for the FA version ... 5

Changes from Revision B (December 2015) to Revision C — **Page**

- Added the FA and FI device options ... 1
- Added the typical bandwidth value to the *Magnetic Characteristics* table ... 5

Changes from Revision A (May 2015) to Revision B — **Page**

- Corrected body size of SOT-23 package and SIP package name to TO-92 ... 1
- Added B_{MAX} to *Absolute Maximum Ratings* ... 4
- Removed table notes regarding testing for the operating junction temperature in *Absolute Maximum Ratings* ... 4
- Updated package tape and reel options for M and blank ... 18
- Added *Community Resources* ... 19

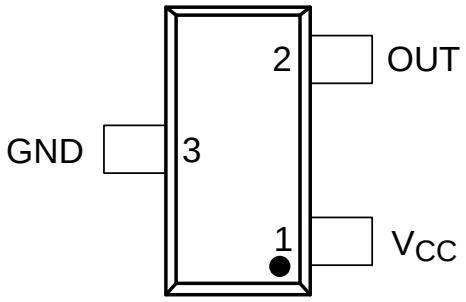
Changes from Original (December 2014) to Revision A — **Page**

- Updated device status to production data ... 1

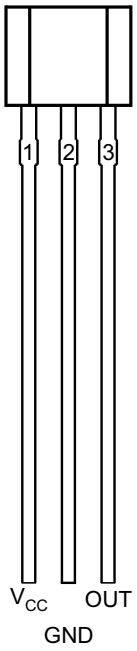
5 Pin Configuration and Functions

For additional configuration information, see *Device Markings* and *Mechanical, Packaging, and Orderable Information*.

DBZ Package
3-Pin SOT-23
Top View



LPG Package
3-Pin TO-92
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DBZ	LPG		
GND	3	2	GND	Ground pin
OUT	2	3	Output	Hall sensor open-drain output. The open drain requires a resistor pullup.
V_{CC}	1	1	Power	2.7 to 38 V power supply. Bypass this pin to the GND pin with a 0.01-µF (minimum) ceramic capacitor rated for V_{CC}.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply voltage	V_{CC}	–22(2)	40	V
	Voltage ramp rate (V_{CC}), V_{CC} < 5 V	Unlimited		V/µs
	Voltage ramp rate (V_{CC}), V_{CC} > 5 V	0	2	
Output pin voltage		–0.5	40	V
Output pin reverse current during reverse supply condition		0	100	mA
Magnetic flux density, B_{MAX}		Unlimited		
Operating junction temperature, T_J	Q, see Figure 23	–40	150	°C
	E, see Figure 23	–40	175	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Ensured by design. Only tested to –20 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Power supply voltage		2.7	38	V
V_O	Output pin voltage (OUT)		0	38	V
I_{SINK}	Output pin current sink (OUT)(1)		0	30	mA
T_A	Operating ambient temperature	Q, see Figure 23	–40	125	°C
		E, see Figure 23	–40	150	

(1) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC(1)		DRV5023-Q1		UNIT
		DBZ (SOT-23)	LPG (TO-92)	
		3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	333.2	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99.9	98.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.9	154.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.9	40	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.2	154.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (V_{CC})						
V_{CC}	V_{CC} operating voltage		2.7		38	V
I_{CC}	Operating supply current	V_{CC} = 2.7 to 38 V, T_A = 25°C		2.7		mA
		V_{CC} = 2.7 to 38 V, T_A = $T_{A, MAX}$ (1)		3	3.5	
t_{on}	Power-on time			35	50	µs
OPEN DRAIN OUTPUT (OUT)						
$r_{DS(on)}$	FET on-resistance	V_{CC} = 3.3 V, I_O = 10 mA, T_A = 25°C		22		Ω
		V_{CC} = 3.3 V, I_O = 10 mA, T_A = 125°C		36	50	
$I_{lkg(off)}$	Off-state leakage current	Output Hi-Z			1	µA
PROTECTION CIRCUITS						
V_{CCR}	Reverse supply voltage		–22			V
I_{OCP}	Overcurrent protection level	OUT shorted V_{CC}	15	30	45	mA

(1) $T_{A, MAX}$ is 125°C for Q Grade 1 devices and 150°C for E Grade 0 devices (see)

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN DRAIN OUTPUT (OUT)						
t_d	Output delay time	B = B_{RP} – 10 mT to B_{OP} + 10 mT in 1 µs		13	25	µs
t_r	Output rise time (10% to 90%)	R1 = 1 kΩ, C_O = 50 pF, V_{CC} = 3.3 V		200		ns
t_f	Output fall time (90% to 10%)	R1 = 1 kΩ, C_O = 50 pF, V_{CC} = 3.3 V		31		ns

6.7 Magnetic Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT (1)
f_{BW}	Bandwidth (2)		20	30		kHz
DRV5023FA, DRV5023FI: 3.5 / 2 mT						
B_{OP}	Operate point (see Figure 12)		1.8	3.5	6.8	mT
B_{RP}	Release point (see Figure 12)		0.5	2	4.2	mT
B_{hys}	Hysteresis; B_{hys}= (B_{OP} – B_{RP})			1.5		mT
B_O	Magnetic offset, B_O = (B_{OP} + B_{RP}) / 2			2.8		mT
DRV5023AJ: 6.9 / 3.2 mT						
B_{OP}	Operate point (see Figure 12)		3	6.9	12	mT
B_{RP}	Release point (see Figure 12)		1	3.2	5	mT
B_{hys}	Hysteresis; B_{hys}= (B_{OP} – B_{RP})			3.7		mT
B_O	Magnetic offset, B_O = (B_{OP} + B_{RP}) / 2			5		mT
DRV5023BI: 14.5 / 6 mT						
B_{OP}	Operate point (see Figure 12)		6	14.5	24	mT
B_{RP}	Release point (see Figure 12)		3	6	9	mT
B_{hys}	Hysteresis; B_{hys} = (B_{OP} – B_{RP}) (3)			8.5		mT
B_O	Magnetic offset, B_O = (B_{OP} + B_{RP}) / 2			10.3		mT

(1) 1 mT = 10 Gauss
(2) Bandwidth describes the fastest changing magnetic field that can be detected and translated to the output.
(3) $|B_{OP}|$ is always greater than $|B_{RP}|$.

6.8 Typical Characteristics

T_A > 125°C data is valid for Grade 0 devices only (E, see Figure 23)

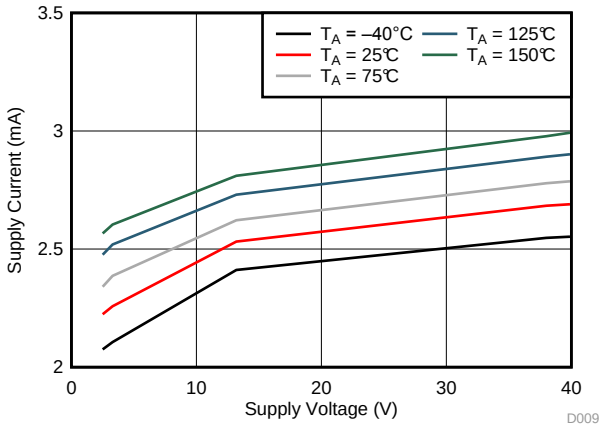


Figure 1. I_{CC} vs V_{CC}

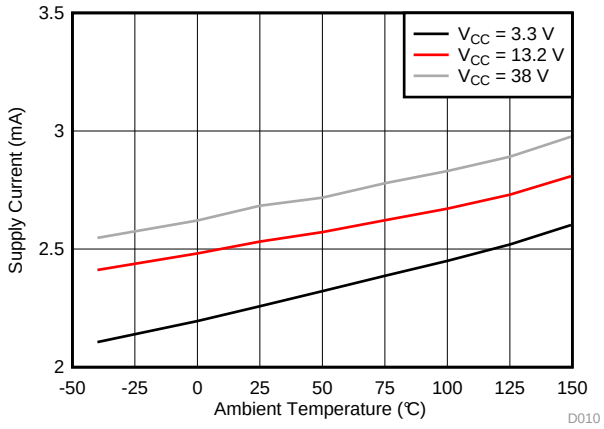


Figure 2. I_{CC} vs Temperature

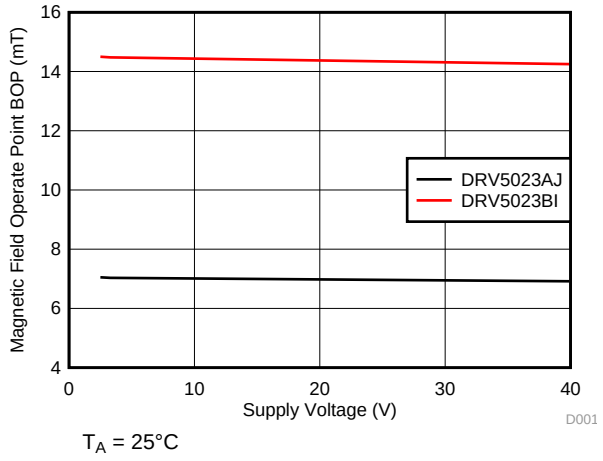


Figure 3. B_{OP} vs V_{CC}

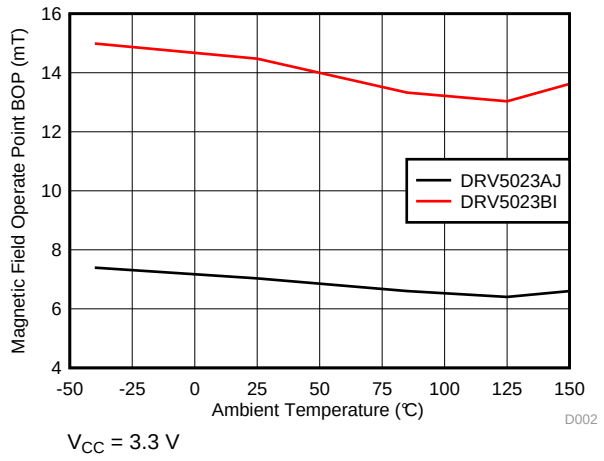


Figure 4. B_{OP} vs Temperature

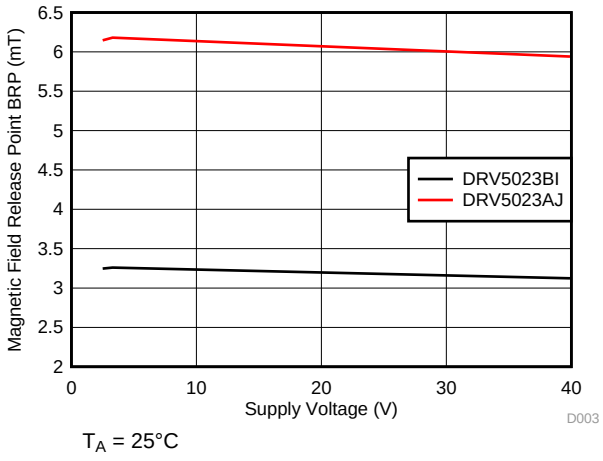


Figure 5. B_{RP} vs V_{CC}

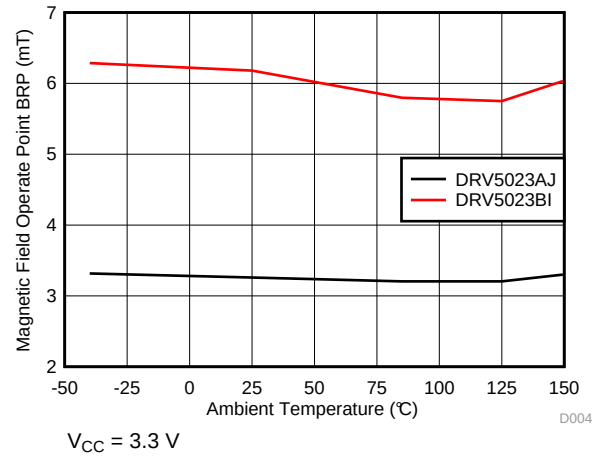


Figure 6. B_{RP} vs Temperature

Typical Characteristics (continued)

T_A > 125°C data is valid for Grade 0 devices only (E, see)

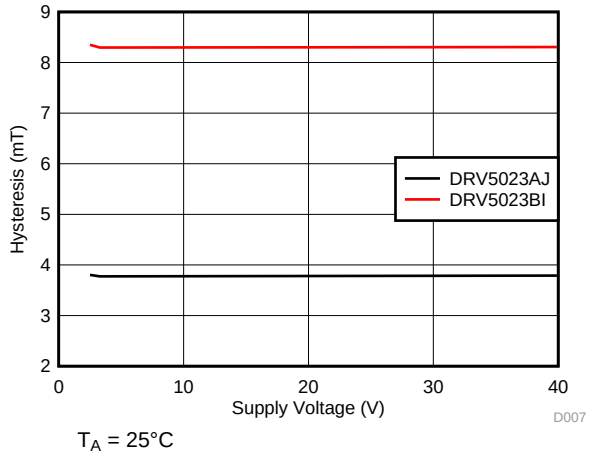


Figure 7. Hysteresis vs V_{CC}

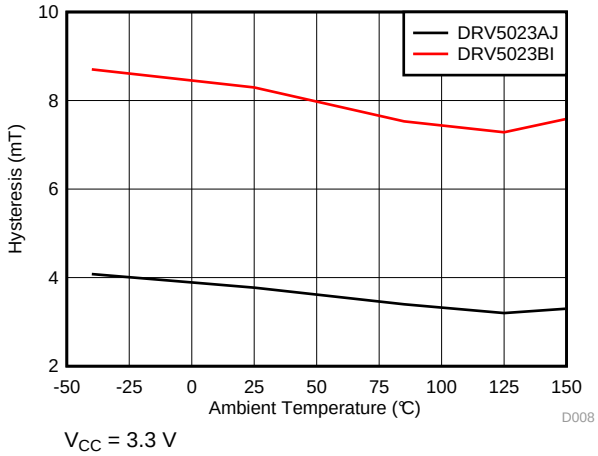


Figure 8. Hysteresis vs Temperature

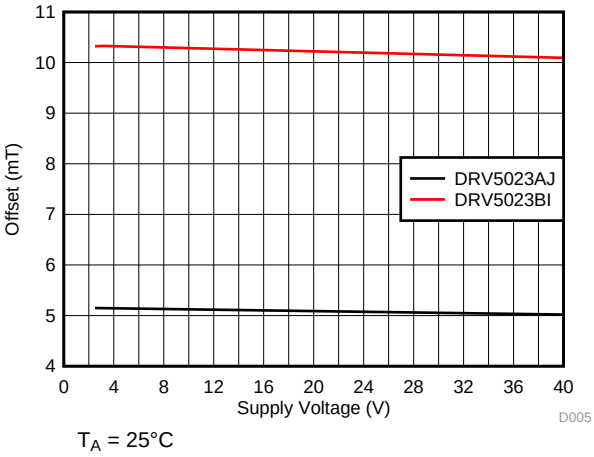


Figure 9. Offset vs V_{CC}

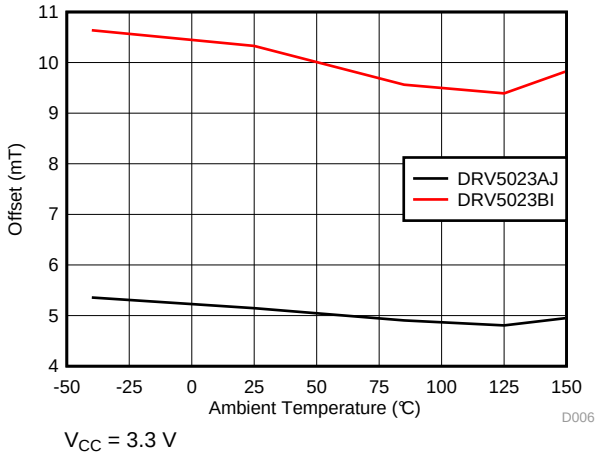


Figure 10. Offset vs Temperature

7 Detailed Description

7.1 Overview

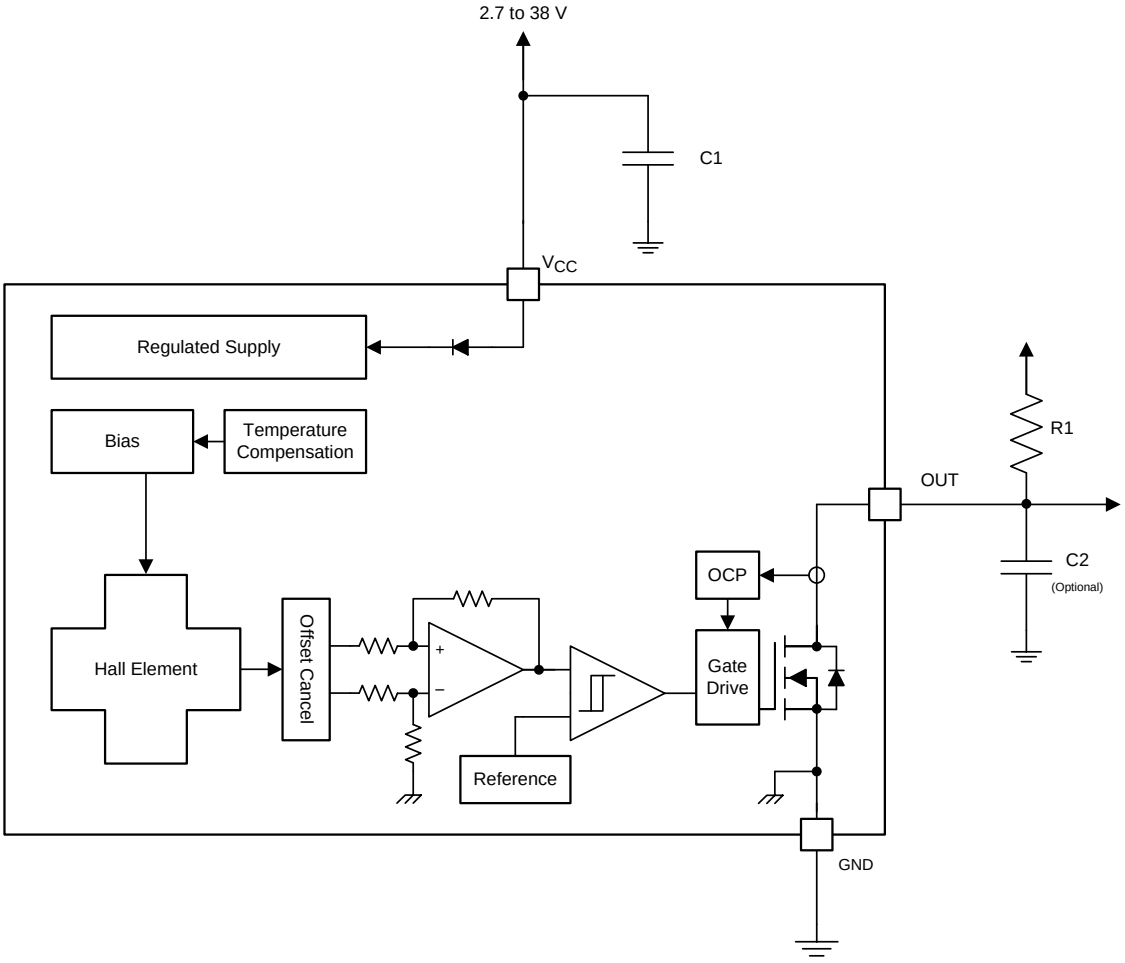
The DRV5023-Q1 device is a chopper-stabilized Hall sensor with a digital output for magnetic sensing applications. The DRV5023-Q1 device can be powered with a supply voltage between 2.7 and 38 V, and will survive –22 V reverse-battery conditions. The DRV5023-Q1 device does not operate when –22 to 2.4 V is applied to the V_{CC} pin (with respect to GND pin). In addition, the device can withstand supply voltages up to 40 V for transient durations.

The field polarity is defined as follows: a south pole near the marked side of the package is a positive magnetic field. A north pole near the marked side of the package is a negative magnetic field. The output state is dependent on the magnetic field perpendicular to the package.

For the FA, AJ, and BI device versions, a strong south pole near the marked side of the package causes the output to pull low, and the absence of a field makes the output high-impedance. The FI device version has a voltage inverter on the output, where a strong south pole causes the output to be high-impedance, and the absence of a field makes the output pull low. Hysteresis is included in between the operate point and the release point to prevent toggling near the magnetic threshold.

An external pullup resistor is required on the OUT pin. The OUT pin can be pulled up to V_{CC}, or to a different voltage supply. This allows for easier interfacing with controller circuits.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Field Direction Definition

A positive magnetic field is defined as a south pole near the marked side of the package as shown in Figure 11.

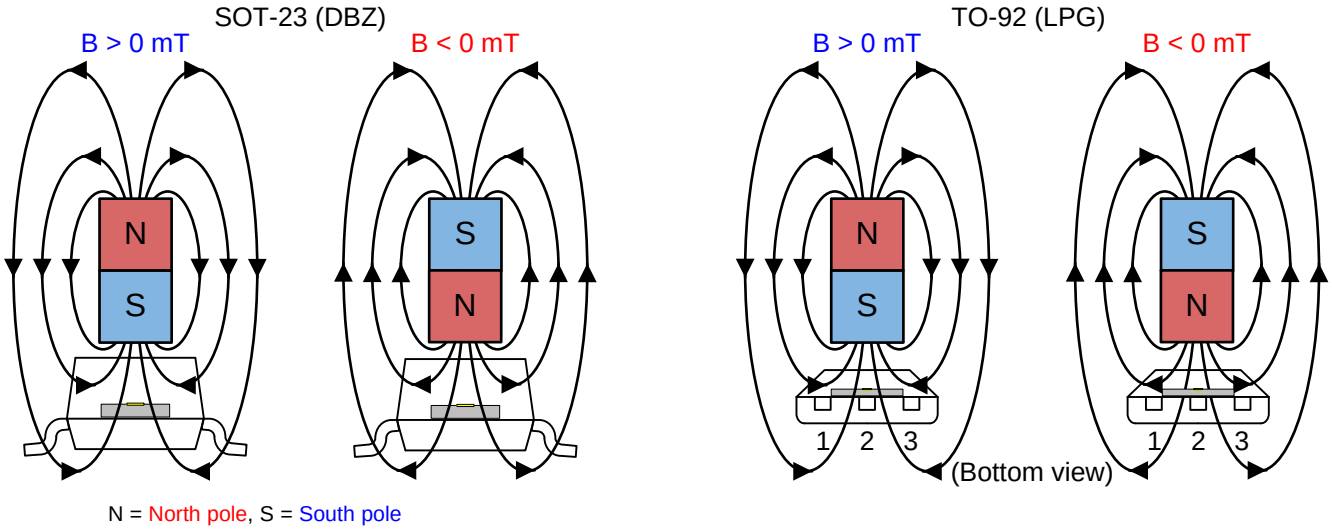


Figure 11. Field Direction Definition

7.3.2 Device Output

If the device is powered on with a magnetic field strength between B_{RP} and B_{OP}, then the device output is indeterminate and can either be Hi-Z or Low. If the field strength is greater than B_{OP}, then the output is pulled low. If the field strength is less than B_{RP}, then the output is released.

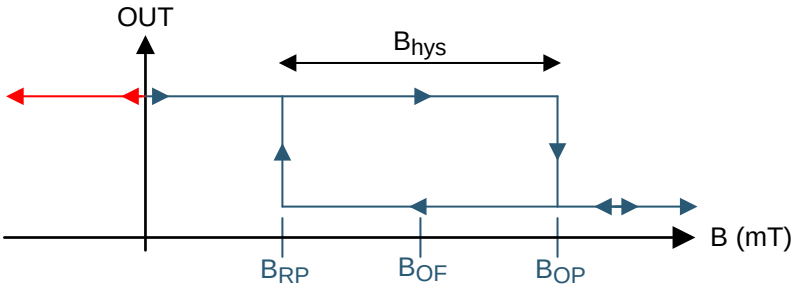


Figure 12. Output State

Feature Description (continued)

7.3.3 Power-On Time

After applying V_{CC} to the DRV5023-Q1 device, t_{on} must elapse before the OUT pin is valid. During the power-up sequence, the output is Hi-Z. A pulse as shown in Figure 13 and Figure 14 occurs at the end of t_{on}. This pulse can allow the host processor to determine when the DRV5023-Q1 output is valid after startup. In Case 1 (Figure 13) and Case 2 (Figure 14), the output is defined assuming a constant magnetic field B > B_{OP} and B < B_{RP}.

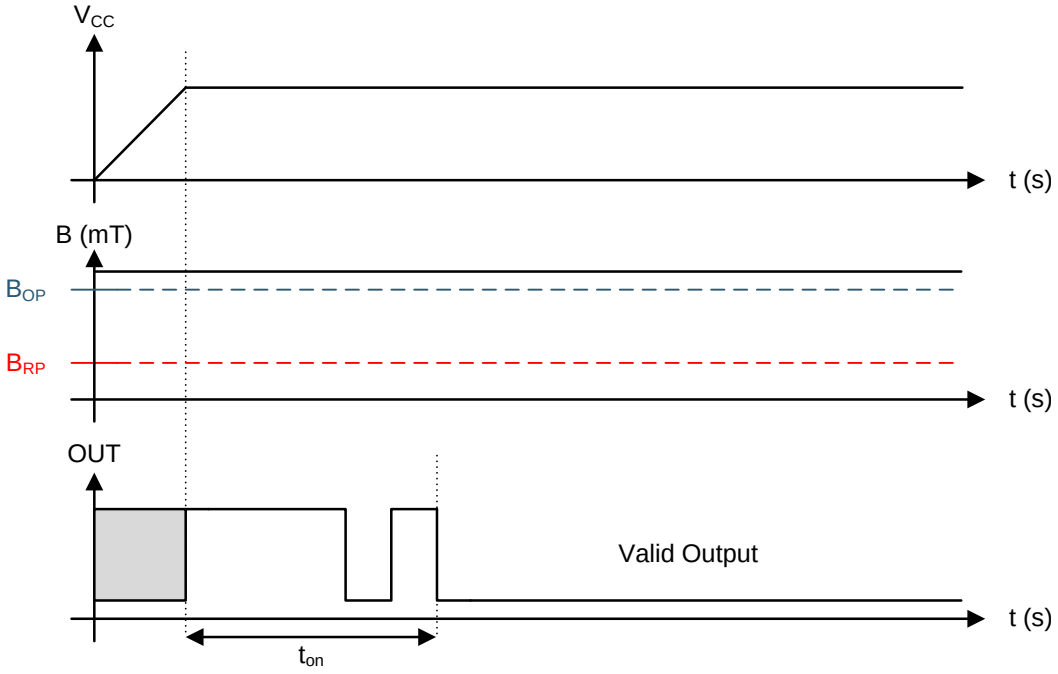


Figure 13. Case 1: Power On When B > B_{OP}

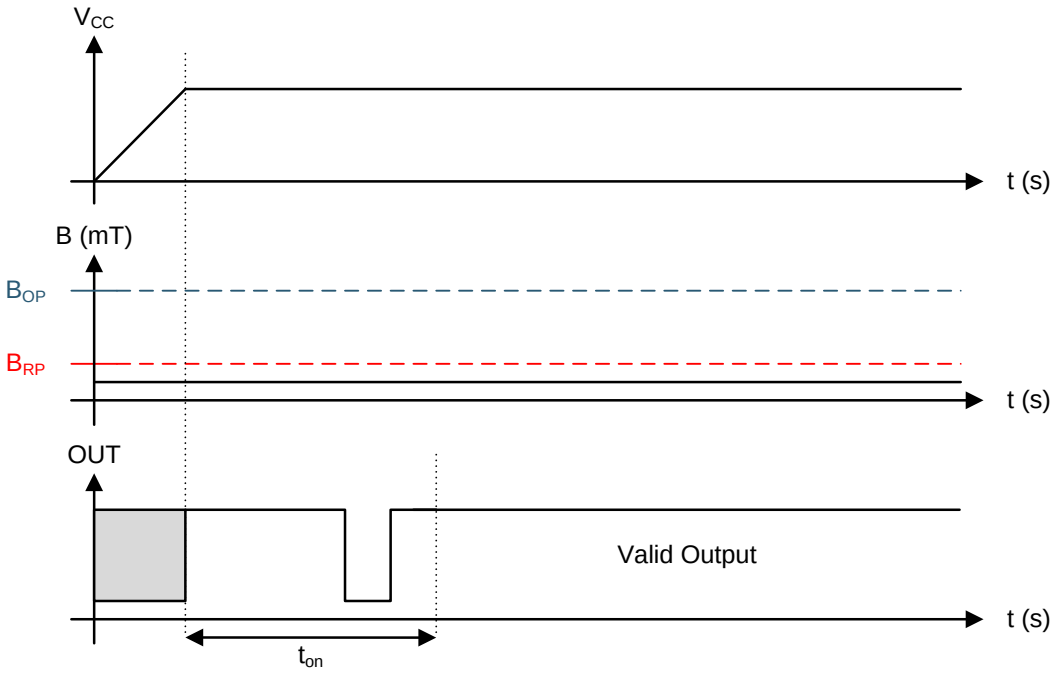


Figure 14. Case 2: Power On When B < B_{RP}

Feature Description (continued)

If the device is powered on with the magnetic field strength $B_{RP} < B < B_{OP}$, then the device output is indeterminate and can either be Hi-Z or pulled low. During the power-up sequence, the output is held Hi-Z until t_{on} has elapsed. At the end of t_{on}, a pulse is given on the OUT pin to indicate that t_{on} has elapsed. After t_{on}, if the magnetic field changes such that $B_{OP} < B$, the output is released. Case 3 (Figure 15) and Case 4 (Figure 16) show examples of this behavior.

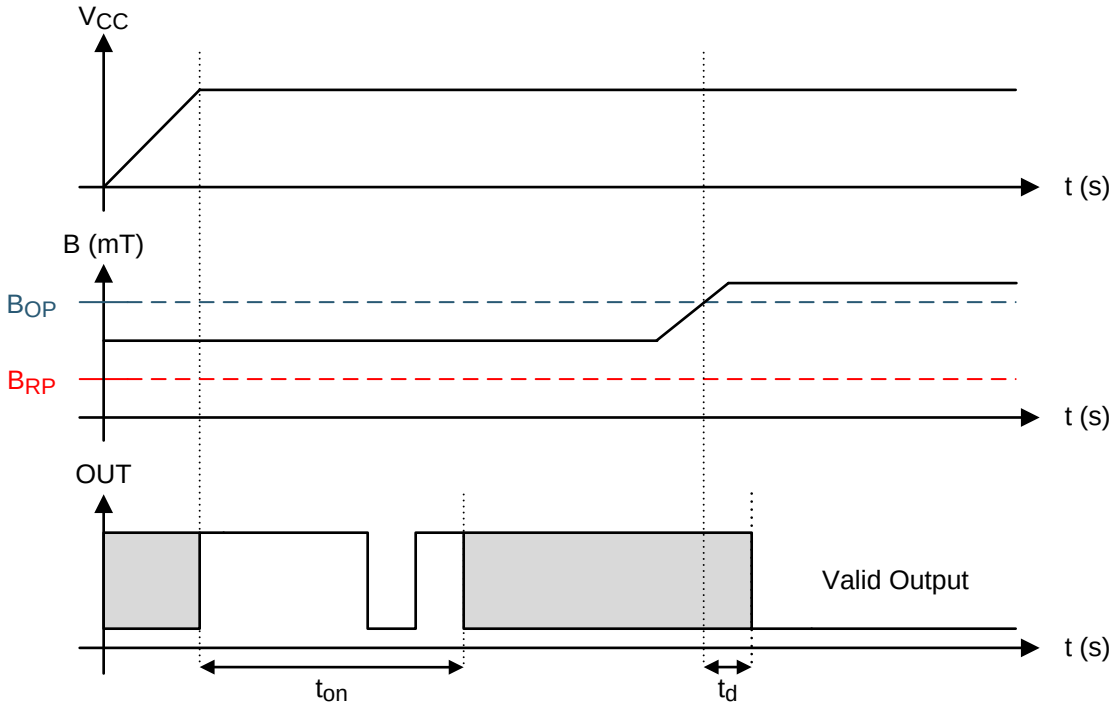


Figure 15. Case 3: Power On When $B_{RP} < B < B_{OP}$, Followed by $B > B_{OP}$

Feature Description (continued)

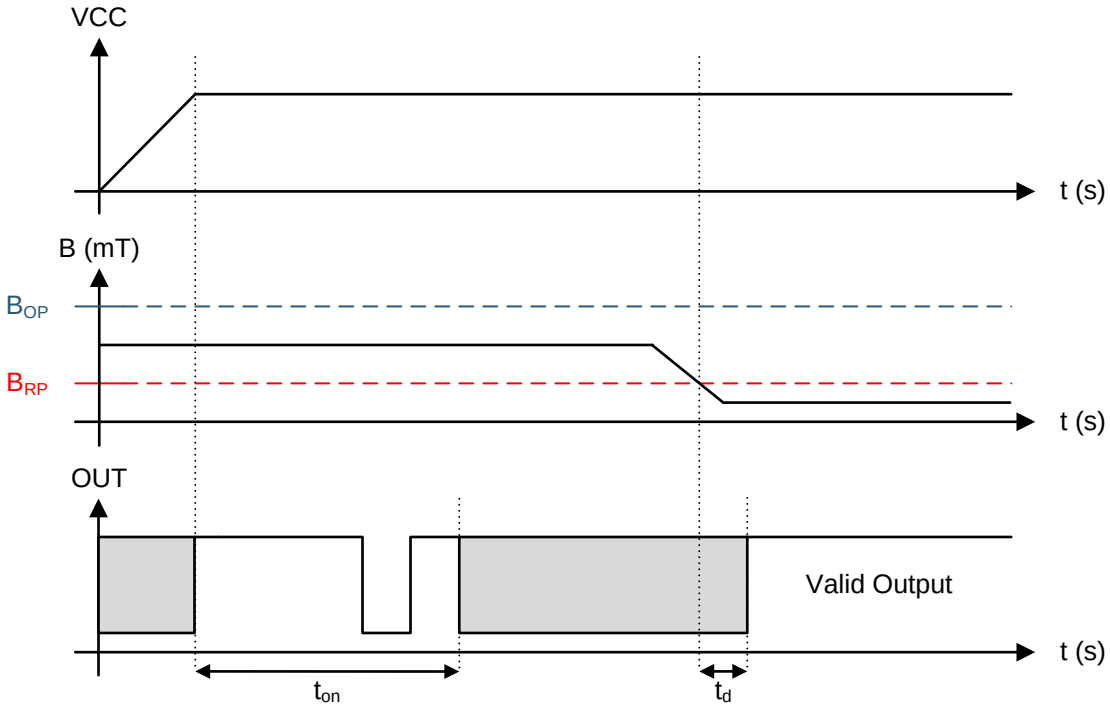


Figure 16. Case 4: Power On When B_{RP} < B < B_{OP}, Followed by B < B_{RP}

Feature Description (continued)

7.3.4 Output Stage

The DRV5023-Q1 output stage uses an open-drain NMOS, and it is rated to sink up to 30 mA of current. For proper operation, calculate the value of the pullup resistor R1 using Equation 1.

$$\frac{V_{ref}\,max}{30\ mA} \le R1 \le \frac{V_{ref}\,min}{100\ \mu A} \quad (1)$$

The size of R1 is a tradeoff between the OUT rise time and the current when OUT is pulled low. A lower current is generally better, however faster transitions and bandwidth require a smaller resistor for faster switching.

In addition, ensure that the value of R1 > 500 Ω to ensure the output driver can pull the OUT pin close to GND.

NOTE

V_{ref} is not restricted to V_{CC}. The allowable voltage range of this pin is specified in the *Absolute Maximum Ratings*.

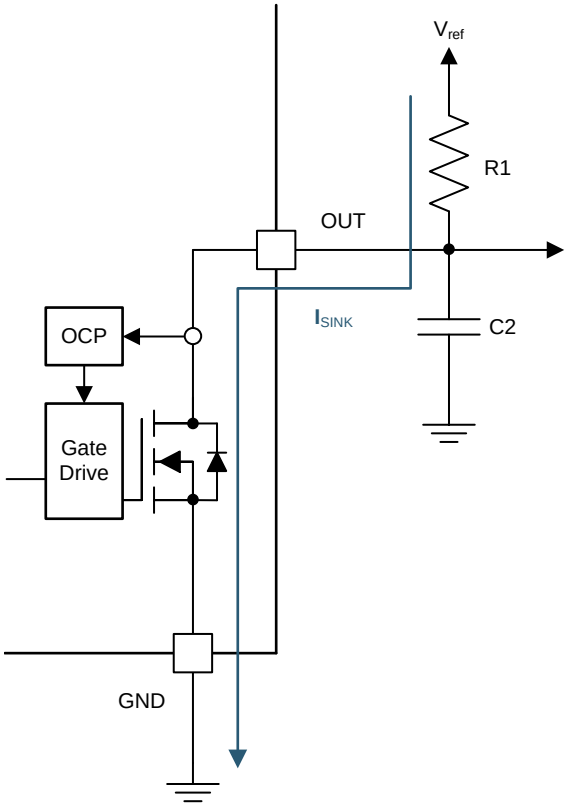


Figure 17.

Select a value for C2 based on the system bandwidth specifications as shown in Equation 2.

$$2 \times f_{BW}\ (Hz) < \frac{1}{2\pi \times R1 \times C2} \quad (2)$$

Most applications do no require this C2 filtering capacitor.

Feature Description (continued)

7.3.5 Protection Circuits

The DRV5023-Q1 device is fully protected against overcurrent and reverse-supply conditions.

7.3.5.1 Overcurrent Protection (OCP)

An analog current-limit circuit limits the current through the FET. The driver current is clamped to I_{OCP}. During this clamping, the $r_{DS(on)}$ of the output FET is increased from the nominal value.

7.3.5.2 Load Dump Protection

The DRV5023-Q1 device operates at DC V_{CC} conditions up to 38 V nominally, and can additionally withstand V_{CC} = 40 V. No current-limiting series resistor is required for this protection.

7.3.5.3 Reverse Supply Protection

The DRV5023-Q1 device is protected in the event that the V_{CC} pin and the GND pin are reversed (up to –22 V).

NOTE

In a reverse supply condition, the OUT pin reverse-current must not exceed the ratings specified in the *Absolute Maximum Ratings*.

Table 1.

FAULT	CONDITION	DEVICE	DESCRIPTION	RECOVERY
FET overload (OCP)	$I_{SINK} \geq I_{OCP}$	Operating	Output current is clamped to I_{OCP}	$I_O < I_{OCP}$
Load dump	38 V < V_{CC} < 40 V	Operating	Device will operate for a transient duration	$V_{CC} \leq$ 38 V
Reverse supply	–22 V < V_{CC} < 0 V	Disabled	Device will survive this condition	$V_{CC} \geq$ 2.7 V

7.4 Device Functional Modes

The DRV5023-Q1 device is active only when V_{CC} is between 2.7 and 38 V.

When a reverse supply condition exists, the device is inactive.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV5023-Q1 device is used in magnetic-field sensing applications.

8.2 Typical Applications

8.2.1 Standard Circuit

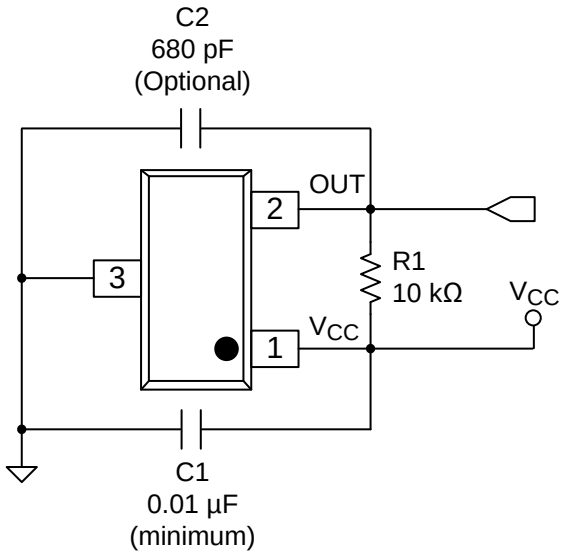


Figure 18. Typical Application Circuit

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{CC}	3.2 to 3.4 V
System bandwidth	f_{BW}	10 kHz

8.2.1.2 Detailed Design Procedure

Table 3. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C1	V_{CC}	GND	A 0.01-µF (minimum) ceramic capacitor rated for V_{CC}
C2	OUT	GND	**Optional**: Place a ceramic capacitor to GND
R1	OUT	REF(1)	Requires a resistor pullup

(1) REF is not a pin on the DRV5023-Q1 device, but a REF supply-voltage pullup is required for the OUT pin; the OUT pin may be pulled up to V_{CC}.

8.2.1.2.1 Configuration Example

In a 3.3-V system, 3.2 V ≤ V_{ref} ≤ 3.4 V. Use Equation 3 to calculate the allowable range for R1.

$$\frac{V_{ref}\,max}{30\ mA} \leq R1 \leq \frac{V_{ref}\,min}{100\ \mu A} \tag{3}$$

For this design example, use Equation 4 to calculate the allowable range of R1.

$$\frac{3.4\ V}{30\ mA} \leq R1 \leq \frac{3.2\ V}{100\ \mu A} \tag{4}$$

Therefore:

$$113\ \Omega \leq R1 \leq 32\ k\Omega \tag{5}$$

After finding the allowable range of R1 (Equation 5), select a value between 500 Ω and 32 kΩ for R1.

Assuming a system bandwidth of 10 kHz, use Equation 6 to calculate the value of C2.

$$2 \times f_{BW}\ (Hz) < \frac{1}{2\pi \times R1 \times C2} \tag{6}$$

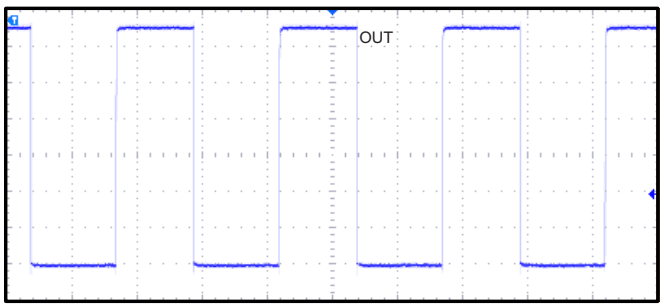
For this design example, use Equation 7 to calculate the value of C2.

$$2 \times 10\ kHz < \frac{1}{2\pi \times R1 \times C2} \tag{7}$$

An R1 value of 10 kΩ and a C2 value less than 820 pF satisfy the requirement for a 10-kHz system bandwidth.

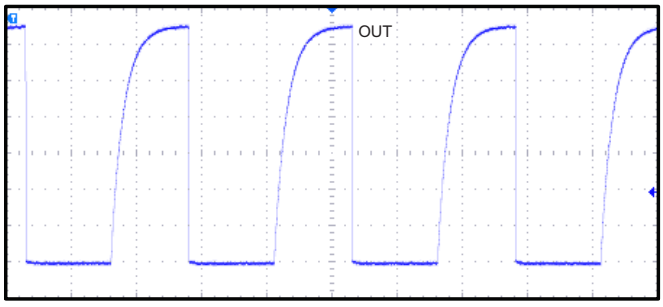
A selection of R1 = 10 kΩ and C2 = 680 pF would cause a low-pass filter with a corner frequency of 23.4 kHz.

8.2.1.3 Application Curves



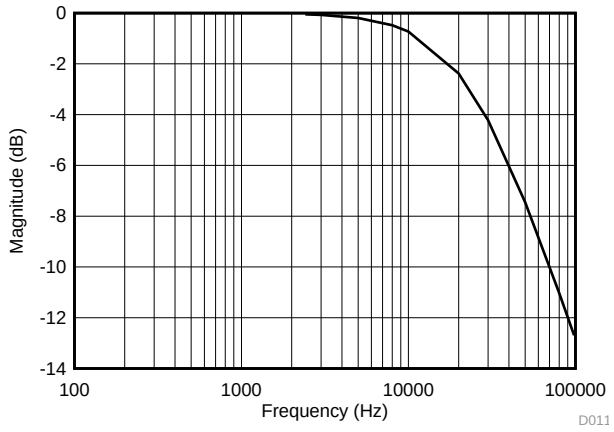
R1 = 10-kΩ pullup No C2

Figure 19. 10-kHz Switching Magnetic Field



R1 = 10-kΩ pullup C2 = 680 pF

Figure 20. 10-kHz Switching Magnetic Field



R1 = 10-kΩ pullup C2 = 680 pF

Figure 21. Low-Pass Filtering

8.2.2 Alternative Two-Wire Application

For systems that require minimal wire count, the device output can be connected to V_{CC} through a resistor, and the total supplied current can be sensed near the controller.

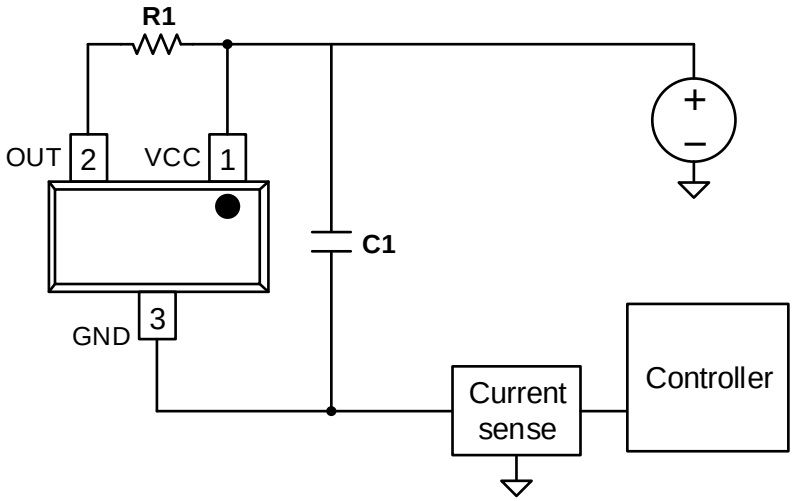


Figure 22. 2-Wire Application

Current can be sensed using a shunt resistor or other circuitry.

8.2.2.1 Design Requirements

Table 4 lists the related design parameters.

Table 4. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{CC}	12 V
OUT resistor	R1	1 kΩ
Bypass capacitor	C1	0.1 µF
Current when B < B_{RP}	$I_{RELEASE}$	About 3 mA
Current when B > B_{OP}	$I_{OPERATE}$	About 15 mA

8.2.2.2 Detailed Design Procedure

When the open-drain output of the device is high-impedance, current through the path equals the I_{CC} of the device (approximately 3 mA).

When the output pulls low, a parallel current path is added, equal to V_{CC} / (R1 + $r_{DS(on)}$). Using 12 V and 1 kΩ, the parallel current is approximately 12 mA, making the total current approximately 15 mA.

The local bypass capacitor C1 should be at least 0.1 µF, and a larger value if there is high inductance in the power line interconnect.

9 Power Supply Recommendations

The DRV5023-Q1 device is designed to operate from an input voltage supply (VM) range between 2.7 and 38 V. A 0.01-µF (minimum) ceramic capacitor rated for V_{CC} must be placed as close to the DRV5023-Q1 device as possible.

10 Device and Documentation Support

10.1 Device Support

10.1.1 Device Nomenclature

Figure 23 shows a legend for reading the complete device name for and DRV5023-Q1 device.

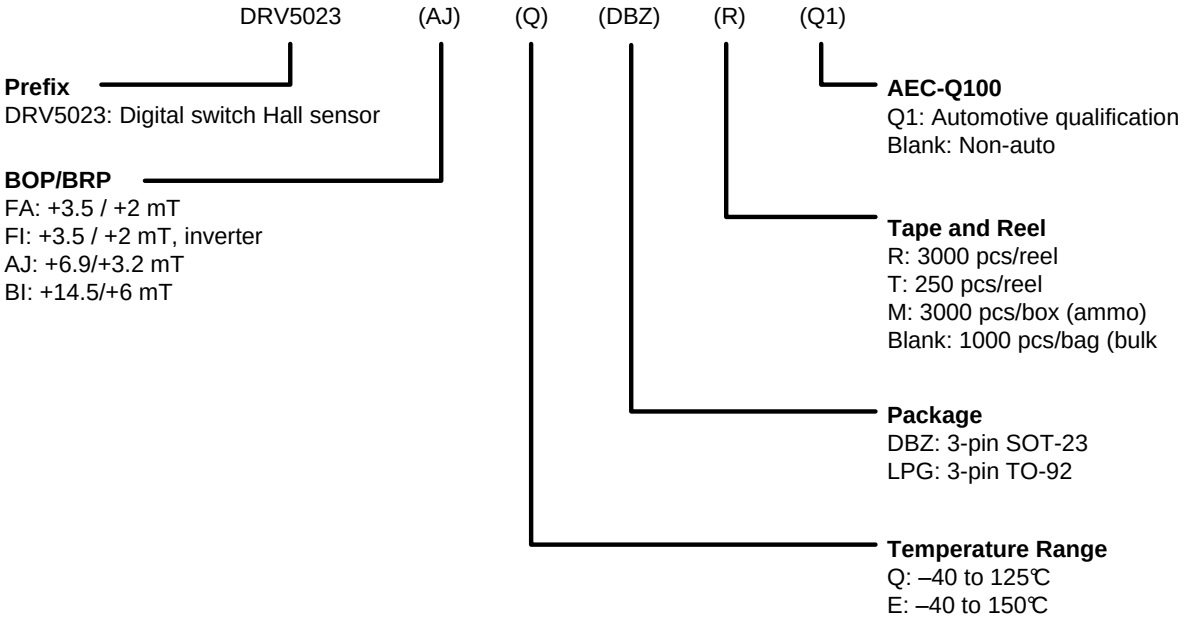


Figure 23. Device Nomenclature

10.1.2 Device Markings

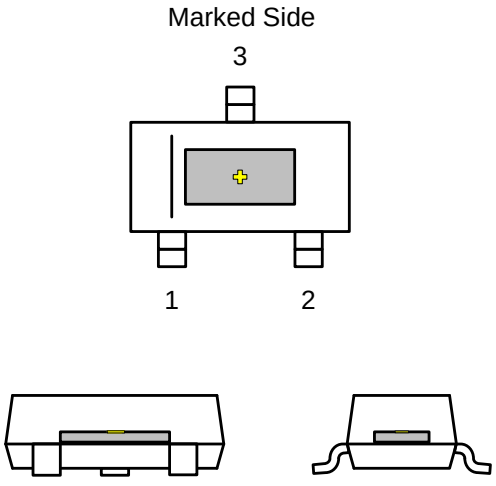


Figure 24. SOT-23 (DBZ) Package

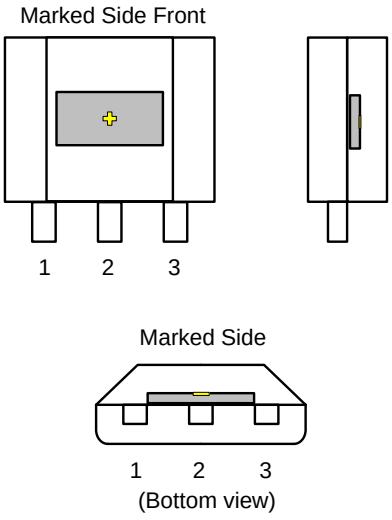


Figure 25. TO-92 (LPG) Package

✚ indicates the Hall effect sensor (not to scale). The Hall element is located in the center of the package with a tolerance of ±100 µm. The height of the Hall element from the bottom of the package is 0.7 mm ±50 µm in the DBZ package and 0.987 mm ±50 µm in the LPG package.

10.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.3 Trademarks

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All other trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV5023AJEDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 150	+PJAJ	Samples
DRV5023AJEDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 150	+PJAJ	Samples
DRV5023AJELPGMQ1	ACTIVE	TO-92	LPG	3	3000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 150	+PJAJ	Samples
DRV5023AJELPGQ1	ACTIVE	TO-92	LPG	3	1000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 150	+PJAJ	Samples
DRV5023AJQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+PKAJ	Samples
DRV5023AJQDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+PKAJ	Samples
DRV5023AJQLPGMQ1	ACTIVE	TO-92	LPG	3	3000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	+PKAJ	Samples
DRV5023AJQLPGQ1	ACTIVE	TO-92	LPG	3	1000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	+PKAJ	Samples
DRV5023BIEDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 150	+PJBI	Samples
DRV5023BIEDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 150	+PJBI	Samples
DRV5023BIELPGMQ1	ACTIVE	TO-92	LPG	3	3000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 150	+PJBI	Samples
DRV5023BIELPGQ1	ACTIVE	TO-92	LPG	3	1000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 150	+PJBI	Samples
DRV5023BIQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+PKBI	Samples
DRV5023BIQDBZTQ1	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+PKBI	Samples
DRV5023BIQLPGMQ1	ACTIVE	TO-92	LPG	3	3000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	+PKBI	Samples
DRV5023BIQLPGQ1	ACTIVE	TO-92	LPG	3	1000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	+PKBI	Samples
DRV5023FAEDBZRQ1	PREVIEW	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	+PJFA	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV5023FIEDBZRQ1	PREVIEW	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	+PJFI	
PDRV5023FAEDBZRQ1	PREVIEW	SOT-23	DBZ	3	3000	TBD	Call TI	Call TI	-40 to 150		
PDRV5023FIEDBZRQ1	PREVIEW	SOT-23	DBZ	3	3000	TBD	Call TI	Call TI	-40 to 150		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF DRV5023-Q1 :

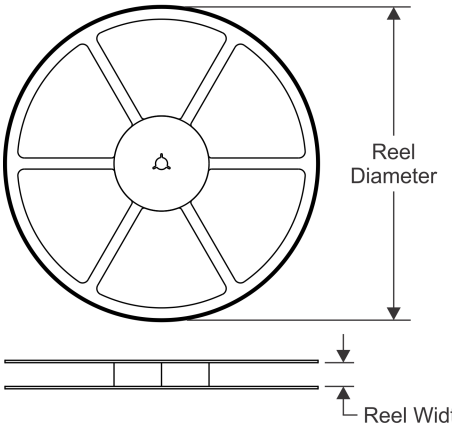
- Catalog: DRV5023

NOTE: Qualified Version Definitions:

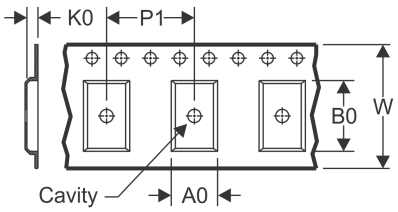
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

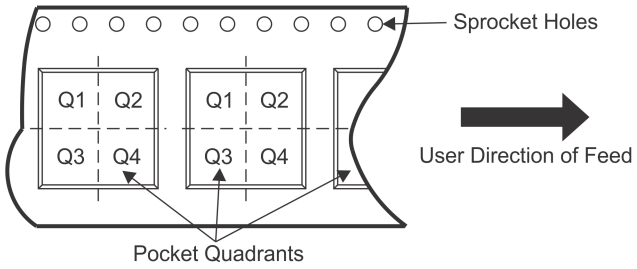


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

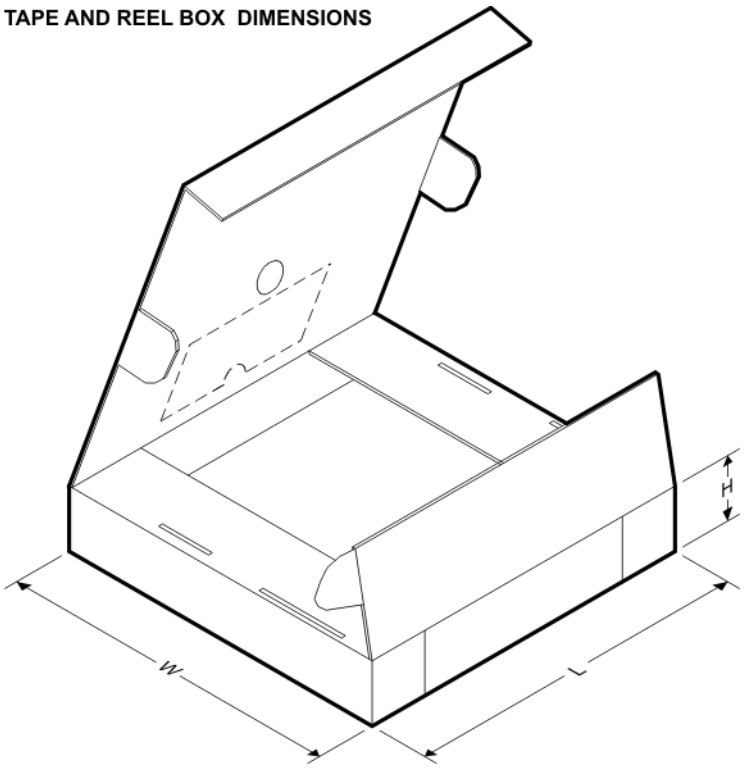
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV5023AJEDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5023AJEDBZTQ1	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5023AJQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5023AJQDBZTQ1	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5023BIEDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5023BIEDBZTQ1	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5023BIQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5023BIQDBZTQ1	SOT-23	DBZ	3	250	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

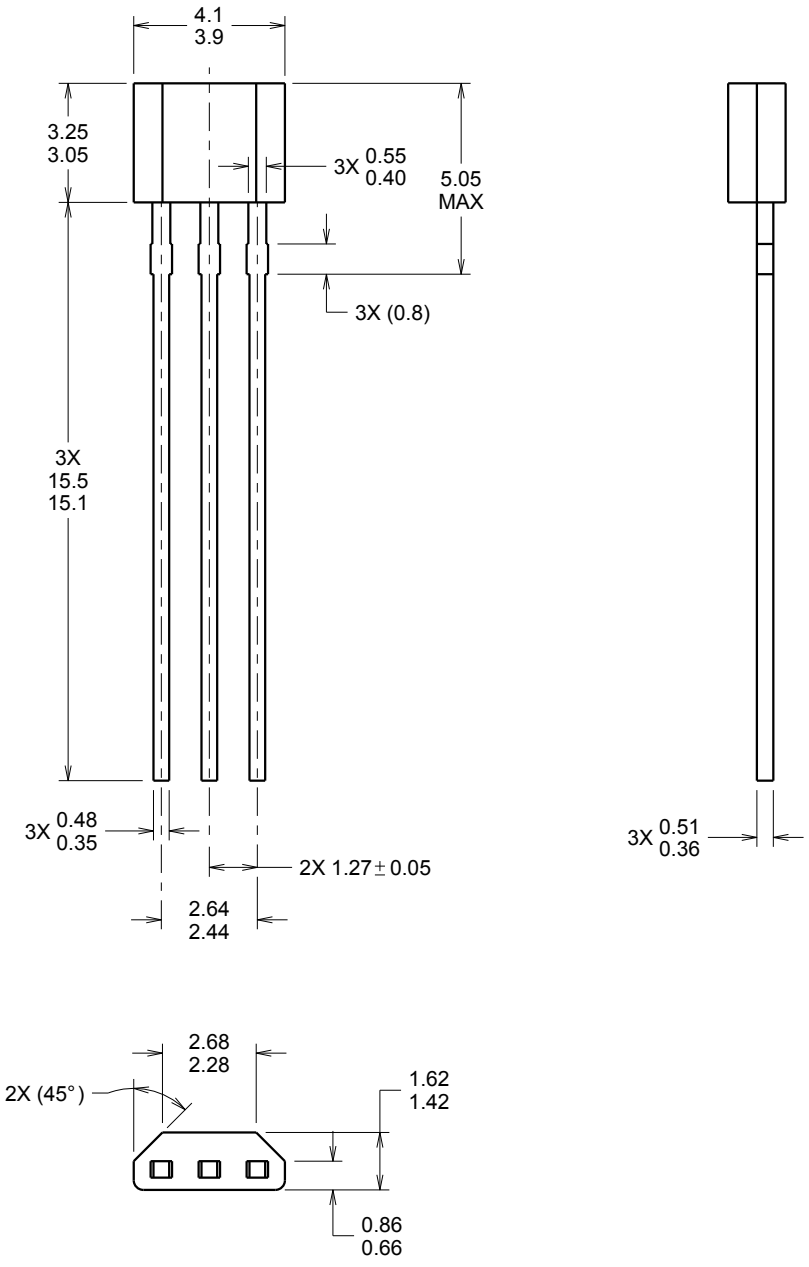
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV5023AJEDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5023AJEDBZTQ1	SOT-23	DBZ	3	250	202.0	201.0	28.0
DRV5023AJQDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5023AJQDBZTQ1	SOT-23	DBZ	3	250	202.0	201.0	28.0
DRV5023BIEDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5023BIEDBZTQ1	SOT-23	DBZ	3	250	202.0	201.0	28.0
DRV5023BIQDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5023BIQDBZTQ1	SOT-23	DBZ	3	250	202.0	201.0	28.0

PACKAGE OUTLINE

LPG0003A

TO-92 - 5.05 mm max height

TO-92

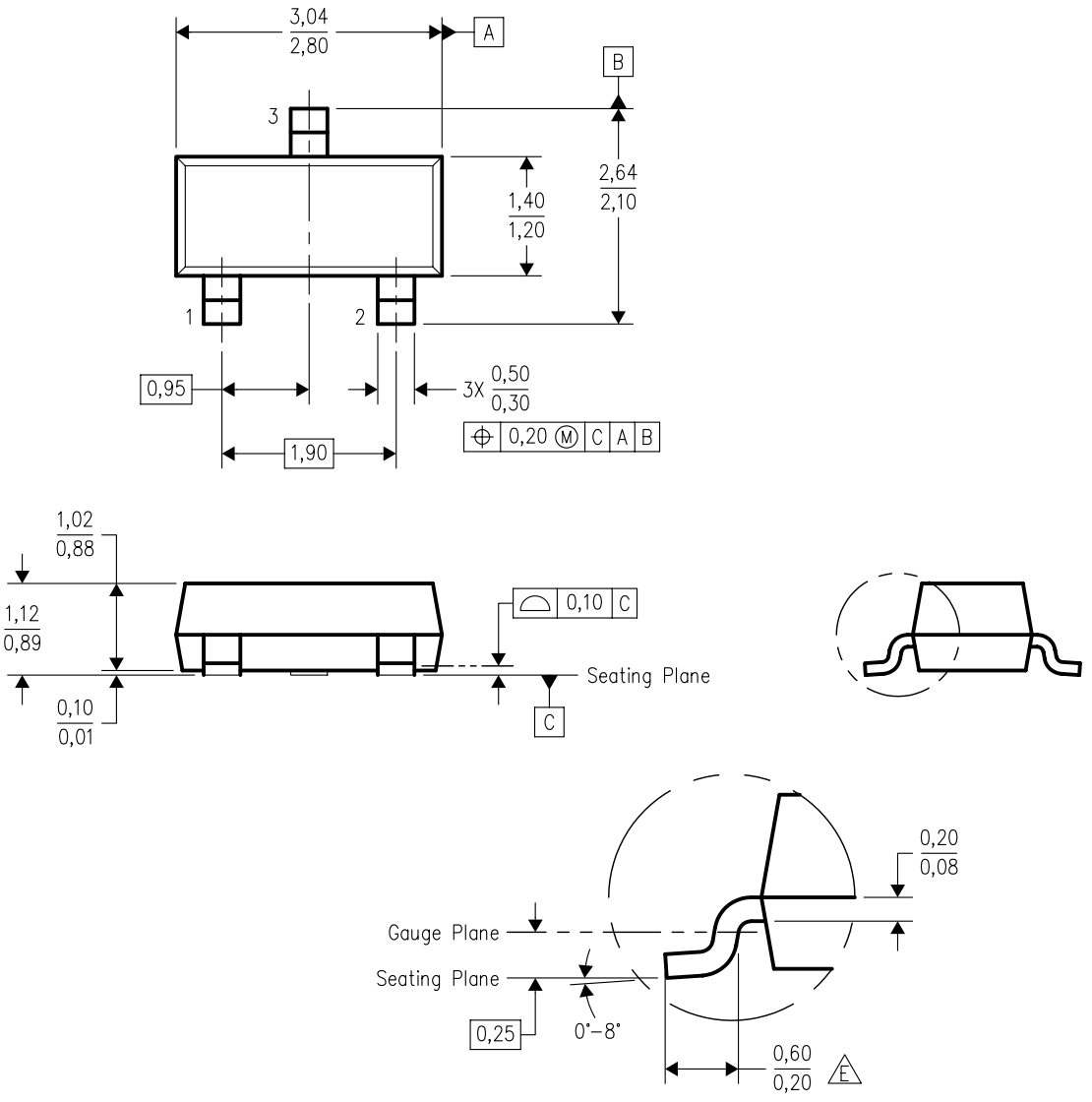


4221343/A 02/2014

NOTES:

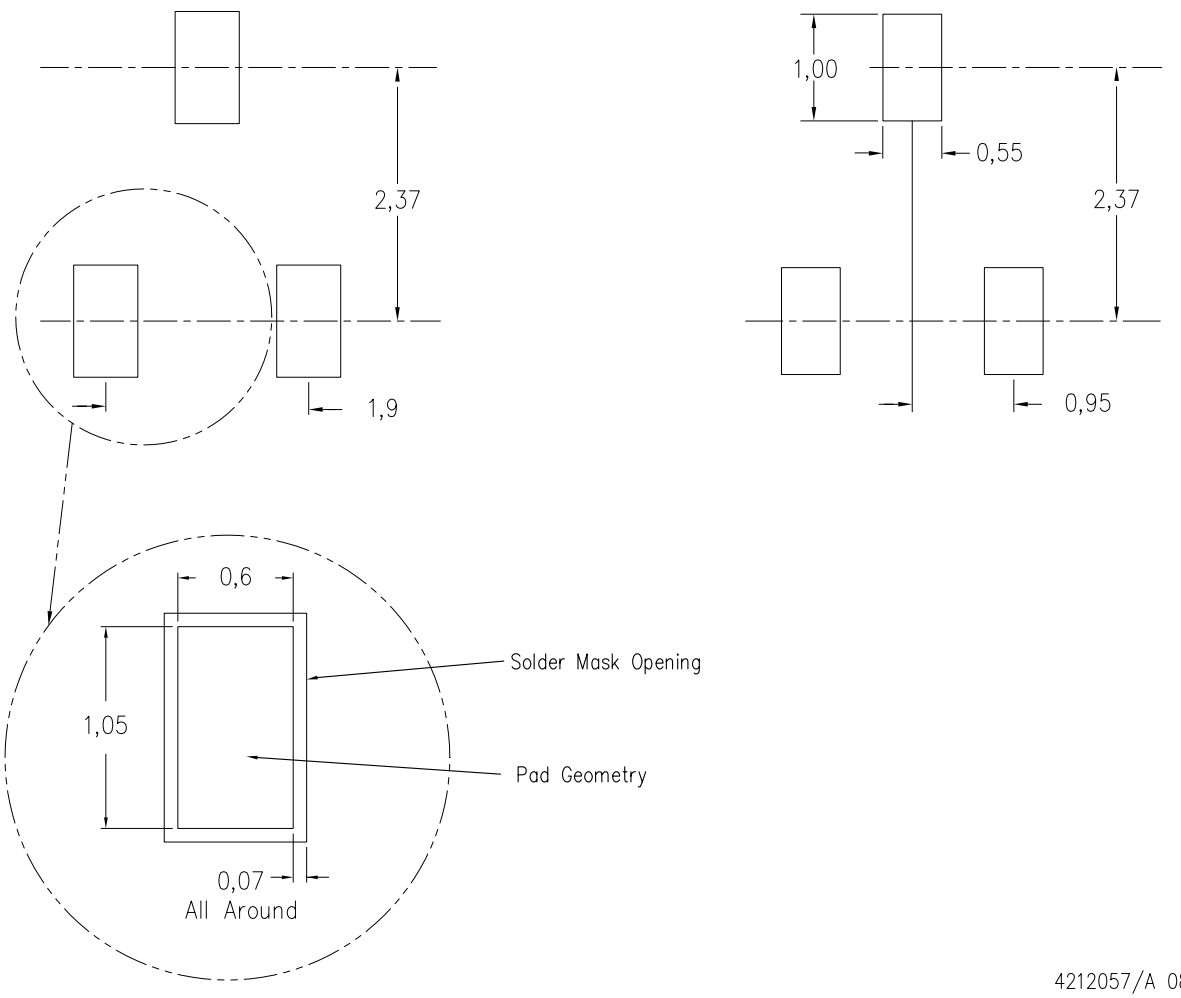
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

DBZ (R–PDSO–G3) PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Lead dimensions are inclusive of plating.
D. Body dimensions are exclusive of mold flash and protrusion. Mold flash and protrusion not to exceed 0.25 per side.
E. Falls within JEDEC TO–236 variation AB, except minimum foot length.

DBZ (R–PDSO–G3) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
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