Preliminary
Subject to Change

PMIC

Flexible Power Management Unit

IRPS5401

FEATURES

- Full power system including 5 integrated outputs
  - o 4A, 4A, 2A and 2A Switching Regulators
  - o 500mA Source/Sink Linear regulator
- Single rail operation 5V to 12V
- Output Range from 0.25V to 5.1V for outputs A-D and 0.5V to 3.6V for LDO
- Allows combining outputs and/or the use of an external PowIRstage to increase output current to as high as 50A
- Emulated current mode control without external compensation
- Differential voltage sensing on Switcher A for higher accuracy
- I2C / PMBus with integrated level shifter
- Advanced Sequencing control
- Extensive PMBus command set of 74 commands
- Integrated current sensing and full telemetry including voltage, current, temperature and faults
- Rated for -40°C to +125°C T_J operation
- Pb-Free, RoHS6, 7x7mm, 56-pin, 0.4mm pitch QFN

DESCRIPTION

The IRPS5401 is a complete power management unit delivering up to 5 output voltages to processors, FPGA's and other multi-rail power systems. Four high efficiency configurable switching regulators and a Source/Sink Linear regulator provide the typical rails required such as core voltage, memory voltage and I/O voltages.

Integrated, accurate current, voltage and temperature sensing allows telemetry and fault reporting through the I2C/PMBus.

The IRPS5401 switching regulators utilize fixed frequency Emulated current mode control, and thus no external compensation is required.

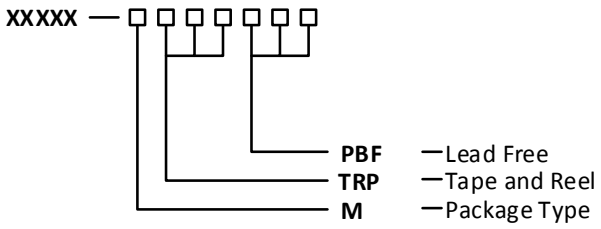
The IRPS5401 is highly flexible. Switchers A and B deliver 2A each. Switchers C and D, deliver 4A each and can also be combined to deliver 8A. Further, Switcher A can be configured to use an external powIRstage® to deliver up to 50A or more.

APPLICATIONS

- High density ASIC, FPGA & CPU multi-rail systems
- Embedded Computing systems
- Communications and Storage systems

ORDERING INFORMATION

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRPS5401	QFN 7 mm x 7 mm	Tape and Reel	3000	IRPS5401MTRPBF



BASIC APPLICATION

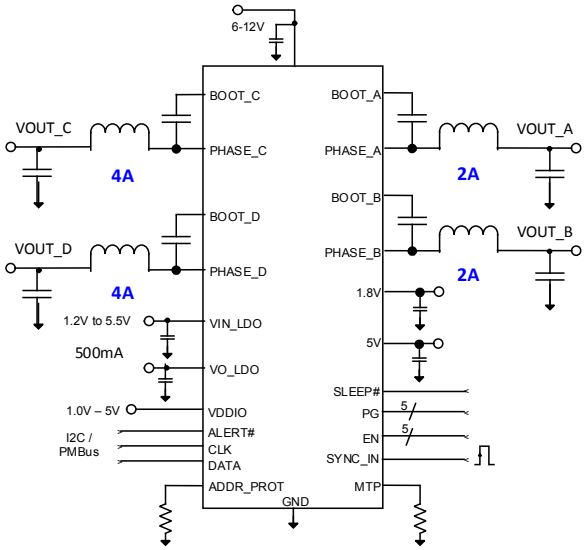


Figure 1: IRPS5401 Basic Application Circuit

Figure 2: Performance Curve

PINOUT DIAGRAM

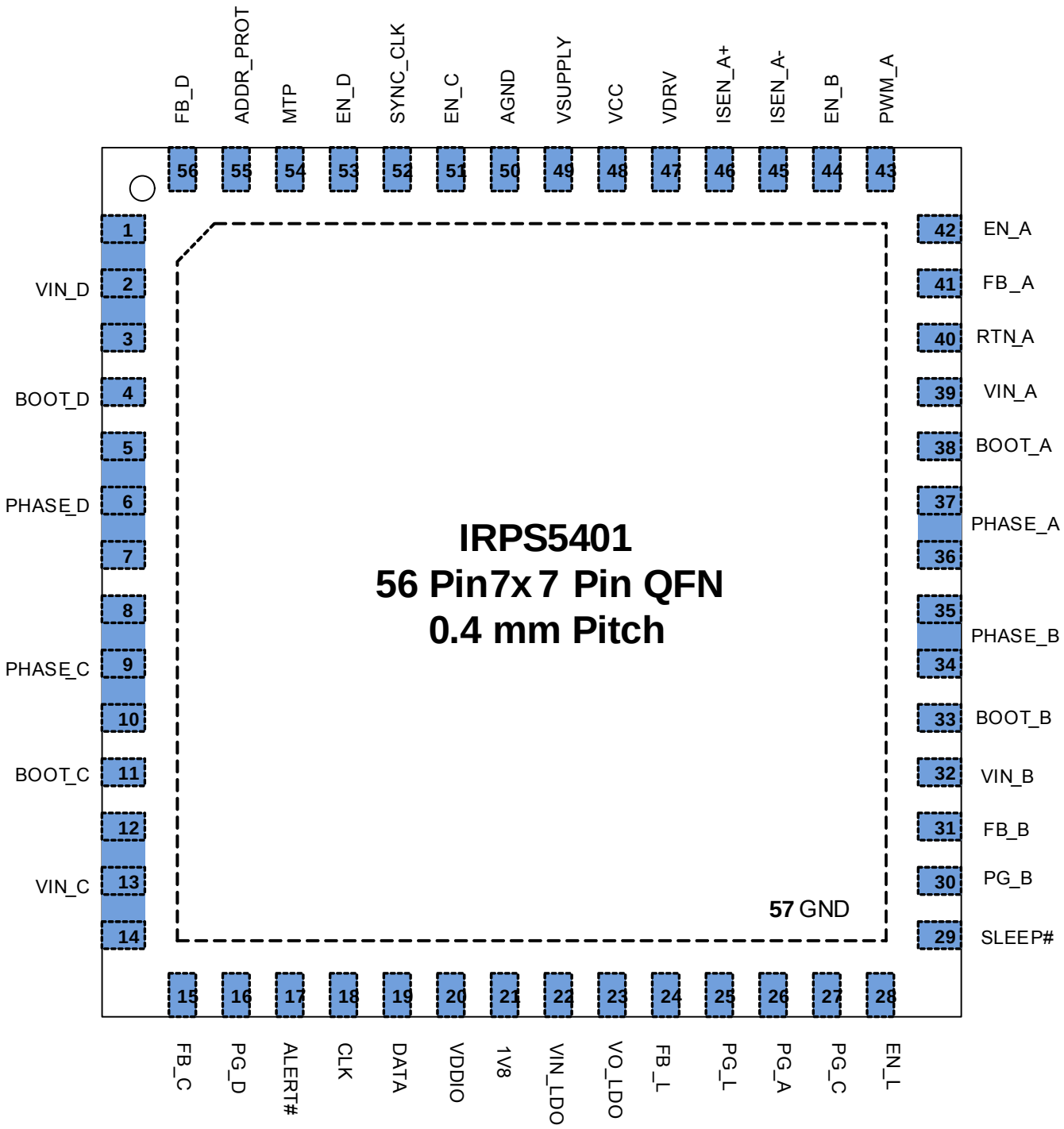


Figure 3: 7mm x 7mm QFN (Top View)

PIN FUNCTION

PIN				IF NOT USED
#	NAME	TYP	DESCRIPTION	
1,2,3	VIN_D	P [I]	Input supply voltage pins for Switcher D. Decouple locally by connecting a ceramic capacitor from this pin to GND.	Short To GND
4	BOOT_D	A [B]	Supply input for Switcher D high side FET gate drive. Connect a 0.1uF MLCC between this pin and PHASE_ D pins. An internal diode is connected between VDRV and this pin	Open
5,6,7	PHASE_D	P [O]	Switch node of Switcher D. Connect directly to the output inductor.	
8,9,10	PHASE_C	P [O]	Switch node of Switcher C. Connect directly to the output inductor.	
11	BOOT_C	A [B]	Supply input for Switcher C high side FET gate drive. Connect a 0.1uF MLCC between this pin and PHASE_C pins. An internal diode is connected between VDRV and this pin	
12,13, 14	VIN_C	P [I]	Input supply voltage pins for Switcher C. Decouple locally by connecting a ceramic capacitor from this pin to GND.	Short To GND
15	FB_C	A [I]	Switcher C feedback input. Connect directly to VOUT_C for output voltages less than 2.55V. Connect to VOUT_C with a 2:1 resistor divider for output voltages greater than 2.55V.	Open
16	PG_D	D [O]	Open drain power good output indicating Switcher D is powered up	
17	ALERT#	D [O]	I2C/PMBus Alert line. This alert signal can indicate one or more faults, allowing the system bus manager to poll the device and identify the root cause. All faults or customer selected faults such as overcurrent or over-temperature may be specifically masked to this pin.	
18	CLK	D [B]	I2C/PMBus Data Line. Pull up to VDDIO with 4.7K	n/a
19	DATA	D [B]	I2C/PMBus Clock Line. Pull up to VDDIO with 4.7K	
20	VDDIO	P [I]	Pull-up signal voltage for I2C communications. Connect to the same I/O rail used by the I2C master.	
21	1V8	A [O]	1.8V reference used by the device for internal analog and digital control. Decouple using a 1.0uF X7R type ceramic capacitor	
22	VIN_LDO	P [I]	Input to the linear regulator. See linear regulator section for specific requirements. This voltage can range from 1.2V to 5.5V, with restrictions on overall power dissipation	Short To GND
23	VO_LDO	A[O]	LDO output	Open
24	FB_L	A [I]	LDO feedback input	
25	PG_L	D[I]	Open drain power good output indicating LDO is powered up. Pull up to 5V with 10K	
26	PG_A	D[I]	Open drain power good output indicating switcher A is powered up. Pull up to 5V with 10K	
27	PG_C	D[I]	Open drain power good output indicating switcher C is powered up. Pull up to 5V with 10K	
28	EN_L	D[I]	LDO enable input control. Active High, external termination required, do not leave floating. LVTTL threshold levels. 'ON' threshold is 2.1V minimum	Short To GND
29	SLEEP#	D[I]	Active low signal to place the device in a low power mode LVTTL threshold levels. 'SLEEP ENABLED' threshold is 0.8V maximum	Short to Vcc
30	PG_B	D[I]	Open drain power good output indicating switcher B is powered up. Pull up to 5V with 10K	Open
31	FB_B	A [I]	Switcher B feedback input. Connect directly to VOUT_B for output voltages less than 2.55V. Connect to VOUT_B with a 2:1 resistor divider for output voltages greater than 2.55V.	Open
32	VIN_B	P [I]	Input supply voltage pin for Switcher B. Decouple locally by connecting a ceramic capacitor from this pin to GND.	Short To GND
33	BOOT_B	A [B]	Supply input for Switcher B high side FET gate drive. Connect a 0.1uF MLCC between this pin and PHASE_ B pins. An internal diode is connected between VDRV and this pin	Open
34,35	PHASE_B	P [O]	Switch node of Switcher B. Connect directly to the output inductor.	
36,37	PHASE_A	P [O]	Switch node of Switcher A. Connect directly to the output inductor.	

PIN				IF NOT USED
#	NAME	TYP	DESCRIPTION	
38	BOOT_A	A [B]	Supply input for Switcher A high side FET gate drive. Connect a 0.1uF MLCC between this pin and PHASE_A pins. An internal diode is connected between VDRV and this pin	
39	VIN_A	P [I]	Input supply voltage pin for Switcher A. Decouple locally by connecting a ceramic capacitor from this pin to GND.	Short To GND
40	RTN_A	A [I]	Differential feedback return signal for Switcher A. This can be connected remotely to the return location of VOUT_A.	Short together
41	FB_A	A [I]	Differential feedback positive signal for Switcher A. Connect directly to VOUT_A for output voltages less than 2.55V. Connect to VOUT_A with a 2:1 resistor divider for output voltages greater than 2.55V.	
42	EN_A	D [I]	Switcher A enable input control; external termination required, do not leave floating. LVTTL threshold levels. 'ON' threshold is 2.1V minimum	Short To GND
43	PWM_A	A [O]	PWM signal for Switcher A to be used when Switcher A is configured for use with an external powIRstage®. This PWM pin drives a powIRstage® such as an IR3555 powIRstage®, and is a tri-state or tri-level signal. Leave floating if this pin is not used	Open
44	EN_B	D [I]	Switcher B enable input control; external termination required, do not leave floating. LVTTL threshold levels. 'ON' threshold is 2.1V minimum	Short To GND
45	ISEN_A-	A[I]	Negative (return) sense point for Switcher A external IOUT sense.	Short together
46	ISEN_A+	A[I]	Positive sense point for Switcher A external IOUT sense.	
47	VDRV	A [O]	5V drive voltage used to power the internal MOSFET drivers. Use a 2Ω, 1uF filter from VCC to insure noise from this switching node is not injected into the VCC pin. See the application section. Terminate decoupling cap to GND (pin 57)	n/a
48	VCC	A [O]	5V source used by the device to power internal analog and digital control. When VCC is self-generated by the device (from VSUPPLY), do not load this pin with any load other than VDRV. Decouple using a 1uF X7R type ceramic capacitor. Terminate decoupling cap to AGND (pin 50)	
49	VSUPPLY	A [I]	Input voltage for internal LDO for internally generated VCC	Short to Vcc
50	AGND		Ground reference for the analog and digital control.	n/a
51	EN_C	D[I]	Switcher C enable input control; external termination required, do not leave floating. LVTTL threshold levels. 'ON' threshold is 2.1V minimum	Short To GND
52	SYNC_CLK	D[I]	External Synchronization pin. LVTTL threshold levels. 'HIGH' threshold is 2.1V minimum, 'LOW' is 0.8V maximum	
53	EN_D	D [I]	Switcher D enable input control; external termination required, do not leave floating. LVTTL threshold levels. 'ON' threshold is 2.1V minimum	
54	MTP	A [I]	A resistor placed to ground on this pin selects which of 15 MTP banks of memory are used. By allowing up to 15 MTP memory banks, a user can use up to 15 identical IRPS5401 devices on a single board using just one customer-configuration file. If this pin is above 2V when POR occurs, the device will not load OTP and the I2C address will be 0Ah. Decouple with 0.01uF cap.	n/a
55	ADDR_PROT		Use a resistor on this pin to set the I2C and/or PMBus Address offset for the device If the I2C register R/W protect security function is used and 'PIN' protect is enabled, this pin must be asserted high to disable the R/W protection. Decouple with 0.01uF cap.	
56	FB_D	A [I]	Switcher D feedback input. Connect directly to VOUT_D for output voltages less than 2.55V. Connect to VOUT_D with a 2:1 resistor divider for output voltages greater than 2.55V.	Open
57	GND		Ground. The large metal pad on the bottom must be connected to Ground.	n/a

BLOCK DIAGRAM

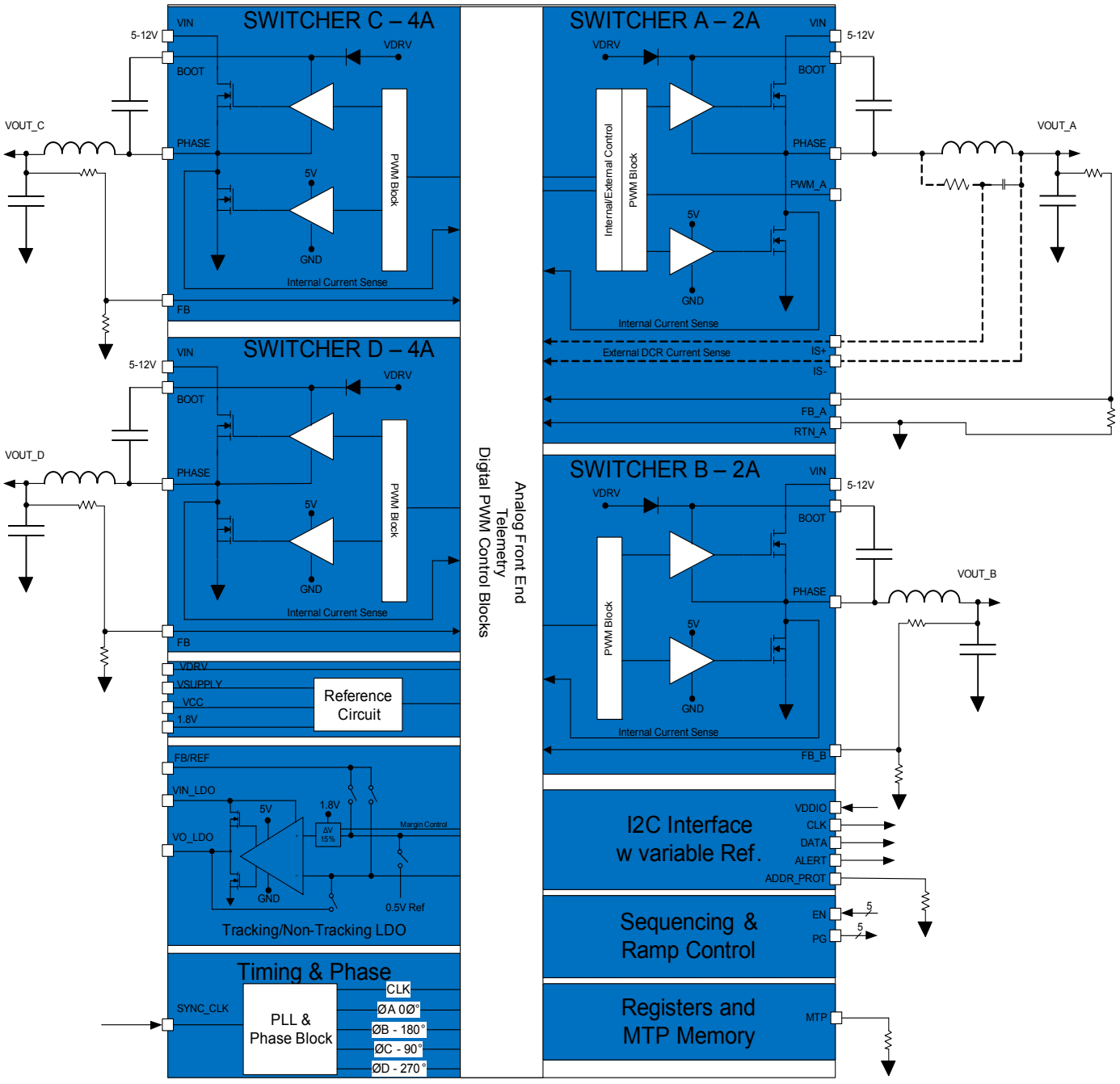


Figure 4: IRPS5401 Block Diagram

ABSOLUTE MAXIMUM RATINGS

Stresses beyond these listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

Voltage Ratings	
Vin [A_B_C_D], VSUPPLY	-0.3V to 16V
VCC, VDRIVE	-0.3V to 6V
1V8	-0.3V to 2V
BOOT [A_B_C_D]	-0.3V to 22V
BOOT [A_B_C_D] <10nS transient	-0.3V to 24V
SW [A_B_C_D]	-0.3V to 16V
SW [A_B_C_D] <10nS transient	-4V to 18V
BOOT to SW [A_B_C_D]	-0.3V to Vcc +0.3V (Note1)
Input / Output Pins	-0.3V to Vcc +0.3V (Note1)
GND to AGND	-0.3V to +0.3V
THERMAL INFORMATION	
Junction to Ambient Thermal Resistance Θ_{JA}	13.5°C/W
Junction to PCB Thermal Resistance $\Theta_{J\text{-}PCB}$	3°C/W
Maximum Storage Temperature Range	-55°C To 150°C
Maximum Junction Operating Temperature Range	-40°C To 125°C (Note 2)
Maximum Lead Temperature (Soldering 10s)	300°C

(Voltages referenced to GND unless otherwise specified)

Note 1: Must not exceed 6V.
Note 2: Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.