Infineon® Power LED Driver

TLD5097EL

Multitopology High Power LED DC/DC IC

Datasheet

Rev. 1.0, 2013-11-12

Automotive Power

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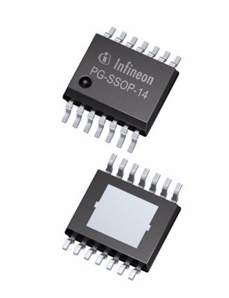
TLD5097EL

1 Overview



PG-SSOP-14

Features

- Wide Input Voltage Range from 4.5 V to 45 V
- Constant Current or Constant Voltage Regulation
- Drives LEDs in Boost, Buck, Buck-Boost, SEPIC and Flyback Topology
- Very Low Shutdown Current: I_{q_OFF} < 10 µA
- Flexible Switching Frequency Range, 100 kHz to 500 kHz
- Synchronization with external clock source
- PWM Dimming
- Analog Dimming feature to adjust average LED current
- Internal 5 V Low Drop Out Voltage Regulator
- Open Circuit Detection
- Output Overvoltage Protection
- Internal Soft Start
- Over Temperature Shutdown
- Wide LED current range via simple adaptation of external components
- 300mV High Side Current Sense to ensure highest flexibility and LED current accuracy
- Available in a small thermally enhanced PG-SSOP-14 package
- Automotive AEC Qualified
- Green Product (RoHS) Compliant

Description

The TLD5097EL is a LED boost controller with built in protection features. The main function of this device is to regulate a constant LED current. The constant current regulation is especially beneficial for LED color accuracy and longer lifetime. The controller concept of the TLD5097EL allows multiple configurations such as Boost, Buck, Buck-Boost, SEPIC and Flyback by simply adjusting the external components. The TLD5097EL offers the most flexible dimming options. Dimming can be achieved with analog or PWM input.The switching frequency is adjustable in the range of 100 kHz to 500 kHz and can be synchronized to an external clock source. The TLD5097EL features an enable function reducing the shut-down current consumption to I_{q_OFF} < 10 µA. The current mode regulation scheme of this device provides a stable regulation loop maintained by small external compensation components. The integrated soft start feature limits the current peak as well as voltage overshoot at start-up. This IC is suited for use in the harsh automotive environments and provides output overvoltage protection and device overtemperature shutdown.

Applications

- Automotive Exterior and Interior Lighting

Type	Package	Marking
TLD5097EL	PG-SSOP-14	TLD5097

2 Block Diagram

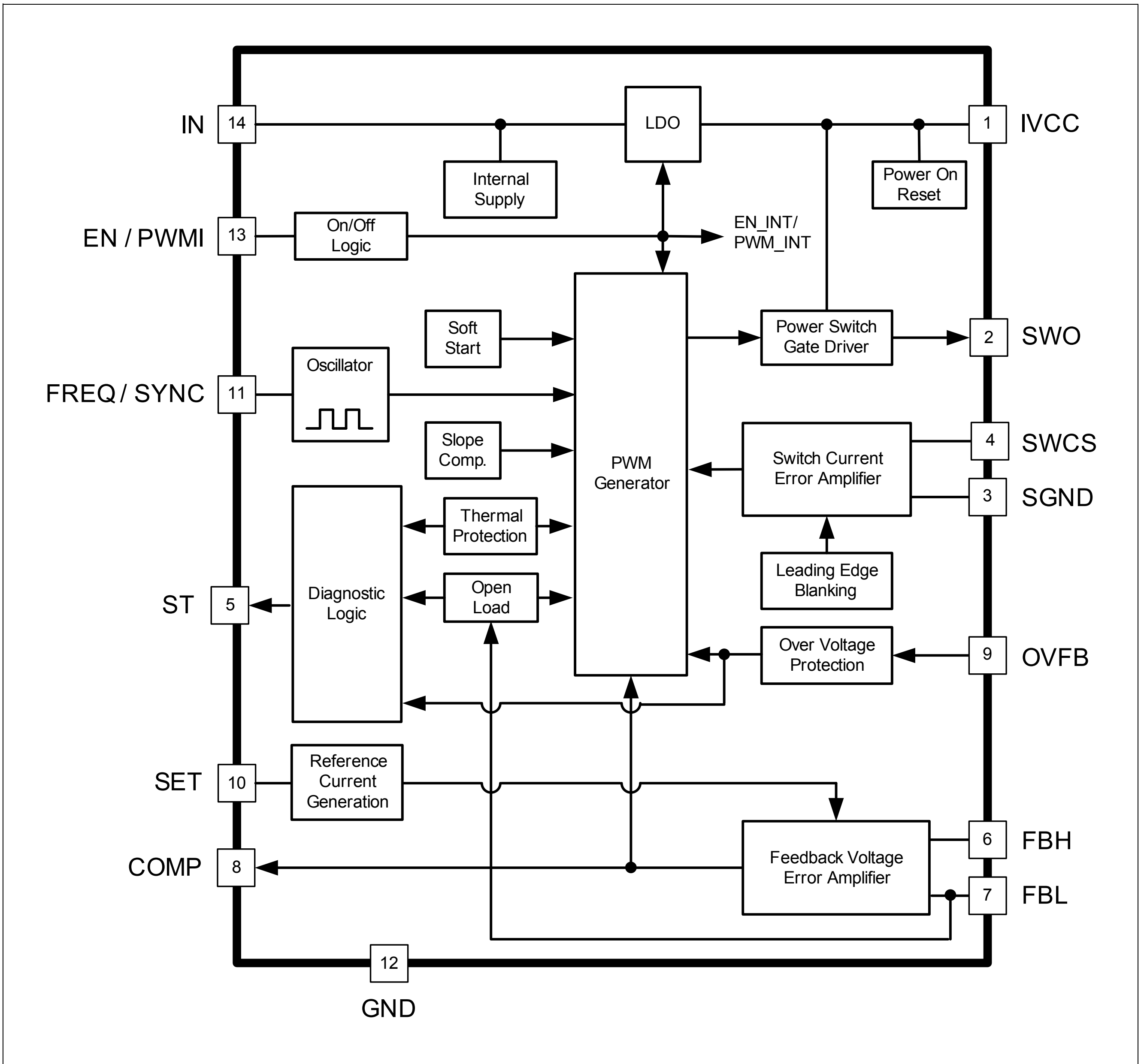


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

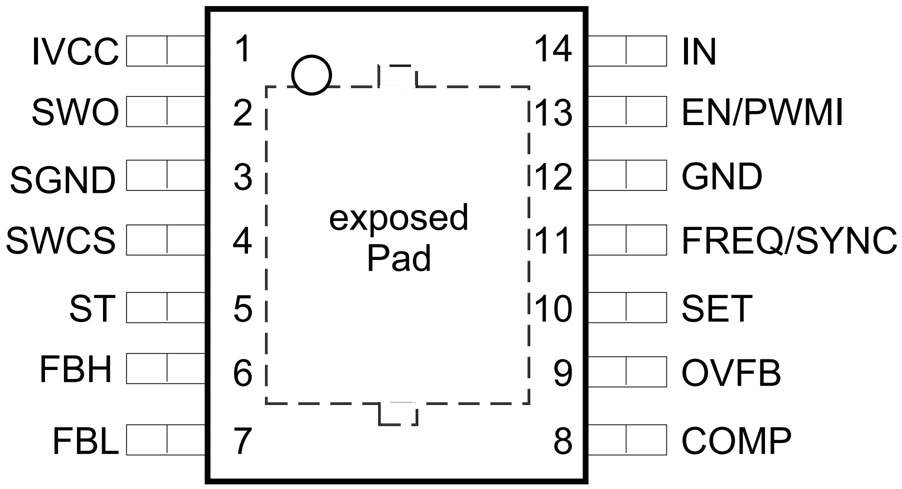


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	IVCC	**Internal LDO Output;** Used for internal biasing and gate drive. Bypass with external capacitor close to the pin. Pin must not be left open.
2	SWO	**Switch Output;** Connect to gate of external switching MOSFET
3	SGND	**Current Sense Ground;** Ground return for current sense switch
4	SWCS	**Current Sense Input;** Detects the peak current through switch
5	ST	**Status Output;** to indicate fault conditions
6	FBH	**Voltage Feedback Positive;** Non inverting Input (+)
7	FBL	**Voltage Feedback Negative;** Inverting Input (-)
8	COMP	**Compensation Input;** Connect R and C network to pin for stability

Pin	Symbol	Function
9	OVFB	**Output Overvoltage Protection Feedback;** Connect to resistive voltage divider to set overvoltage threshold.
10	SET	**Analog Dimming Input;** Load current adjustment Pin. Pin must not be left open. If analog dimming feature is not used connect to IVCC pin.
11	FREQ / SYNC	**Frequency Select or Synchronization Input;** Connect external resistor to GND to set frequency. Or apply external clock signal for synchronization within frequency capture range.
12	GND	**Ground;** Connect to system ground.
13	EN / PWMI	**Enable or PWM Input;** Apply logic HIGH signal to enable device or PWM signal for dimming LED.
14	IN	**Supply Input;** Supply for internal biasing.
EP		**Exposed Pad;** Connect to external heatspreading GND Cu area (e.g. inner GND layer of multilayer PCB with thermal vias).

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings[1)]

T_j = -40 ·C to +150 ·C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	IN Supply Input	V_{IN}	-0.3	45	V	–
4.1.2	EN / PWMI Enable or PWM Input	V_{EN}	-40	45	V	–
4.1.3	FBH-FBL Feedback Error Amplifier Differential	V_{FBH}-V_{FBL}	-40	61	V	The maximum delta must not exceed 61V
4.1.4	FBH Feedback Error Amplifier Positive Input	V_{FBH}	-40	61	V	The difference between V_{FBH} and V_{FBL} must not exceed 61V, refer to Parameter 4.1.3
4.1.5	FBL Feedback Error Amplifier Negative Input	V_{FBL}	-40	61	V	The difference between V_{FBH} and V_{FBL} must not exceed 61V, refer to Parameter 4.1.3
4.1.6	FBH and FBL current	$I_{FBL,FBH}$	–	1	mA	t < 100ms, V_{FBH} - V_{FBL} = 0.3V
4.1.7	OVFB Over Voltage Feedback Input	V_{OVP}	-0.3	5.5	V	–
4.1.8			-0.3	6.2	V	t < 10s
4.1.9	SWCS Switch Current Sense Input	V_{SWCS}	-0.3	5.5	V	–
4.1.10			-0.3	6.2	V	t < 10s
4.1.11	SWO Switch Gate Drive Output	V_{SWO}	-0.3	5.5	V	–
4.1.12			-0.3	6.2	V	t < 10s
4.1.13	SGND Current Sense Switch GND	V_{SGND}	-0.3	0.3	V	–
4.1.14	COMP Compensation Input	V_{COMP}	-0.3	5.5	V	–
4.1.15			-0.3	6.2	V	t < 10s
4.1.16	FREQ / SYNC; Frequency and Synchronization Input	$V_{FREQ / SYNC}$	-0.3	5.5	V	–
4.1.17			-0.3	6.2	V	t < 10s
4.1.18	ST	V_{ST}	-0.3	5.5	V	–
4.1.19			-0.3	6.2	V	t < 10s
4.1.20	ST current	I_{ST}	-2	2	mA	–
4.1.21	SET	V_{SET}	-0.3	45	V	–
4.1.22	IVCC Internal Linear Voltage Regulator Output	V_{IVCC}	-0.3	5.5	V	–
4.1.23			-0.3	6.2	V	t < 10s
Temperatures						

Absolute Maximum Ratings[1)]

T_j = -40 ·C to +150 ·C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.1.24	Junction Temperature	T_j	-40	150	°C	–
4.1.25	Storage Temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.26	ESD Resistivity of all Pins	$V_{ESD,HBM}$	-2	2	kV	HBM[2)]
4.1.27	ESD Resistivity of IN, EN/PWMI, FBH, FBL and SET pin to GND	$V_{ESD,HBM}$	-4	4	kV	HBM[2)]

1) Not subject to production test, specified by design.

2) ESD susceptibility, Human Body Model “HBM” according to ANSI/ESDA/JEDEC JS-001 (1.5kΩ, 100pF)

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Extended Supply Voltage Range	V_{IN}	4.5	45[1)]	V	$V_{IVCC} > V_{IVCC,RTH,d;}$ Parameter deviations possible
4.2.2	Nominal Supply Voltage Range	V_{IN}	8	34	V	–
4.2.3	Feedback Voltage Input	$V_{FBH;}$ V_{FBL}	3	60	V	–
4.2.4	Junction Temperature	T_j	-40	150	°C	–

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to ***www.jedec.org***.

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case[1) 2)]	R_{thJC}	–	10	–	K/W	–
4.3.2	Junction to Ambient[1) 3)]	R_{thJA}	–	47	–	K/W	2s2p
4.3.3		R_{thJA}	–	54	–	K/W	1s0p + 600 mm^2
4.3.4		R_{thJA}	–	64	–	K/W	1s0p + 300 mm^2

1) Not subject to production test, specified by design.

2) Specified RthJC value is simulated at natural convection on a cold plate setup (all pins and the exposed pad are fixed to ambient temperature). Ta=25°C; The IC is dissipating 1W.

3) Specified R_{thJA} value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board; The device was simulated on a 76.2 x 114.3 x 1.5 mm board. The 2s2p board has 2 outer copper layers (2 x 70µm Cu) and 2 inner copper layers (2 x 35µm Cu). A thermal via (diameter = 0.3 mm and 25 µm plating) array was applied under the exposed pad and connected the first outer layer (top) to the first inner layer and second outer layer (bottom) of the JEDEC PCB. Ta=25°C; The IC is dissipating 1W.

5 Switching Regulator

5.1 Description

The TLD5097EL regulator is suitable for Boost, Buck, Buck-Boost, SEPIC and Flyback configurations. The constant output current is especially useful for light emitting diode (LED) applications. The switching regulator function is implemented by a pulse width modulated (PWM) current mode controller.

The PWM current mode controller uses the peak current through the external power switch and error in the output current to determine the appropriate pulse width duty cycle (on time) for constant output current. The current mode controller provides a PWM signal to an internal gate driver which then outputs to an external n-channel enhancement mode metal oxide field effect transistor (MOSFET) power switch.

The current mode controller also has built-in slope compensation to prevent sub-harmonic oscillations which is a characteristic of current mode controllers operating at high duty cycles (>50% duty).

An additional built-in feature is an integrated soft start that limits the current through the inductor and external power switch during initialization. The soft start function gradually increases the inductor and switch current over t_{SS} (Parameter 5.2.9) to minimize potential overvoltage at the output.

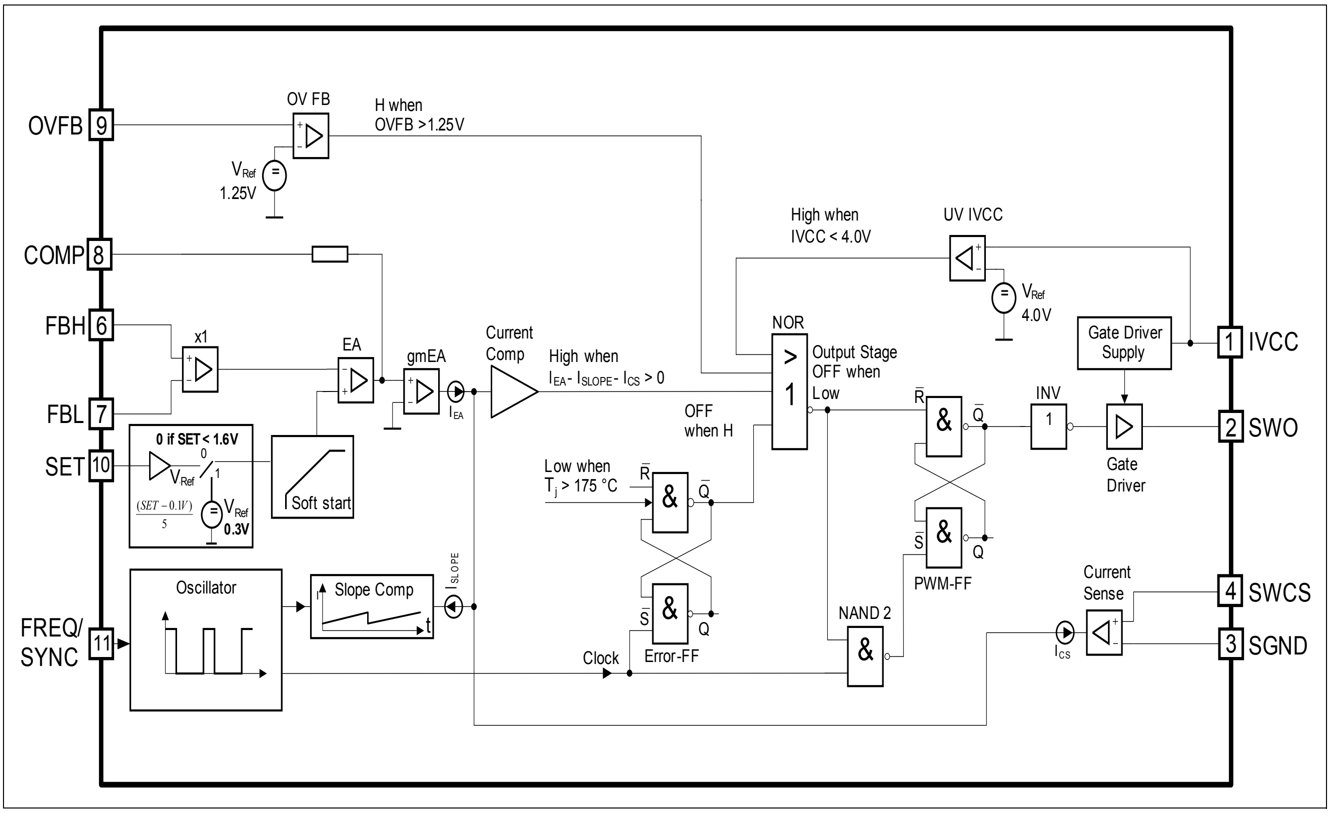


Figure 3 Switching Regulator Block Diagram

5.2 Electrical Characteristics

1)

Table 1 EC Switching Regulator

V_{IN} = 8V to 34V; T_j = -40 ·C to +150 ·C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Regulator:							
5.2.1	Feedback Reference Voltage	V_{REF}	0.29	0.30	0.31	V	refer to **Figure 28** $V_{REF} = V_{FBH} - V_{FBL}$ V_{SET} = 5V I_{LED} = 350 mA
5.2.2	Feedback Reference Voltage	V_{REF}	0.057	0.06	0.063	V	refer to **Figure 28** $V_{REF} = V_{FBH} - V_{FBL}$ V_{SET} = 0.4V I_{LED} = 70mA
5.2.3	Feedback Reference Voltage Offset	V_{REF_offset}	–	–	5	mV	refer to **Figure 16** and **Figure 28** $V_{REF} = V_{FBH} - V_{FBL}$ V_{SET} = 0.1V $V_{OUT} > V_{IN}$
5.2.4	Voltage Line Regulation	$(\Delta V_{REF} / V_{REF}) / \Delta V_{IN}$	–	–	0.15	%/V	refer to **Figure 28** V_{IN} = 8V to 19V; V_{SET} = 5V; I_{LED} = 350mA
5.2.5	Voltage Load Regulation	$(\Delta V_{REF} / V_{REF}) / \Delta I_{BO}$	–	–	5	%/A	refer to **Figure 28** V_{SET} = 5V; I_{LED} = 100 to 500mA
5.2.6	Switch Peak Over Current Threshold	V_{SWCS}	130	150	170	mV	$V_{FBH} = V_{FBL}$ = 5V V_{COMP} = 3.5V
5.2.7	Maximum Duty Cycle	$D_{MAX,fixed}$	91	93	95	%	Fixed frequency mode
5.2.8	Maximum Duty Cycle	$D_{MAX,sync}$	88	–	–	%	Synchronization mode
5.2.9	Soft Start Ramp	t_{SS}	350	1000	1500	µs	V_{FB} rising from 5% to 95% of V_{FB}, typ.
5.2.10	IFBH Feedback High Input Current	I_{FBH}	38	46	54	µA	$V_{FBH} - V_{FBL}$ = 0.3V
5.2.11	IFBL Feedback Low Input Current	I_{FBL}	15	21	27	µA	$V_{FBH} - V_{FBL}$ = 0.3V
5.2.12	Switch Current Sense Input Current	I_{SWCS}	10	50	100	µA	V_{SWCS} = 150mV
5.2.13	Input Undervoltage Shutdown	$V_{IN,off}$	3.5	–	4.5	V	V_{IN} decreasing
5.2.14	Input Voltage Startup	$V_{IN,on}$	–	–	4.85	V	V_{IN} increasing

1) Not subject to production test, specified by design

Table 1 EC Switching Regulator

V_{IN} = 8V to 34V; T_j = -40 ·C to +150 ·C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Gate Driver for external Switch							
5.2.15	Gate Driver Peak Sourcing Current	$I_{SWO,SRC}$	–	380	–	mA	[1] V_{SWO} = 1V to 4V
5.2.16	Gate Driver Peak Sinking Current	$I_{SWO,SNK}$	–	550	–	mA	[1] V_{SWO} = 4V to 1V
5.2.17	Gate Driver Output Rise Time	$t_{R,SWO}$	–	30	60	ns	[1] $C_{L,SWO}$ = 3.3nF; V_{SWO} = 1V to 4V
5.2.18	Gate Driver Output Fall Time	$t_{F,SWO}$	–	20	40	ns	[1] $C_{L,SWO}$ = 3.3nF; V_{SWO} = 4V to 1V
5.2.19	Gate Driver Output Voltage	V_{SWO}	4.5	–	5.5	V	[1] $C_{L,SWO}$ = 3.3nF;

1) Not subject to production test, specified by design

6 Oscillator and Synchronization

6.1 Description

The internal oscillator is used to determine the switching frequency of the boost regulator. The switching frequency can be selected from 100 kHz to 500 kHz with an external resistor to GND. To set the switching frequency with an external resistor the following formula can be applied.

$$R_{FREQ} = \frac{1}{\left(141 \times 10^{-12}\left[\frac{s}{\Omega}\right]\right) \times \left(f_{FREQ}\left[\frac{1}{s}\right]\right)} - \left(3.5 \times 10^{3}[\Omega]\right)\ [\Omega]$$

In addition, the oscillator is capable of changing from the frequency set by the external resistor to a synchronized frequency from an external clock source. If an external clock source is provided on the pin FREQ/SYNC, then the internal oscillator synchronizes to this external clock frequency and the boost regulator switches at the synchronized frequency. The synchronization frequency capture range is 250 kHz to 500 kHz.

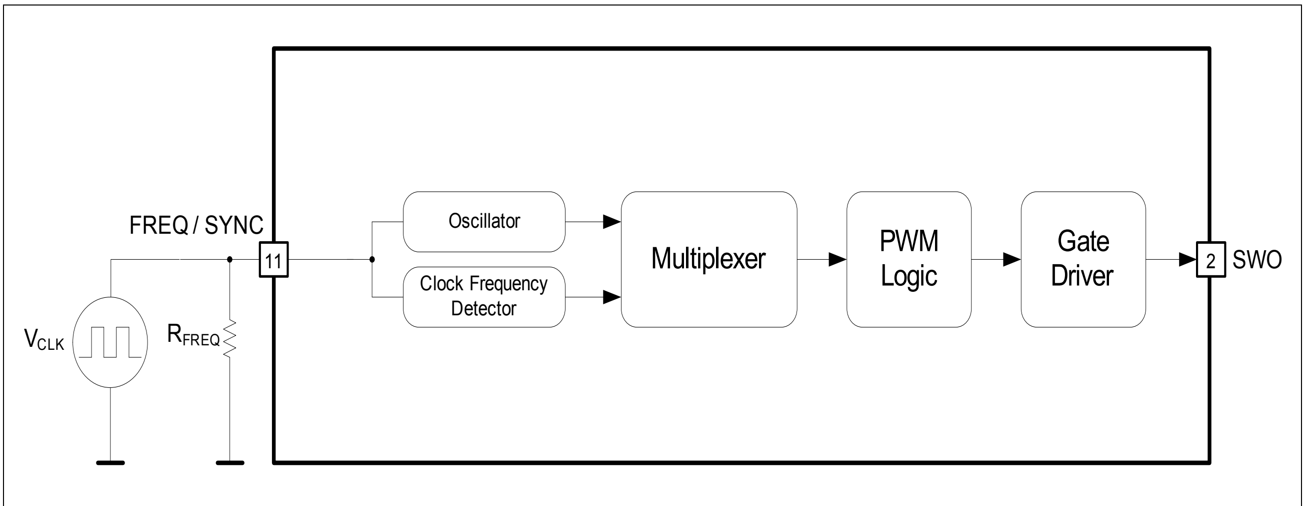


Figure 4 Oscillator and Synchronization Block Diagram and Simplified Application Circuit

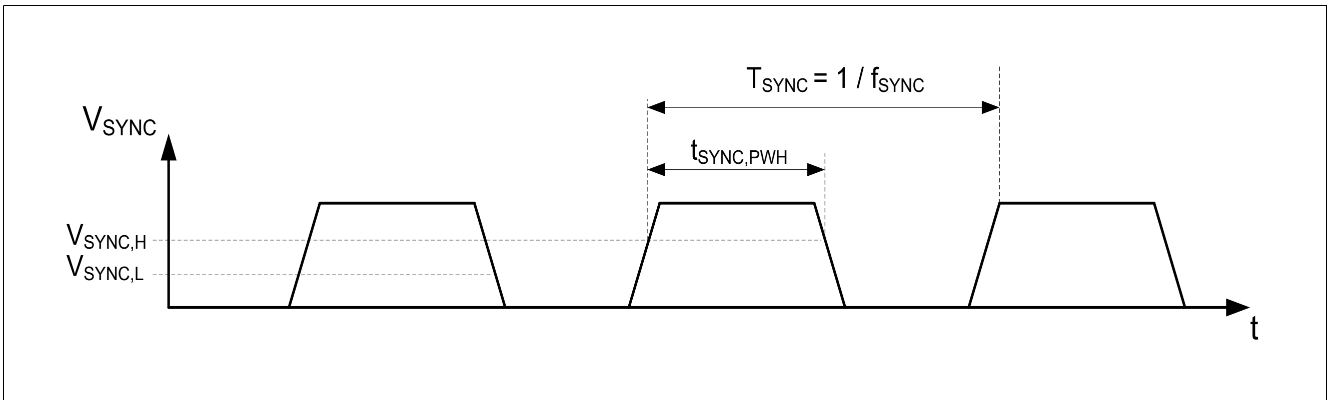


Figure 5 Synchronization Timing Diagram

6.2 Electrical Characteristics

Table 2 EC Oscillator and Synchronization

V_{IN} = 8V to 34V; T_j = -40 ·C to +150 ·C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

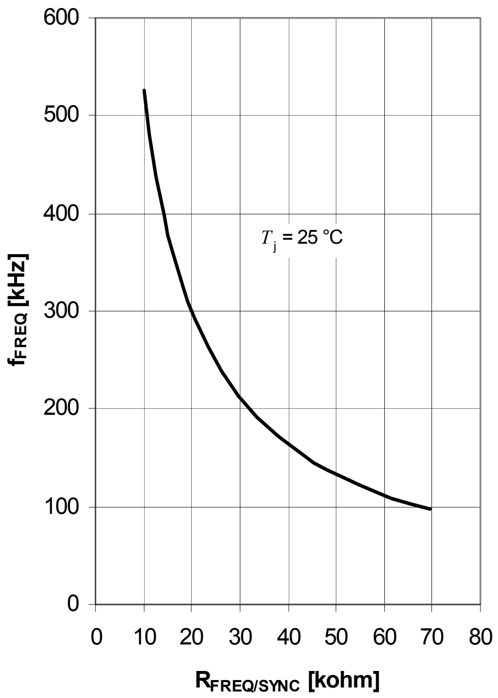
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Oscillator:							
6.2.1	Oscillator Frequency	f_{FREQ}	250	300	350	kHz	R_{FREQ} = 20kΩ
6.2.2	Oscillator Frequency Adjustment Range	f_{FREQ}	100	–	500	kHz	
6.2.3	FREQ / SYNC Supply Current	I_{FREQ}	–	–	-700	µA	V_{FREQ} = 0V
6.2.4	Frequency Voltage	V_{FREQ}	1.16	1.24	1.32	V	f_{FREQ} = 100kHz
Synchronization							
6.2.5	Synchronization Frequency Capture Range	f_{SYNC}	250	–	500	kHz	–
6.2.6	Synchronization Signal High Logic Level Valid	$V_{SYNC,H}$	3.0	–	–	V	1) 2)
6.2.7	Synchronization Signal Low Logic Level Valid	$V_{SYNC,L}$	–	–	0.8	V	1) 2)
6.2.8	Synchronization Signal Logic High Pulse Width	$t_{SYNC,PWH}$	200	–	–	ns	1) 2)

1) Synchronization of external PWM ON signal to falling edge

2) Not subject to production test, specified by design

Typical Performance Characteristics of Oscillator

**Switching Frequency f_{SW} versus
Frequency Select Resistor to GND $R_{FREQ/SYNC}$**



7 Enable and Dimming Function

7.1 Description

The enable function powers ON or OFF the device. A valid logic LOW signal on enable pin EN/PWMI powers OFF the device and current consumption is less than I_{q_OFF} (Parameter 7.2.8). A valid logic HIGH enable signal on enable pin EN/PWMI powers on the device. The enable function features an integrated pull down resistor which ensures that the IC is shut down and the power switch is OFF in case the enable pin EN is left open.

In addition to the enable function described above, the EN/PWMI pin detects a pulse width modulated (PWM) input signal that is fed through to the internal gate driver. The EN/PWMI enables and disables the gate driver for the main switch during PWM operation. PWM dimming an LED is a commonly practiced dimming method and can prevent color shift in an LED light source.

The enable and PWM input function share the same pin. Therefore a valid logic LOW signal at the EN/PWMI pin needs to differentiate between an enable power OFF or an PWM dimming LOW signal. The device differentiates between enable OFF and PWM dimming signal by requiring the enable OFF at the EN/PWMI pin to stay LOW for the Enable Turn OFF Delay Time ($t_{EN,OFF,DEL}$ Parameter 7.2.6).

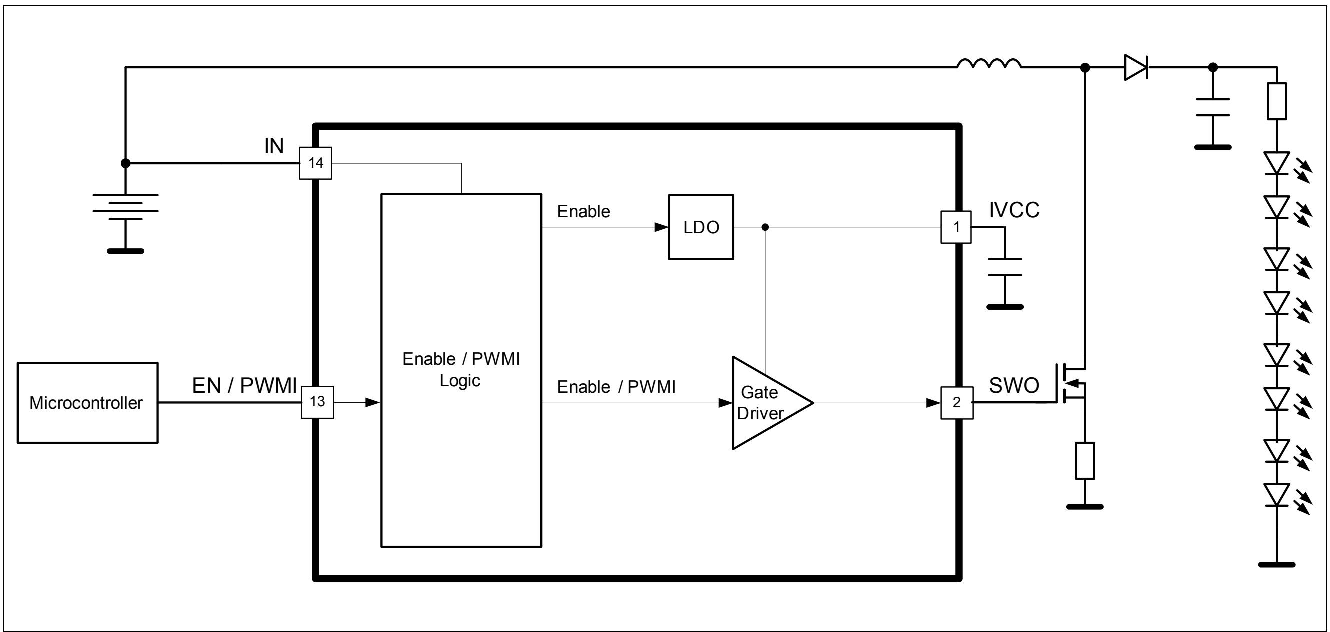


Figure 6 Block Diagram and Simplified Application Circuit Enable and LED Dimming

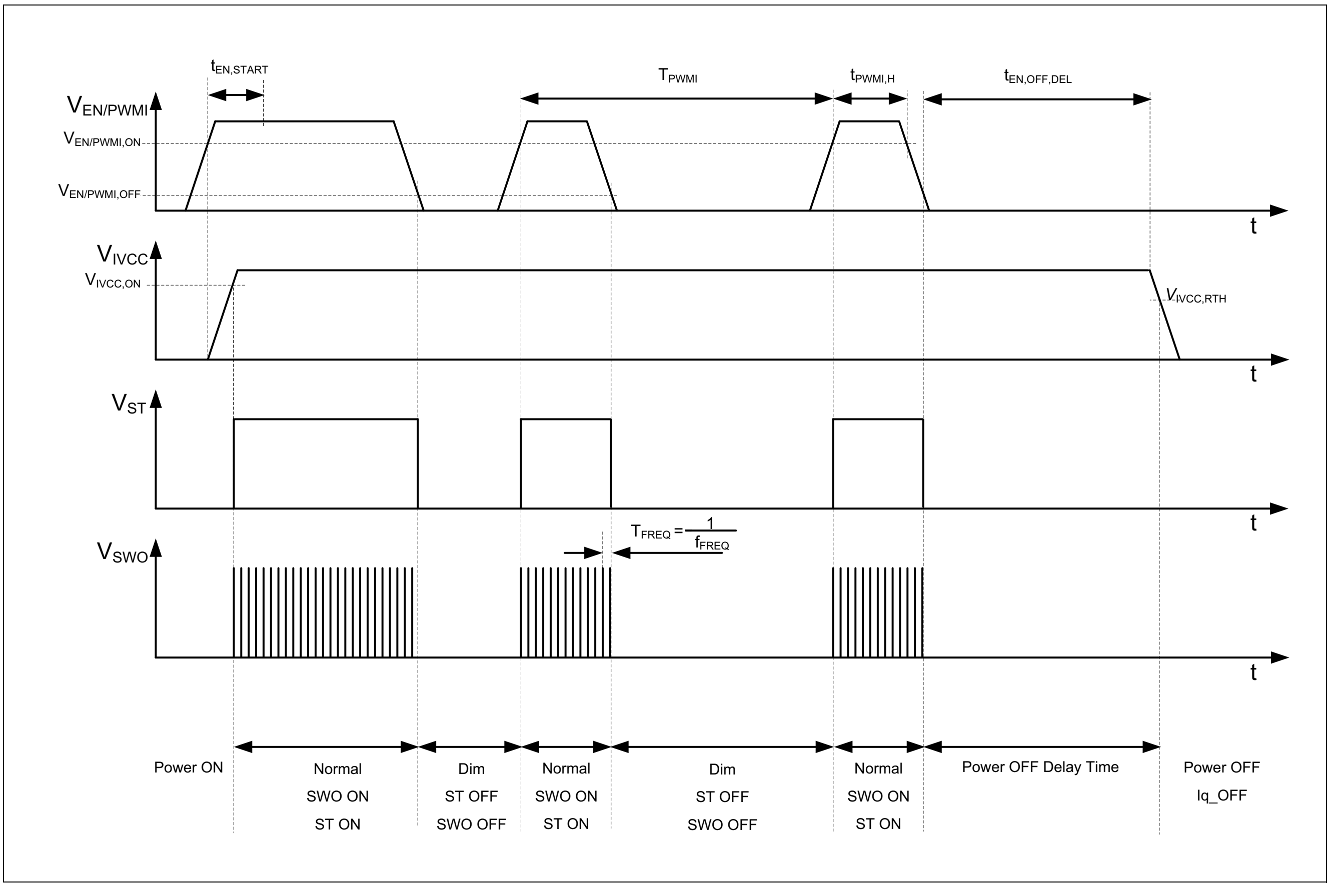


Figure 7 Timing Diagram Enable and LED Dimming

Note: The ST signal is LOW during soft-start.

7.2 Electrical Characteristics

Table 3 EC Enable and Dimming

V_{IN} = 8V to 34V; T_j = -40 ·C to +150 ·C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Enable/PWM Input:							
7.2.1	Enable/PWMI Turn On Threshold	$V_{EN/PWMI,ON}$	3.0	–		V	–
7.2.2	Enable/PWMI Turn Off Threshold	$V_{EN/PWMI,OFF}$	–	–	0.8	V	–
7.2.3	Enable/PWMI Hysteresis	$V_{EN/PWMI,HYS}$	50	200	400	mV	1)
7.2.4	Enable/PWMI High Input Current	$I_{EN/PWMI,H}$	–	–	30	µA	$V_{EN/PWMI}$ = 16.0V
7.2.5	Enable/PWMI Low Input Current	$I_{EN/PWMI,L}$	–	0.1	1	µA	$V_{EN/PWMI}$ = 0.5V
7.2.6	Enable Turn Off Delay Time	$t_{EN,OFF,DEL}$	8	10	12	ms	–

Table 3 EC Enable and Dimming

V_{IN} = 8V to 34V; T_j = -40 ·C to +150 ·C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
7.2.7	Enable Startup Time	$t_{EN,START}$	100	–	–	µs	[1]
Current Consumption							
7.2.8	Current Consumption, Shutdown Mode	I_{q_OFF}	–	–	10	µA	$V_{EN/PWMI}$ = 0.8 V; $T_j \leq$ 105C; V_{IN} = 16V
7.2.9	Current Consumption, Active Mode[2]	I_{q_ON}	–	–	7	mA	$V_{EN/PWMI} \geq$ 4.75V; I_{BO} = 0mA; V_{SWO} = 0% Duty Cycle

1) Not subject to production test, specified by design

2) Dependency on switching frequency and gate charge of boost and dimming switch.

8 Linear Regulator

8.1 Description

The internal linear voltage regulator supplies the internal gate drivers with a typical voltage of 5V and current up to $I_{LIM,min}$ (Parameter 8.2.2). An external output capacitor with ESR lower than $R_{IVCC,ESR}$ (Parameter 8.2.5) is required on pin IVCC for stability and buffering transient load currents. During normal operation the external boost and dimming MOSFET switches will draw transient currents from the linear regulator and its output capacitor. Proper sizing of the output capacitor must be considered to supply sufficient peak current to the gate of the external MOSFET switches.

Integrated undervoltage protection for the external switching MOSFET:

An integrated undervoltage reset threshold circuit monitors the linear regulator output voltage (V_{IVCC}) and resets the device in case the output voltage falls below the IVCC Undervoltage Reset switch OFF Threshold ($V_{IVCC,RTH,d}$ Parameter 8.2.7). The Undervoltage Reset threshold for the IVCC pin helps to protect the external switches from excessive power dissipation by ensuring the gate drive voltage is sufficient to enhance the gate of an external logic level N-channel MOSFET.

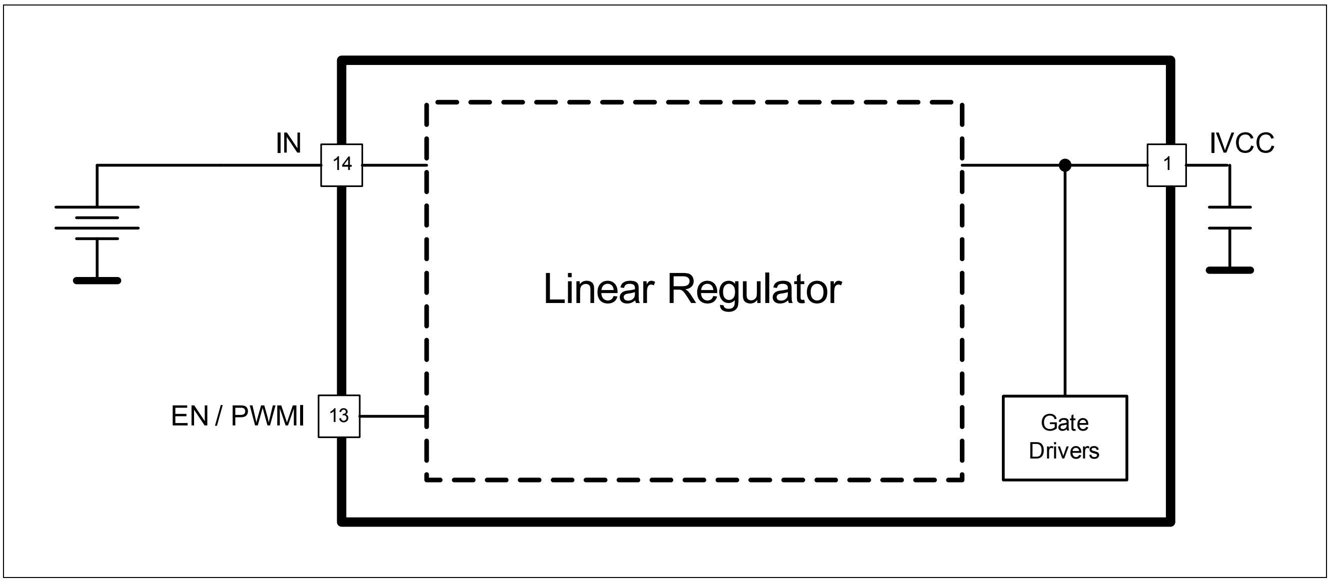


Figure 8 Voltage Regulator Block Diagram and Simplified Application Circuit

8.2 Electrical Characteristics

Table 4 EC Line Regulator

V_{IN} = 8V to 34V; T_j = -40 ·C to +150 ·C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
8.2.1	Output Voltage	V_{IVCC}	4.85	5	5.15	V	$6V \leq V_{IN} \leq 45V$ $0.1mA \leq I_{IVCC} \leq 40mA$
8.2.2	Output Current Limitation	I_{LIM}	51	–	90	mA	V_{IN} = 13.5V V_{IVCC} = 4.5V
8.2.3	Drop out Voltage	V_{DR}	–	–	0.5	V	V_{IN} = 4.5V I_{IVCC} = 25mA
8.2.4	IVCC Buffer Capacitor	C_{IVCC}	0.47	1	100	µF	[1] [2]
8.2.5	IVCC Buffer Capacitor ESR	$R_{IVCC,ESR}$	–	–	0.5	Ω	[1]
8.2.6	Undervoltage Reset Headroom	$V_{IVCC,HDRM}$	100	–	–	mV	V_{IVCC} decreasing V_{IVCC} - $V_{IVCC,RTH,d}$
8.2.7	IVCC Undervoltage Reset switch OFF Threshold	$V_{IVCC,RTH,d}$	3.6	–	4.0	V	[3] V_{IVCC} decreasing.
8.2.8	IVCC Undervoltage Reset switch ON Threshold	$V_{IVCC,RTH,i}$	–	–	4.5	V	V_{IVCC} increasing

1) Not subject to production test, specified by design
2) Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum.
3) Selection of external switching MOSFET is crucial and the $V_{IVCC,RTH,d}$ min. as worst case V_{GS} must be considered.

9 Protection and Diagnostic Functions

9.1 Description

The TLD5097EL has integrated circuits to diagnose and protect against output overvoltage, open load, open feedback and overtemperature faults. In case of a fault condition, the SWO signal stops operation. The ST signal will change to an active logic LOW signal to communicate that a fault has occurred (detailed overview in **Figure 9** and **Figure 10** below). **Figure 11** illustrates the various open load and open feedback conditions. In case of an overtemperature condition the integrated thermal shutdown function turns off the gate driver and internal linear voltage regulator. The typical junction shutdown temperature is 175°C ($T_{j,SD}$ Parameter **9.2.3**). After cooling down the IC will automatically restart. Thermal shutdown is an integrated protection function designed to prevent IC destruction and is not intended for continuous use in normal operation (**Figure 13**). To calculate the proper overvoltage protection resistor values an example is given in **Figure 14**.

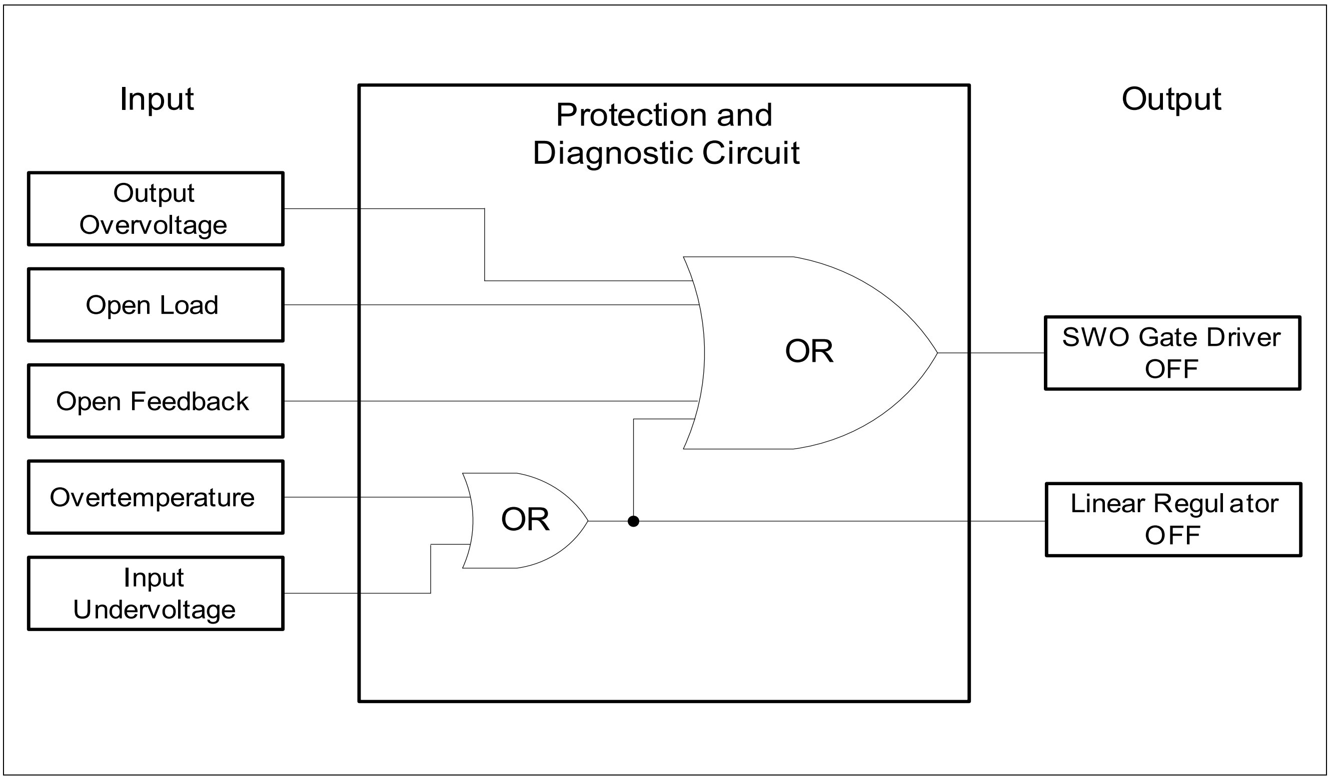
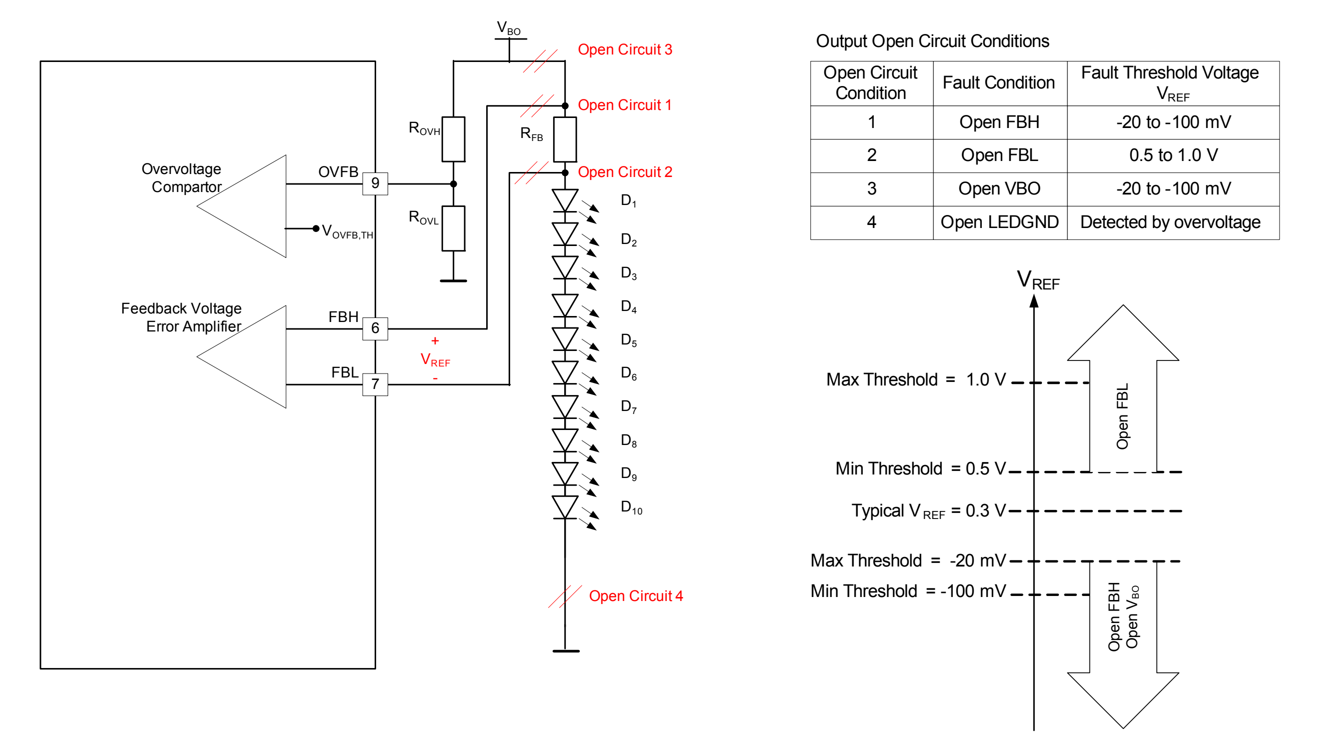


Figure 9 Protection and Diagnostic Function Block Diagram

Input		Output		
Condition	Level*	ST	SWO	IVCC
Overvoltage @ Output	False	H or Sw*	Sw*	Active
	True	L	L	Active
Open Load	False	H or Sw*	Sw*	Active
	True	L	L	Active
Open Feedback	False	H or Sw*	Sw*	Active
	True	L	L	Active
Overtemperature	False	H or Sw*	Sw*	Active
	True	L	L	Shutdown
Undervoltage @ Input	False	H or Sw*	Sw*	Active
	True	L	L	Shutdown

*Note:
Sw = Switching
False = Condition does not exist
True = Condition does exist

Figure 10 Diagnosis Truth Table



Open Circuit Condition	Fault Condition	Fault Threshold Voltage V_{REF}
1	Open FBH	-20 to -100 mV
2	Open FBL	0.5 to 1.0 V
3	Open VBO	-20 to -100 mV
4	Open LEDGND	Detected by overvoltage

Figure 11 Open Load and Open Feedback Conditions

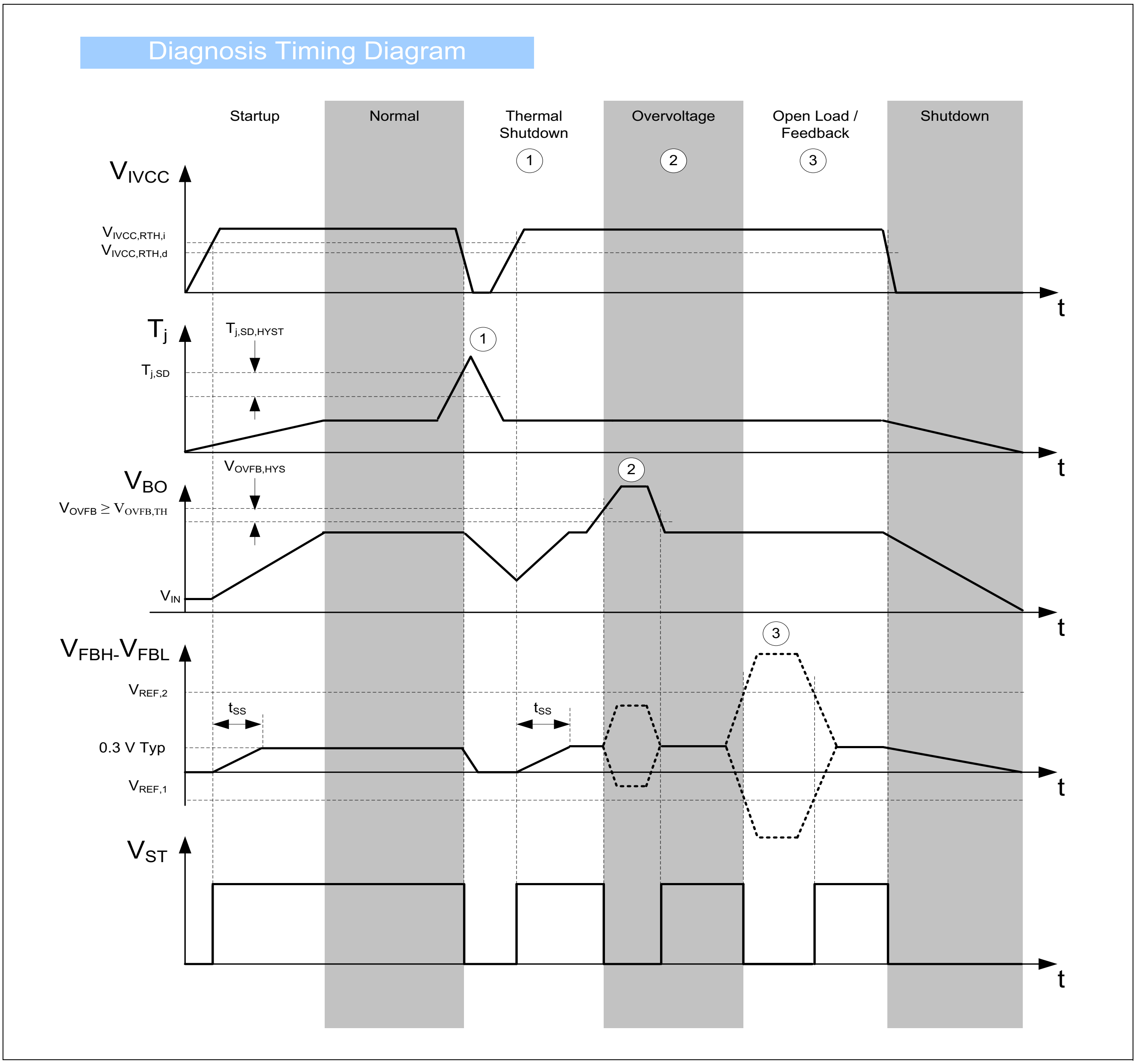


Figure 12 Open load, Overvoltage and Overtemperature Timing Diagram

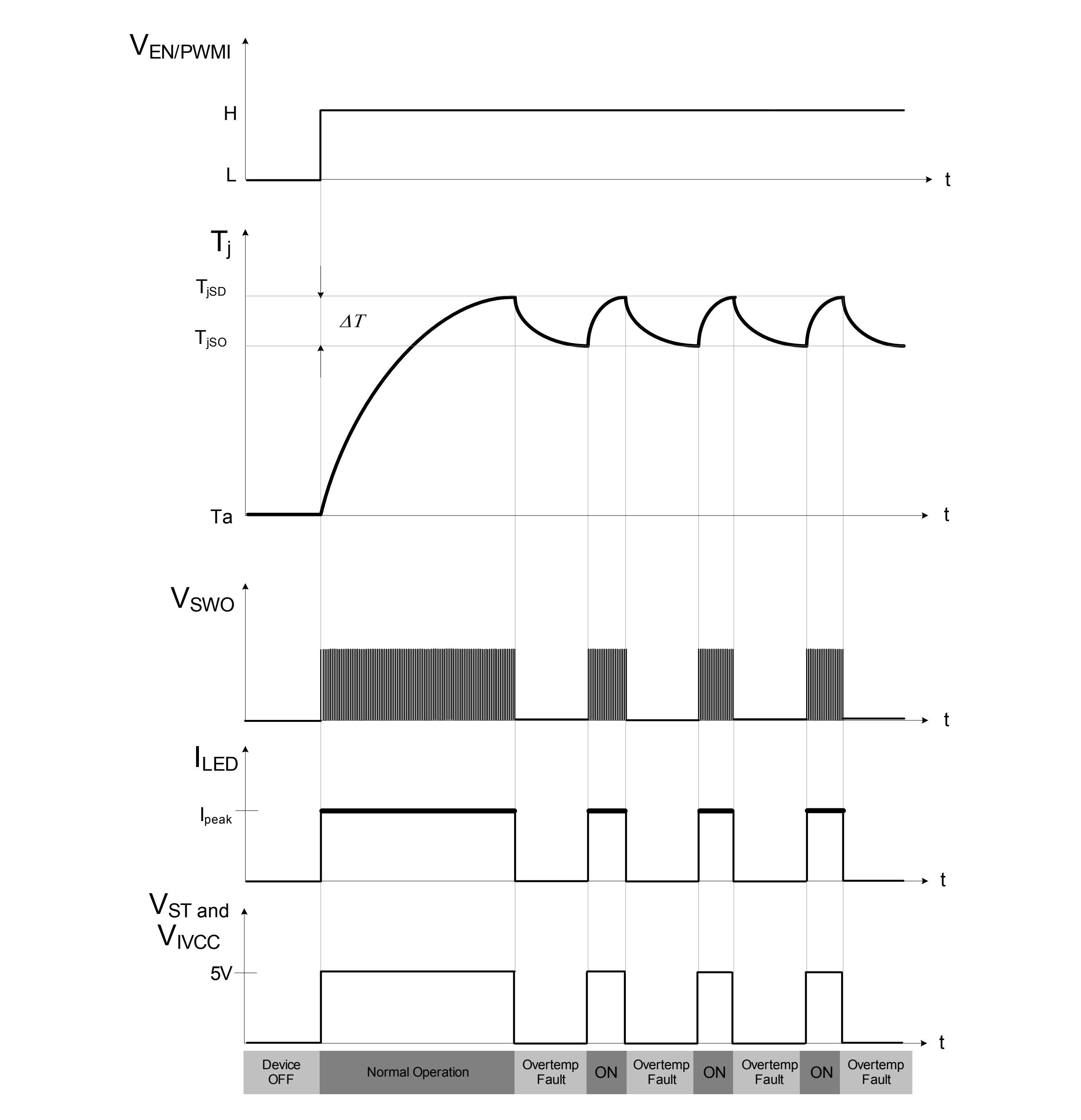


Figure 13 Device overtemperature protection behavior

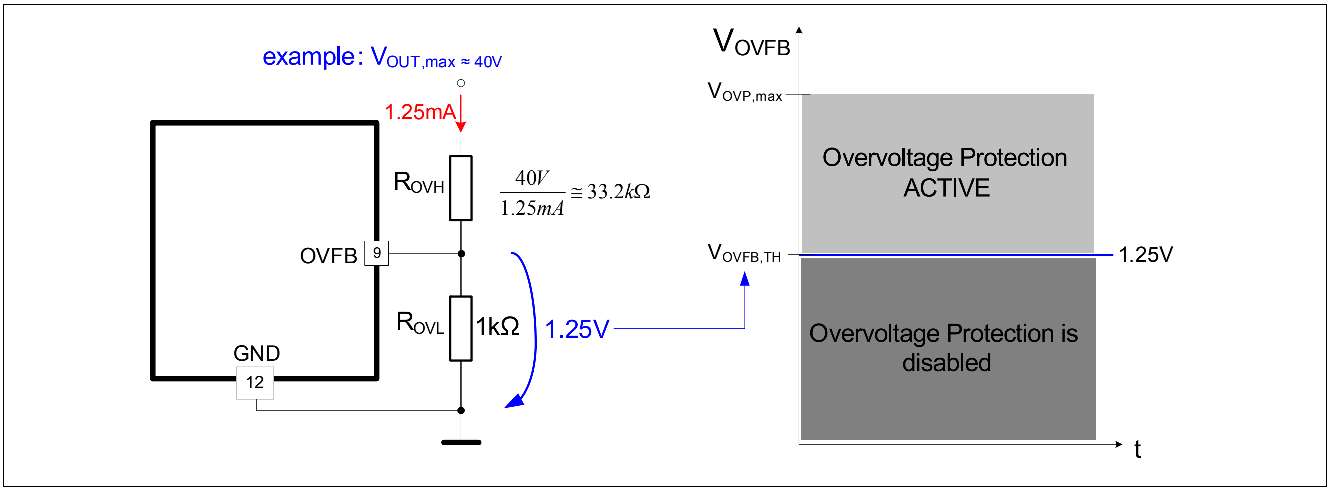


Figure 14 Overvoltage Protection description

9.2 Electrical Characteristics

Table 5 EC Protection and Diagnosis

V_{IN} = 8V to 34V; T_j = -40 ·C to +150 ·C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Status Output							
9.2.1	Status Output Voltage Low	$V_{ST,LOW}$	–	–	0.4	V	[1] I_{ST} = 1mA
9.2.2	Status Output Voltage High	$V_{ST,HIGH}$	V_{IVCC} - 0.4	–	V_{IVCC}	V	[1] I_{ST} = -1mA
Temperature Protection:							
9.2.3	Over Temperature Shutdown	$T_{j,SD}$	160	175	190	°C	[1] refer to **Figure 13**
9.2.4	Over Temperature Shutdown Hystereses	$T_{j,SD,HYST}$	–	15	–	°C	[1]
Overvoltage Protection:							
9.2.5	Output Over Voltage Feedback Threshold Increasing	$V_{OVFB,TH}$	1.21	1.25	1.29	V	refer to **Figure 14**
9.2.6	Output Over Voltage Feedback Hysteresis	$V_{OVFB,HYS}$	50	–	150	mV	[1] Output Voltage decreasing
9.2.7	Over Voltage Reaction Time	t_{OVPRR}	2	–	10	µs	[1] Output Voltage decreasing
9.2.8	Over Voltage Feedback Input Current	I_{OVFB}	-1	0.1	1	µA	V_{OVFB} = 1.25V

Table 5 EC Protection and Diagnosis

V_{IN} = 8V to 34V; T_j = -40 ·C to +150 ·C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Open Load and Open Feedback Diagnostics							
9.2.9	Open Load/Feedback Threshold	$V_{REF,1,3}$	-100	–	-20	mV	refer to **Figure 11** $V_{REF} = V_{FBH} - V_{FBL}$ Open Circuit 1 or 3
9.2.10	Open Feedback Threshold	$V_{REF,2}$	0.5	–	1	V	$V_{REF} = V_{FBH} - V_{FBL}$ Open Circuit 2

1) Specified by design; not subject to production test.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

10 Analog Dimming

This pin is influencing the Feedback Voltage Error Amplifier by generating an internal current accordingly to an external reference voltage (V_{SET}). If the analog dimming feature is not needed this pin must be connected to IVCC or external > 1.6V supply. Different application scenarios are described in **Figure 17**. This pin can also go outside of the ECU for instance if a thermistor is connected on a separated LED Module and the Analog Dimming Input is used to thermally protect the LEDs. For reverse battery protection of this pin an external series resistor should be placed to limit the current.

10.1 Purpose of Analog Dimming:

1) It is difficult for LED manufacturers to deliver LEDs which have the same Brightness, Colorpoint and Forward Voltage Class. Due to this relatively wide spread of the crucial LED parameters automotive customers order LEDs from one or maximum two different colorpoint classes. The LED manufacturer must preselect the LEDs to deliver the requested colorpoint class. Those preselected LEDs are matched in terms of the colorpoint but a variation of the brightness remains. To correct the brightness deviation an analog dimming feature is needed. The mean LED current can be adjusted by applying an external voltage V_{SET} at the SET pin.

2) If the DC/DC application is separated from the LED loads the ECU manufacturers aim is to develop one hardware which should be able to handle different load current conditions (e.g. 80mA to 400mA) to cover different applications. To achieve this average LED current adjustment the analog dimming is a crucial feature.

10.2 Description

Application Example:

Desired LED current = 400mA. For the calculation of the correct Feedback Resistor R_{FB} the following equation can be used: This formula is valid if the analog dimming feature is disabled and V_{SET} > 1.6V.

$$I_{LED} = \frac{V_{REF}}{R_{FB}} \quad \text{-->} \quad R_{FB} = \frac{V_{REF}}{I_{LED}} \quad \text{-->} \quad R_{FB} = \frac{0.3V}{400mA} = 750m\Omega$$

A decrease of the average LED current can be achieved by controlling the voltage at the SET pin (V_{SET}) between 0V and 1.6V. The mathematical relation is given in the formula below:

$$I_{LED} = \frac{V_{SET} - 0{,}1V}{5 * R_{FB}}$$

If V_{SET} is 100mV the LED current is only determined by the internal offset voltages of the comparators. For this example I_{LED} = 0A if $V_{SET} < 100mV$. Refer to the concept drawing in **Figure 16**.

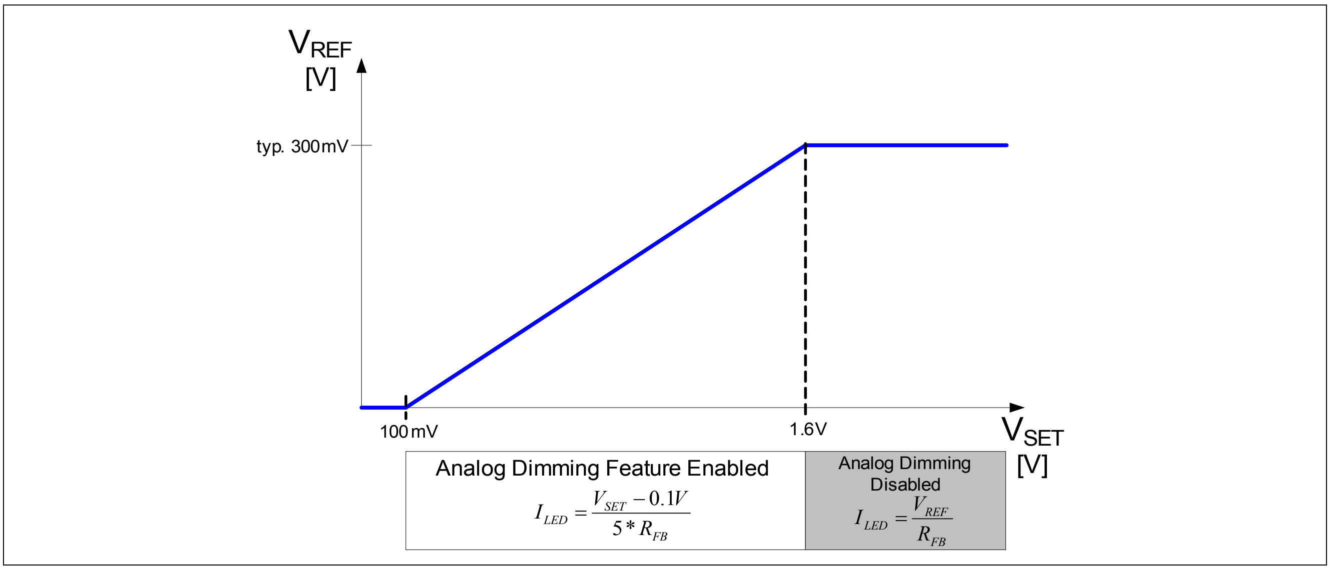


Figure 15 Basic relationship between V_{REF} and V_{SET} Voltage

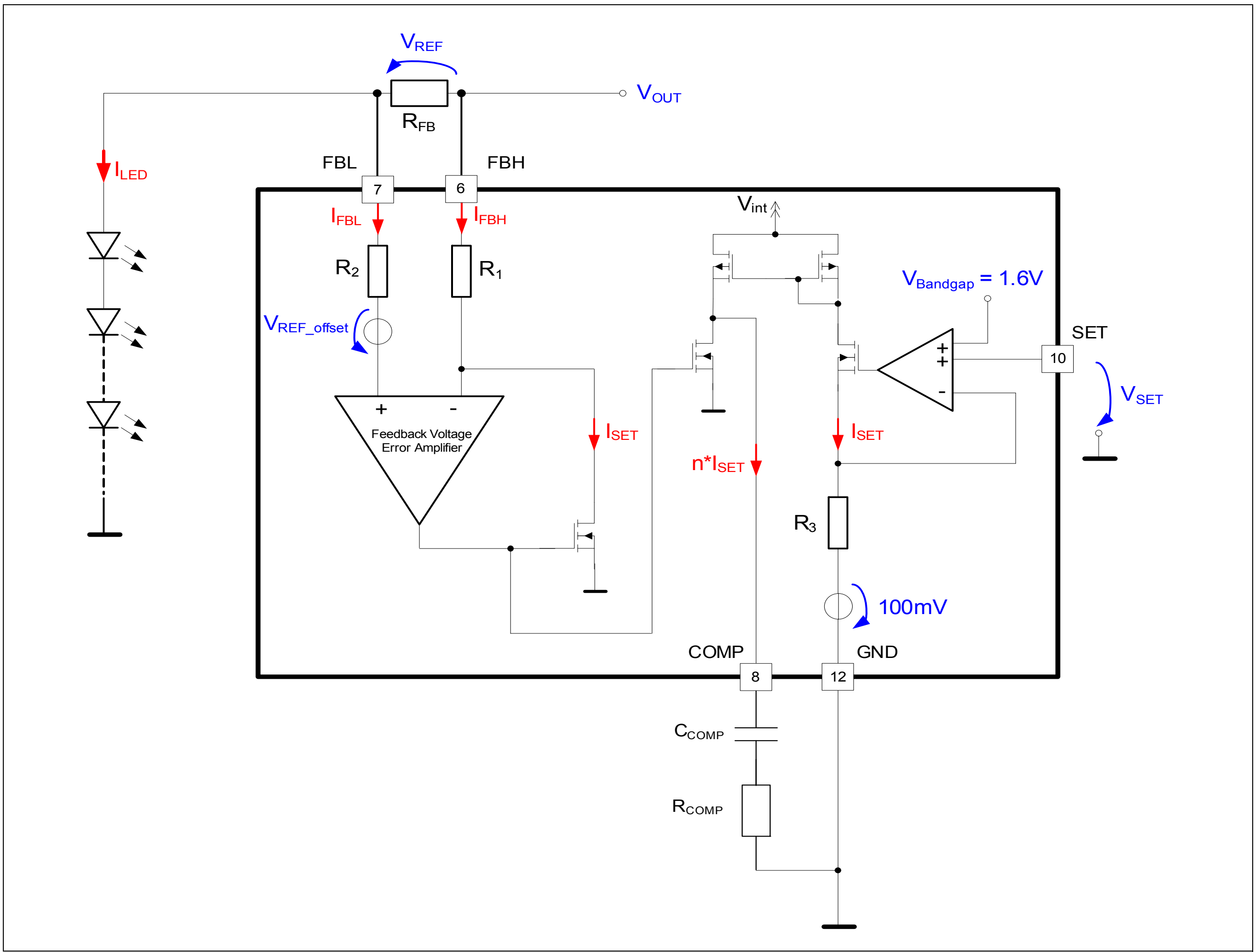


Figure 16 Concept Drawing Analog Dimming

Multi-purpose usage of the Analog dimming feature

1) A µC integrated digital analog converter (DAC) output or a stand alone DAC can be used to supply the SET pin of the TLD5097EL. The integrated voltage Regulator (V_{IVCC}) can be used to supply the µC or external components if the current consumption does not exceed 20mA.

2) The analog dimming feature is directly connected to the input voltage of the system. In this configuration the LED current is reduced if the input voltage V_{IN} is decreasing. The DC/DC boost converter is changing (increasing) the switching duty cycle if V_{IN} drops to a lower potential. This is causing an increase of the input current consumption. If applications require a decrease of the LED current in respect to VIN variations this setup can be choosen.

3) The usage of an external resistor divider connected between IVCC (integrated 5V regulator output and gate buffer pin) SET and GND can be choosen for systems without µC on board. The concept allows to control the LED current via placing cheap low power resistors. Furthermore a temperature sensitive resistor (Thermistor) to protect the LED loads from thermal destruction can be connected additionally.

4) If the analog dimming feature is not needed the SET pin must be connected directly to >1.6V potential (e.g. IVCC potential)

5) Instead of an DAC the µC can provide a PWM signal and an external R-C filter is producing a constant voltage for the analog dimming. The voltage level is depending on the PWM frequency (f_{PWM}) and duty cycle (DC) which can be controlled by the µc software after reading the coding resistor placed at the LED module.

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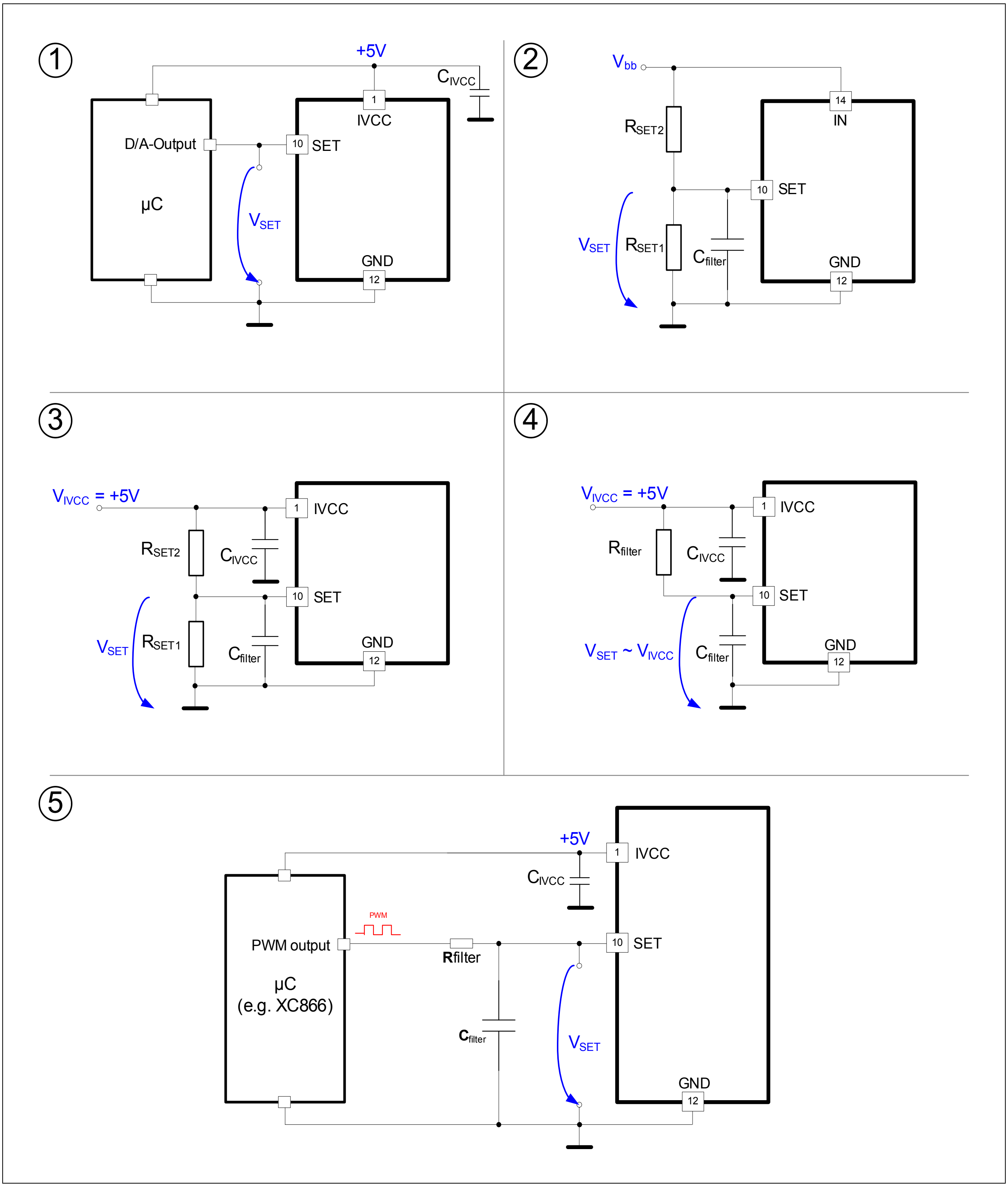

Figure 17 Analog Dimming in various applications

10.3 Electrical Characteristics

Table 6 EC Analog Dimming

V_{IN} = 8V to 34V; T_j = -40 ·C to +150 ·C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Analog Dimming Range							
10.3.1	SET programming range	V_{SET}	0	–	1.6	V	[1] refer to **Figure 15**

1) Specified by design; not subject to production test.

11 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

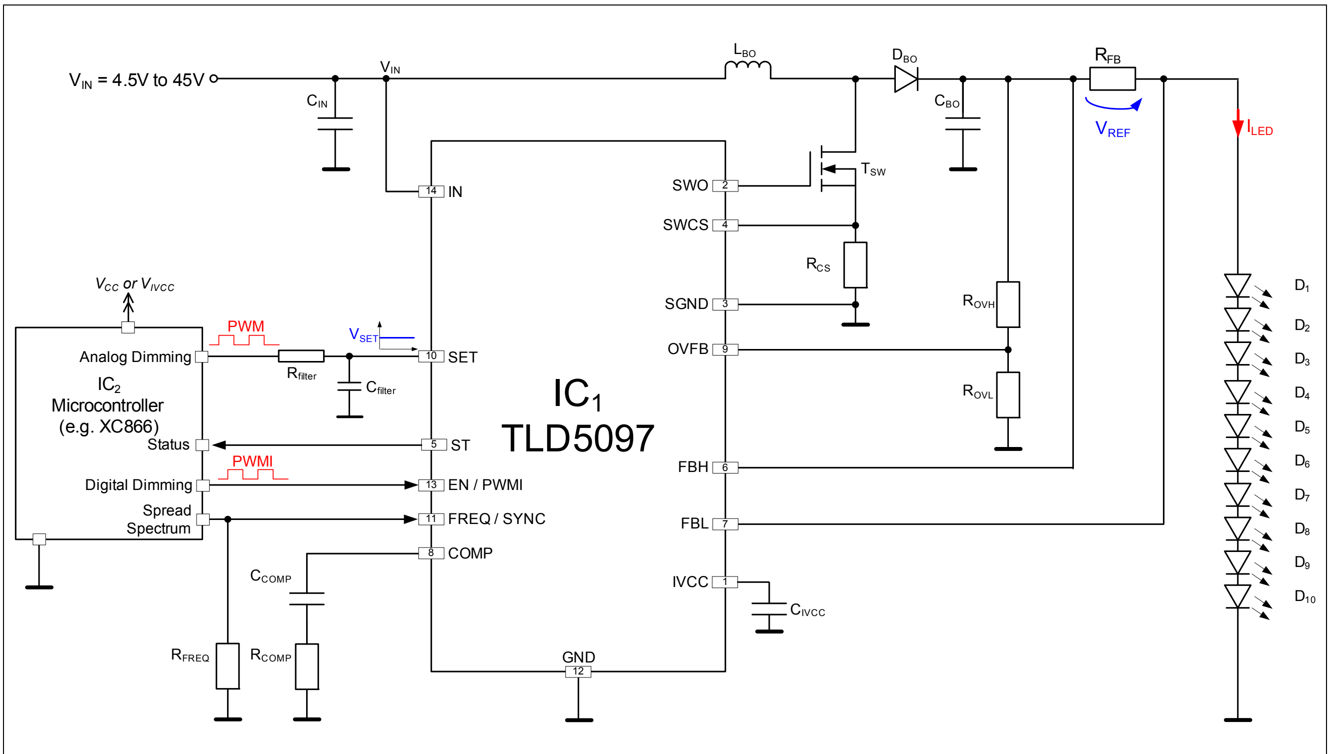

Figure 18 Boost to Ground Application Circuit - B2G (Boost configuration)

Reference Designator	Value	Manufacturer	Part Number	Type	Quantity
D_{1-10}	White	Osram	LUW H9GP	LED	10
D_{BO}	Schottky, 3 A, 100 V_R	Vishay	SS3H10	Diode	1
C_{IN}	100 uF, 50V	Panasonic	EEEFK1H101GP	Capacitor	1
C_{BO}	10 uF, 50V	Panasonic	Electrolytic or Ceramic Bank	Capacitor	1
C_{COMP}	100 nF	EPCOS	X7R	Capacitor	1
C_{IVCC}	1uF , 6.3V	EPCOS	MLCC CCNPZC105KBW X7R	Capacitor	1
IC_1	--	Infineon	TLD5097	IC	1
IC_2	--	Infineon	XC866	IC	1
L_{BO}	100 uH	Coilcraft	MSS1278T-104ML	Inductor	1
R_{COMP}	10 kΩ, 1%	Panasonic	ERJ3EKF1002V	Resistor	1
R_{FB}	820 mΩ, 1%	Panasonic	ERJ14BQFR82U	Resistor	1
R_{FREQ}	20 kΩ, 1%	Panasonic	ERJ3EKF2002V	Resistor	1
R_{OVH}	33.2 kΩ, 1%	Panasonic	ERJ3EKF3322V	Resistor	1
R_{OVL}	1 kΩ, 1%	Panasonic	ERJ3EKF1001V	Resistor	1
R_{CS}	50 mΩ, 1%	Panasonic	ERJB1CFR05U	Resistor	1
T_{SW}	100V N-ch, 35A	Infineon	IPG20N10S4L-22	Transistor	1
	alternativ: 60V N-ch, 30A	Infineon	IPD30N06S4L-23	Transistor	1

Figure 19 Bill of Materials for B2G Application Circuit

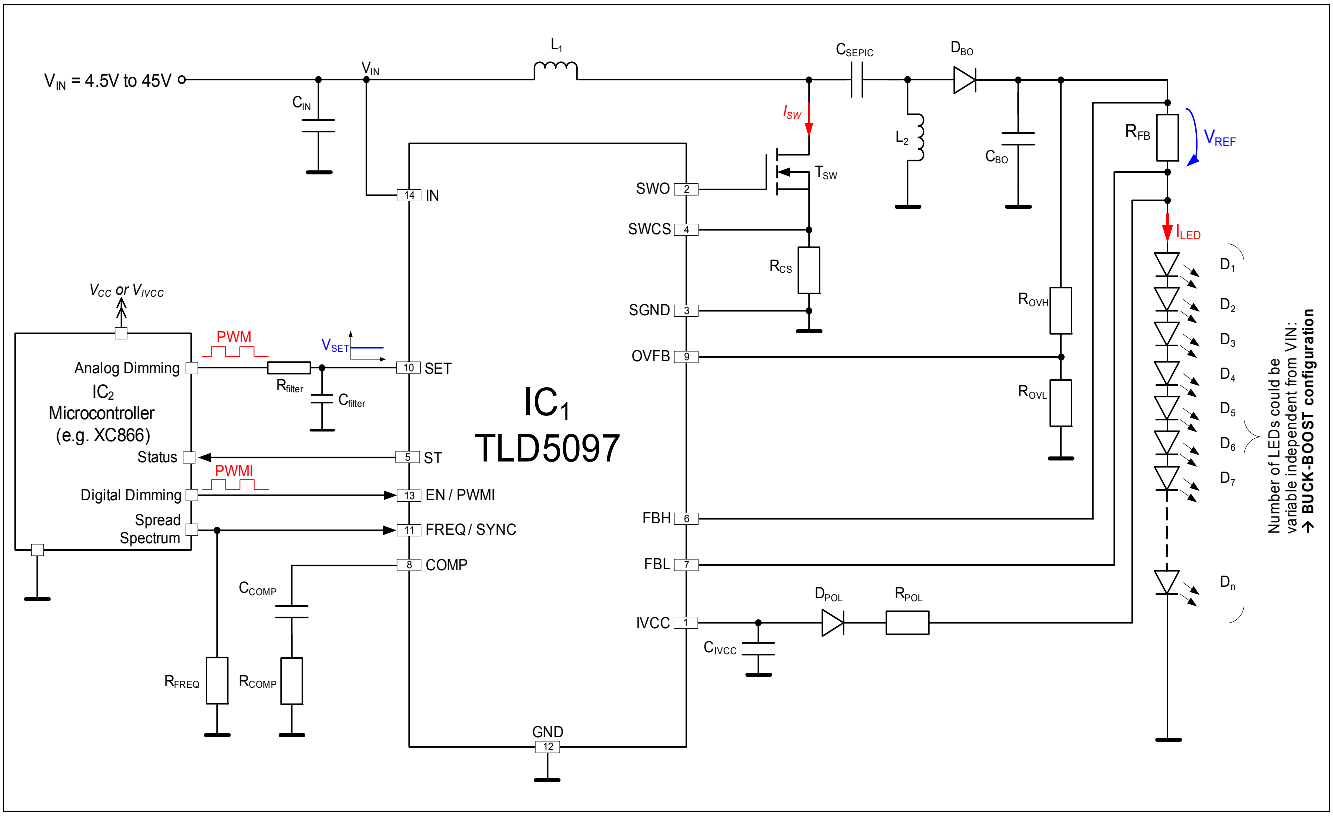

Figure 20 SEPIC Application Circuit (Buck-Boost configuration)

Reference Designator	Value	Manufacturer	Part Number	Type	Quantity
D_{1-n}	White	Osram	LUW H9GP	LED	variable
D_{BO}	Schottky, 3 A, 100 V_R	Vishay	SS3H10	Diode	1
D_{POL}	80V Diode	Infineon	BAS1603W	Diode	1
C_{SEPIC}	3.3 uF, 20V	EPCOS	X7R, Low ESR	Capacitor	1
C_{IN}	100 uF, 50V	Panasonic	EEEFK1H101GP	Capacitor	1
C_{BO}	10 uF, 50V	Panasonic	EEEFK1H100P	Capacitor	1
C_{COMP}	100 nF	EPCOS	X7R	Capacitor	1
C_{IVCC}	1uF , 6.3V	EPCOS	X7R	Capacitor	1
IC_1	--	Infineon	TLD5097	IC	1
IC_2	--	Infineon	XC866	IC	1
L_1 , L_2	47 uH	Coilcraft	MSS1278T-473ML	Inductor	2
	alternativ: 22uH coupled inductor	Coilcraft	MSD1278-223MLD	Inductor	1
R_{COMP}, R_{POL}	10 kΩ, 1%	Panasonic	ERJ3EKF1002V	Resistor	2
R_{FB}	820 mΩ, 1%	Panasonic	ERJ14BQFR82U	Resistor	1
R_{FREQ}	20 kΩ, 1%	Panasonic	ERJ3EKF2002V	Resistor	1
R_{OVH}	33.2 kΩ, 1%	Panasonic	ERJ3EKF3322V	Resistor	1
R_{OVL}	1 kΩ, 1%	Panasonic	ERJ3EKF1001V	Resistor	1
R_{CS}	50 mΩ, 1%	Panasonic	ERJB1CFR05U	Resistor	1
T_{SW}	100V N-ch, 35A	Infineon	IPD35N10S3L-26	Transistor	1
	alternativ: 60V N-ch, 30A	Infineon	IPD30N06S4L-23	Transistor	1

Figure 21 Bill of Materials for SEPIC Application Circuit

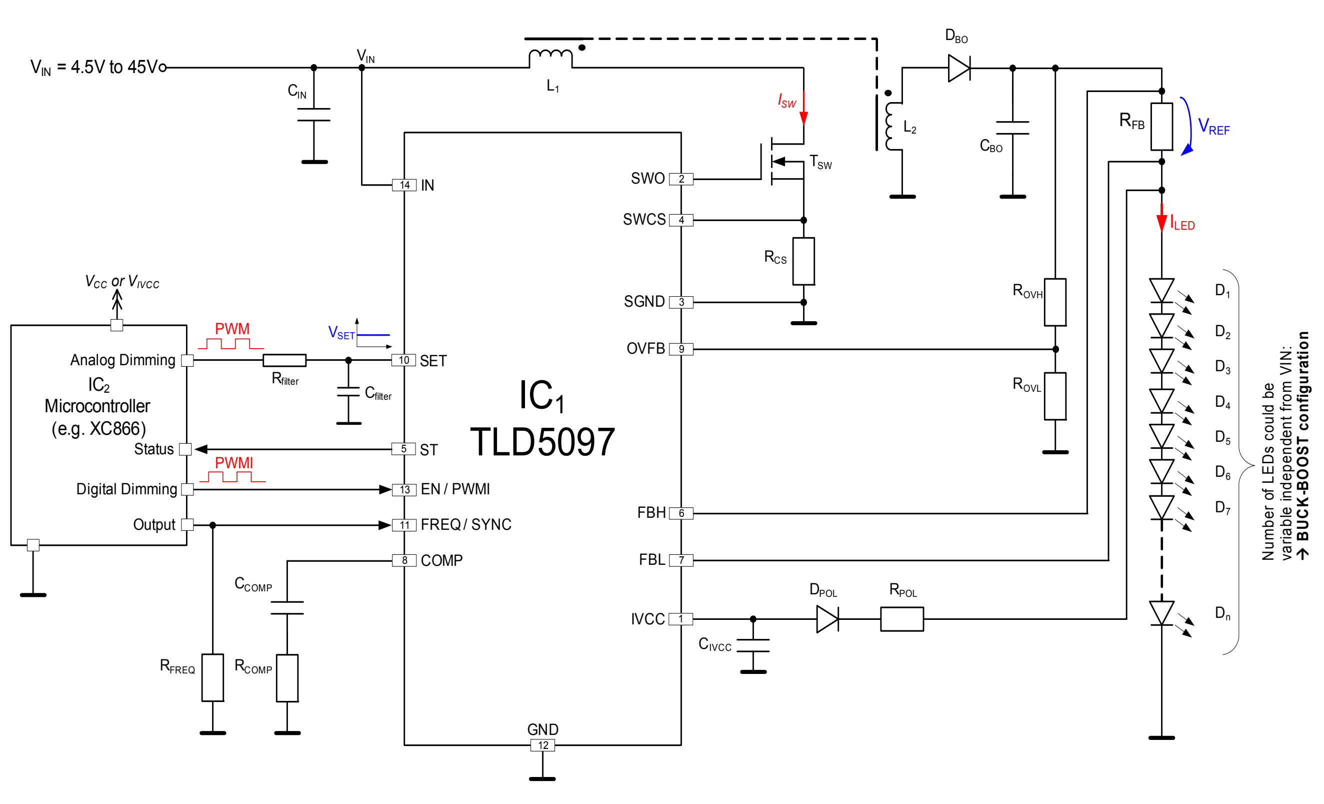

Figure 22 Flyback Application Circuit (Buck-Boost configuration)

Reference Designator	Value	Manufacturer	Part Number	Type	Quantity
D_{1-n}	White	Osram	LUW H9GP	LED	variable
D_{BO}	Schottky, 3 A, 100 V_R	Vishay	SS3H10	Diode	1
C_{BO}	3.3 uF, 50V (100V)	EPCOS	X7R, Low ESR	Capacitor	1
C_{IN}	100 uF, 50V	Panasonic	EEEFK1H101GP	Capacitor	1
C_{COMP}	47 nF	EPCOS	X7R	Capacitor	1
C_{IVCC}	1 uF , 6.3V	EPCOS	X7R	Capacitor	1
IC_1	--	Infineon	TLD5097	IC	1
IC_2	--	Infineon	XC866	IC	1
L_1 , L_2	1 µH / 9 uH	EPCOS	Transformer EHP 16	Inductor	1
R_{COMP}, R_{POL}	10 kΩ, 1%	Panasonic	ERJ3EKF1002V	Resistor	2
D_{POL}	80 V Diode	Infineon	BAS1603W	Diode	1
R_{FB}	820 mΩ, 1%	Isabellenhütte	SMS – Power Resistor	Resistor	1
R_{FREQ}	10 kΩ, 1%	Panasonic	ERJ3EKF1002V	Resistor	1
R_{OVH}	56.2 kΩ, 1%	Panasonic	ERJ3EKF5622V	Resistor	1
R_{OVL}	1.24 kΩ, 1%	Panasonic	ERJ3EKF1241V	Resistor	1
R_{CS}	5 mΩ, 1%	Isabellenhütte	SMS - Power Resistor	Resistor	1
T_{SW}	100V N-ch, 35A	Infineon	IPG20N10S4L-22	Transistor	1
	alternativ: 60V N-ch, 30A	Infineon	IPD30N06S4L-23	Transistor	1

Figure 23 Bill of Materials for Flyback Application Circuit

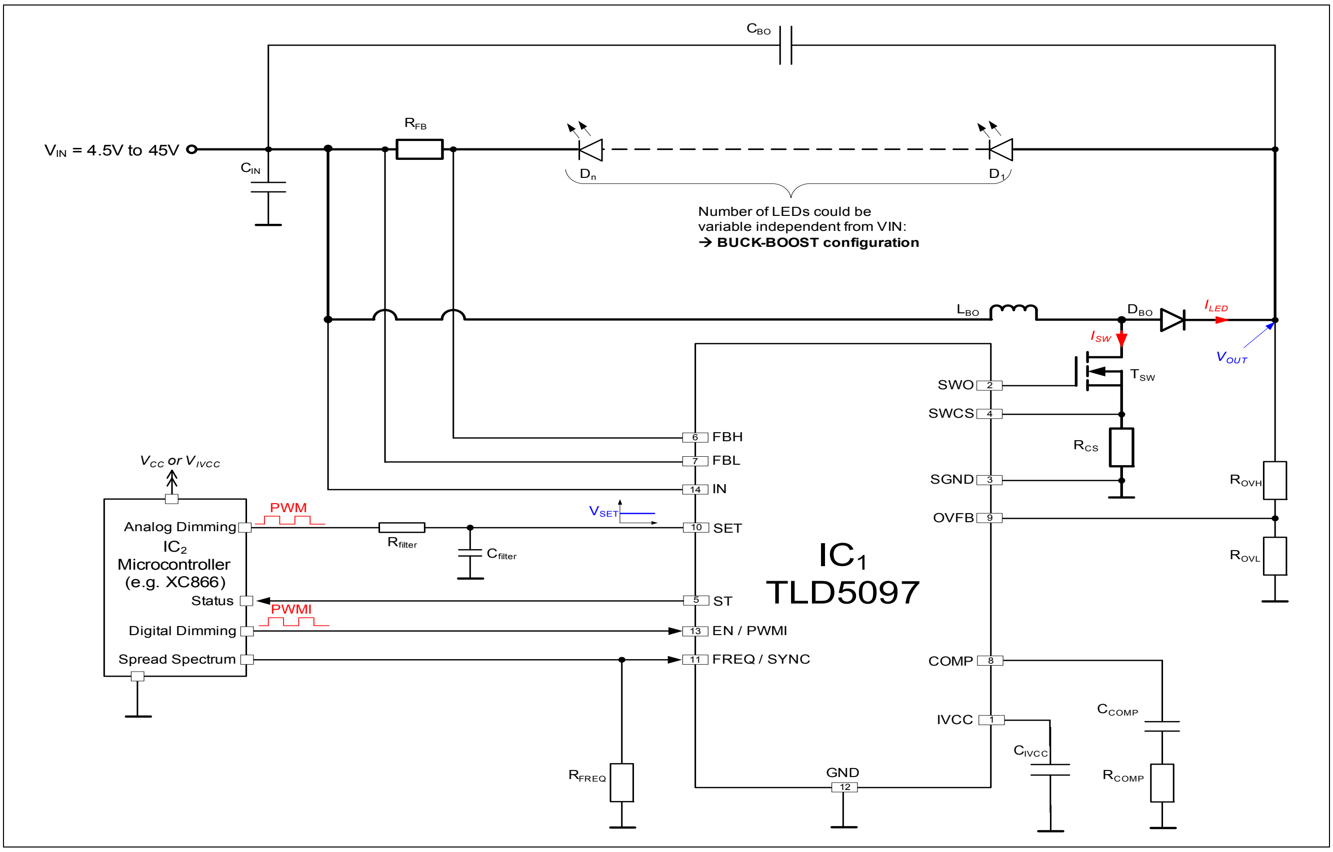

Figure 24 Boost to Battery Application Circuit - B2B (Buck-Boost configuration)

Reference Designator	Value	Manufacturer	Part Number	Type	Quantity
D_{1-n}	White	Osram	LUW H9GP	Diode	variable
D_{BO}	Schottky, 3 A, 100 V_R	Vishay	SS3H10	Diode	1
C_{BO}	10 uF, 80V	Panasonic	EEEFK1K100P	Capacitor	1
C_{IN}	100 uF, 50V	Panasonic	EEEFK1H101GP	Capacitor	1
C_{COMP}	100 nF	EPCOS	X7R	Capacitor	1
C_{IVCC}	1 uF, 6.3V	EPCOS	MLCC CCNPZC105KBW X7R	Capacitor	1
IC_1	--	Infineon	TLD5097	IC	1
IC_2	--	Infineon	XC866	IC	1
L_{BO}	100 uH	Coilcraft	MSS1278T-104ML_	Inductor	1
R_{COMP}	10 kΩ, 1%	Panasonic	ERJ3EKF1002V	Resistor	1
R_{FB}	820 mΩ, 1%	Panasonic	ERJ14BQFR82U	Resistor	1
R_{FREQ}	20 kΩ, 1%	Panasonic	ERJ3EKF2002V	Resistor	1
R_{OVH}	33.2 kΩ, 1%	Panasonic	ERJP06F5102V	Resistor	1
R_{OVL}	1 kΩ, 1%	Panasonic	ERJ3EKF1001V	Resistor	1
R_{CS}	50 mΩ, 1%	Panasonic	ERJB1CFR05U	Resistor	1
T_{SW}	N-ch, OptiMOS-T2 100V, 35A	Infineon	IPD35N10S3L-26	Transistor	1
	alternativ: 60V N-ch, 30A	Infineon	IPD30N06S4L-23	Transistor	1

Figure 25 Bill of Materials for B2B Application Circuit

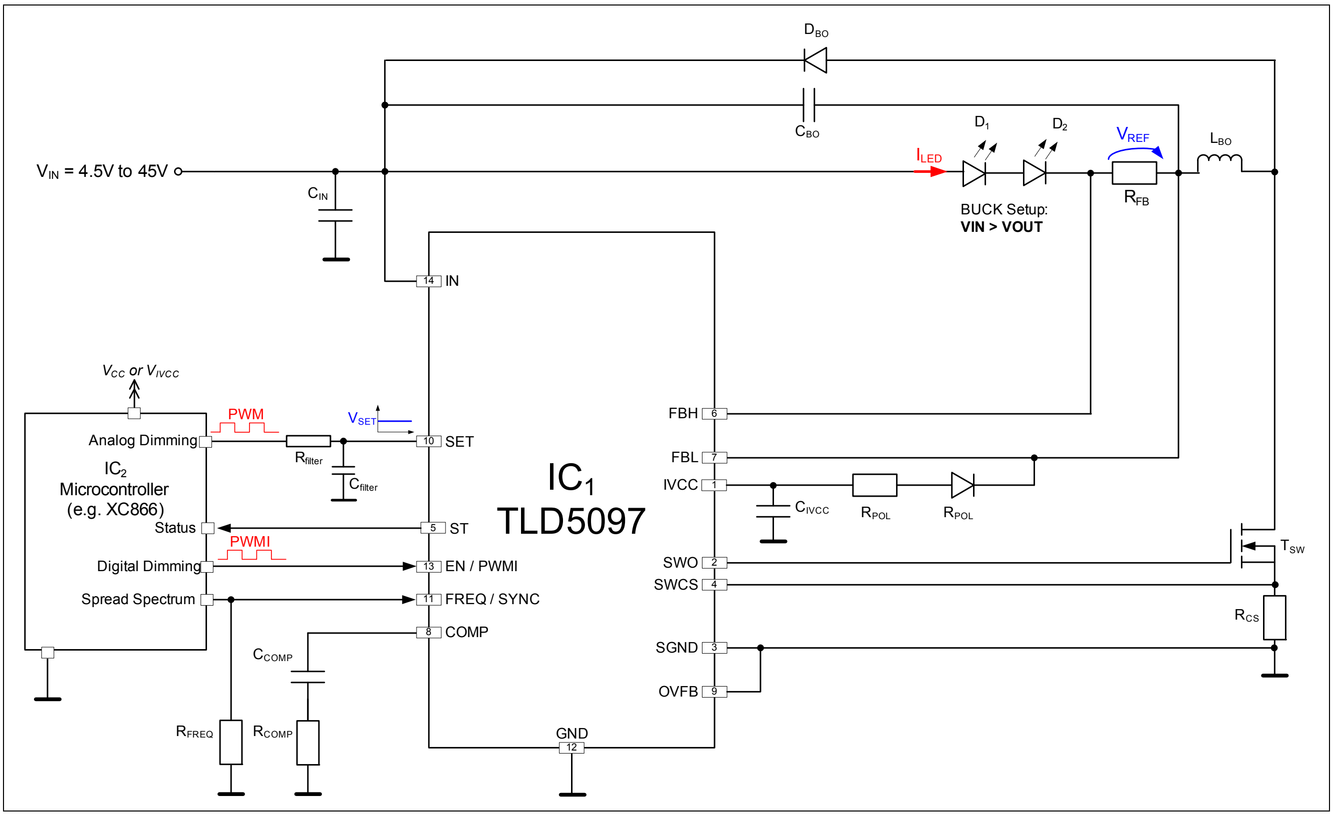

Figure 26 Buck Application Circuit

Reference Designator	Value	Manufacturer	Part Number	Type	Quantity
D_{1-2}	White	Osram	LE UW Q9WP	LED	2
D_{BO}	Schottky, 3 A, 100 V_R	Vishay	SS3H10	Diode	1
D_{POL}	80V Diode	Infineon	BAS1603W	Diode	1
C_{BO}	4.7 uF, 50V	EPCOS	X7R	Capacitor	1
C_{IN}	100 uF, 50V	Panasonic	EEEFK1H101GP	Capacitor	1
C_{COMP}	47 nF	EPCOS	X7R	Capacitor	1
C_{IVCC}	1 uF , 6.3V	EPCOS	MLCC CCNPZC105KBW X7R	Capacitor	1
IC_1	--	Infineon	TLD5097	IC	1
IC_2	--	Infineon	XC866	IC	1
L_1	22 µH	Coilcraft	MSS1278T	Inductor	1
R_{POL}	10 kΩ, 1%	Panasonic	ERJ3EKF1002V	Resistor	1
R_{FB}	820 mΩ, 1%	Isabellenhütte	SMS – Power Resistor	Resistor	1
R_{FREQ}	20 kΩ, 1%	Panasonic	ERJ3EKF2002V	Resistor	1
R_{CS}	50 mΩ, 1%	Isabellenhütte	SMS - Power Resistor	Resistor	1
T_{SW}	100V N-ch, 35A	Infineon	IPG20N10S4L-22	Transistor	1
	alternativ: 60V N-ch, 30A	Infineon	IPD30N06S4L-23	Transistor	1

Figure 27 Bill of Materials for Buck Application Circuit

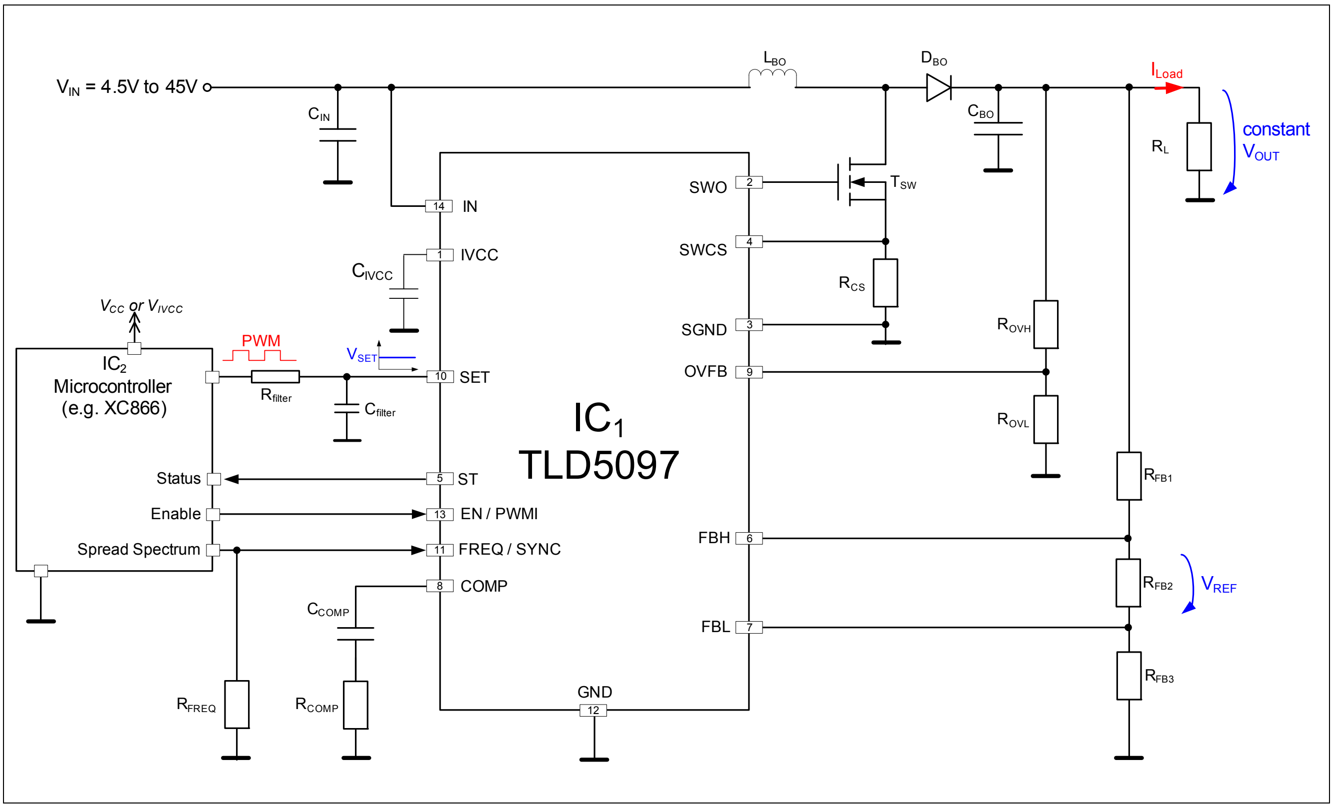

Figure 28 Boost Voltage Application Circuit

Reference Designator	Value	Manufacturer	Part Number	Type	Quantity
D_{BO}	Schottky, 3 A, 100 V_R	Vishay	SS3H10	Diode	1
C_{BO}	100 uF, 80V	Panasonic	EEVFK1K101Q	Capacitor	1
C_{IN}	100 uF, 50V	Panasonic	EEEFK1H101GP	Capacitor	1
C_{COMP}	10 nF, 16V	EPCOS	X7R	Capacitor	1
C_{IVCC}	1 uF, 6.3V	Panasonic	X7R	Capacitor	1
IC_1	--	Infineon	TLD5097	IC	1
IC_2	--	Infineon	XC866	IC	1
L_{BO}	100 uH	Coilcraft	MSS1278T-104ML_	Inductor	1
R_{COMP}	10 kohms, 1%	Panasonic	ERJ3EKF1002V	Resistor	1
R_{FB1},R_{FB3}	51 kohms, 1%	Panasonic	ERJ3EKF5102V	Resistor	1
R_{FB2}	1 kohms, 1%	Panasonic	ERJ3EKF1001V	Resistor	1
R_{FREQ}	20 kohms, 1%	Panasonic	ERJ3EKF2002V	Resistor	1
R_{OVH}	33.2 kohms, 1%	Panasonic	ERJ3EKF3322V	Resistor	1
R_{OVL}	1 kohms, 1%	Panasonic	ERJ3EKF1001V	Resistor	1
R_{CS}	50 mohms, 1%	Panasonic	ERJB1CFR05U	Resistor	1
T_{SW}	N-ch, OptiMOS-T2 100V	Infineon	IPG20N10S4L-22	Transistor	1

Figure 29 Bill of Materials for Boost Voltage Application Circuit

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

11.1 Further Application Information

- For further information you may contact **http://www.infineon.com/**
- Application Note: TLD509x DC-DC Multitopology Controller IC “Dimensioning and Stability Guideline - Theory and Practice”

12 Package Outlines

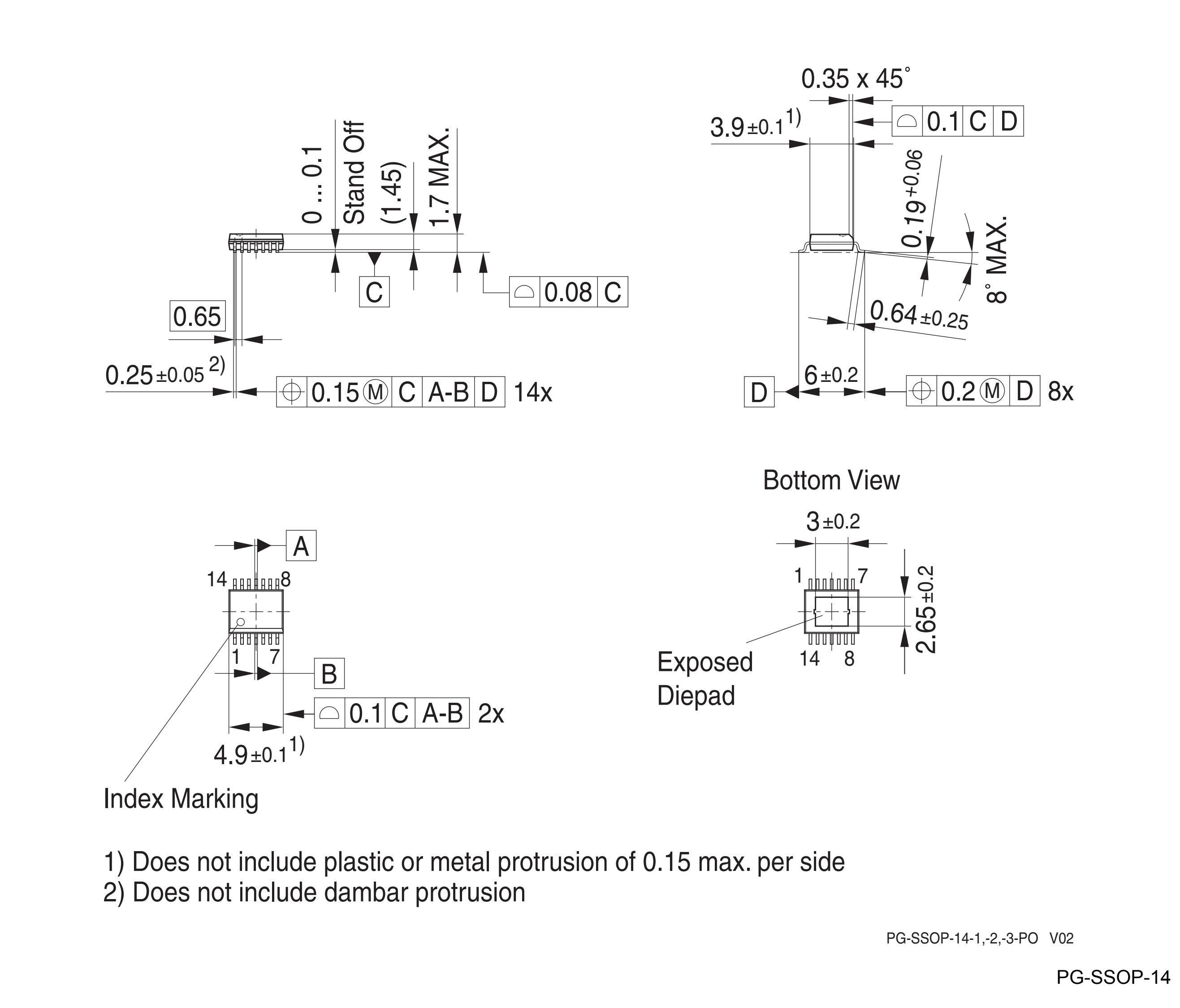

Figure 30 PG-SSOP-14

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further package information, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

13 Revision History

Revision	Date	Changes
1.0	2013-11-12	Initial Datasheet

Edition 2013-11-12

Published by
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