1.125Gbps to 6.25Gbps 4 Channel Signal Repeater

89HP0604Q
Data Sheet

Device Overview

The IDT 89HP0604Q (P0604Q) is a 1.125Gbps to 6.25Gbps Repeater device featuring IDT EyeBoost™ technology that compensates for cable and board trace attenuations and ISI jitter, thereby extending connection reach. The device is optimized for high speed serial data streams and contains four data channels, each able to process 6.25Gbps transmission rates. Each channel consists of an input equalizer and amplifier, signal detection with glitch filter, as well as programmable output swing, slew rate, and de-emphasis with delay control. Since all of these features are user programmable, they allow for application specific optimization.

Besides the per channel programmable features, the P0604Q provides global programmable settings - termination resistance values and transfer modes.

The P0604Q, with its many programmable receiver and transmitter features, is ideal for applications using any combination of cables and board trace materials.

All modes of active data transfer are designed with minimized power consumption. Also, a wide selection of power reducing modes allows the user to eliminate power of unused blocks. In full shutdown mode, the part consumes less than 40mW in worst case environmental conditions.

Applications

- **Protocols:**
  - XAUI, SRIO, CX4, INFINIBAND, CPRI, etc.
- **Systems:**
  - Servers, Telecommunications, Storage, Instrumentation, Active Cabling

Features

- **Compensates for cable and PCB trace attenuation and ISI jitter**
- **Programmable receiver equalization up to 30db**
- **Programmable de-emphasis up to -8.5dB**
- **Recovers data stream even when the differential signal eye is completely closed due to trace attenuation and ISI jitter**
- **Configurable via I^2C interface**
- **Supports automatic download of configuration from external EEPROM with a single or multiple repeaters on I2C bus**
- **Leading edge power minimization in active and shutdown modes**
- **No external bias resistors or reference clocks required**
- **Channel mux mode, demux mode, 1 to 2 channels multicast, and Z-switch function mode**
- **Available in a 36-pin QFN package (4.0x7.5mm & 0.5mm pitch)**

Benefits

- **Extends maximum cable length to over 10 meters and trace length over 65 inches**
- **Speeds up system design time by allowing usage of longer trace and cable lengths**
- **Minimizes BER**

Typical Application

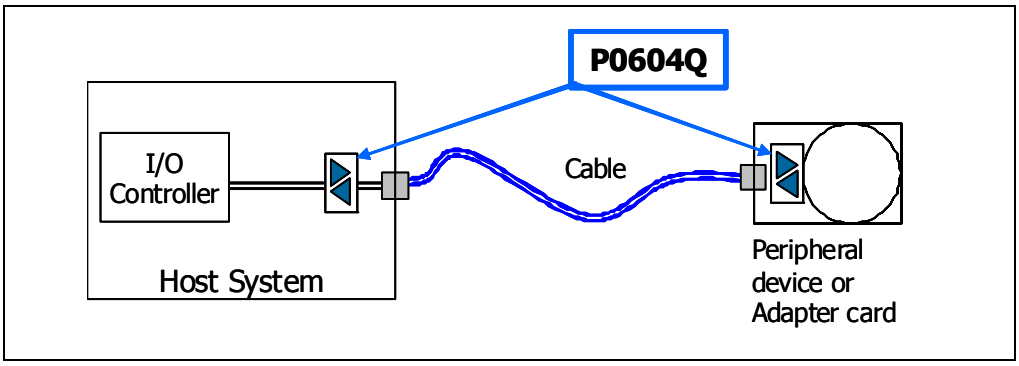

Figure 1 IDT Repeaters in Cabled Applications

P0604Q Block Diagram

The P0604Q contains four high speed channels. Each channel can be routed to different outputs. Depending on user configuration via mode selections, input traffic can be muxed, demuxed, or looped back. Please, refer to modes of operation chapter for details.

Each channel's configuration and performance can be optimized via the I^2C interface (SCL, SDA, A0-A2). The programming option allows the user to optimize the repeater's performance in a wide range of applications, making it an ideal solution for most applications requiring cancellation of trace or cable attenuation and ISI jitter.

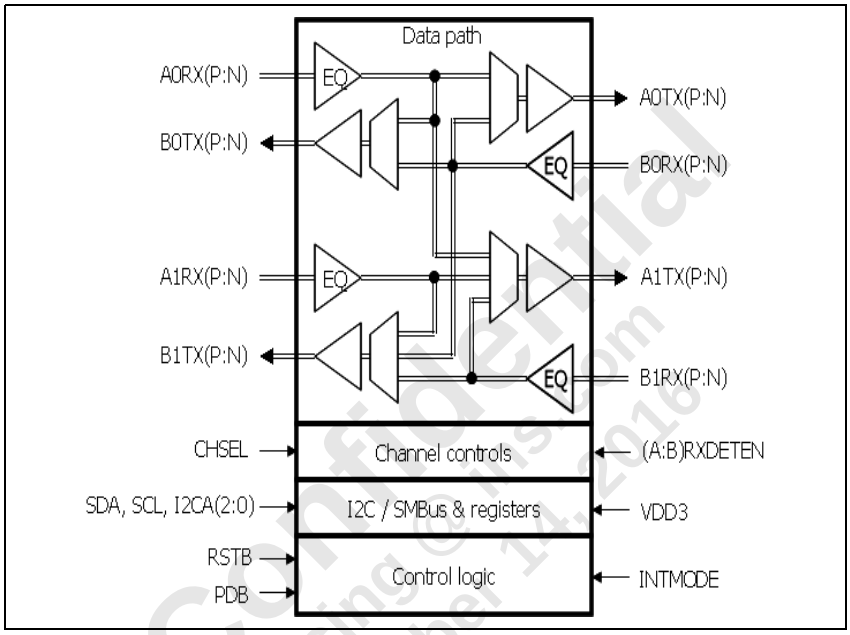

Figure 2 P0604Q Block Diagram

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Data Units

The following data unit terminology is used in this document.

Term	Words	Bytes	Bits
Byte	1/2	1	8
Word	1	2	16
Doubleword (DWord)	2	4	32

Table 1 Data Unit Terminology

In doublewords, bit 31 is always the most significant bit and bit 0 is the least significant bit. In words, bit 15 is always the most significant bit and bit 0 is the least significant bit. In bytes, bit 7 is always the most significant bit and bit 0 is the least significant bit.

Register Terminology

Software in the context of this register terminology refers to modifications made by PCI Express root configuration writes, writes to registers made through the slave SMBus interface, or serial EEPROM register initialization. See Table 4.

Type	Abbreviation	Description
Hardware Initialized	HWINIT	Register bits are initialized by firmware or hardware mechanisms such as pin strapping or serial EEPROM. (System firmware hardware initialization is only allowed for system integrated devices.) Bits are read-only after initialization and can only be reset (for write-once by firmware) with reset.
Read Only and Clear	RC	Software can read the register/bits with this attribute. Reading the value will automatically cause the register/bit to be reset to zero. Writing to a RC location has no effect.
Read Clear and Write	RCW	Software can read the register/bits with this attribute. Reading the value will automatically cause the register/bits to be reset to zero. Writes cause the register/bits to be modified.
Reserved	Reserved	The value read from a reserved register/bit is undefined. Thus, software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. In addition to reserved registers, some valid register fields have encodings marked as reserved. Such register fields must never be written with a value corresponding to an encoding marked as reserved. Violating this rule produces undefined operation in the device.
Read Only	RO	Software can only read registers/bits with this attribute. Contents are hardwired to a constant value or are status bits that may be set and cleared by hardware. Writing to a RO location has no effect.

Table 2 Register Terminology (Part 1 of 2)

Type	Abbreviation	Description
Read and Write	RW	Software can both read and write bits with this attribute.
Read and Write Clear	RW1C	Software can read and write to registers/bits with this attribute. However, writing a value of zero to a bit with this attribute has no effect. A RW1C bit can only be set to a value of 1 by a hardware event. To clear a RW1C bit (i.e., change its value to zero) a value of one must be written to the location. An RW1C bit is never cleared by hardware.
Read and Write when Unlocked		Software can read the register/bits with this attribute. Writing to register/bits with this attribute will only cause the value to be modified if the REGUNLOCK bit in the SWCTL register is set. When the REGUNLOCK bit is cleared, writes are ignored and the register/bits are effectively read-only.

Table 2 Register Terminology (Part 2 of 2)

Functional Description

The P0604Q has 4 channels, each with the individually programmable features listed below. Figure 3 diagrams the channel and Tables 5 and 6 summarize key configuration options.

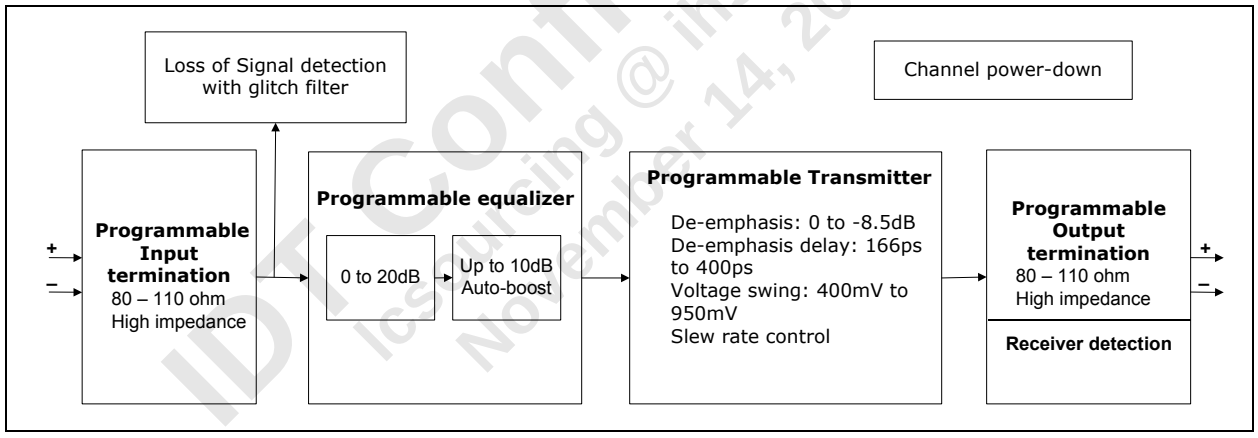

Figure 3 Channel Block Diagram with Channel Features

- Per-channel programmable features used at the RX side (ranges refer to I^2C programming method).
  - Input equalization with 11 levels: 0 to 20dB compensation for high frequency signal attenuation due to cables and board traces. Additionally, up to 10dB boost is added automatically by the equalizer for applications using long cables. The total equalization range is between 0dB and 30dB.
  - Input amplifier DC gain with 7 levels: -2dB to -14dB plus 4 levels for further tuning: -3db to 3dB. The total DC gain is the sum of 7-level gain and 3-level gain controls. This function can be useful for input signals with large swing.
  - Input Loss of Signal detection with 8 levels: 50mV pk-pk to 170mV pk-pk. Measures the envelope of the incoming differential signal (peak-to-peak) and puts the device in Loss of Signal mode when the envelope has fallen below a programmable threshold. In this mode, the transmitter stops toggling, and maintains its common-mode voltage level.
  - Input Loss of Signal detection glitch filter with 4 levels: 2.6ns to 4ns negative glitch removal avoids detection of extremely short spurious signal losses. This is an advanced feature with suggested default setting for most users.
  - Input high impedance control via channel enable: disabled (active mode) and hi-Z (power-down).
- Per-channel programmable features used at the TX side.

- Output de-emphasis with 8 levels: 0 to -8.5dB. The de-emphasis boosts the magnitude of higher frequencies sent by the transmitter to compensate for high frequency losses travelling through output side cable or output side board traces. This ensures that the final received signal has a wider eye opening.
- Output differential swing with 8 levels: 0.4V to 0.95V (peak-to-peak).
- Output slew rate with 4 levels: 45ps to 150ps.
- Output de-emphasis delay control with 4 levels: 166ps to 400ps. When used, this feature should be set to a value of 1UI, which is 166ps for 6Gbps rate, 200ps for 5Gbps rate, 333ps for 3Gbps rate, and 400ps for 2.5Gbps.
- Individual channel power-down (includes Rx and Tx power-down).
- Receiver detection: enable or disable. This function is activated following an RSTB pulse and is done for every channel. The detection results are stored in registers for each channel.

In addition, the device contains global programmable settings:

- Input and output differential termination resistance with 4 levels: 80 ohm, 90 ohm, 100 ohm, 110 ohm.
- Transfer modes: direct connect, cross-connect, multicast, and loopback.

Data Units

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Table 4 Register Terminology (Part 1 of 2)

Type	Abbreviation	Description
Reserved	Reserved	The value read from a reserved register/bit is undefined. Thus, software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. In addition to reserved registers, some valid register fields have encodings marked as reserved. Such register fields must never be written with a value corresponding to an encoding marked as reserved. Violating this rule produces undefined operation in the device.
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Table 4 Register Terminology (Part 2 of 2)

Power-Up

After the power supplies reach their minimum required levels, the P0604Q powers up by setting all input and output pins to known states:

- All the device's input configuration pins are set internally to VSS or VDD for 2-level pins and to VDD/2 for 3-level pins.
- High speed differential input and output pins, status output pins indicating signal detection at high speed inputs, and Receiver detection output states depend on various conditions described below:
  - High speed differential input and output pins are in high impedance if any of the following conditions is true:
    - Powerdown is set (PDB pin = 0V) or
    - Channels containing high speed differential inputs are disabled via pins or
    - Receiver detection is enabled and no receiver termination was detected at TX outputs

  In all other cases, high speed differential input and output pins are set to 50 ohms per pin, with 100 ohms differential impedance. Also refer to Table 9, Power Reducing Modes, Table 7, P0604Q Receiver Impedance, and Table 8, P0604Q Transmitter Impedance.
- Other power-up settings:
  - If INTMODE=OPEN then the programming pins set the configuration for the part.
  - If INTMODE=VDD then the P0604Q is in I^2C master mode (used when external EEPROM is needed).

Power-Up/Power-Down Sequencing

To avoid potential damage to the part, adhere to the following sequence during power supply ramp-up:

– VDD3 supply must be ramped-up and stable at 3.3V prior to VDD supply reaching 1.2V
– Power ramp-up time for VDD should be less than 1 ms to avoid potential I^2C reset and receiver detect issues.

Note: VDD3 supply should be common to all devices communicating on the same I^2C bus.

The power-down sequence can occur in any order.

IDT EyeBoost™ Technology

IDT EyeBoost™ technology is a method of data stream recovery even when the differential signal eye is completely closed due to cable or trace attenuation and ISI jitter. With IDT EyeBoost™ technology, the system designer can both recover the incoming data and retransmit it to target device with a maximized eye width and amplitude. An example of IDT EyeBoost™ usage in a system application and eye diagram results are shown in Figure 4. In this figure, the (a) diagram shows incoming differential signal (closed eye) after 62 inch FR4 connection from signal source and the (b) diagram shows differential signal at the output of repeater maximized eye opening with IDT EyeBoost™ technology.

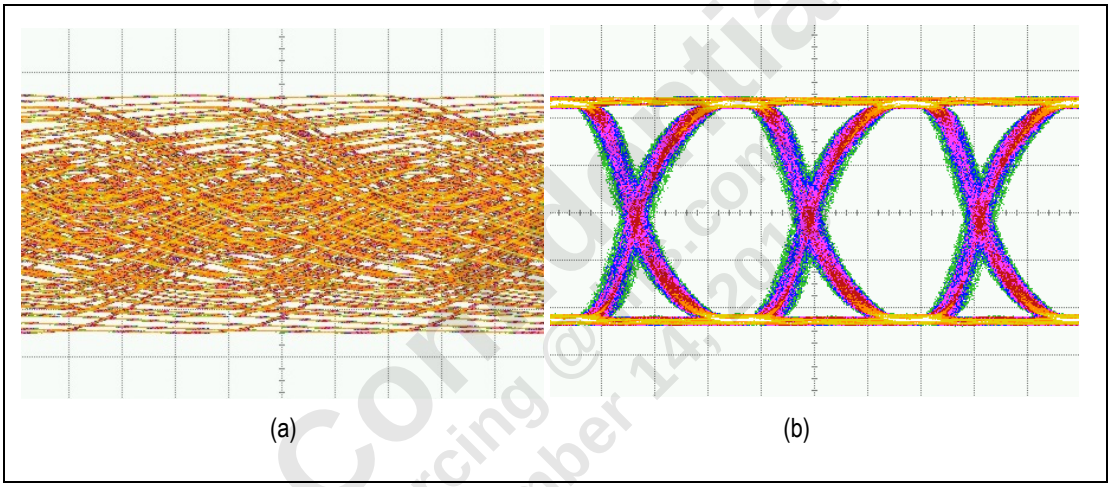


Figure 4 Eye Diagram

Eye Diagram Parameters

Feature	Feature Type	Parameter Names for Programming via I^2C
Input equalization	Main eye optimization	EQ Range: 0dB to 20dB (plus additional auto-boost up to 10dB for long connections)
Input equalization data rate	Main eye optimization	EQDATARATE Range: 2.5Gbps to 8Gbps
Output de-emphasis	Main eye optimization	TX_DEEMP Range: 0dB to -8.5dB
Output differential signal swing (peak-to-peak)	Main eye optimization	TX_SWING Range*: 0.4V to 0.95V*
Output slew rate	Main eye optimization	TX_SLEW Range: 45ps to 150ps

Table 5 Quick Reference: Parameters Used for Eye Optimization (Part 1 of 2)

Feature	Feature Type	Parameter Names for Programming via I²C
Output de-emphasis delay	Main eye optimization	TX_EMP_DELAY Range: 166ps to 400ps
DC gain of Input amplifier	Eye optimization for large swing inputs	DC_GAIN Range: -2dB to -14dB
Equalizer DC gain	Eye optimization for large swing inputs	EQDCGAIN Range: -3dB to 3dB
Limiting Amplifier swing (intermediate stage)	Fine optimization	LA_SWING Range: 560mV to 840mV
Output de-emphasis delay cell offset cancellation loop control	Fine optimization	TX_OC_ENA Range: enable / disable
Channel speed control optimization	Fine optimization	CHEN Range: Disable and 3Gpbs to 6Gbps

Table 5 Quick Reference: Parameters Used for Eye Optimization (Part 2 of 2)

Feature	Feature Type	Parameter Names for Programming via I²C
Rx Loss of Signal detection threshold used for Loss of Signal mode, differential peak-to-peak	NA	SIG_THRESH Range: 50mV to 170mV
Input and output differential termination resistance	NA	TERM_CTL Range: 80 ohm to 110 ohm
Minimum Loss of Signal detection glitch removal	NA	SIG_GLITCHRM Range: 2.6ns to 4ns

Table 6 Quick Reference: Parameters Used for Functions other than Eye Optimization

Receiver Impedance

The table below shows how the receiver impedance changes based on input and output pin states.

Mode	RSTB	Rx Terminations	Description
Full IC Power-down	X	Hi-Z	Receiver terminations placed in Hi-Z.
Channel Enabled	1	50Ω	Receiver detect enabled. Valid receiver detected. Receiver terminations set to 50Ω.

Table 7 P0604Q Receiver Impedance

Transmitter Impedance

The table below shows how the transmitter impedance changes based on input and output pin states.

Mode	RSTB	Tx Terminations	Description
Full IC Power-down	X	1kΩ	Receiver terminations placed in Hi-Z.
Channel Enabled but inactive (loss of signal)	1	50Ω	TX output is squelched. A valid receiver was detected. Receiver terminations set to 50Ω. Output common-mode is held at its active value.
Channel Enabled and active	1	50Ω	TX output is active. A valid receiver was detected. Receiver terminations set to 50Ω.

Table 8 P0604Q Transmitter Impedance

Receiver Detection Support

The P0604Q transmitter fully supports Receiver Detection requirements. For receiver detection to occur, a low pulse (minimum 200ns) must be applied at pin RSTB. The rising edge of the RSTB signal starts the receiver detection procedure. Neither ARXDETEN nor BRXDETEN can be toggled during the receiver detection procedure, i.e., they must be kept high for at least 200ns before the RSTB rising edge and they cannot go to low sooner than 2ms from the time the RSTB goes high. The receiver detection takes place once per RSTB pulse.

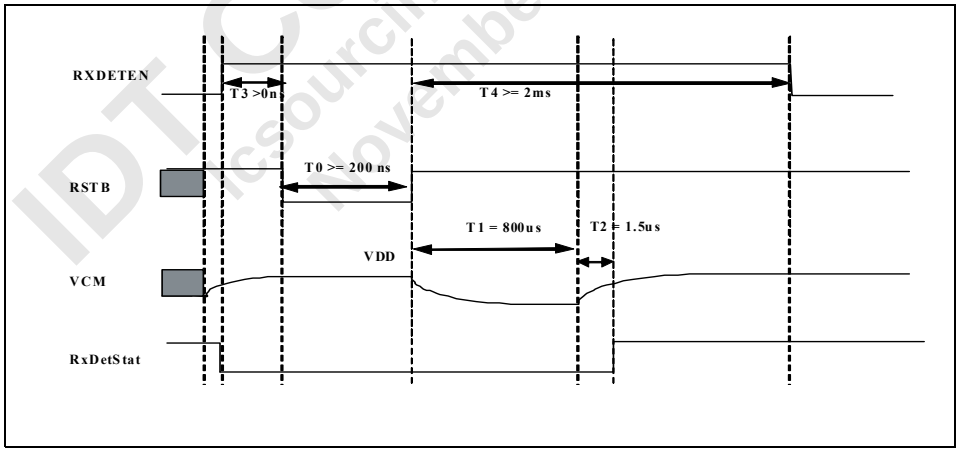


Figure 5 Receiver Detection Timing

Modes of Operation

The device supports several data transfer modes, Loss of Signal mode, loopback mode, and several power reducing modes.

Loss of Signal Mode

In Loss of Signal mode, the transmitter stops toggling and maintains its common-mode voltage level. The device enters this mode when the envelope of the incoming signal on a given channel has fallen below a programmable threshold level.

Power Reducing Modes

The Repeater supports five power-down states and one active state as shown in Table 9. The user can choose between full chip power-down, channel based power-down, and Loss of Signal modes. Power reducing modes can be selected via PDB or RSTB.

Power Reducing Mode	PDB	RSTB	State Description
Full IC power-down	0	X	All channels are powered-down Receiver detect reset Rx termination is set to Hi-Z Tx termination is set to 1kΩ Tx common-mode is at VDD
Receiver Detect reset	1	0	Receiver detect state machine Receiver terminations placed in Hi-Z Tx termination is set to 1kΩ Tx common-mode is at VDD
Channel enabled but inactive. Rx and Tx set to hi-Z	1	1	Tx output is squelched No receiver was Detected Receiver terminations placed in Hi-Z Tx termination is set to 1kΩ Tx common-mode is at VDD
Channel enabled but inactive. Rx and Tx set to 50 Ohms	1	1	Tx output is squelched A valid receiver was detected Receiver terminations set to 50Ω Output common-mode is held at its active value Tx termination is set to 50Ω
Channel enabled and active. No power-down	1	1	Tx output is active A valid receiver was detected Receiver terminations set to 50Ω Transmitter terminations set to 50Ω

Table 9 Power Reducing Modes

Loopback Mode

The P0604Q fully supports data loopbacks on all channels via I^2C using the CTRL register. Refer to Table 14 for this parameter setting.

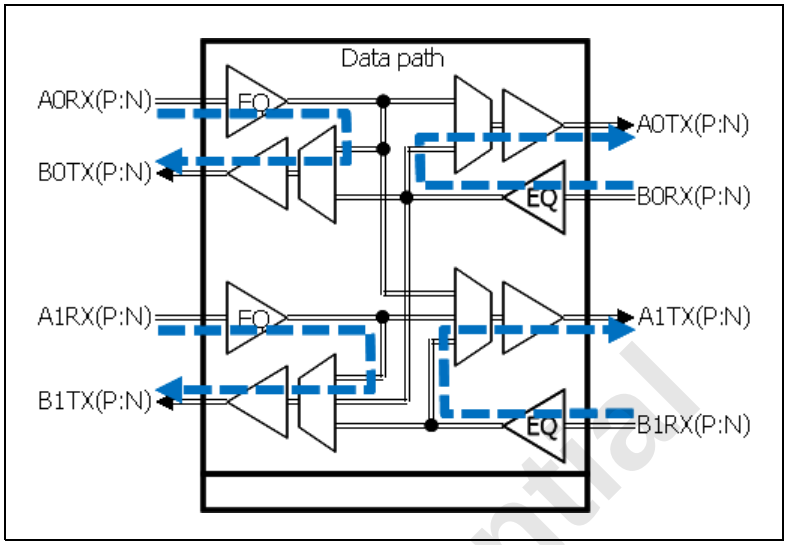


Figure 6 Diagram of P0604Q Configuration in Loopback Mode

Channel Muxing

The P0604Q repeater permits a variety of muxing, demuxing, and switching configurations, and it can mux/de-mux 1 or 2 bi-directional lanes into 2 target devices. These configurations require the selection of specific pins for input and output ports. In the following sections, each configuration is described in terms of pin connectivity to external upstream and downstream devices. The configurations shown are those often used in system designs:

- Uni-directional 2:1 Mux (1 or 2 instances)
- Uni-directional 1:2 De-Mux (1 or 2 instances)
- Bi-directional 2:1 Mux/De-Mux
- Bi-directional Z-function (also called Partial Cross Function)

The P0604Q supports channel muxing in both upstream and downstream channel directions via the CHSEL pin, as shown below. Figure 7 shows the channel/reference muxing modes and Table 10 shows how CHSEL (Channel transfer selection) pin allows for various modes of data transfers: Multicast mode, Direct-connect, and Cross-connect. Both Direct-connect, and Cross-connect modes are used to build uni-directional and bi-directional 2:1 mux and Z-switch functions.

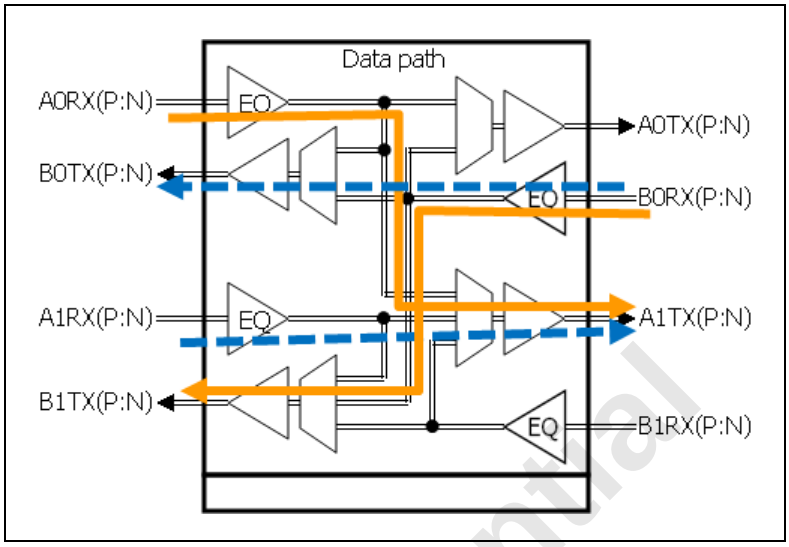


Figure 7 Diagram of P0604Q Channel/Reference Muxing Modes

Input Pins					Output Pins			
CHSEL	**A0RX[P,N]**	**A1RX[P,N]**	**B0RX[P,N]**	**B1RX[P,N]**	**A0TX[P,N]**	**A1TX[P,N]**	**B0TX[P,N]**	**B1TX[P,N]**
CHSEL=VSS (Multicast Mode)	A0 DATA	X	B0 DATA	X	A0 DATA	A0 DATA	B0 DATA	B0 DATA
CHSEL=Open (Direct-Connect Mode)	A0 DATA	A1 DATA	B0 DATA	B1 DATA	A0 DATA	A1 DATA	B0 DATA	B1 DATA
CHSEL=VDD (Cross-Connect Mode)	A0 DATA	X	B0 DATA	X	Squelched	A0 DATA	Squelched	B0 DATA

Table 10 Description of Channel Muxing/De-Muxing Functionality

The signal detect output pins support the functionality shown in Table 11.

Input Pins				
CHSEL	**A0RX[P,N]**	**A1RX[P,N]**	**B0RX[P,N]**	**B1RX[P,N]**
CHSEL=VSS (Multicast Mode)	A0 Data	A1 Data	B0 Data	B1 Data
CHSEL=Open (Direct-Connect Mode)	A0 Data	A1 Data	B0 Data	B1 Data
CHSEL=VDD (Cross-Connect Mode)	A0 Data	X	B0 Data	X

Table 11 Description of Signal Detect Muxing/De-Muxing Functionality

Uni-directional 2:1 Mux or Two Instances of Unidirectional 2:1 Mux

This function can be achieved by using the CHSEL pin as a mux control signal. CHSEL should be set to either VDD or OPEN. The ports should be configured as shown in Figure 8.

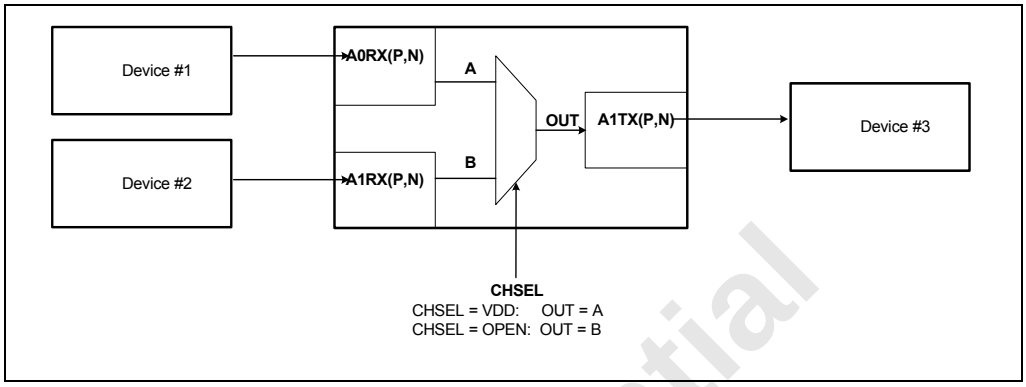


Figure 8 Implementation of Unidirectional 2:1 Mux

As an alternative, different chip channels can also be selected as shown in Figure 9. This solution can be combined with the previous one to obtain two instances of Uni-directional 2:1 Mux.

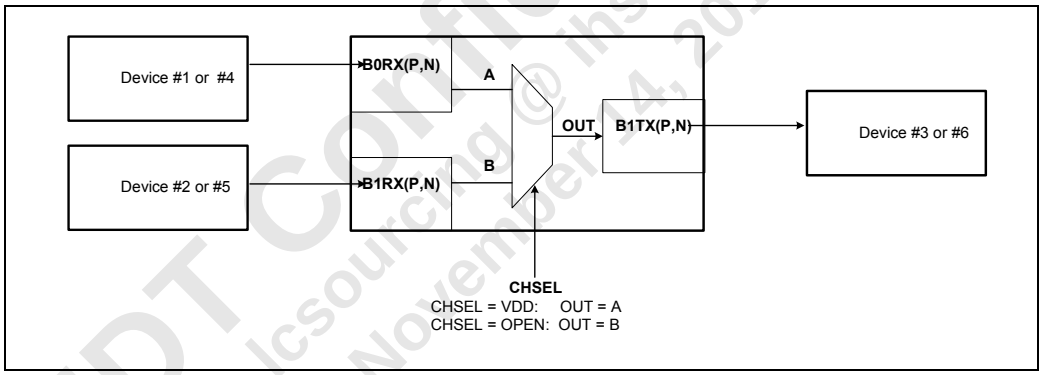


Figure 9 Implementation of Second Instance of Unidirectional 2:1 Mux

Uni-directional 1:2 De-Mux or Two Instances of Unidirectional 1:2 De-Mux

This function can be achieved by using CHSEL pin as a de-mux control signal. CHSEL should be set to either VDD or OPEN. The ports should be configured as shown in Figure 10.

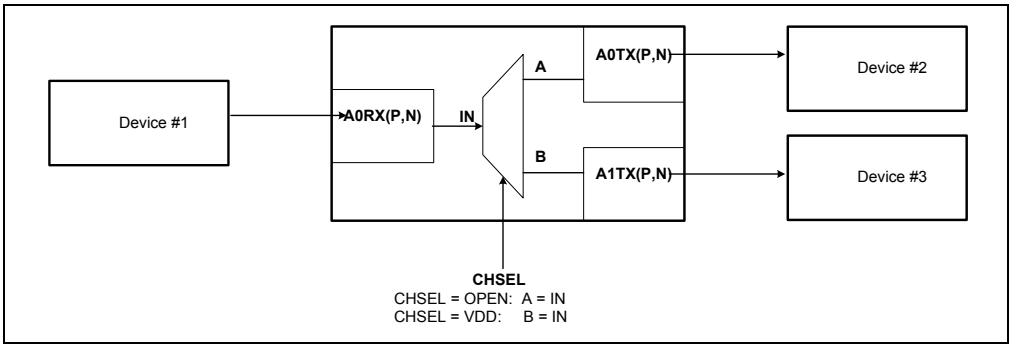


Figure 10 Implementation of Unidirectional 1:2 De-Mux

As an alternative, different chip channels can also be selected as shown in Figure 11. This solution can be combined with the previous one to obtain two instances of Uni-directional 1:2 De-Mux.

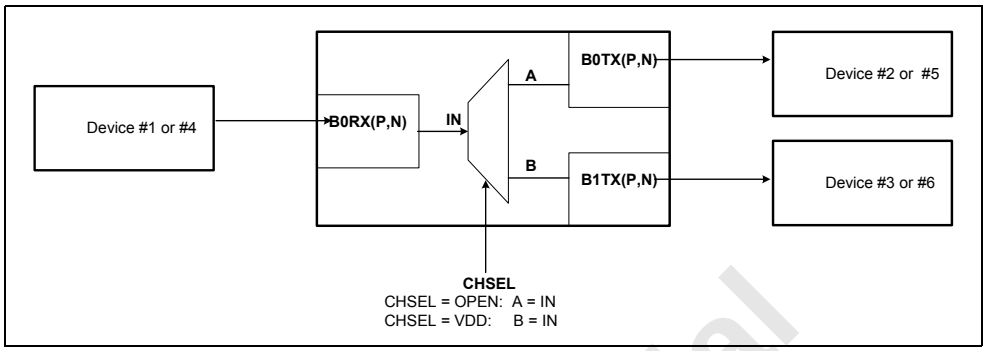


Figure 11 Implementation of Second Instance of Unidirectional 1:2 De-Mux

Bi-directional 2:1 Mux/De-Mux

The bi-directional Mux and De-Mux function can also be achieved by using the CHSEL pin as a mux control signal. CHSEL should be set to either VDD or OPEN. The ports should be configured as shown in Figure 12.

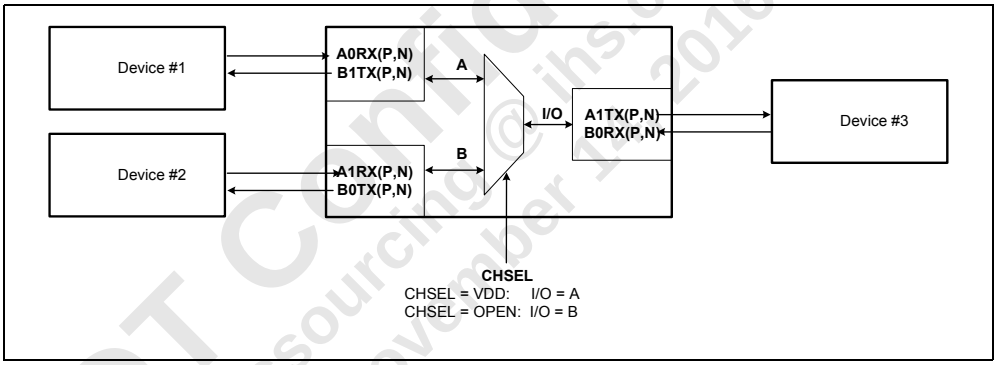


Figure 12 Implementation of Bi--directional 2:1 Mux/De-Mux

Bi-directional Z-function (also called Partial Cross Function)

This function can also be achieved by using the CHSEL pin as a flow control signal. CHSEL should be set to either VDD or OPEN. The ports should be configured as shown in Figure 13.

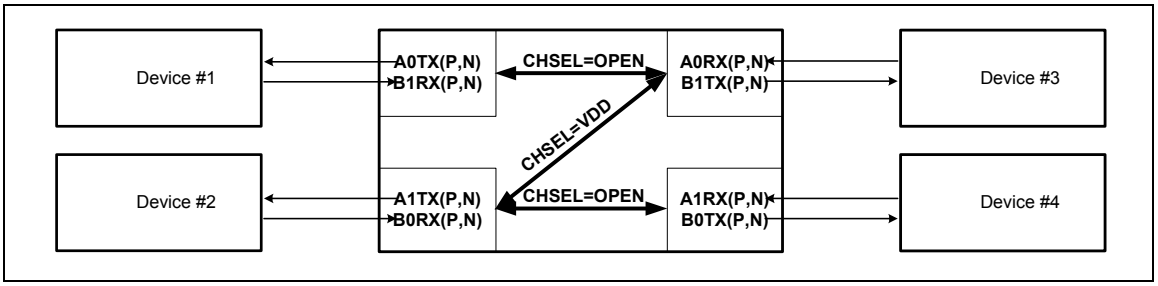


Figure 13 Implementation of Z-function

I²C Registers

I²C Register Description Summary

Table 12 provides a summary of the P0604Q register set. Registers are organized as 4-bytes (Dword). Channel-specific parameters are assigned one byte for each channel within the Dword. The following sections describe the serial slave and master/EEPROM modes of operation.

	Bits			
	[31:24]	[23:16]	[15:08]	[07:00]
Address Offset (hex)	Channel B1	Channel B0	Channel A1	Channel A0
00	Vendor ID (VID)			
01	Device ID (DID)			
02	Revision ID (RID)			
03	DC_GAIN	DC_GAIN	DC_GAIN	DC_GAIN
04	EQDATARATE	EQDATARATE	EQDATARATE	EQDATARATE
05	EQDCGAIN	EQDCGAIN	EQDCGAIN	EQDCGAIN
06	EQ	EQ	EQ	EQ
07	LA_SWING	LA_SWING	LA_SWING	LA_SWING
08	SIG_THRESH	SIG_THRESH	SIG_THRESH	SIG_THRESH
09	SIG_GLITCHRM	SIG_GLITCHRM	SIG_GLITCHRM	SIG_GLITCHRM
0A	SIG_FORCESIGDET	SIG_FORCESIGDET	SIG_FORCESIGDET	SIG_FORCESIGDET
0B	TX_SWING	TX_SWING	TX_SWING	TX_SWING
0C	TX_DEEMP	TX_DEEMP	TX_DEEMP	TX_DEEMP
0D	TX_SLEW	TX_SLEW	TX_SLEW	TX_SLEW
0E	TX_EMP_DELAY	TX_EMP_DELAY	TX_EMP_DELAY	TX_EMP_DELAY
0F	TX_OC_ENA	TX_OC_ENA	TX_OC_ENA	TX_OC_ENA
10	DET_STATUS	DET_STATUS	DET_STATUS	DET_STATUS
11	CHEN	CHEN	CHEN	CHEN
12	Global control register			
13	Reserved			
14	I2CSTS register			
15	I2CCTL register			
16	EEPROM control register			

Table 12 I²C Register Description Summary

The I2C registers are implemented in 32 bit wide (DWord).

Vendor Identification Register

Address Offset (hex)	Field Name	Type	Default Value	Description
00h	VID	R0	111Dh	16 bit Vendor ID for IDT

Device Identification Register

Address Offset (hex)	Field Name	Type	Default Value	Description
01h	DID	R0	80AAh	16 bit Device ID for P0604Q

Revision Identification Register

Address Offset (hex)	Field Name	Type	Default Value	Description
02h	RID	R0	08h	Revision ID for device version

Channel Based Register

The I^2C register shown below is implemented in a 32-bit wide format. For each register, bits 31:24 are for channel B1, 23:16 for B0, 15:8 for A1, and 7:0 for A0.

Address Offset (hex)	Register Name	Type	Default Value	Description
03h	DC_GAIN	RW	01h	DC Gain of Input Amplifier. Used for reducing input signal swings to adapt them better to internal RX circuits.[1] 00h: -2dB 04h: -8dB 01h: -4dB(default) 05h: -10dB 02h: -6dB 06h: -12dB 03h: -8dB 07h: -14dB Usage details: Settings between -6db and -14db might reduce output jitter if input swing is larger than 800mVpp diff. Corresponding programming pins: N/A.
04h	EQDATARATE	RW	02h	Input Equalization Data Rate 00h: 2.5 to 3 Gbps data rate 01h: 5 Gbps data rate 02h: 6 Gpbs data rate (default) 03h: 8 Gpbs data rate Usage details: Set to the data rate used in end application. Sometimes, a minor improvement can be seen by setting 5Gbps at 6Gbps speeds (or vice versa). This depends on the number of connectors and line length. Corresponding programming pins: N/A
05h	EQDCGAIN	RW	01h	Equalizer DC Gain Control. Used for large swing input signals. 00h: -3dB 01h: -1dB (default) 02h: 1dB 03h: 3dB Usage details: Typically left at default, but might need to be set to -3db if the input swing is above 1000mVppdiff. Corresponding programming pins: N/A
06h	EQ	RW	03h	Input Equalization at selected F=EQDATARATE/2 00h: +0dB 08h: +16dB 01h: +2dB 09h: +18dB 02h: +4dB 0Ah: +20dB 03h: +6dB 0Bh: Reserved 04h: +8dB 0Ch: Reserved 05h: +10dB 0Dh: Reserved 06h: +12dB 0Eh: Reserved 07h: +14dB 0Fh: Reserved Usage details: Set to 0dB - 10db for traces and cables based on input channel length. Can also be set to higher dB values for very long input cables. Corresponding programming pins: N/A

Table 13 P0604Q I^2C Register (Part 1 of 3)

Address Offset (hex)	Register Name	Type	Default Value	Description
07h	LA_SWING	RW	02h	Internal Limiting Amplifier Programmable Swing. Used for fine optimization. 00h: 700mV$_{diff-pkpk}$ - 20% 01h: 700mV$_{diff-pkpk}$ 02h: 700mV$_{diff-pkpk}$(default) 03h: 700mV$_{diff-pkpk}$+ 20% Usage details: Typically left at default. Used for fine optimization. May slightly reduce jitter for some combinations of connectors and line lengths. Does not interact with TX_SWING settings. Corresponding programming pins: N/A
08h	SIG_THRESH	RW	03h	Rx Loss of Signal Detection Threshold 00h: 50mV$_{diff-pkpk}$ 01h: 70mV$_{diff-pkpk}$ 02h: 90mV$_{diff-pkpk}$ 03h: 110mV$_{diff-pkpk}$ (default) 04h: 120mV$_{diff-pkpk}$ 05h: 140mV$_{diff-pkpk}$ 06h: 150mV$_{diff-pkpk}$ 07h: 170mV$_{diff-pkpk}$ Usage details: Set to desired value based on end application. Loss of signal can be disabled completely via SIG_PD_TRANDET and SIG_PD_LVLDET bits. Corresponding programming pins: N/A
09h	SIG_GLITCHRM	RW	00h	Minimum Loss of Signal Detection Glitch Removal. Advanced feature. 00h: 2.6n (default) 01h: 3.1n 02h: 3.5n 03h: 4.0n Usage details: Typically left at default (2.6ns). Corresponding programming pins: N/A
0Ah	SIG_FORCESIGDET	RW	00h	Force Output of Signal Detection 00h: Normal operation 01h: Force RX_SIGNALDET to 1 Usage details: Not used.
0Bh	TX_SWING	RW	04h	Transmitter Differential Swing Peak-to-Peak (typical) (see $V_{TX-DIFF-PP}$ and $V_{TX-DIFF-PP-LOW}$ transmitter specifications) 00h - 0.4Vdiff-pkpk 01h - 0.5Vdiff-pkpk 02h - 0.6Vdiff-pkpk 03h - 0.7Vdiff-pkpk 04h - 0.8Vdiff-pkpk 05h - 0.85Vdiff-pkpk 06h - 0.90Vdiff-pkpk 07h - 0.95Vdiff-pkpk Usage details: Set to desired TX driver amplitude. Typically, higher values are recommended when TX has to drive over longer distances. Corresponding programming pins: N/A

Table 13 P0604Q I^{2}C Register (Part 2 of 3)

Address Offset (hex)	Register Name	Type	Default Value	Description
0Ch	TX_DEEMP	RW	02h	Output De-emphasis. Defined as 20log($V_{TX-DE-EMP}$ / $V_{TX-DIFF}$) [dB] 00h: +0dB 01h: -2.5dB 02h: -3.5dB 03h: -4.5dB 04h: -5.5dB 05h: -6.5dB 06h: -7.5dB 07h: -8.5dB Usage details: Typically, value should be more negative when TX has to drive over longer distances. Corresponding programming pins: N/A
0Dh	TX_SLEW	RW	00h	Output Rise/Fall (20% - 80% levels) 00h: 45ps (default) 01h: 50ps 02h: 70ps 03h: 150ps Usage details: Set to desired TX slew rate Corresponding programming pins: N/A
0Eh	TX_EMP_DELAY	RW	00h	Output De-emphasis Delay 00h: 166ps, 6Gbps mode (default) 01h: 200ps, 5Gbps mode 02h: 333ps, 3Gbps mode 03h: 400ps, 2.5Gbps mode Usage details: Needed only when de-emphasis is used. Select delay closest to data rate period (example: 5Gb->200ps). See Figure 21. Corresponding programming pins: N/A
0Fh	TX_OC_ENA	RW	01h	Transmitter De-emphasis Delay Cell Offset Cancellation Loop Control. Used for fine optimization. 00h: disable the loop 01h: enable the loop (default) Usage details: Left at default (enabled). Corresponding programming pins: N/A
10h	DET_STATUS	R	00h	Input Loss of Signal Detection and Rx Detection Status Bit 0: 1 = input has signal Bit 1: 1 = output has receiver
11h	CHEN	RW	03h	Channel Enable and Speed Control Bit 0: 1 = enable, 0 = disable Bit 1: 1 = used for wide frequencies of operation from 1.5Gbps to 6Gbps, 0 = used for frequencies of operation from 1.5Gbps to 3Gbps. Usage details: Based on channel usage and frequencies of operation required in end applications. Corresponding programming pins: N/A

Table 13 P0604Q I^2C Register (Part 3 of 3)

1. During the readout of this register for channel A0 only: Readout value = (Last value written into DC-GAIN register) + 08h (e.g. 00h setting reads out as 08h).

Global Control Register (address offset=012h)

Bit Field	Field Name	Type	Default Value	Description
1:0	TERM_CTL	RW	10	Input and Output Differential Termination (typical) 00 – 80Ω differential impedance 01 – 90Ω differential impedance 10 – 100Ω differential impedance (default) 11 – 110Ω differential impedance Usage details: Set to value 2 times higher than line impedance. Corresponding programming pins: N/A
5:2	CTRL	RW	0001	Data Transfer Control 0001: direct connect (default) 0010: multicast mode 0100: cross connect mode 1000: loopback mode Usage details: Set to desired mode of transfer. Corresponding programming pins: N/A
11:6	Reserved	RO	000000	Reserved bits
12	RXDET_EXT	RW	0	Write 1 to this bit to extend the time allowed for Tx common mode voltage negative step from 800µs to 1.2ms. Advanced feature.
20:13	Reserved	RO	00h	Reserved bits
21	SIG_PD_TRANDET	RW	0	Transition Detection in Input Signal Detector 0: enable 1: disable Usage details: Typically left at default. Signal detection can be disabled completely via SIG_PD_TRANDET and SIG_PD_LVLDET bits. Corresponding programming pins: N/A
22	SIG_PD_LVLDET	RW	0	Level Detection in Input Signal Detector 0: enable 1: disable Usage details: Typically left at default. Signal detection can be disabled completely via SIG_PD_TRANDET and SIG_PD_LVLDET bits. Corresponding programming pins: N/A
23	LA_EQ_ENA	RW	1	Limiting Amplifier Equalization Peaking Control. Advanced feature. 0: disable 1: enable Usage details: Typically left at default. Corresponding programming pins: N/A
24	Reserved	RW	1	Reserved bit
31:25	Reserved	RO	0000000	Reserved bits

Table 14 Global Control Register (OFFSET = 012h)

Test Control Register — Reserved (address offset=013h)

I²C Status Register (I2CSTS) (address offset=014h)

Bit Field	Field Name	Type	Default Value	Description
0	Reserved	RO	0	Reserved
7:1	SI2CADDR	RO	HWINIT	Slave I²C address
8	Reserved	RO	0	Reserved
15:9	MI2CADDR	RO	HWINIT	Master I²C address
16	MODE	RO	HWINIT	This field specifies the mode that the device's I²C master interface initialize in. 0x0: talking mode 0x1: listening mode
21:17	Reserved	RO	00000	Reserved
22	BLANK	RW1C	0	Blank Serial EEPROM
23	ROLLOVER	RW1C	0	EEPROM rolled over
24	EEPROMDONE	RO	0	EEPROM_DONE
25	NAERR	RW1C	0	No Acknowledge Error
26	Reserved	RO	0	Reserved
27	OTHERERR	RW1C	0	Other Error
28	CSERR	RW1C	0	Checksum Error
29	URIA	RW1C	0	Unmapped register initialization attempt
31:30	Reserved	RO	0	Reserved

Table 15 I²C Status Register (OFFSET=014h)

I²C Control Register (I2CCTL) (address offset=015h)

Bit Field	Field Name	Type	Default Value	Description
15:0	MI2CCP	RO		Master I²C clock prescaler Final Master I²C clk freq = msmbcp x 8 x oscillator_clk_period
16	Reserved	RO	0	Reserved
17	ICHECKSUM	RW	0	Ignore checksum error
19:18	SI2CMODE	RW	01	Slave I²C mode 00: Glitch counters operate with 1 us delay 01: Glitch counters operate with 100 ns delay 10: Disabled

Table 16 I²C Control Register (OFFSET=015h)

Bit Field	Field Name	Type	Default Value	Description
21:20	MI2CMODE	RW	00	Master I^2C mode Same encodings as Slave I^2C mode
22	I2CDTO	RW	0	I^2C disable timeout
31:23	Reserved	RO	000000000	Reserved

Table 16 I^2C Control Register (OFFSET=015h)

EEPROM Control Register (address offset=16h)

Bit Field	Field Name	Type	Default Value	Description
7:0	SIZE	HWINIT	00h	This field sets the size of each partition in EEPROM, according to 64*2^SIZE: 00h: 64 bytes 01h: 128 bytes 02h: 256 bytes 03h: 512 bytes 04h: 1024 bytes 05h: 2048 bytes 06h: 4096 bytes 07h: 8192 bytes 08h: 16384 bytes others: reserved This field, and the other fields in this register are critical for external EEPROM operation and must be stored at the address 0 of EEPROM memory space using single Double-word format. Other register configurations must be stored in EEPROM space after this register configuration.
15:8	VECTOR	HWINIT	FFh	This field indicates which P0604Qs are present on the shared I2C bus. Bit 8: P0604Q(0) is present (I2CA[2:0]=000) Bit 9: P0604Q(1) is present (I2CA[2:0]=001) Bit 10: P0604Q(2) is present (I2CA[2:0]=010) … Bit 15: P0604Q(7) is present (I2CA[2:0]=111) This field, and the other fields in this register are critical for external EEPROM operation and must be stored at the address 0 of EEPROM memory space using single Double-word format. Other register configurations must be stored in EEPROM space after this register configuration.
31:16	Reserved	RO	0000h	Reserved

Table 17 External EEPROM Control Register (OFFSET=016h)

Serial Interface

The P0604Q interface supports I2C interfaces. The P0604Q has two interface operating modes, slave and master. The slave I2C mode provides full access to all software-visible registers, allowing every register in the device to be read or written by an external I2C master. The master I2C mode provides connection for an optional external serial EEPROM used for initialization. Once initialized, the P0604Q switches to slave mode. I2C interfaces contain an I2C clock pin and an I2C data pin. The master and slave interfaces share the same set of address pins I2CA[2:0].

The pin INTMODE controls if the I2C is in the master or the slave mode. When INTMODE=low, the interface is in the slave mode, when INTMODE=high, it is in the master mode. When INTMODE=mid, the P0604Q is in pin control mode.

I2C Slave Mode

The slave I2C mode provides the P0604Q with a configuration, management, and debug interface. Using the slave I2C mode, an external master can read or write any software-visible register in the device.

Initialization

Slave I2C initialization occurs during a switch fundamental reset. During the switch fundamental reset initialization sequence, the slave I2C address is initialized. The address is specified by the I2CA[2:0] signals as shown in Table 18.

Address Bit	Address Bit Value
1	I2CA0
2	I2CA1
3	I2CA2
4	0
5	1
6	1
7	1

Table 18 Slave I2C Address

I2C Transactions

The slave I2C interface responds to the following I2C transactions initiated by an I2C master. Refer to the I2C 2.0 specification for a detailed description of these transactions.

- Byte and Word Write/Read
- Block Write/Read

Initiation of any I2C transaction other than those listed above to the slave I2C interface produces undefined results. Associated with each of the above transactions is a command code. The command code format for operations supported by the slave I2C interface is shown in Table 19 and described in Table 20.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PEC	SIZE		FUNCTION			START	END

Table 19 Slave I2C Command Code Format

Bit Field	Name	Description
0	END	End of transaction indicator. Setting both START and END signifies a single transaction sequence 0 - Current transaction is not the last read or write sequence. 1 - Current transaction is the last read or write sequence.
1	START	Start of transaction indicator. Setting both START and END signifies a single transaction sequence 0 - Current transaction is not the first of a read or write sequence. 1 - Current transaction is the first of a read or write sequence.
4:2	FUNCTION	This field encodes the type of I^2C operation. 0 - CSR register read or write operation 1 - 7 Reserved
6:5	SIZE	This field encodes the data size of the I^2C transaction. 0 - Byte 1 - Word 2 - Block 3 - Reserved
7	PEC	This bit controls whether packet error checking is enabled for the current I^2C transaction. 0 - Packet error checking disabled for the current I^2C transaction. 1 - Packet error checking enabled for the current I^2C transaction.

Table 20 Slave I^2C Command Code Fields

The FUNCTION field in the command code indicates if the I^2C operation is a system address register read/write or a serial EEPROM read/write operation, since the format of these transactions is different. Both operations are described in the following sections. If a command is issued while one is already in progress or if the slave is unable to supply data associated with a command, then the command is NACKed. This indicates to the master that the transaction should be retried.

CSR Register Read or Write Operation

Table 21 indicates the sequence of data as it is presented on the slave I^2C following the byte address of the Slave I^2C interface.

Byte Position	Field Name	Description
0	CCODE	**Command Code.** Slave Command Code field described in Table 20.
1	BYTCNT	**Byte Count.** The byte count field is only transmitted for block type I^2C transactions. I^2C word and byte accesses do not contain this field. The byte count field indicates the number of bytes following the byte count field when performing a write or setting up for a read. The byte count field is also used when returning data to indicate the number of following bytes (including status). *Note that the byte count field does not include the PEC byte if PEC is enabled.*
2	CMD	**Command.** This field encodes fields related to the CSR register read or write operation.
3	ADDRL	**Address Low.** Lower 8-bits of the double-word system address of register to access.

Table 21 CSR Register Read or Write Operation Byte Sequence (Part 1 of 2)

Byte Position	Field Name	Description
4	ADDRU	**Address Upper.** Upper 8-bits of the double-word system address of register to access.
5	DATALL	**Data Lower.** Bits [7:0] of data double-word.
6	DATALM	**Data Lower Middl**e. Bits [15:8] of data double-word.
7	DATAUM	**Data Upper Middle.** Bits [23:16] of data double-word.
8	DATAUU	**Data Upper.** Bits [31:24] of data double-word.

Table 21 CSR Register Read or Write Operation Byte Sequence (Part 2 of 2)

The format of the CMD field is shown in Table 22 and described in Table 23.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WERR	RERR	0	OP	Fh			

Table 22 CSR Register Read or Write CMD Field Format

Bit Field	Name	Type	Description
0	1	1	Reserved. Must be One.
1	1	1	Reserved. Must be One.
2	1	1	Reserved. Must be One.
3	1	1	Reserved. Must be One.
4	OP	Read/Write	CSR Operation. This field encodes the CSR operation to be performed. 0 - CSR write 1 - CSR read
5	0	0	Reserved. Must be zero
6	RERR	Read-Only and Clear	Read Error. This bit is set if the last CSR read I^2C transaction was not claimed by a device. Success indicates that the transaction was claimed and not that the operation completed without error.
7	WERR	Read-Only and Clear	Write Error. This bit is set if the last CSR write I^2C transaction was not claimed by a device. Success indicates that the transaction was claimed and not that the operation completed without error.

Table 23 CSR Register Read or Write CMD Field Description

Sample Slave I²C Operation

This section illustrates sample Slave I²C operations. Shaded items are driven by the P0604Q's slave I²C interface and non-shaded items are driven by an I²C host.

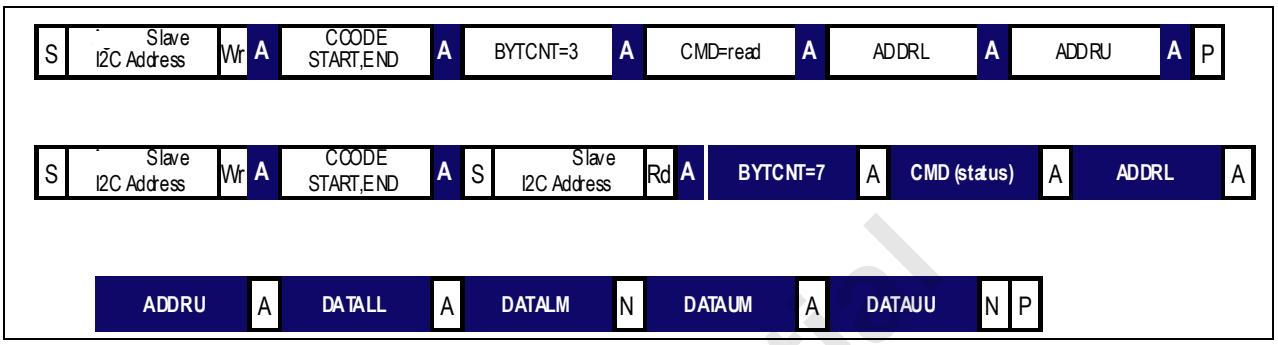


Figure 14 CSR Register Read Using I²C block Write/Read Transactions with PEC Disabled

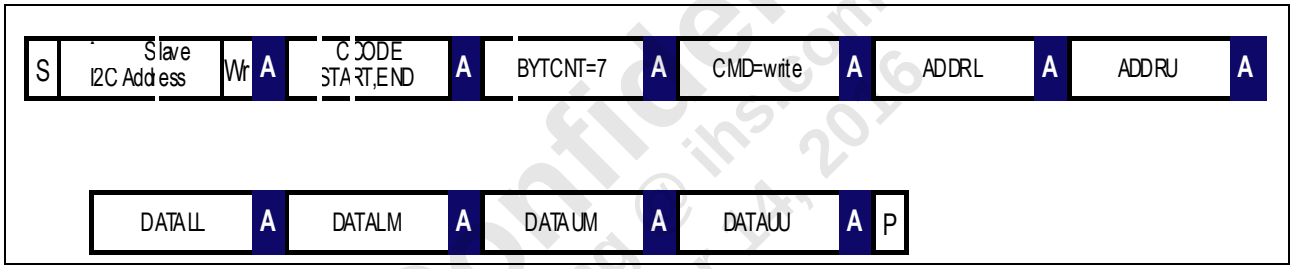


Figure 15 CSR Register Write Using I²C Block Write transactions with PEC Disabled

I²C Master Interface

The P0604Q master interface is used to read and download the contents of EEPROM into the P0604Q configuration registers. The master interface can be used in two modes: standalone mode (single repeater) and shared mode (up to 8 repeaters). The master interface does not support I²C arbitration. As a result, when the P0604Q I²C interface is in master mode, either standalone or shared mode, care needs to be taken to avoid any potential bus contention with other masters on the bus. During the transfer from EEPROM, no other master can be active on the bus. Once the configuration is read and loaded from EEPROM, the P0604Q master automatically enters slave mode. If there are other masters, they can then take control of the bus if needed.

Figure 16 shows a standalone application of a single P0604Q with a dedicated EEPROM. In this mode, the P0604Q acts as a master and can be set to any address via I2CA[2:0] pins.

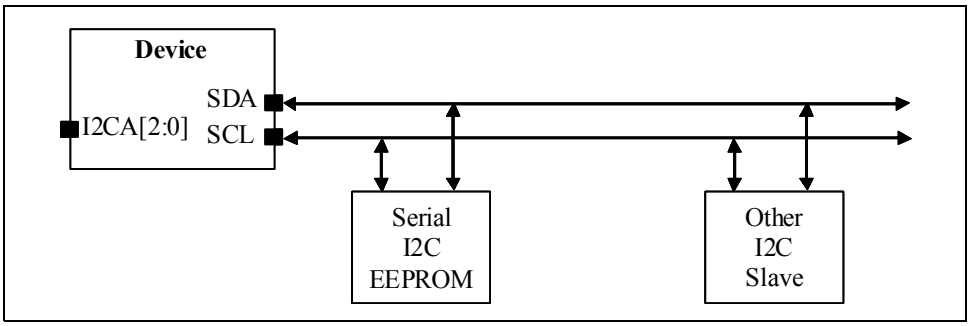


Figure 16 Single P0604Q Implementation

Figure 17 shows an example of a shared mode implementation where multiple P0604Qs are connected on the I^2C bus. This allows a single EEPROM to be shared across all P0604Qs in the system. In this configuration, P0604Q(0) = I2CA[2:0] = 0 is the only master on the bus. There must be a P0604Q(0) in shared mode, otherwise download behavior is undefined. P0604Q(0) is responsible for reading all initialization data for all devices from the external EEPROM. As the master P0604Q device reads the configuration data from EEPROM, the other P0604Qs connected to the bus will only listen to the initialization data and extract and apply register configuration data relevant to them. Each slave device can recognize its portion of configuration data stored in EEPROM, because EEPROM mapping is based on a slave address as shown in Figure 18.

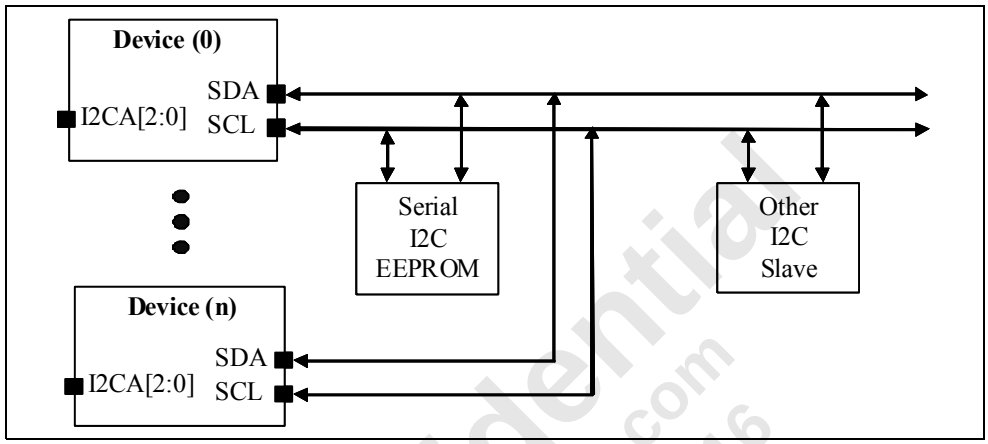


Figure 17 Multiple P0604Qs Implementation

Serial EEPROM Access

At power-up, if EEPROM is present on the I^2C bus, it is used to initialize P0604Q configuration registers in the device. The address used by the I^2C interface is set to default 1010b for the upper four bits. The address used by the I^2C interface to access the serial EEPROM is specified by the I2CA[2:0] signals as shown in Table 24.

Address Bit	Address Bit Value
1	I2CA0
2	I2CA1
3	I2CA2
4	0
5	1
6	0
7	1

Table 24 Serial EEPROM I2C Address

Creating and Saving EEPROM Device Configuration

There are two ways to create/save the desired configuration content into EEPROM:

- Create the EEPROM content manually by following the guidelines in the EEPROM Content Format section of this document .
- Create a working copy of the desired register settings in a live system and save these settings into the EEPROM by using the Device Management (GUI) software provided by IDT.

Serial EEPROM Compatibility

Any serial EEPROM equivalent to those listed in Table 25 may be used to store initialization values.

Serial EEPROM	Size
24C32	4 KB
24C64	8 KB
24C128	16 KB
24C256	32 KB
24C512	64 KB

Table 25 P0604Q Compatible Serial EEPROMs

Initialization from Serial EEPROM

At power-up, the P0604Q master waits 5ms (max) after de-assertion of the internally-generated power on reset to make sure all P0604Qs on the bus come out of reset before starting to read EEPROM data. When the P0604Q slave devices come out of reset, they immediately start listening to the bus and internally write the configuration data into their configuration registers as it becomes available on the bus during master-controlled EEPROM reading (download).

If there is only one P0604Q on the bus (standalone mode) with I2CA[2:0] address different from zero, it will wait up to a maximum of 10ms after de-assertion of the internally-generated power on reset at power-up before starting to act as the master and read EEPROM data.

EEPROM Content Format

The P0604Q master begins reading bytes starting at serial EEPROM address zero. The content of bytes starting from EEPROM address 0 must define the value in the P0604Q EEPROM Control Register settings (register offset = 16h, SIZE and VECTOR fields, see Table 17 for details). The P0604Q EEPROM Control Register is used to set up the EEPROM start addresses for each P0604Q and to define which P0604Q I^2C addresses are present via SIZE and VECTOR. Refer to Figure 18. The EEPROM Control Register can only be set up in EEPROM via single double-word format described later in this section. The user has an option to store any number of P0604Q configuration register values in EEPROM. The registers, whose configurations are not stored in the EEPROM, will be initialized to their default values as shown in the I^2C Registers section.

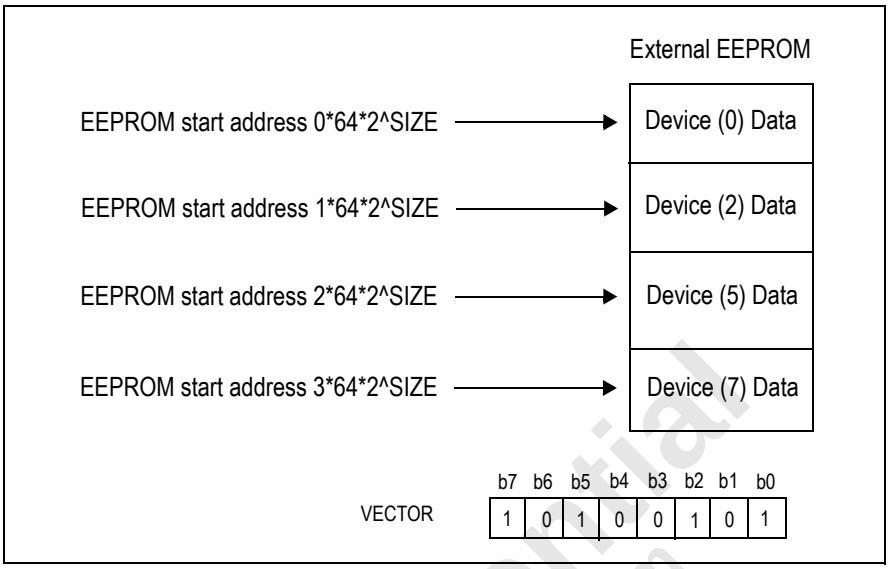


Figure 18 EEPROM Start Address

The P0604Q contains 4 channels and each EEPROM-initialized configuration register needs to be defined in EEPROM. Refer to Figure 18 showing the mapping of 4 channels in EEPROM space.

There are three allowable configuration formats that can be stored in the serial EEPROM. These 3 formats are recognizable by P0604Q devices during the download process. Allowable formats are:

- Single double-word format: used to store one P0604Q configuration register (32 bits of configuration + header).
- Sequential double-word format: used to store multiple P0604Q configuration registers (n*32 bits of configuration + header). This format can be used in combination with the single double-word format.
- Configuration-done format: must be placed right after configuration space used by the formats described above. If there are multiple P0604Q devices, the configuration-done format also needs to be placed multiple times, once for every block shown in the example in Figure 18.

The first format type, a single double-word initialization sequence, occupies seven bytes in the serial EEPROM. A single double-word format consists of three fields and is shown in Table 26. The TYPE field indicates the type of the configuration format. For a single double-word format, this value is 00 by definition. The SYSADDR field is the address offset of a P0604Q configuration register as defined in the I^2C Registers section. The final DATA field contains the value that defines the P0604Q configuration register with address offset SYSADDR.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0	TYPE 00		Reserved (must be zero)					
Byte 1	SYSADDR[7:0]							
Byte 2	SYSADDR[15:8]							
Byte 3	DATA[7:0]							
Byte 4	DATA[15:8]							
Byte 5	DATA[23:16]							
Byte 6	DATA[31:24]							

Table 26 Single Double-word Initialization Sequence Format

The second type of configuration format is the sequential double-word format. It consists of a header (TYPE, SYSADDR, NUMDW) and one to 65535 double-word initialization data fields. The format of a sequential double-word format is shown in Table 27.

The TYPE field indicates the type of the configuration block. For a sequential double-word initialization format, this value is always 01 by definition. The SYSADDR field contains the starting address offset of a P0604Q configuration register. The NUMDW field specifies the number of P0604Q configuration registers to be sequentially stored. This is followed by the number of DATA fields specified in the NUMDW field. The DATA fields define the content of the P0604Q configuration registers starting from address offset SYSADDR.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0	TYPE 01		Reserved (must be zero)					
Byte 1	SYSADDR[7:0]							
Byte 2	SYSADDR[15:8]							
Byte 3	NUMDW[7:0]							
Byte 4	NUMDW[15:8]							
Byte 5	DATA[7:0]							
Byte 6	DATA[15:8]							
Byte 5	DATA[23:16]							
Byte 6	DATA[31:24]							
	▪ ▪ ▪ ▪ ▪ ▪							
Byte 4n+ 5	DATAn[7:0]							
Byte 4n+ 6	DATAn[15:8]							
Byte 4n+7	DATAn[23:16]							
Byte 4n+ 8	DATAn[31:24]							

Table 27 Sequential Double-word Initialization Sequence Format

The third type of configuration format is the configuration-done sequence which consists of two fields as shown in Table 28. The TYPE field is 11 by definition for the configuration-done format. The CHECKSUM field is done per every P0604Q device present (checksum for each P0604Q in the system). This field contains the 1's complement of the sum of all the bytes in all of the fields stored in the serial EEPROM for the corresponding P0604Q device present in the system. The counting starts from the first configuration byte to the last byte of the configuration-done format. All bytes from all 3 types of configuration formats need to be counted.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0	TYPE 11		Reserved (must be zero)					
Byte 1	CHECKSUM[7:0]							

Table 28 Configuration-Done Sequence Format

The checksum in the configuration-done sequence enables the integrity of the serial EEPROM initialization to be verified. The checksum is verified in the following manner. An 8-bit counter is cleared and the 8-bit sum is computed over the bytes read from the serial EEPROM during the initialization process, including the entire contents of the configuration-done sequence. The correct result should always be FF (i.e., all ones). Checksum checking may be disabled by setting the Ignore Checksum Errors (ICHECKSUM) bit in the I^2C Control (I2CCTL) register.

Troubleshooting EEPROM Download Issues

The P0604Q has a built-in I^2C Status Register (address offset = 14h) that stores flags if certain error events occur during configuration downloads from EEEPROM. By reading this register, a user can verify which errors, if any, occurred during the reading from EEPROM. If an error is detected during loading of the serial EEPROM, then loading of the serial EEPROM is aborted. Once serial EEPROM initialization completes, is aborted, or when an error is detected, the EEPROM Done (EEPROMDONE) bit is set in the I^2C Status (I2CSTS) register. Table 29 summarizes possible error types and the associated flag bits.

Error	Action Taken
Configuration-Done Sequence checksum mismatch with that computed	- CSERR bit is set in the I2CSTS register - Abort initialization, set EEPROMDONE bit in the I2CSTS register
Invalid configuration block type (only invalid type is 0x2)	- CSERR bit is set in the I2CSTS register - Abort initialization, set EEPROMDONE bit in the I2CSTS register
An unexpected NACK is observed during a master I^2C transaction	- NAERR bit is set in the I2CSTS register - Abort initialization, set EEPROMDONE bit in the I2CSTS register
A misplaced START or STOP condition is detected by the master I^2C interface	- OTHERERR bit is set in the I2CSTS register - Abort initialization, set EEPROMDONE bit in the I2CSTS register
Serial EEPROM address rollover error detected	- ROLLOVER bit is set in the I2CSTS register - Abort initialization, set EEPROMDONE bit in the I2CSTS register
Blank serial EEPROM detected	- BLANK bit is set in the I2CSTS register - Abort initialization, set EEPROMDONE bit in the I2CSTS register
Checksum error detected	- CSERR bit is set in the I2CSTS register - Abort initialization, set EEPROMDONE bit in the I2CSTS register
Unmapped register initialization attempt	- URIA bit is set in the I2CSTS register - Abort initialization, set EEPROMDONE bit in the I2CSTS register

Table 29 Serial EEPROM Initialization Errors

Rollover Flag Details

During serial EEPROM initialization, the master I^2C interface begins reading bytes starting at serial EEPROM address zero. These bytes are interpreted as configuration blocks and sequential reading of the serial EEPROM continues until the end of a configuration-done block is reached or the serial EEPROM address rolls over from 0xFFFF to 0x0 due to insufficient EEPROM memory. When a serial EERPROM address roll over is detected, loading of the serial EEPROM is aborted and the Serial EEPROM Rollover (ROLLOVER) bit is set in the I2C Status (I2CSTS) register.

Blank Flag Details

A blank serial EEPROM contains 0xFF in all data bytes. When the P0604Q is configured to initialize from serial EEPROM and the first 256 bytes read from the EEPROM all contain the value 0xFF, then loading of the serial EEPROM is aborted, the computed checksum is ignored, the Blank Serial EEPROM (BLANK) bit is set in the I^2C Status Register (I2CSTS), and normal device operation begins (i.e., the device operates in the same manner as though it were not configured to initialize from the serial EEPROM). This behavior allows a board manufacturing flow that utilizes uninitialized serial EEPROMs.

Unmapped Register Initialization Attempt Flag Details

All register initialization performed by the serial EEPROM is done in DWord (32-bit) quantities. Byte values may be modified by writing the entire DWord. If during serial EEPROM initialization an attempt is made to initialize a register that is not defined in a configuration space, then the Unmapped Register Initialization Attempt (URIA) bit is set in the I2CSTS register and the write is ignored. This bit is only set in the device when the start address is such that it would write this block into its register space.

Electrical Specifications

Absolute Maximum Ratings

Note: All voltage values, except differential voltages, are measured with respect to ground pins.

Parameter	Value	Unit
Supply voltage range VDD	–0.5 to 1.35	V
Supply voltage range VDD3	–0.5 to 4.0	V
Voltage range Differential I/O	–0.5 to VDD +0.5	V
Control I/O	–0.5 to VDD + 0.5	V
ESD requirements: Electrostatic discharge Human body model	±2000	V
ESD requirements: Charged-Device Model (CDM)	±500	V
ESD requirements: Machine model	±125	V
Storage ambient temperature	-55 to 150	°C

Table 30 Absolute Maximum Ratings

Warning: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Notes	Min	Typical	Max	Unit
Power Supply Pin Requirements					
VDD	1.2V DC analog supply voltage (specified at bump pins)	1.14	1.2	1.26	V
VDD3	3.3V DC supply voltage for I^2C interface	3.0	3.3	3.6	V

Table 31 P0604Q Operating Conditions (Part 1 of 2)

Parameter	Notes	Min	Typical	Max	Unit
Temperature Requirements					
TA	Ambient operating temperature - Commercial	0	—	70	°C
	Ambient operating temperature - Industrial	-40	—	85	°C
TJUNCTION	Junction operating temperature	-40	—	125	°C

Table 31 P0604Q Operating Conditions (Part 2 of 2)

Power Consumption

Table 32 below lists power consumption values under typical and maximum operating conditions.

Parameter	Notes	Min	Typical	Max	Unit
Active Mode					
I_{VDD}	Current into VDD supply	—	330	500	mA
I_{VDD3}	Current into VDD3 supply		80	150	µA
P_D	Full chip power[1]		400	600	mW
P_{D-ch}	Power per channel[1]		100	150	mW
Standby Mode	Full chip standby		30	40	mW

Table 32 P0604Q Power Consumption

1. Maximum power under all conditions. Power is reduced by selecting smaller de-emphasis settings (closer or equal to 0dB).

Package Thermal Considerations

The data in Table 33 below contains information that is relevant to the thermal performance of the 36-pin QFN package.

Parameter	Description	Value	Conditions	Units
$T_{J(max)}$	Junction Temperature	125	Maximum	°C
$T_{A(max)}$	Ambient Temperature	70	Maximum for commercial-rated products	°C
		85	Maximum for industrial-rated products	°C
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	41.8	Zero air flow	°C/W
		36.1	1 m/S air flow	°C/W
		35.3	2 m/S air flow	°C/W
		34.3	3 m/S air flow	°C/W
		33.7	4 m/S air flow	°C/W
		33.2	5 m/S air flow	°C/W
θ_{JB}	Thermal Resistance, Junction-to-Board	14.5	NA	°C/W
θ_{JC}	Thermal Resistance, Junction-to-Case	37.2	NA	°C/W

Table 33 Thermal Specifications for P0604Q, 4.0x7.5mm 36-QFN Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 33. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 33), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board).

DC Specifications

Parameter	Description	Min	Typical	Max	Unit
1.2V, 2-Level Input and Output Pin Requirements					
V_{IL}	Digital Input Signal Voltage Low Level[1]	- 0.3		0.6	V
V_{IH}	Digital Input Signal Voltage High Level[1]	1.1		VDD + 0.3	V
V_{OL}	Digital Output Signal Voltage Low Level, I_{OL}=3mA[2]			0.4	V
V_{OH}	Digital Output Signal Voltage High Level, I_{OH}=3mA[2]	VDD - 0.4			V
V_{HYS}	Hysteresis of Schmitt Trigger Input	0.1			V
I_{IL}	Input current with internal pull-up resistor[3]			100	µA
I_{IH}	Input current with internal pull-down resistor[4,5]			100	µA
$R_{WEAK\_PD\_2L}$	Internal weak pull-down resistor at 2-level input pads[4,5.]	11			K ohm
$R_{WEAK\_PU\_2L}$	Internal weak pull-up resistor at 2-level input pads[3]	11			K ohm
3.3V Pin Requirements					
V_{IL_VDD3}	Digital Input Signal Voltage Low Level[6]	-0.3		0.8	V
V_{IH_VDD3}	Digital Input Signal Voltage High Level[6]	2.1		VDD3 + 0.3	V
$V_{OL\_VDD3\_HP}$	Digital Output Signal Voltage Low Level, High Power, IOL=4mA[7,8]			0.4	V
$V_{OL\_VDD3\_LP}$	Digital Output Signal Voltage Low Level, Low Power, IOL=350uA[7,8]			0.4	V
1.2V, 3-Level Input Pin Requirements					
V_{IL}	Digital Input Signal Voltage Low Level	-0.3		0.25*VDD-0.1	V
V_{IM}	Digital Input Signal Voltage Mid Level	0.25*VDD+0.1		0.75*VDD-0.1	V
V_{IH}	Digital Input Signal Voltage High Level	0.75*VDD+0.1		VDD+0.3	V
I_{IL}	Input Current for V_{IL}			180	µA
I_{IH}	Input Current for V_{IH}			180	µA
$R_{WEAK\_PD\_3L}$	Internal weak pull-down resistor at all 3-level input pads	6.3			K ohm
$R_{WEAK\_PU\_3L}$	Internal weak pull-up resistor at all 3-level input pads	6.3			K ohm

Table 34 DC Specification

1. Applies to input pins.
2. Applies to output pins.
3. Applies only to 2-level input pins with default values set to VDD in the Pin Description table (Table 39).
4. Applies only to 2-level input pins with default values set to VSS in the Pin Description table (Table 39).
5. Applies to I2CA pins in the Pin Description table (Table 39).
6. Applies to I2C interface pins.
7. VOL low power and high power state is controlled via an external pull-up design in the end-application.
8. Applies to SDA and SCL pins.

AC Specifications

Receiver Specifications

Parameter	Description	Min	Typical	Max	Unit
Receiver Input Jitter Specifications					
T_{RX-DDJ}	Receive Input Signal Data Dependent Jitter (Inter-Symbol Interference).	—	—	>1	UI
T_{RX-TJ}	Receive Input Signal Total Jitter	—	—	>1	UI
T_{RX-EYE}	Receiver eye time opening (can recover from closed eye due to trace attenuation and ISI jitter)	0	—	—	UI
Receiver Input Eye Specification					
$V_{RX-DIFF}$	Receiver Differential Peak-Peak Voltage[1]	0	—	2000	mV
$V_{RX-CM-DC}$	Receiver DC Common Mode Voltage	—	0	—	mV
V_{RX_IN}	Absolute Input Voltage (measured at device pins)	-0.1	—	VDD + 0.1	V
$V_{RX-CM-AC}$	Receiver AC Common Mode Voltage	—	—	100	mVp-p
$T_{skew-RX}$	RX Differential Skew (P-N skew)	—	—	30	ps
Receiver Return Loss					
$RL_{DD11,RX}$	RX Differential Mode Return Loss				
	0 MHz - 150 MHz	18	—	—	dB
	150 MHz - 300 MHz	18	—	—	
	300 MHz - 600 MHz	14	—	—	
	600 MHz - 1.2 GHz	12	—	—	
	1.2 GHz - 2.4 GHz	10	—	—	
	2.4 GHz - 3.125 GHz	8	—	—	
$RL_{RX-CM-DC}$	Receiver Common Mode Return Loss (0Hz - 3.125GHz)	8	—	—	dB
$C_{RX-CAPACITANCE}$	Receiver Input Capacitance for Return Loss	—	—	1.1	pF
Receiver DC Impedance					
$Z_{RX-DIFF-DC}$	DC differential impedance	85	—	115	Ohm
Receiver Signal Detection					
$V_{RX-Threshold}$	Signal Detection Threshold	50	110	160	mVppd
$V_{RX-CM-DC-ACTIVELOS-DELTA-P}$	RX AC Common Mode Voltage during the active to loss of signal state transition	—	—	200	mV
$T_{RX-LOS-DET-DIFF-ENTER-TIME}$	Loss of Signal Enter Detect Threshold Integration Time	—	—	10	ms
$T_{LOS-EXIT}$	Loss of Signal Exit Time (Turn-on time)	—	—	15	ns
$T_{LOS-ENTER}$	Loss of Signal Enter Time (Turn-off time)	—	—	15	ns
$T_{LOS-DECAY-MIS}$	Signal Detect Attack / Decay Time Mismatch	—	—	5	ns

Table 35 Receiver Electrical Specifications

1. The minimum value of 0 mV represents the case when Eye is completely closed.

Transmitter Specifications

Parameter	Description	Min	Typical	Max	Unit
Output Eye and Common Voltage Specification					
$V_{TX-DIFF-PP}$	Differential Transmitter swing[1]	800	950	1100	mV
$V_{TX-DIFF-PP-LOW}$	Low power differential p-p Transmitter swing[2]	400		650	mV
$D_{TX-DEEMP}$	Output De-emphasis (programmable). Defined as $20log(V_{TX-DE-EMP} / V_{TX-DIFF})$ [dB][3]	-9.5		0	dB
$T_{RES-DJ-1}$	Residual Deterministic Jitter at output pins (1 inch FR4 trace before receiver input pins)[4]	—	—	<0.05	UI
$T_{RES-DJ-5GBPS-2}$	Residual Deterministic Jitter at output pins (62 inch FR4 trace before receiver input pins, 5Gbps)[4]	—	0.17	0.23	UI
$T_{RES-DJ-6GBPS-3}$	Residual Deterministic Jitter at output pins (62 inch FR4 trace before receiver input pins, 6Gbps)[4]	—	0.2	0.28	UI
$T_{20-80TX}$	TX Rise/Fall Time (20-80%)	33	—	90	ps
T_{skewTX}	TX Differential Skew (P-N skew)	—	—	20	ps
R/F_{bal}	TX Rise/Fall Imbalance	—	—	20	%
AMP_{bal}	TX Amplitude Balance	—	—	10	%
$T_{TX-RISE-FALL}$	Rise/Fall Time (programmable)	0.125	—	—	UI
$T_{RF-MISMATCH}$	Tx rise/fall mismatch	—	—	0.1	UI
$V_{TX-CM-AC-PP}$	Pk-Pk AC Common Mode Voltage Variation	—	—	50	mV
$V_{TX-CM-AC-P}$	Tx AC common mode voltage	—	—	20	mV
$V_{TX-CM-RMS-AC}$	RMS AC Common Mode Voltage Variation	—	—	20	mV
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	0	—	VDD	V
$V_{TX-CM-DC-LINEDELTA}$	Absolute Delta of DC Common Mode Voltage between P and N	0	—	25	mV
Latency	Input to output signal propagation device	—	300	—	ps
$T_{TX-SKEW-LL}$	Lane-to-Lane Output Skew	—	5	10	ps
C_{TX}	AC Coupling Capacitor	12	—	200	nF
Transmitter DC Impedance					
$Z_{TX-DIFF-DC}$	Transmitter Output Differential DC Impedance[5]	85	100	115	Ohm
$I_{TX-SHORT}$	Transmitter short-circuit current limit	—	—	60	mA
Transmitter Return Loss					
$RL_{TX-DIFF-F1}$	Transmitter Differential Return Loss (0 - 1.25GHz)	10	—	—	dB
$RL_{TX-DIFF-F2}$	Transmitter Differential Return Loss (1.25 - 3.125GHz)	8	—	—	dB
RL_{TX-CM}	TX Common Mode Return Loss				
	0 MHz - 300 MHz	8	—	—	dB
	300 MHz - 3.125 GHz	6	—	—	
$C_{TX-CAPACITANCE}$	Transmitter Input Capacitance for Return Loss	—	—	1.25	pF

Table 36 Transmitter Electrical Requirements (Part 1 of 2)

Parameter	Description	Min	Typical	Max	Unit
Loss of Signal					
V_{TX-LOS}	Output Voltage when signal is lost (squelch)	—	—	20	mV
$V_{CM-DELTA-LOS}$	Maximum Common-Mode Step Entering/Exiting Loss of Signal State (squelched)	—	—	50	mV
$V_{TX-CM-DC-ACTIVE-LOS-DELTA}$	Absolute Delta of DC Common Mode Voltage between Active Mode and Loss of Signal State	0	—	100	mV
$V_{TX-LOS-DIFF-AC-p}$	Differential Peak Output Voltage in Loss of Signal State	0	—	10	mV
$V_{TX-LOS-DIFF-DC}$	DC Differential Output Voltage in Loss of Signal State	0	—	5	mV

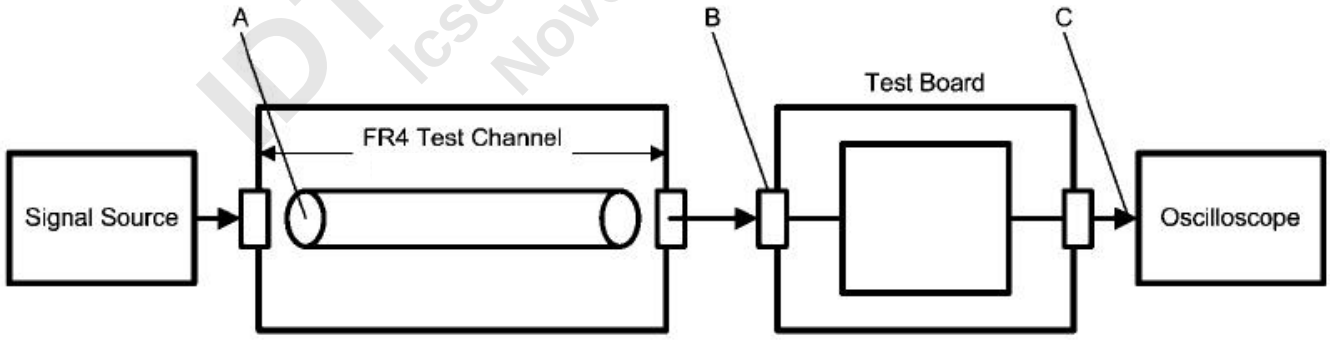
Table 36 Transmitter Electrical Requirements (Part 2 of 2)

1. When the TX_SWING register is set to 0.95V.
2. When the TX_SWING register is set to 0.5V. Other settings are also available.
3. Programmable via the TX_DEEMP register.
4. Refer to Figure 19.
5. When TERM_CTL bit is set to 100Ω.

Repeater Additive Jitter

Parameter	Description	Min	Typical	Max	Unit
D_J	Repeater Data Dependent Jitter			<0.05	UI
R_J	Random Jitter			1	psrms

Table 37 P0604Q Repeater Additive Jitter



A — FR4 Trace **B — SMA Connector** **C — Measurement Point**

Note: FR4 test channel is bypassed for 1-inch input trace case.

Figure 19 Residual Jitter Characterization Test Setup

I²C Specifications

Parameter	Description	Min	Typ	Max	Unit
f_{SCL}	Clock frequency	10		400	kHz
t_{HIGH}	Clock pulse width high time	600			ns
t_{LOW}	Clock pulse width low time	1300			ns
$t_{TIMEOUT(L)}$	Detect clock low timeout	24		40	ms
$t_{TIMEOUT(H)}$	Detect clock high timeout	40		66	us
t_R	SDA rise time	20		300	ns
t_F	SDA fall time	20		300	ns
$t_{SU:DAT}$	Data in setup time	100			ns
$t_{HD:DI}$	Data in hold time	0			ns
$t_{HD:DAT}$	Data out hold time	200		900	ns
$t_{SU:STA}$	Start condition setup time	600			ns
$t_{HD:STA}$	Start condition hold time	600			ns
$t_{SU:STO}$	Stop condition setup time	600			ns
t_{BUF}	Time between Stop Condition and next Start Condition	1300			ns
t_{GLITCH_FILTER}	SDA and SCL glitch removal time	80		130	ns

Table 38 I²C AC Timing Specifications

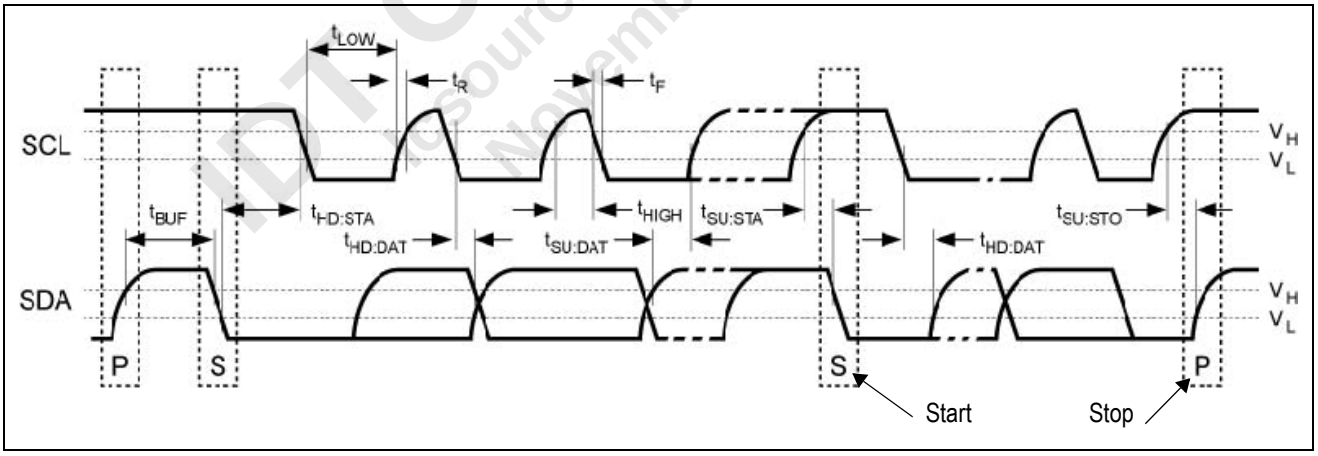


Figure 20 I²C AC Waveforms

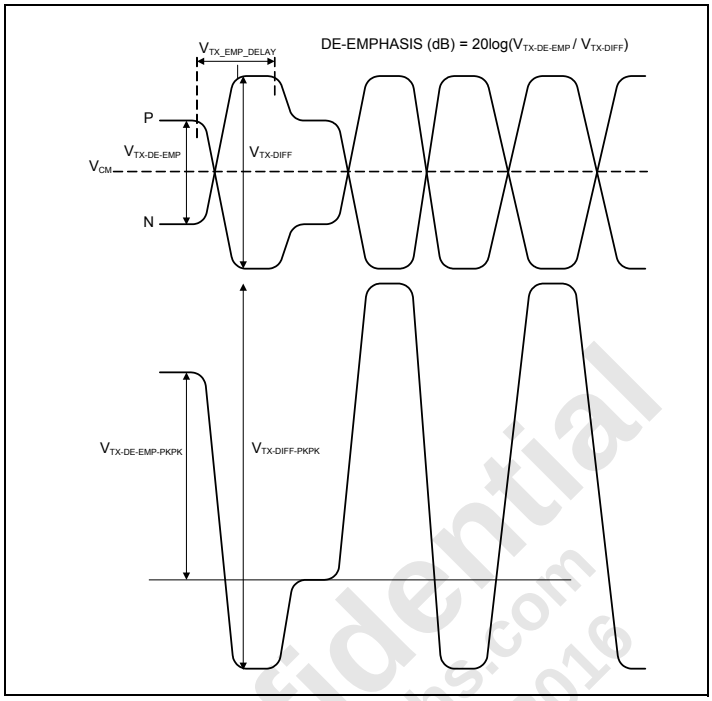


Figure 21 Transmitter Swing Levels With and Without De-emphasis

Note: $V_{TX\text{-}DIFF\text{-}PKPK}$ Peak to Peak voltage is twice as large as voltage difference between P pins and N pins of differential pairs. For example, if the P pin swings from 0.8V to 1.4V while the N pin swings from 1.4V to 0.8V, then:$V_{TX\text{-}DIFF\text{-}PKPK}$ = 2*(1.4-0.8)=1.2V.

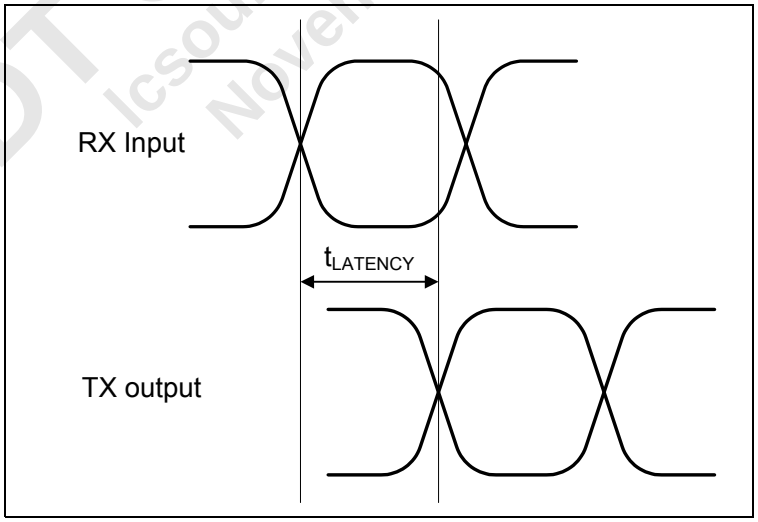


Figure 22 Definition of Latency Timing

Pin Description

Note: Unused pins can be left floating except when a Note in this table specifies otherwise (see VDD3, SCL, and SDA below).

Pin Name	Pin #	Description	Input/ Output/ Power 2 or 3 Level
Power			
VDD	3, 6, 9, 18, 22, 25, 28	1.2V (typ) Power supply for Repeater high speed channels and internal logic. Each VDD pin should be connected to the VDD plane through a low inductance path, with a via located as close as possible to the landing pad of VDD pins. It is recommended to have a 0.01 µF or 0.1 µF, X7R, size-0402 bypass capacitor from each VDD pin to ground plane.	Power
VDD3	13	3.3V (typ) Power supply for Repeater I^2C interface signals It is recommended to have a 0.01 µF or 0.1 µF, X7R, size-0402 bypass capacitor from this pin to ground plane. Note: If not used, tie to VDD.	Power
VSS	Center Pad	VSS reference. Each VSS pin should be connected to the ground plane through a low inductance path, with a via located as close as possible to the landing pad of the VSS pin.	Power
Data Signals			
A0RXN A0RXP	2 1	Channel A0 Receive Data Ports	Input
A0TXN A0TXP	29 30	Channel A0 Transmit Data Ports	Output
B0RXN B0RXP	26 27	Channel B0 Receive Data Ports	Input
B0TXN B0TXP	5 4	Channel B0 Transmit Data Ports	Output
A1RXN A1RXP	8 7	Channel A1 Receive Data Ports	Input
A1TXN A1TXP	23 24	Channel A1 Transmit Data Ports	Output
B1RXN B1RXP	20 21	Channel B1 Receive Data Ports	Input
B1TXN B1TXP	11 10	Channel B1 Transmit Data Ports	Output
Other Control Signals			
I2CA[0] I2CA[1] I2CA[2]	16 15 33	I^2C Address Identifier Pins. Must be shorted on the board to a distinct, unique address. Default Tied Off Value in the IO = VSS via internal 11K ohm minimum weak pull-down. Note: Use 1.2V VDD supply to set these pins to 1.	Input - 2 level

Table 39 Pin Description (Part 1 of 2)

Pin Name	Pin #	Description	Input/ Output/ Power 2 or 3 Level
INTMODE	34	Interface Control Mode. 3 Level Input Pin. INTMODE Setting VSS I^2C slave mode with register programming Open Pin programming is enabled (Default) VDD I^2C master mode	Input - 3 level
PDB	36	Power-down Enable. PDB Setting VSS Powerdown IC. RX terminations are in Hi-Z, TX is disabled. Recommended resistance to ground with value between 0 ohms and 1k ohm. VDD Normal operation (internal 11K ohm minimum pull-up applied). No external termination is required.	Input - 2 level
RSTB	35	Receiver Detection Start. RSTB Setting VSS Resets Channel Receiver Detection State Machine VDD Normal operation (internal 11K ohm minimum pull-up applied) Note: the rising edge of RSTB will start the receiver detection.	Input - 2 level
ARXDETEN BRXDETEN	17 32	Output Channel Receiver Detect Enable Input. Programming of channel ARXDETEN via pins is shown below. To program BRXDETEN, use pins for that channel. ARXDETEN Setting VSS Receiver Detection is disabled for A0 and A1 channels (internal 11K ohm minimum pull-down applied) VDD Receiver Detection is enabled for A0 and A1 channels	Input - 2 level
CHSEL	31	Channel Transfer Mode. CHSEL Setting VSS Multi-cast mode Open Direct-connect mode (default) VDD Cross-connect mode	Input - 3 level
SCL	14	I^2C Clock Pin. Note: If not used, tie to ground.	I/O
SDA	12	I^2C Data Pin. Note: If not used, tie to ground.	I/O
RSVD	19	Reserved. Do not connect.	

Table 39 Pin Description (Part 2 of 2)

36-QFN Pinout

Table 40 lists the pin numbers and signal names for the P0604Q QFN device.

Function	Pin	Function	Pin	Function	Pin
A0RXN	2	B0TXP	4	RSTB	35
A0RXP	1	B1RXN	20	RSVD	19
A0TXN	29	B1RXP	21	SCL	14
A0TXP	30	B1TXN	11	SDA	12
A1RXN	8	B1TXP	10	VDD	3
A1RXP	7	BRXDETEN	32	VDD	6
A1TXN	23	CHSEL	31	VDD	9
A1TXP	24	INTMODE	34	VDD	18
ARXDETEN	17	I2CA0	16	VDD	22
B0RXN	26	I2CA1	15	VDD	25
B0RXP	27	I2CA2	33	VDD	28
B0TXN	5	PDB	36	VDD3	13

Table 40 P0604Q Alphabetical Pin List

QFN Pin Diagram

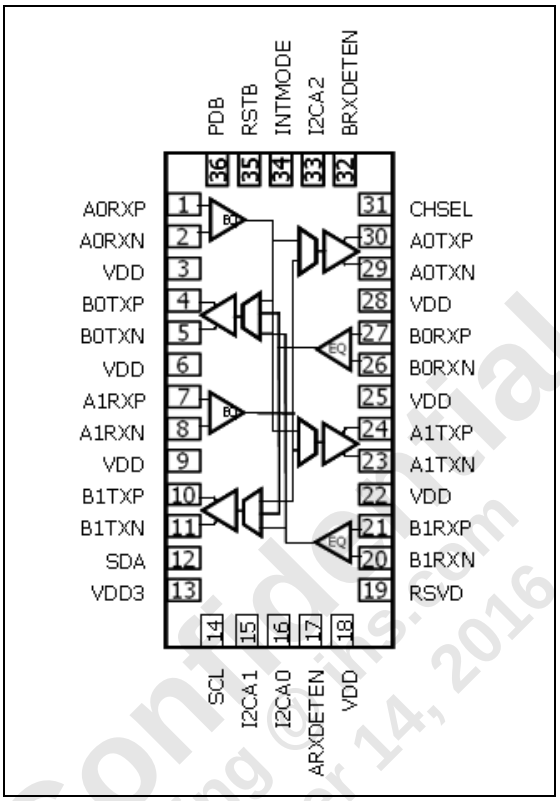
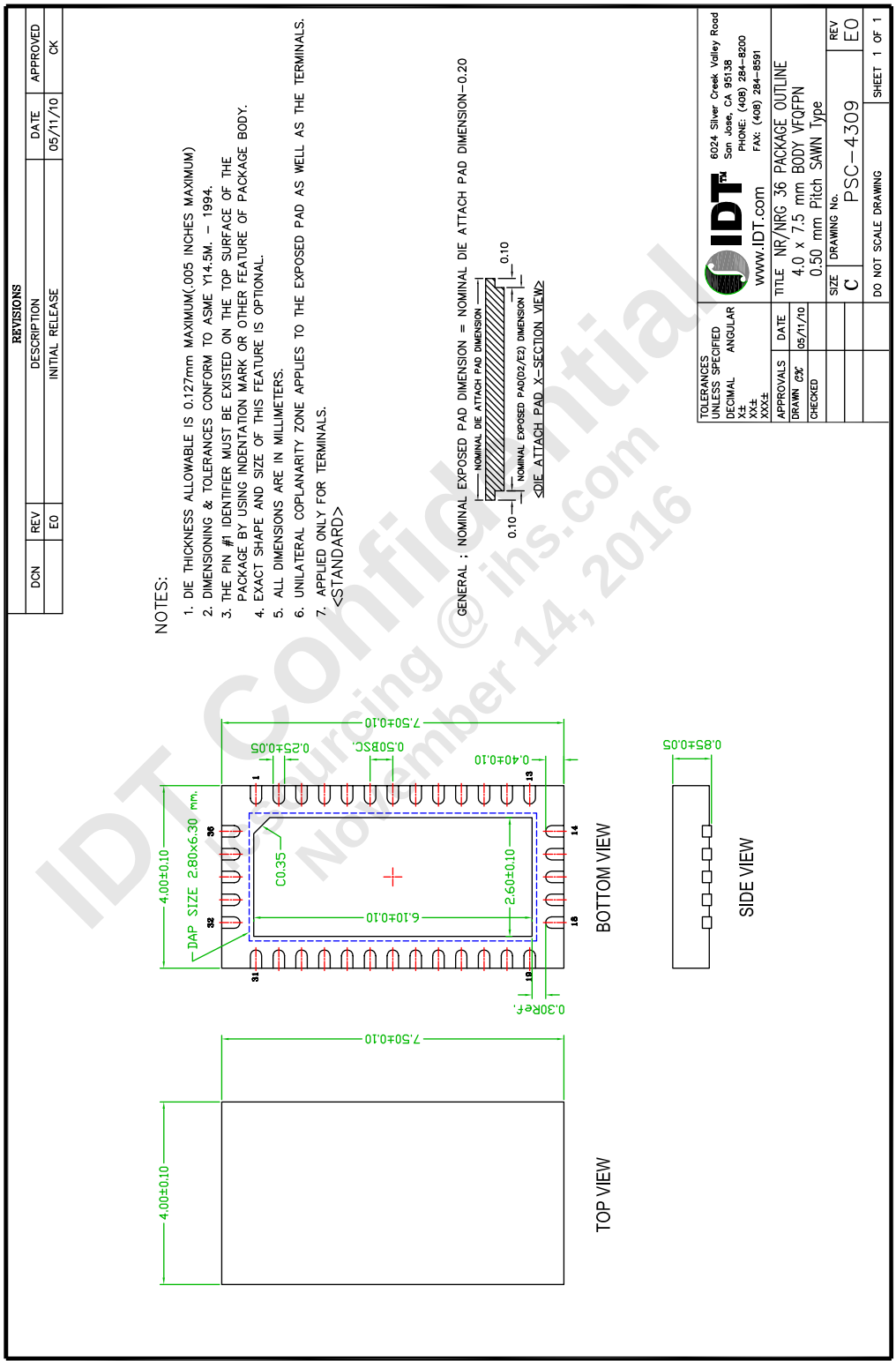


Figure 23 P0604Q QFN Pin Diagram — Top View

Note: Data positive (P) and negative (N) pins may be switched without any protocol impact provided channel polarity from host to target is maintained. Example: pins A0RXN (2) and A0RXP (1) may be switched provided that pins A0TXN (29) and A0TXP (30) are also switched; pins B1RXN (20) and B1RXP (21) may be switched provided that pins B1TXN (11) and B1TXP (10) are also switched.

QFN Package Dimension



Revision History

October 25, 2010: Initial publication of final datasheet.

November 2, 2010: Added minimum speed of 1.125Gbps and added new protocol CPRI.

November 22, 2010: Deleted incorrect reference to PCIe.

January 24, 2011: Changed Power Sequencing section to Power-Up/Power-Down Sequencing and revised text.

February 10, 2011: Revised footnote in Table 13. Removed black packaging options from Order page.

April 8, 2011: In Table 14, Global Control Register, changed bit 24 to Reserved, RW, 0x1 default value.

May 25, 2011: Added Note regarding data pin swaps under Figure 23.

August 18, 2011: In Tables 13 and 14, added "Usage details" to a number of Fields. Added new Table 37, Repeater Additive Jitter. In Table 39, Pin Description, added information to Description for PDB.

September 28, 2011: In EEPROM Control Register (Table 17), changed bit 7 in VECTOR field from 011 to 111.

November 9, 2011: In Power-Up section, clarified that output pins indicate signal detection at high speed input.

December 16, 2011: In Table 13, revised Description for TX_EMP_DELAY field.

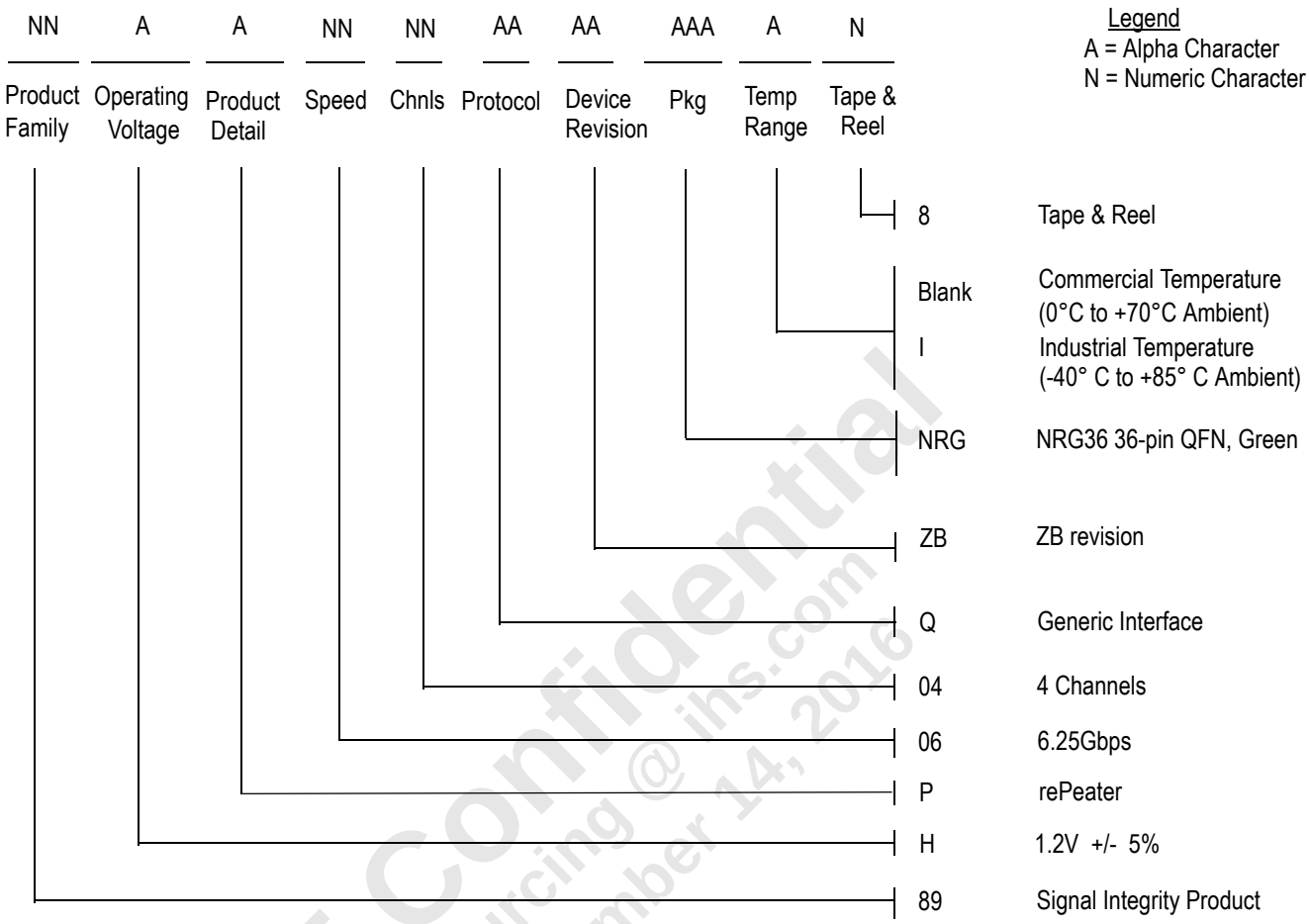
February 14, 2012: In Power-Up/Power-Down Sequencing section, revised ramp-up time description for VDD.

February 28, 2012: Added sections Data Units and Register Terminology.

April 6, 2012: In Table 36, made slight changes to parameters $D_{TX\text{-}DEEMP}$ and $T_{TX\text{-}RISE\text{-}FALL}$.

July 30, 2013: In Table 31, changed min temperature for TJUNCTION from 0 to -40.

Ordering Information



Legend
A = Alpha Character
N = Numeric Character

Valid Combinations

89HP0604QZBNRG / 89HP0604QZBNRG8	36-pin Green QFN package, Commercial Temperature
89HP0604QZBNRGI / 89HP0604QZBNRGI8	36-pin Green QFN package, Industrial Temperature

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