

### **DATASHEET**

## **General Description**

The XLL is an LVDS Crystal Oscillator with 0.89ps typical phase jitter over 12kHz to 20 MHz bandwidth. Available in a wide frequency range from 0.750MHz to 1350MHz, the IDT XLL Series Crystal Oscillator utilizes a family of proprietary ASICs, with a key focus on noise reduction technologies.

The 3rd order Delta Sigma Modulator reduces noise to the levels that are comparable to traditional Bulk Quartz and SAW oscillators. With short lead-time, low cost, low noise, wide frequency range, excellent ambient performance, the XLL is an excellent choice over the conventional technologies. The XLL has stabilities as tight as ±20ppm with extremely quick delivery for both standard and custom frequencies

#### **Features**

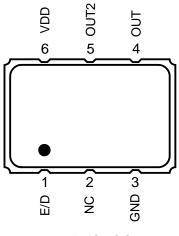
- Frequency range: 0.750MHz to 1350MHz
- Output Type: LVDS
- Frequency Stability: ± 20ppm, ± 25ppm, ± 50ppm, or ± 100 ppm
- Supply Voltage: 2.5V or 3.3V
- Phase Jitter (1.875MHz to 20MHz): 225fs typical
- Phase Jitter (12kHz to 20MHz): 0.89ps typical
- Package options: 3.2mm x 2.5mm x 1.0mm (JX6)

5.0mm x 3.2mm x 1.2mm (JS6)

7.0mm x 5.0mm x 1.3mm (JU6)

Operating Temperatures: -20°C to +70°C or -40°C to +85°C

### **Pin Assignment**



6-pin CLCC

1

# **Pin Descriptions**

Pin Number	Pin Name	Description
1	E/D	Enable/Disable <sup>1</sup> (0=Output Disabled)
2	NC	No connect
3	GND	Connect to ground
4	OUT	Output
5	OUT2	Complementary Output
6	VDD	Supply voltage

<sup>1.</sup> Pulled high internally.



### **Absolute Maximum Ratings**

Stresses above the ratings listed below can cause permanent damage to the XLL. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
VDD	-0.5 to +5.0 V
E/D	-0.5 V to VDD + 0.5 V
OUT	-0.5 V to VDD + 0.5 V
Storage Temperature	-55°C to 125°C
Theta Ja (Junction to Ambient)	102°C/W – Still Air

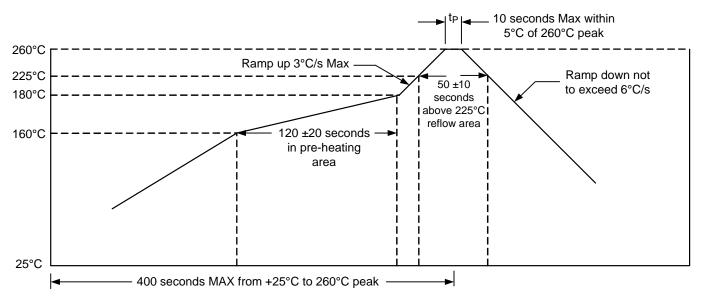
### **ESD Compliance**

Human Body Model (HBM	1000V
Machine Model (MM)	150V

### **Mechanical Testing**

Parameter	Test Method
Mechanical Shock	Drop from 75cm to hardwood surface–3 times
Mechanical Vibration	10~55Hz, 1.5mm amplitude, 1 minute sweep 2 hours each in 3 directions (X, Y, Z)
High Temperature Burn-in	Under power @ 125°C for 2000 hours
Hermetic Seal	He pressure: 4 ±1kgf/cm <sup>2</sup> 2 hour soak

### **Solder Reflow Profile**





### **DC Characteristics**

 $(V_{DD}= 3.3 V \pm 5\%, T_A= -20^{\circ}C \text{ to } +70^{\circ}C; -40^{\circ} \text{ to } +85^{\circ}C)$ 

Parameter	Symbol	Condition	Min	Тур	Max	Units
Power Supply Current	I <sub>DD</sub>	Common Frequencies			100	mA
Differential Output Voltage	V <sub>OD</sub>	Standard LVDS load		0.6		V
Output Offset Voltage	Vos	Standard LVDS load		1.3		V
Enable/Disable Input HIGH Voltage (Output enabled)*	V <sub>IH</sub>		70%V <sub>DD</sub>			V
Enable/Disable Input LOW Voltage (Output disabled)	V <sub>IL</sub>				30%V <sub>DD</sub>	V

<sup>\*</sup> A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

### **AC Characteristics**

 $(V_{DD}= 3.3 V \pm 5\%, T_A= -20^{\circ}C \text{ to } +70^{\circ}C; -40^{\circ} \text{ to } +85^{\circ}C)$ 

Parameter	Symbol	Condition	Min	Тур	Max	Units
Output Frequency Range	F <sub>OUTR</sub>		0.750		1350	MHz
Frequency Stability		Temperature = -20°C to +70°C	±20		±100	ppm
		Temperature = -40°C to +85°C	±25		±100	ppm
Aging (1 <sup>st</sup> year)		Ta = 25°C			3	
Aging (10 years)		Ta = 25°C			10	
Output Load		Differential		100		Ohms
Start-up Time	T <sub>ST</sub>	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% V <sub>PP</sub>			400	ps
Output Fall Time		80% to 20% V <sub>PP</sub>			400	ps
Output Clock Duty Cycle	T <sub>DTCY</sub>	50%VP-P	45		55	%
Output Enable/ Disable Time	T <sub>OE</sub>				100	ns
Period Jitter, RMS	J <sub>PER</sub>	Frequency = 156.25MHz		3.0		ps
Random Jitter	R <sub>J</sub>	Frequency = 156.25MHz		1.3		ps
Deterministic Jitter	DJ	Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		5.8		ps
Total Jitter	T <sub>J</sub>	omor and digital quality opcomouncing,		23.6		ps
Phase Jitter (12kHz – 20MHz)	Ф <sub>ЛІТТЕК</sub>	Common Frequencies		0.89		ps
Phase Noise Performance	φ <sub>NOISE</sub>	100Hz of Carrier		-80		dBc/Hz
Frequency = 156.25MHz		1kHz of Carrier		-115		dBc/Hz
		10kHz of Carrier		-118		dBc/Hz
		100kHz of Carrier		-124		dBc/Hz
		1MHz of Carrier		-142		dBc/Hz
		10MHz of Carrier		-151		dBc/Hz
Output Frequency (Common)	F <sub>OUT</sub>	100MHz, 106.25MHz, 1258MHz, 150MH 212.5MHz, 250MHz, 300MHz, 312.5MH (Contact IDT for additional frequencies)		lHz, 156.25	MHz, 200M	Hz,

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at 25°C. We do not recommend hand soldering the devices



### **DC Characteristics**

 $(V_{DD}= 2.5 V \pm 5\%, T_A= -20^{\circ}C \text{ to } +70^{\circ}C; -40^{\circ} \text{ to } +85^{\circ}C)$ 

Parameter	Symbol	Condition	Min	Тур	Max	Units
Power Supply Current	I <sub>DD</sub>	Common Frequencies	26		65	mA
Differential Output Voltage	V <sub>OD</sub>	Standard LVDS load		0.4		V
Output Offset Voltage	Vos	Standard LVDS load		1.25		V
Enable/Disable Input HIGH Voltage (Output enabled)*	V <sub>IH</sub>		70%V <sub>DD</sub>			V
Enable/Disable Input LOW Voltage (Output disabled)	V <sub>IL</sub>				30%V <sub>DD</sub>	V

<sup>\*</sup> A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

### **AC Characteristics**

 $(V_{DD}= 2.5 V \pm 5\%, T_A= -20^{\circ}C \text{ to } +70^{\circ}C; -40^{\circ} \text{ to } +85^{\circ}C)$ 

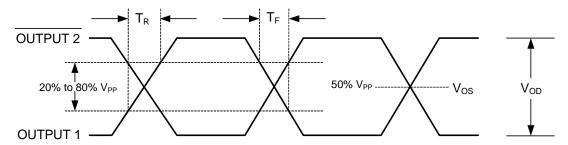
Parameter	Symbol	Condition	Min	Тур	Max	Units
Output Frequency Range	F <sub>OUTR</sub>		0.750		1000	MHz
Frequency Stability		Temperature = -20°C to +70°C	±20		±100	ppm
		Temperature = -40°C to +85°C	±25		±100	ppm
Output Load		Differential		100		Ohms
Start-up Time	T <sub>ST</sub>	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% V <sub>PP</sub>			400	ps
Output Fall Time		80% to 20% V <sub>PP</sub>			400	ps
Output Clock Duty Cycle	T <sub>DTCY</sub>	50%VP-P	45		55	%
Output Enable/ Disable Time	T <sub>OE</sub>				100	ns
Period Jitter, RMS	J <sub>PER</sub>	Frequency = 156.25MHz		4.0		ps
Random Jitter	R <sub>J</sub>	Frequency = 156.25MHz		1.4		ps
Deterministic Jitter	DJ	Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		9.2		ps
Total Jitter	T <sub>J</sub>	onter and digital equality specimeations,		29.2		ps
Phase Jitter (12kHz – 20MHz)	Ф <sub>ЛІТТЕК</sub>	Frequency = 156.25MHz		1.04		ps
Phase Noise Performance	φ <sub>NOISE</sub>	100Hz of Carrier		-83		dBc/Hz
Frequency = 156.25MHz		1kHz of Carrier		-105		dBc/Hz
		10kHz of Carrier		-113		dBc/Hz
		100kHz of Carrier		-119		dBc/Hz
		1MHz of Carrier		-137		dBc/Hz
		10MHz of Carrier		-146		dBc/Hz
Output Frequency (Standards)	F <sub>OUT</sub>	100MHz, 106.25MHz, 1258MHz, 150MH 212.5MHz, 250MHz, 300MHz, 312.5MH (Contact IDT for additional frequencies)		Hz, 156.25	MHz, 200M	Hz,

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at 25°C. We do not recommend hand soldering the devices



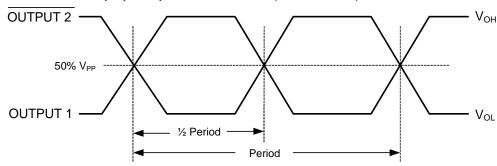
### **Output Waveform**

#### **Output Levels/Rise Time/Fall Time Measurements**

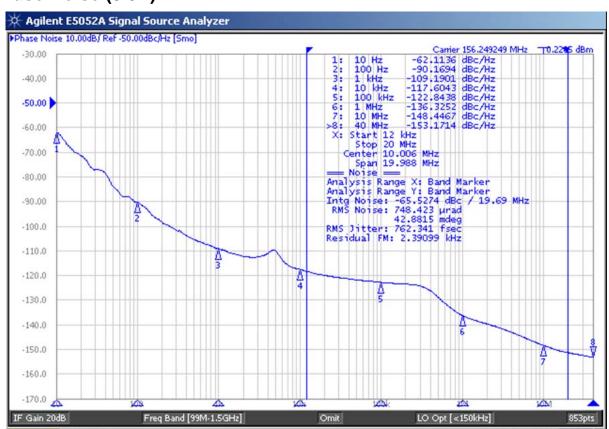


#### **Oscillator Symmetry**

Ideally, Symmetry should be 50/50 for  $1\!\!\!/_2$  period –Other expressions are 45/55 or 55/45



# **Typical Phase Noise (3.3V)**

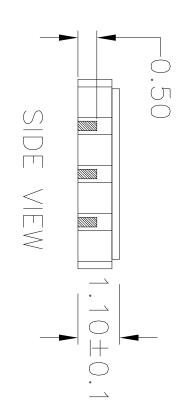


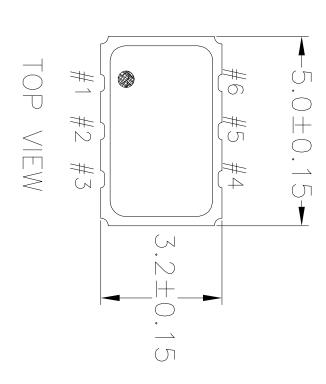


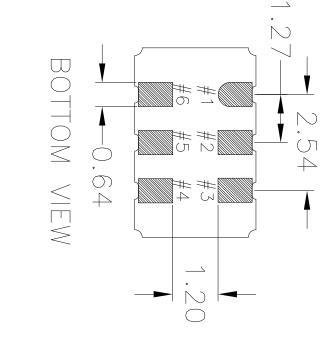
# JS6 Package Outline and Dimensions

NOTES:

1. ALL DIMENSIONS IN MM.







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C PSC=4411	SIZE DRAWING No.	1.1 mm Thick	5.0 x 3.2 mm BODY	TITLE JS6 PACKAGE OUTLINE	www.IDT.com FAX: (408) 492-8674	PHONE: (408) 727-6116	San Jose, CA 95138	TW 6024 Silver Creek Valle	



# JS6 Package Outline and Dimensions (cont.)

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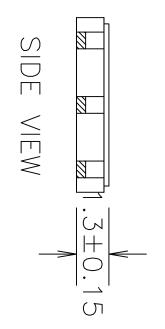
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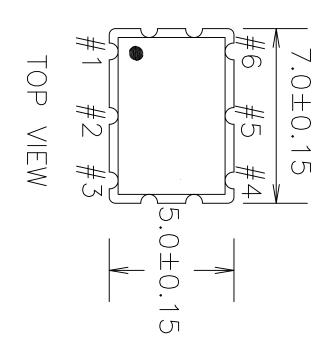
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03	UPDATE PACKAGE DRAWING	8/8/14	J.HUA

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					P̈	E	FAX: (408) 492-8674	PHONE: (408) 727-6116	San Jose, CA 95138	6024 Silver Creek Valley Rd
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# **JU6 Package Outline and Dimensions**





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NOTES:
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PSC-4430	DRAWING No.	1.3 mm Thick	7.0 x 5.0 mm BODY	JU6 PACKAGE OUTLINE	WWW.IDT.com FAX: (408) 492-8674	PHONE: (408) 727-6116	San Jose, CA 95138	TM 6024 Silver Creek Valley Ro	
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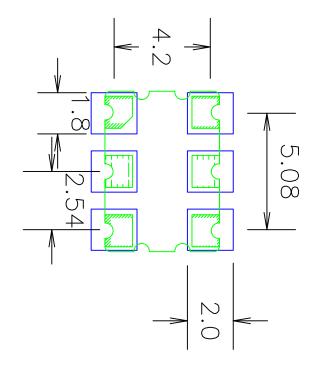


# JU6 Package Outline and Dimensions (cont.)

RECOMMENDED LAND PATTERN

- COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN. AND PATTERN IN BLUE. NSMD PATTERN ASSUMED. AND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT

FOR SURFACE MOUNT DESIGN AND LAND PATTERN.



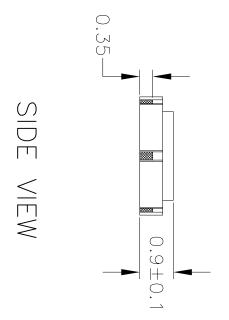
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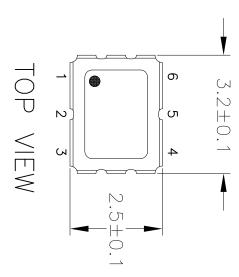
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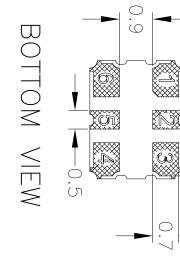


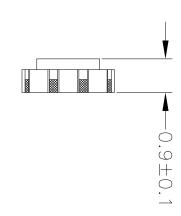
# JX6 Package Outline and Dimensions

1. ALL DIMENSIONS IN MM.







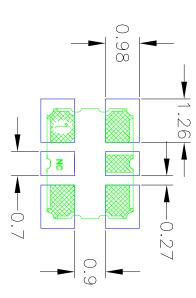


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DO NOT SCALE DRAWING	C PSC-4412	3.2 × 2.5 mm BODY 0.9 mm Thick	TITLE JX6 PACKAGE OUTLINE	WWW. IDT. com FAX: (408) 492-8
SHEE1				Creek Creek CA 95 CA 95 8) 727 492-8



# JX6 Package Outline and Dimensions (cont.)

FOR SURFACE MOUNT DESIGN AND LAND PATTERN



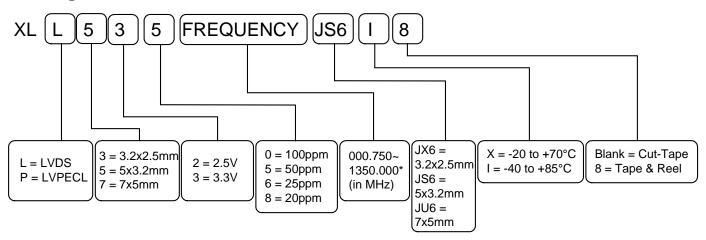
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SHEET 2 OF 2						492-8674	08) 727-6	CA 95138	r Creek Vo
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# **Ordering Information**



<sup>\*</sup> See table or contact IDT for custom frequencies

# **Revision History**

Rev	Date	Originator	Description of Change
Α	12/10/14	B. Chandhoke	Initial release.



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