

IS32FL3738

6×8 DOTS MATRIX LED DRIVER WITH INDIVIDUAL AUTO BREATH FUNCTION

Preliminary Information
February 2017

GENERAL DESCRIPTION

The IS32FL3738 is a general purpose 6×8 LEDs matrix driver with 1/12 cycle rate. The device can be programmed via an I2C compatible interface. Each LED can be dimmed individually with 8-bit × 4 PWM data which allowing 512 steps of linear dimming.

IS32FL3738 features 3 Auto Breathing Modes which are noted as ABM-1, ABM-2 and ABM-3. For each Auto Breathing Mode, there are 4 timing characters which include current rising / holding / falling / off time and 3 loop characters which include Loop-Beginning / Loop-Ending / Loop-Times. Every LED can be configured to be any Auto Breathing Mode or No-Breathing Mode individually.

Additionally each LED open and short state can be detected, IS32FL3738 store the open or short information in Open-Short Registers. The Open-Short Registers allowing MCU to read out via I2C compatible interface. Inform MCU whether there are LEDs open or short and the locations of open or short LEDs.

The IS32FL3738 operates from 2.7V to 5.5V and features a very low shutdown and operational current.

IS32FL3738 is available in eTSSOP-28 package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 2.7V to 5.5V
- 8 current source outputs for row control
- 6 switch current inputs for column scan control
- Up to 48 LEDs (6×8) in dot matrix
- Programmable 6×8 (16 RGBs) matrix size with de-ghost function
- 1MHz I2C-compatible interface
- Selectable 3 Auto Breath Modes for each dot
- Auto breath loop features interrupt pin inform MCU auto breath loop completed
- Auto breath offers 128 steps gamma current, interrupt and state look up registers
- 256 steps global current setting
- Individual on/off control
- Individual 512 PWM control steps
- Individual Auto Breath Mode select
- Individual open and short error detect function
- Cascade for synchronization of chips
- eTSSOP-28 package
- Automotive AEC-Q100 qualified (pending)

APPLICATIONS

- Mobile phones and other hand-held devices for LED display
- Gaming device (Keyboard, Mouse etc.)
- LED in white goods application

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TYPICAL APPLICATION CIRCUIT

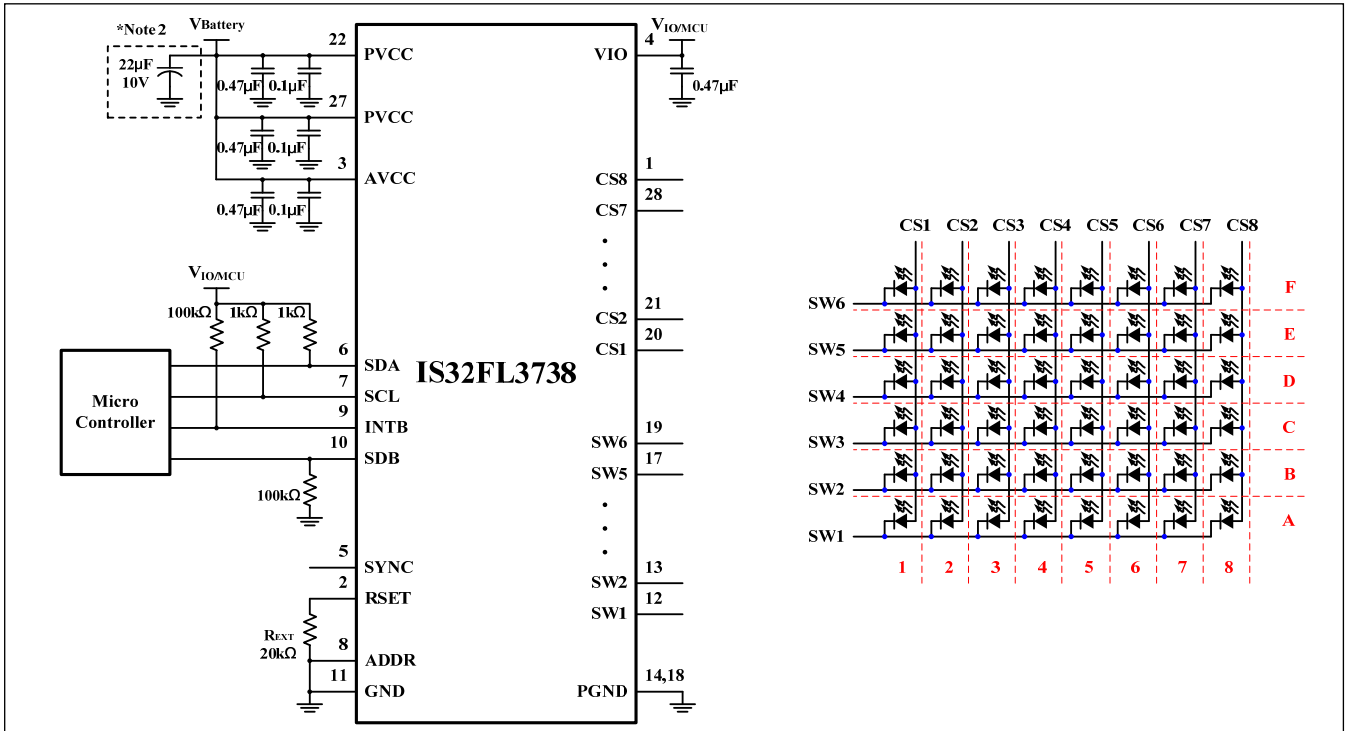


Figure 1 Typical Application Circuit (6x8)

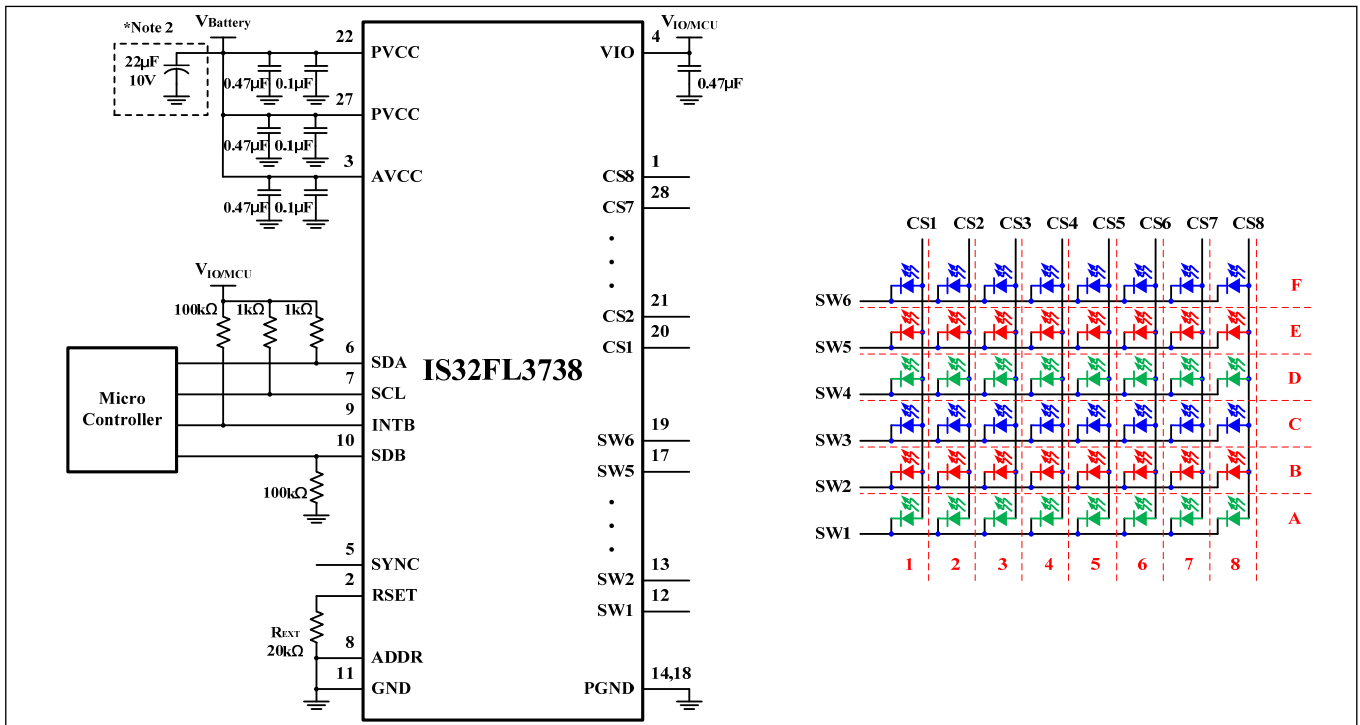


Figure 2 Typical Application Circuit (RGB)

Note 1: For the mobile applications the IC should be placed far away from the mobile antenna in order to prevent the EMI.

Note 2: Electrolytic/Tantalum Capacitor may considerable for high current application to avoid audible noise interference.

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TYPICAL APPLICATION CIRCUIT (CONTINUED)

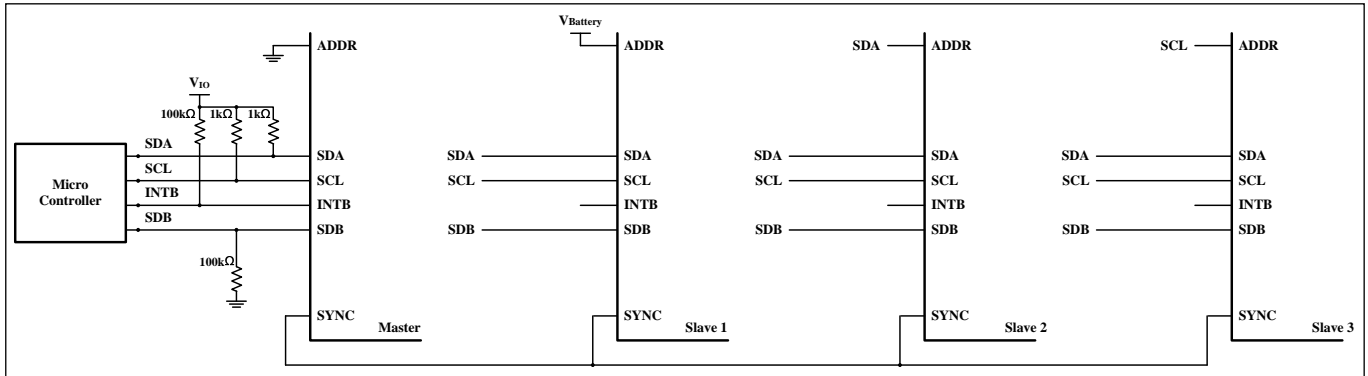
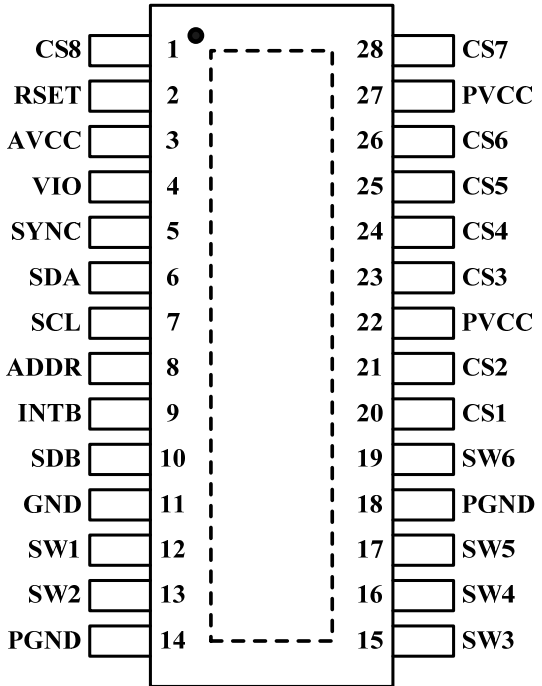


Figure 3 Typical Application Circuit (Four Parts Synchronization-Work)

Note 3: One part is configured as master mode, all the other 3 parts configured as slave mode. Work as master mode or slave mode specified by Configuration Register (Function register, address 00h). Master part output master clock, and all the other parts which work as slave input this master clock.

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PIN CONFIGURATION

| Package | Pin Configuration (Top View) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|---|-----|------|----|-----|------|---|----|------|------|---|----|-----|-----|---|----|-----|------|---|----|-----|-----|---|----|-----|-----|---|----|------|------|---|----|-----|------|---|----|-----|-----|----|----|-----|-----|----|----|------|-----|----|----|-----|-----|----|----|-----|------|----|----|-----|
| eTSSOP-28 |  <p>The diagram shows a top view of the eTSSOP-28 package. Pin 1 is located at the top-left corner, indicated by a solid dot. Pins 1 through 14 are arranged vertically along the left edge, and pins 15 through 28 are arranged vertically along the right edge. A dashed line connects pin 1 to pin 14, and another dashed line connects pin 14 to pin 15, forming a U-shape that defines the package's footprint.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>CS8</td><td>1</td><td>28</td><td>CS7</td> </tr> <tr> <td>RSET</td><td>2</td><td>27</td><td>PVCC</td> </tr> <tr> <td>AVCC</td><td>3</td><td>26</td><td>CS6</td> </tr> <tr> <td>VIO</td><td>4</td><td>25</td><td>CS5</td> </tr> <tr> <td>SYNC</td><td>5</td><td>24</td><td>CS4</td> </tr> <tr> <td>SDA</td><td>6</td><td>23</td><td>CS3</td> </tr> <tr> <td>SCL</td><td>7</td><td>22</td><td>PVCC</td> </tr> <tr> <td>ADDR</td><td>8</td><td>21</td><td>CS2</td> </tr> <tr> <td>INTB</td><td>9</td><td>20</td><td>CS1</td> </tr> <tr> <td>SDB</td><td>10</td><td>19</td><td>SW6</td> </tr> <tr> <td>GND</td><td>11</td><td>18</td><td>PGND</td> </tr> <tr> <td>SW1</td><td>12</td><td>17</td><td>SW5</td> </tr> <tr> <td>SW2</td><td>13</td><td>16</td><td>SW4</td> </tr> <tr> <td>PGND</td><td>14</td><td>15</td><td>SW3</td> </tr> </table> | CS8 | 1 | 28 | CS7 | RSET | 2 | 27 | PVCC | AVCC | 3 | 26 | CS6 | VIO | 4 | 25 | CS5 | SYNC | 5 | 24 | CS4 | SDA | 6 | 23 | CS3 | SCL | 7 | 22 | PVCC | ADDR | 8 | 21 | CS2 | INTB | 9 | 20 | CS1 | SDB | 10 | 19 | SW6 | GND | 11 | 18 | PGND | SW1 | 12 | 17 | SW5 | SW2 | 13 | 16 | SW4 | PGND | 14 | 15 | SW3 |
| CS8 | 1 | 28 | CS7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RSET | 2 | 27 | PVCC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| AVCC | 3 | 26 | CS6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VIO | 4 | 25 | CS5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SYNC | 5 | 24 | CS4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SDA | 6 | 23 | CS3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SCL | 7 | 22 | PVCC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ADDR | 8 | 21 | CS2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INTB | 9 | 20 | CS1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SDB | 10 | 19 | SW6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GND | 11 | 18 | PGND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW1 | 12 | 17 | SW5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SW2 | 13 | 16 | SW4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PGND | 14 | 15 | SW3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

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PIN DESCRIPTION

| No. | Pin | Description |
|--------|-------------|--|
| 1 | CS8 | Current source. |
| 2 | RSET | Input terminal used to connect an external resistor. This regulates current source DC current value. |
| 3 | AVCC | Power for analog circuits. |
| 4 | VIO | Input logic reference voltage. |
| 5 | SYNC | Synchronize pin. It is used for more than one part work synchronize. If it is not used please float this pin. |
| 6 | SDA | I2C compatible serial data. |
| 7 | SCL | I2C compatible serial clock. |
| 8 | ADDR | I2C address setting. |
| 9 | INTB | Interrupt output pin. Register F0h sets the function of the INTB pin and active low when the interrupt event happens. Can be NC (float) if interrupt function no used. |
| 10 | SDB | Shutdown the chip when pull to low. |
| 11 | GND | Ground |
| 12, 13 | SW1, SW2 | Switch pin for LED matrix scanning. |
| 14, 18 | PGND | Power GND, connect to GND. |
| 15~17 | SW3~ SW5 | Switch pin for LED matrix scanning. |
| 19 | SW6 | Switch pin for LED matrix scanning. |
| 20, 21 | CS1, CS2 | Current source. |
| 22, 27 | PVCC | Power for current source. |
| 23~26 | CS3~ CS6 | Current source. |
| 28 | CS7 | Current source. |
| | Thermal Pad | Need to connect to GND pins. |



IS32FL3738

ORDERING INFORMATION

Automotive Range: -40°C to +125°C

| Order Part No. | Package | QTY |
|--------------------|----------------------|-----------|
| IS32FL3738-ZLA3-TR | eTSSOP-28, Lead-free | 2500/Reel |
| IS32FL3738-ZLA3 | | 50/Tube |

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- b.) the user assume all such risks; and
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IS32FL3738

ABSOLUTE MAXIMUM RATINGS

| | |
|--|-----------------------|
| Supply voltage, V_{CC} | -0.3V ~ +6.0V |
| Voltage at any input pin | -0.3V ~ $V_{CC}+0.3V$ |
| Maximum junction temperature, T_{JMAX} | 150°C |
| Storage temperature range, T_{STG} | -65°C ~ +150°C |
| Operating temperature range, T_A | -40°C ~ +125°C |
| Thermal resistance, junction to ambient, θ_{JA} | 40.6°C/W |
| ESD (HBM) | ±2kV |
| ESD (CDM) | ±750V |

Note:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for $V_{CC} = 3.6V$, $T_A = 25^\circ C$, unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|------------|---|---|------|------|------|---------|
| V_{CC} | Supply voltage | | 2.7 | | 5.5 | V |
| I_{CC} | Quiescent power supply current | $V_{SDB} = V_{CC}$, all LEDs off | | 2.17 | | mA |
| I_{SD} | Shutdown current | $V_{SDB} = 0V$ | | 3 | | μA |
| | | $V_{SDB} = V_{CC}$, Configuration Register written "0000 0000" | | 3 | | |
| I_{OUT} | Maximum constant current of CS1~CS8 | $R_{SET}=20k\Omega$ | | 84 | | mA |
| I_{LED} | Average current on each LED $I_{LED} = (I_{OUT}/12.75) \times 2$ | $R_{SET}=20k\Omega$, GCC=255, PWM = 255 | | 13.2 | | mA |
| V_{HR} | Current sink headroom voltage SW1~SW6 | $I_{SINK} = 672mA$ (Note 1,2) | | 350 | | mV |
| | Current source headroom voltage CS1~C8 | $I_{SOURCE} = 84mA$ (Note 1) | | 350 | | |
| t_{SCAN} | Period of scanning | | | 128 | | μs |
| t_{NOL} | Non-overlap blanking time during scan, the SWy and CSx are all off during this time | | | 8 | | μs |

Logic Electrical Characteristics (SDA, SCL, ADDR, SYNC, SDB)

| | | | | | | |
|-----------|-----------------------------------|-------------------------------|--------------|-----|-------------|----|
| V_{IL} | Logic "0" input voltage | $V_{IO}=3.6V$ | GND | | $0.2V_{IO}$ | V |
| V_{IH} | Logic "1" input voltage | $V_{IO}=3.6V$ | $0.75V_{IO}$ | | V_{IO} | V |
| V_{HYS} | Input Schmitt trigger hysteresis | $V_{IO}=3.6V$ | | 0.2 | | V |
| V_{OL} | Logic "0" output voltage for SYNC | $I_{OL} = 8mA$ | | | 0.4 | V |
| V_{OH} | Logic "1" output voltage for SYNC | $I_{OH} = 8mA$ | $0.75V_{IO}$ | | | V |
| I_{IL} | Logic "0" input current | $V_{INPUT} = 0V$ (Note 3) | | 5 | | nA |
| I_{IH} | Logic "1" input current | $V_{INPUT} = V_{IO}$ (Note 3) | | 5 | | nA |

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DIGITAL INPUT SWITCHING CHARACTERISTICS (NOTE 3)

| Symbol | Parameter | Fast Mode | | | Fast Mode Plus | | | Units |
|---------------|--|-----------|------|------|----------------|------|------|---------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| f_{SCL} | Serial-clock frequency | - | | 400 | - | | 1000 | kHz |
| t_{BUF} | Bus free time between a STOP and a START condition | 1.3 | | - | 0.5 | | - | μ s |
| $t_{HD, STA}$ | Hold time (repeated) START condition | 0.6 | | - | 0.26 | | - | μ s |
| $t_{SU, STA}$ | Repeated START condition setup time | 0.6 | | - | 0.26 | | - | μ s |
| $t_{SU, STO}$ | STOP condition setup time | 0.6 | | - | 0.26 | | - | μ s |
| $t_{HD, DAT}$ | Data hold time | - | | - | - | | - | μ s |
| $t_{SU, DAT}$ | Data setup time | 100 | | - | 50 | | - | ns |
| t_{LOW} | SCL clock low period | 1.3 | | - | 0.5 | | - | μ s |
| t_{HIGH} | SCL clock high period | 0.7 | | - | 0.26 | | - | μ s |
| t_R | Rise time of both SDA and SCL signals, receiving | - | | 300 | - | | 120 | ns |
| t_F | Fall time of both SDA and SCL signals, receiving | - | | 300 | - | | 120 | ns |

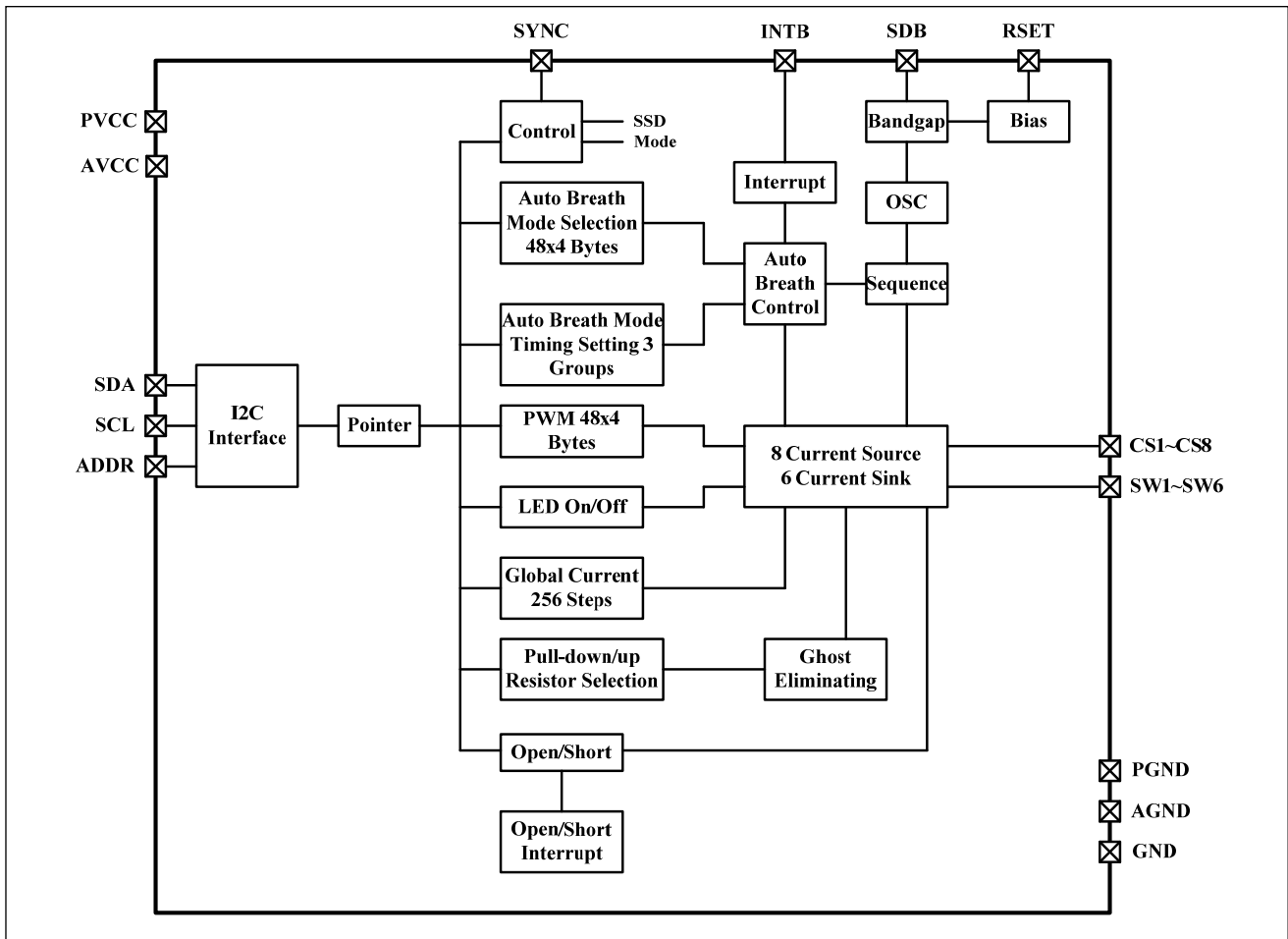
Note 1: In case of $R_{EXT} = 20k\Omega$, Global Current Control Register (PG3, 01h) written "1111 1111", GCC = "1111 1111".

Note 2: All LEDs are on and PWM = "1111 1111", GCC = "1111 1111".

Note 3: Guaranteed by design.

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FUNCTIONAL BLOCK DIAGRAM



IS32FL3738

DETAILED DESCRIPTION

I2C INTERFACE

The IS32FL3738 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS32FL3738 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A4:A1 are decided by the connection of the ADDR pin. The complete slave address is:

Table 1 Slave Address:

| ADDR2 | ADDR1 | A7:A5 | A4:A1 | A0 |
|-------|-------|-------|-------|-----|
| GND | GND | 101 | 0000 | 0/1 |
| SCL | SCL | | 0101 | |
| SDA | SDA | | 1010 | |
| VCC | VCC | | 1111 | |

ADDR connected to GND, (A4:A1)=0000;
 ADDR connected to VCC, (A4:A1)=1111;
 ADDR connected to SCL, (A4:A1)=0101;
 ADDR connected to SDA, (A4:A1)=1010;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 1kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS32FL3738.

The timing diagram for the I2C is shown in Figure 4. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS32FL3738's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS32FL3738 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the

SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS32FL3738, the register address byte is sent, most significant bit first. IS32FL3738 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS32FL3738 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS32FL3738, load the address of the data register that the first data byte is intended for. During the IS32FL3738 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS32FL3738 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS32FL3738 (Figure 7).

READING OPERATION

Register FEh, F1h and 18h~2Dh, 30h~45h of Page 0, 11h of Page 3 can be read.

To read the FEh and F1h, after I2C start condition, the bus master must send the IS32FL3738 device address with the R/\bar{W} bit set to "0", followed by the register address (FEh or F1h) which determines which register is accessed. Then restart I2C, the bus master should send the IS32FL3738 device address with the R/\bar{W} bit set to "1". Data from the register defined by the command byte is then sent from the CHROMA-96 to the master (Figure 8).

To read the 18h~2Dh, 30h~45h of Page 0, 11h of Page 3, the FDh should write with 00h before follow the Figure 8 sequence to read the data, that means, when you want to read 18h~2Dh, 30h~45h of Page 0, 11h of Page 3, the FDh should point to Page 0 or Page 3 first and you can read the Page 0 and Page 3 data.

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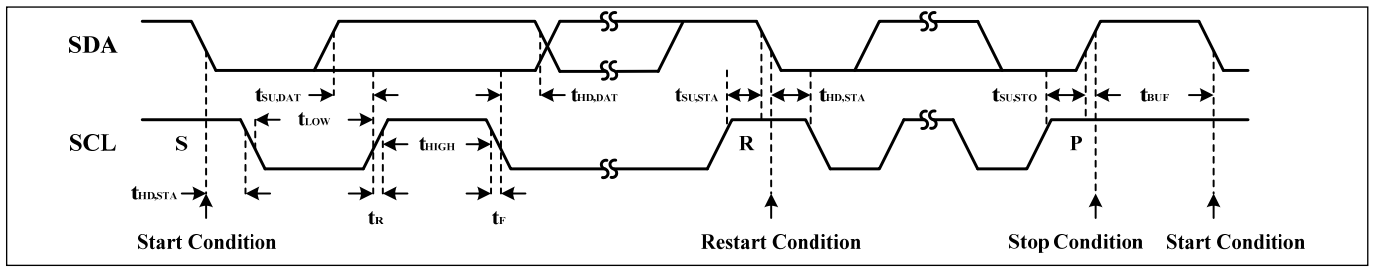


Figure 4 Interface timing

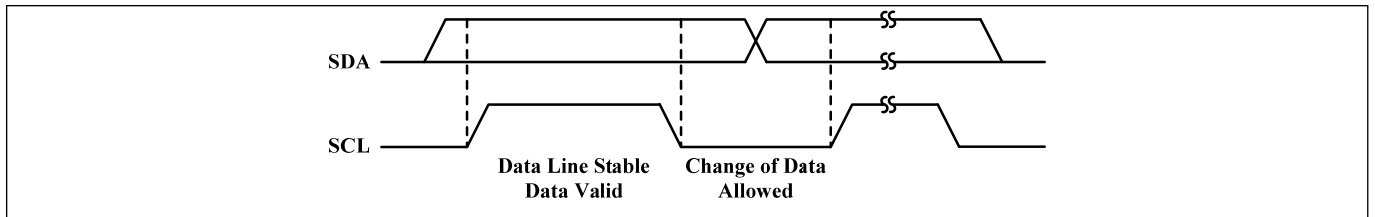


Figure 5 Bit transfer

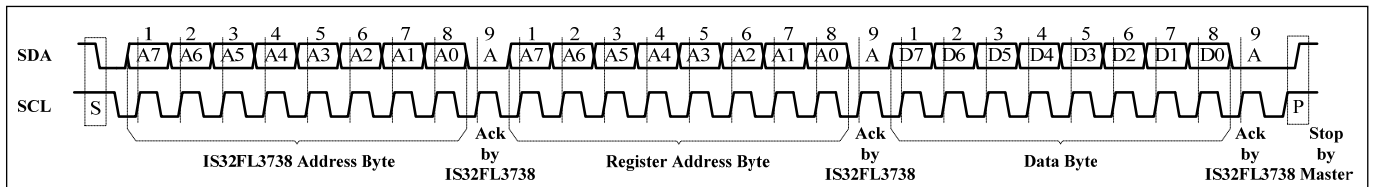


Figure 6 Writing to IS32FL3738 (Typical)

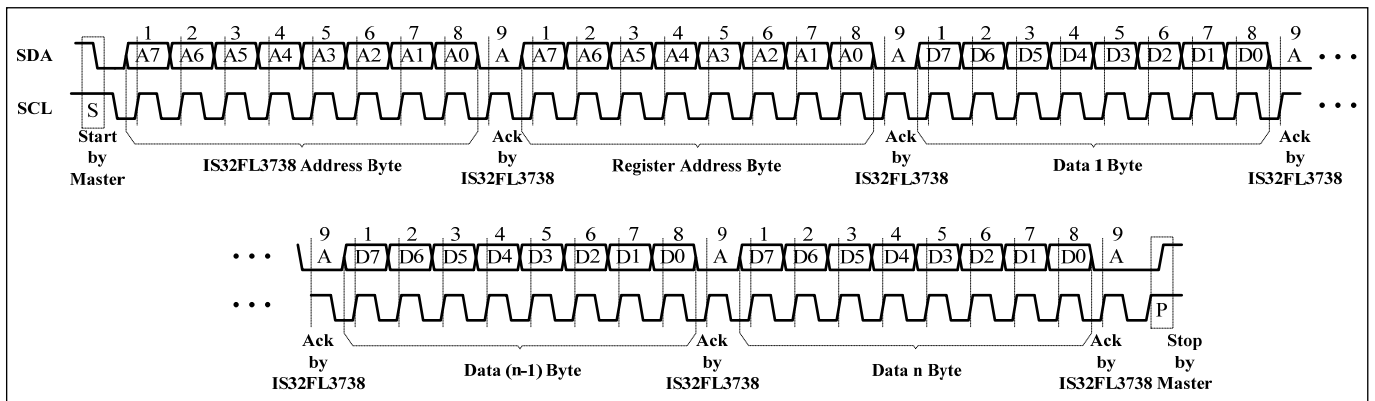


Figure 7 Writing to IS32FL3738 (Automatic address increment)

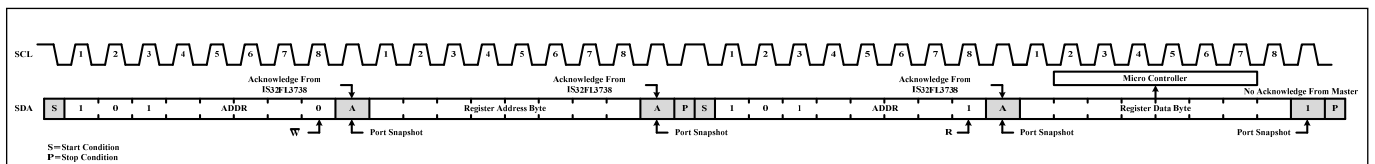


Figure 8 Reading from IS32FL3738

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REGISTER DEFINITION-1

| Address | Name | Function | Table | R/W | Default |
|---------|-----------------------------|--------------------------------------|-------|-----|-----------|
| FDh | Command Register | Available Page 0 to Page 3 Registers | 2 | W | xxxx xxxx |
| FEh | Command Register Write lock | To lock/unlock Command Register | 3 | R/W | 0000 0000 |
| F0h | Interrupt Mask Register | Configure the interrupt function | 4 | W | |
| F1h | Interrupt Status Register | Show the interrupt status | 5 | R | |

REGISTER CONTROL

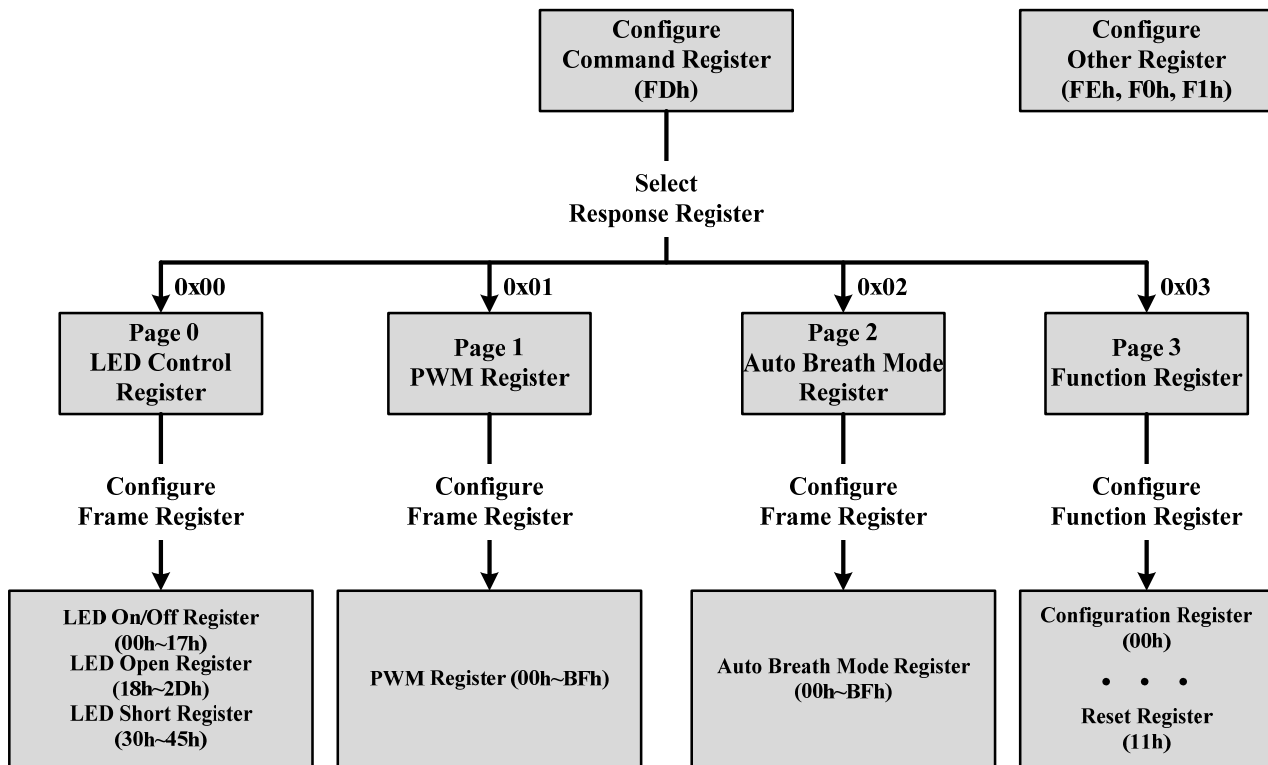


Table 2 FDh Command Register (Write Only)

| Data | Function |
|-----------|---|
| 0000 0000 | Point to Page 0 (PG0, LED Control Register is available) |
| 0000 0001 | Point to Page 1 (PG1, PWM Register is available) |
| 0000 0010 | Point to Page 2 (PG2, Auto Breath Mode Register is available) |
| 0000 0011 | Point to Page 3 (PG3, Function Register is available) |
| Others | Reserved |

Note: FDh is locked when power up, need to unlock this register before write command to it. See Table 3 for detail.

The Command Register should be configured first after writing in the slave address to choose the available register. Then write data in the choosing register. Power up default state is "0000 0000".

For example, when write "0000 0001" in the Command Register (FDh), the data which writing after will be stored in the Auto breath mode Register. Write new data can configure other registers.

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Table 3 FEh Command Register Write Lock (Read/Write)

| Bit | D7:D0 |
|---------|-------------------------------|
| Name | CRWL |
| Default | 0000 0000 (FDh write disable) |

To select the PG0~PG3, need to unlock this register first, with the purpose to avoid misoperation of this register. When FEh is written with 0xC5, FDh is allowed to modify once, after the FDh is modified the FEh will reset to be 0x00 at once.

CRWL Command Register Write Lock
 0x00 FDh write disable
 0xC5 FDh write enable once

Table 4 F0h Interrupt Mask Register

| Bit | D7:D4 | D3 | D2 | D1 | D0 |
|---------|-------|-----|-----|----|----|
| Name | - | IAC | IAB | IS | IO |
| Default | 0000 | 0 | 0 | 0 | 0 |

Configure the interrupt function for IC.

IAC Auto Clear Interrupt Bit
 0 Interrupt could not auto clear
 1 Interrupt auto clear when INTB stay low exceeds 8ms

IAB Auto Breath Interrupt Bit
 0 Disable auto breath loop finish interrupt
 1 Enable auto breath loop finish interrupt

IS Dot Short Interrupt Bit
 0 Disable dot short interrupt
 1 Enable dot short interrupt

IO Dot Open Interrupt Bit
 0 Disable dot open interrupt
 1 Enable dot open interrupt

Table 5 F1h Interrupt Status Register

| Bit | D7:D5 | D4 | D3 | D2 | D1 | D0 |
|---------|-------|------|------|------|----|----|
| Name | - | ABM3 | ABM2 | ABM1 | SB | OB |
| Default | 000 | 0 | 0 | 0 | 0 | 0 |

Show the interrupt status for IC.

ABM3 Auto Breath Mode 3 Finish Bit
 0 ABM3 not finish
 1 ABM3 finish

ABM2 Auto Breath Mode 2 Finish Bit
 0 ABM2 not finish
 1 ABM2 finish

ABM1 Auto Breath Mode 1 Finish Bit
 0 ABM1 not finish
 1 ABM1 finish

SB Short Bit
 0 No short
 1 Short happens

OB Open Bit
 0 No open
 1 Open happens

IS32FL3738

REGISTER DEFINITION-2

| Address | Name | Function | Table | R/W | Default |
|--|---|--|-------|-----|-----------|
| PG0 (0x00): LED Control Register | | | | | |
| 00h ~ 17h | LED On/Off Register | Set on or off state for each LED | 7 | W | 0000 0000 |
| 18h ~ 2Dh | LED Open Register | Store open state for each LED | 8 | R | |
| 30h ~ 45h | LED Short Register | Store short state for each LED | 9 | R | |
| PG1 (0x01): PWM Register | | | | | |
| 00h~BFh | PWM Register | Set PWM duty for LED | 10 | W | 0000 0000 |
| PG2 (0x02): Auto Breath Mode Register | | | | | |
| 00h~BFh | Auto Breath Mode Register | Set operating mode of each dot | 11 | W | 0000 0000 |
| PG3 (0x03) : Function Register | | | | | |
| 00h | Configuration Register | Configure the operation mode | 13 | W | 0000 0000 |
| 01h | Global Current Control Register | Set the global current | 14 | W | |
| 02h | Auto Breath Control Register 1 of ABM-1 | Set fade in and hold time for breath function of ABM-1 | 15 | W | |
| 03h | Auto Breath Control Register 2 of ABM-1 | Set the fade out and off time for breath function of ABM-1 | 16 | W | |
| 04h | Auto Breath Control Register 3 of ABM-1 | Set loop characters of ABM-1 | 17 | W | |
| 05h | Auto Breath Control Register 4 of ABM-1 | Set loop characters of ABM-1 | 18 | W | |
| 06h | Auto Breath Control Register 1 of ABM-2 | Set fade in and hold time for breath function of ABM-2 | 15 | W | |
| 07h | Auto Breath Control Register 2 of ABM-2 | Set the fade out and off time for breath function of ABM-2 | 16 | W | |
| 08h | Auto Breath Control Register 3 of ABM-2 | Set loop characters of ABM-2 | 17 | W | |
| 09h | Auto Breath Control Register 4 of ABM-2 | Set loop characters of ABM-2 | 18 | W | |
| 0Ah | Auto Breath Control Register 1 of ABM-3 | Set fade in and hold time for breath function of ABM-3 | 15 | W | |
| 0Bh | Auto Breath Control Register 2 of ABM-3 | Set the fade out and off time for breath function of ABM-3 | 16 | W | |
| 0Ch | Auto Breath Control Register 3 of ABM-3 | Set loop characters of ABM-3 | 17 | W | |
| 0Dh | Auto Breath Control Register 4 of ABM-3 | Set loop characters of ABM-3 | 18 | W | |
| 0Eh | Time Update Register | Update the setting of 02h ~ 0Dh registers | - | W | |
| 0Fh | SWy Pull-Up Resistor Selection Register | Set the pull-up resistor for SWy | 19 | W | |
| 10h | CSx Pull-Down Resistor Selection Register | Set the pull-down resistor for CSx | 20 | W | |
| 11h | Reset Register | Reset all register to POR state | - | R | |

Table 6-1 Page 0 (PG0, 0x00): LED Control Register - On Off Register

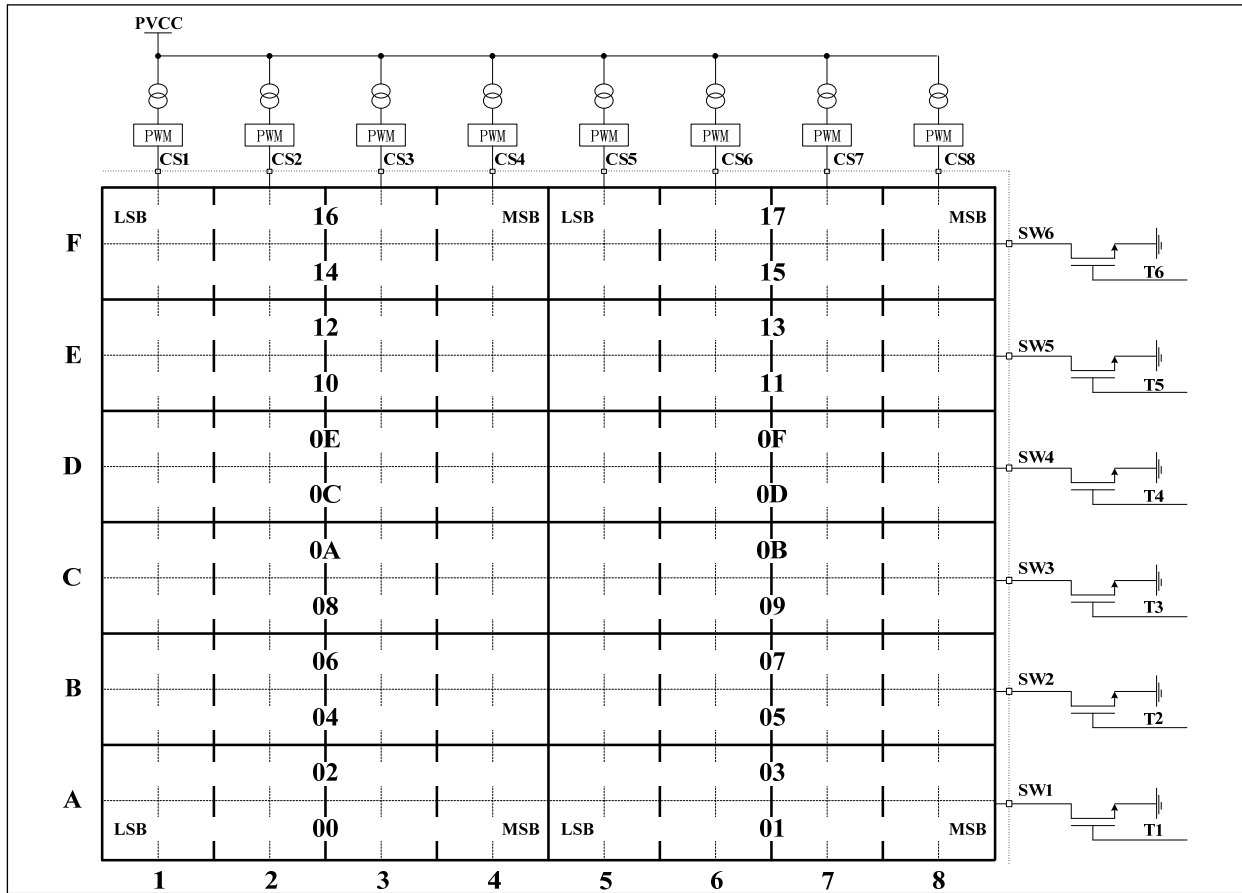


Figure 9 On off Register

Table 7 00h ~ 17h LED On/Off Register

| Bit | D7:D0 |
|---------|---|
| Name | C _{CS8} : C _{CS1} or C _{CS16} : C _{CS9} |
| Default | 0000 0000 |

The LED On/Off Registers store the on or off state of each LED in the Matrix.

Each LED has 4 bits on and off state, need to turn on/off them when turn on/off the LED.

For example:

When turn on LED 1-A, need to turn on D1:D0 of 00h, and D1:D0 of 02h

- C_{x-y} LED State Bit
- 0 LED off
- 1 LED on

Table 6-2 Page 0 (PG0, 0x00): LED Control Register – Open Detect Register

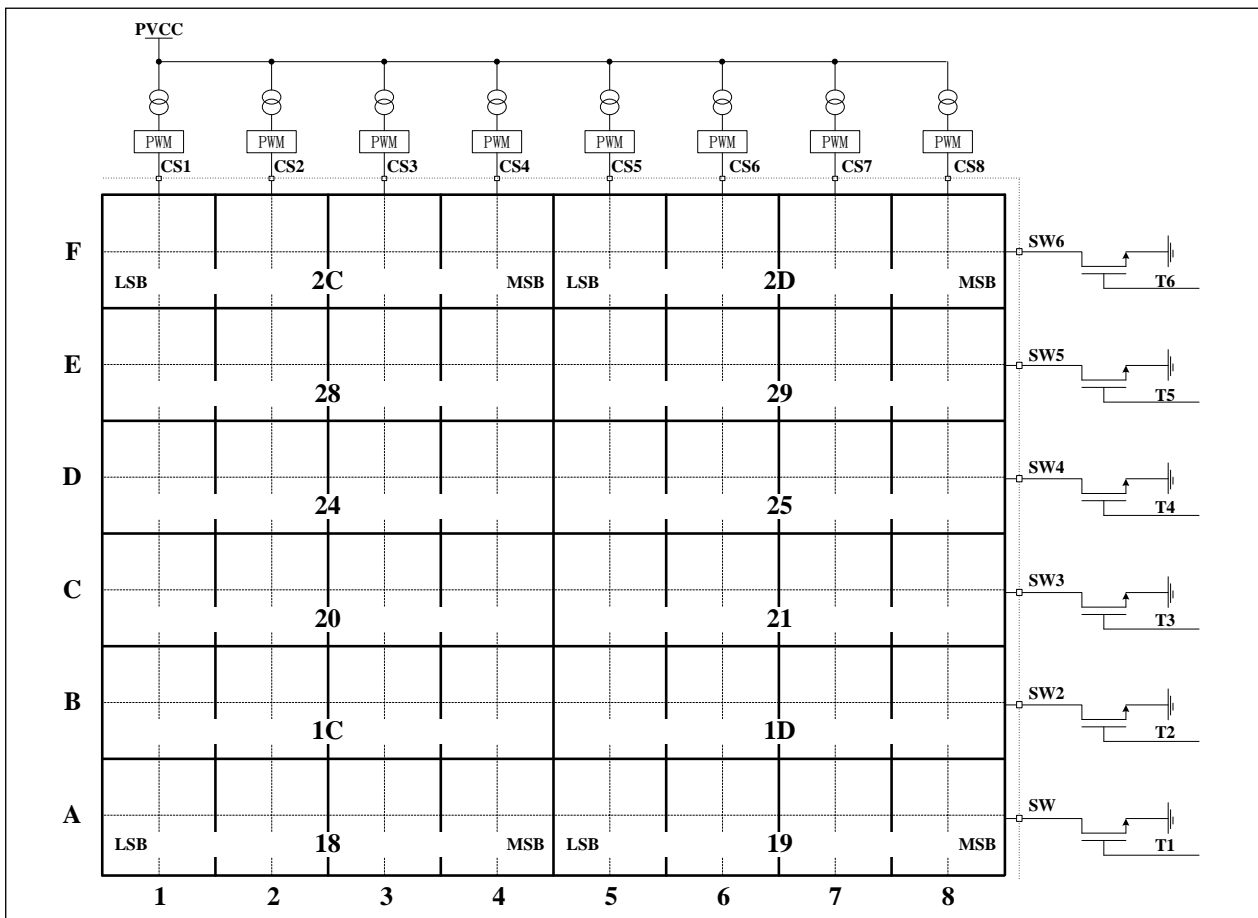


Figure 10 On off Register

Table 8 18h ~ 2Dh LED Open Register

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------|-----------------|----|-----------------|----|-----------------|----|-----------------|----|
| Name | OP ₈ | - | OP ₆ | - | OP ₄ | - | OP ₂ | - |
| Default | 0 | - | 0 | - | 0 | - | 0 | - |

The LED Open Registers store the open or normal state of each LED in the Matrix.

- OPx** LED Open Bit
- 0 LED normal
- 1 LED open

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Table 6-3 Page 0 (PG0, 0x00): LED Control Register – Short Detect Register

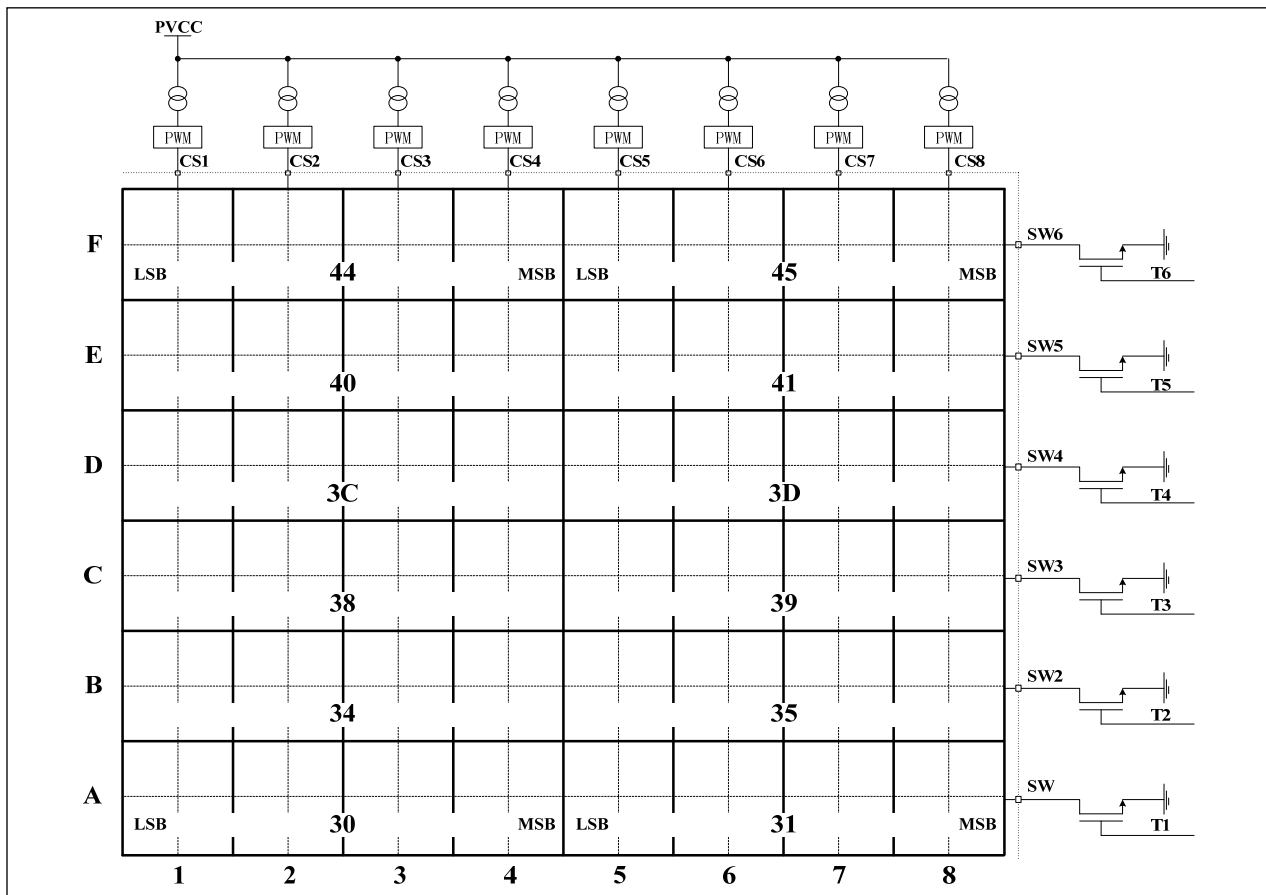


Figure 10 On off Register

Table 9 30h ~ 45h LED Short Register

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------|-----------------|----|-----------------|----|-----------------|----|-----------------|----|
| Name | ST ₈ | - | ST ₆ | - | ST ₄ | - | ST ₂ | - |
| Default | 0 | - | 0 | - | 0 | - | 0 | - |

The LED Short Registers store the short or normal state of each LED in the Matrix.

- STx** LED Short Bit
- 0 LED normal
- 1 LED short

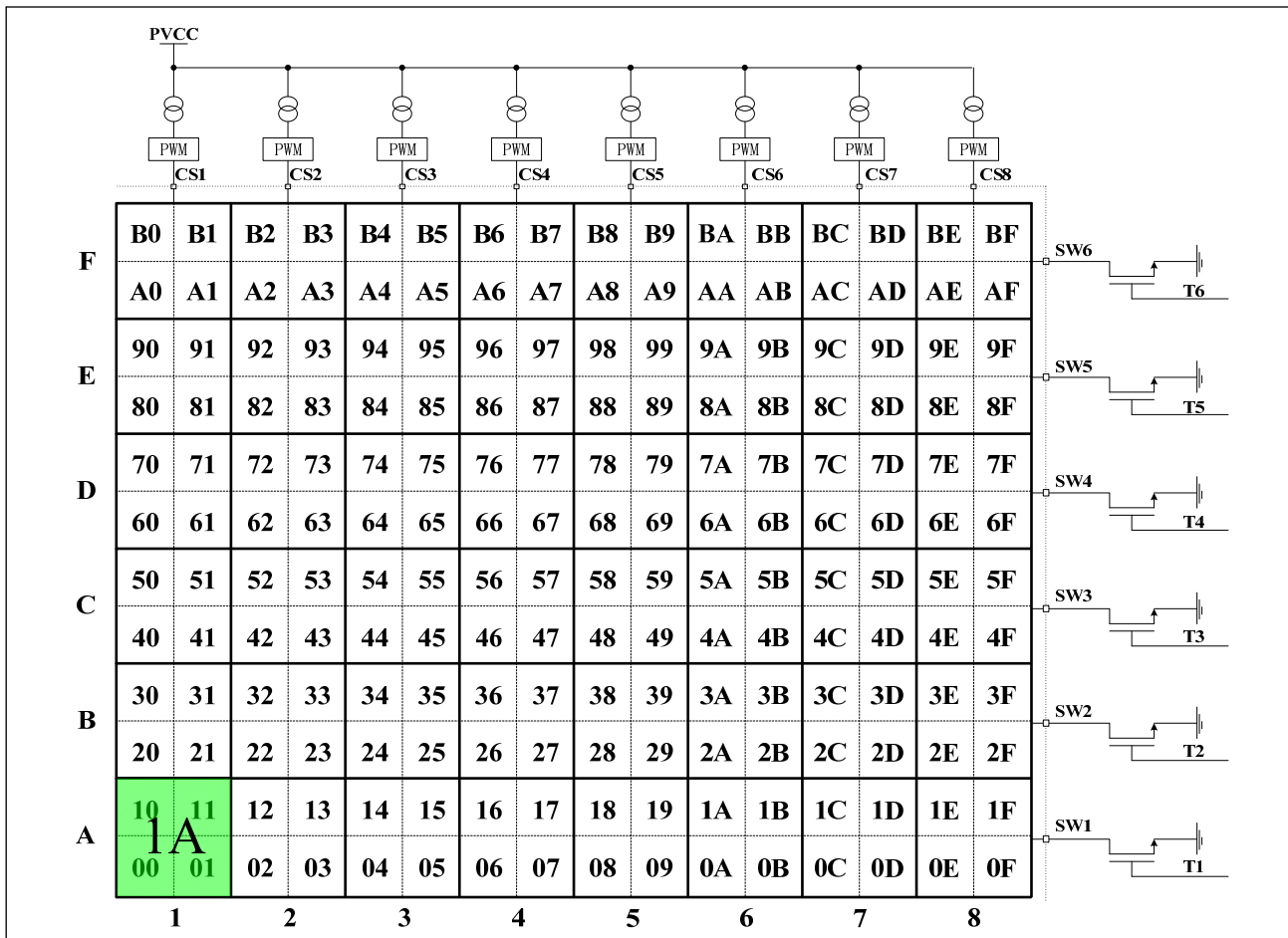
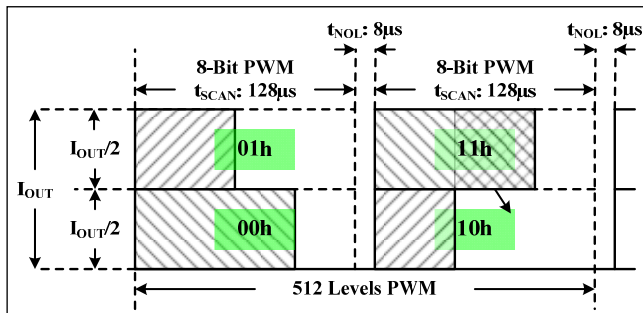


Figure 11 PWM Register

Table 10 00h ~ BFh PWM Register

| Bit | D7:D0 |
|---------|-----------|
| Name | PWM |
| Default | 0000 0000 |

Each dot has 4 bytes to modulate the PWM duty in 512 steps. Each byte controls half of the I_{OUT} and half of the duty, like LED 1A, the current will be as shown below:



The value of the PWM Registers decides the average current of each LED noted I_{LED} .

I_{LED} computed by Formula (1):

$$I_{LED} = \frac{\sum PWM}{512} \times I_{OUT} \times Duty \quad (1)$$

$$PWM = \sum_{n=0}^7 D[n] \cdot 2^n$$

Where Duty is the duty cycle of SWy/2,

$$Duty = \frac{128\mu s}{(128\mu s + 8\mu s)} \times \frac{1}{6} \times \frac{1}{2} = \frac{1}{12.75} \quad (2)$$

I_{OUT} is the output current of CSx (x=1~8),

$$I_{OUT} = \frac{840}{R_{EXT}} \times \frac{GCC}{256} \times 2 \quad (3)$$

GCC is the Global Current Control register (PG3, 01h) value and R_{EXT} is the external resistor of R_{SET} pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example 1:

If 00h=0xff, 01h=0xff, 10h=0xff, 11h=0xff, GCC=255, R_{EXT} =20k Ω (I_{OUT} =84mA),

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$$I_{LED-1A} = \frac{0xff + 0xff + 0xff + 0xff}{512} \times I_{OUT} \times \frac{1}{12.75}$$
$$= 13.13mA$$

For example 2:

If 00h=0x80, 01h=0x80, 10h=0x80, 11h=0x00,
GCC=255. R_{EXT}=20kΩ (I_{OUT}=84mA),

$$I_{LED-1A} = \frac{0x80 + 0x80 + 0x80 + 0x00}{512} \times I_{OUT} \times \frac{1}{12.75}$$
$$= 4.94mA$$

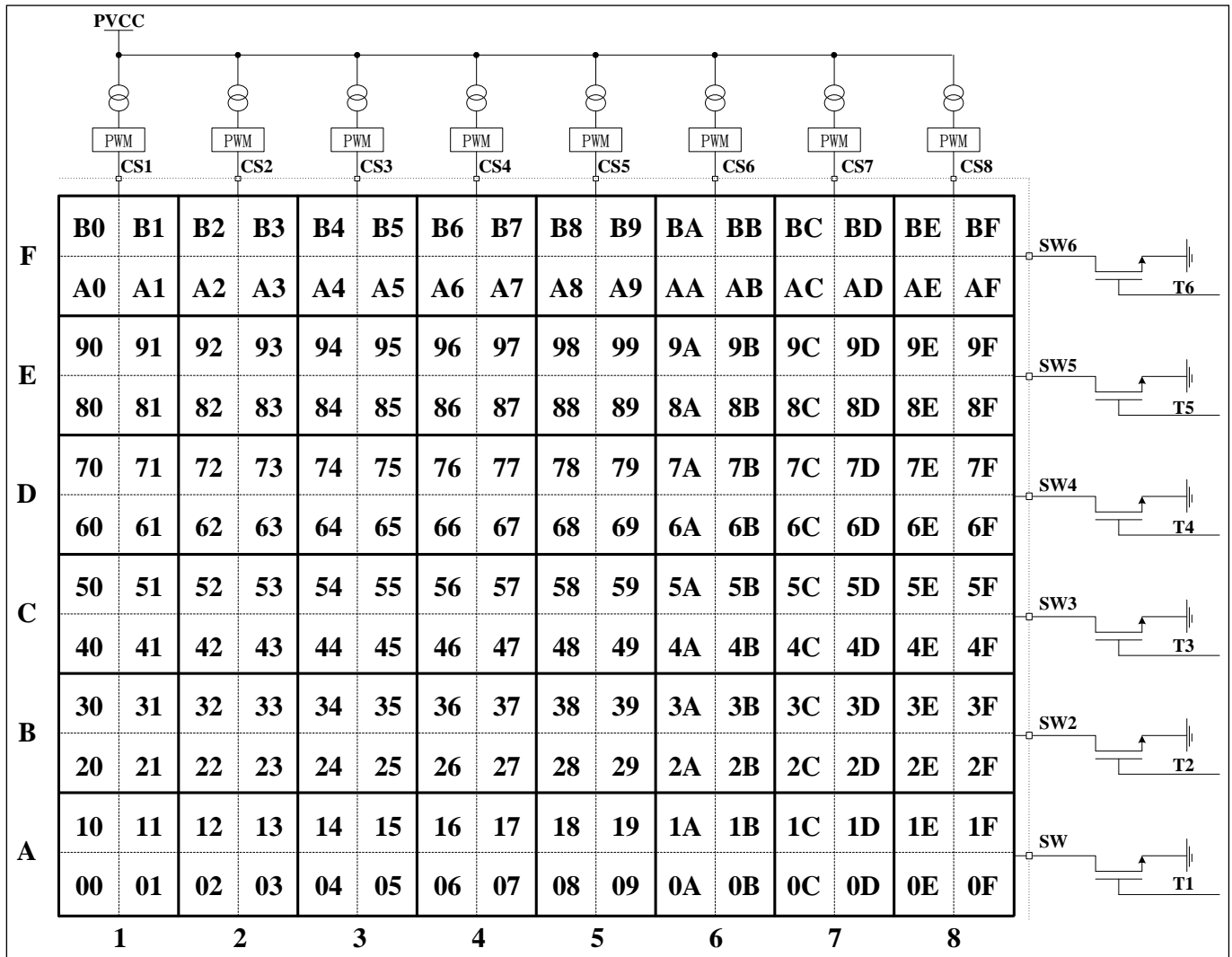


Figure 12 Auto Breath Mode Selection Register

Table 11 00h ~ BFh Auto Breath Mode Register

| Bit | D7:D2 | D1:D0 |
|---------|-------|-------|
| Name | - | ABMS |
| Default | - | 00 |

ABMS Auto Breath Mode Selection Bit

- 00 PWM control mode
- 01 Select Auto Breath Mode 1 (ABM-1)
- 10 Select Auto Breath Mode 2 (ABM-2)
- 11 Select Auto Breath Mode 3 (ABM-3)

The Auto Breath Mode Register sets operating mode of each dot, notice four registers should be the same value when you selecting the mode.

For example, if 00h=0x01, 01h=0x01, 10h=0x01, 11h=0x01, then LED 1A work as ABM-1 mode.

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Table 12 Page 3 (PG3, 0x03): Function Register

| Register | Name | Function | R/W | Default |
|----------|---|--|-----|--------------|
| 00h | Configuration Register | Configure the operation mode | W | 0000 0000 |
| 01h | Global Current Control Register | Set the global current | W | |
| 02h | Auto Breath Control Register 1 of ABM-1 | Set fade in and hold time for breath function of ABM-1 | W | |
| 03h | Auto Breath Control Register 2 of ABM-1 | Set the fade out and off time for breath function of ABM-1 | W | |
| 04h | Auto Breath Control Register 3 of ABM-1 | Set loop characters of ABM-1 | W | |
| 05h | Auto Breath Control Register 4 of ABM-1 | Set loop characters of ABM-1 | W | |
| 06h | Auto Breath Control Register 1 of ABM-2 | Set fade in and hold time for breath function of ABM-2 | W | |
| 07h | Auto Breath Control Register 2 of ABM-2 | Set the fade out and off time for breath function of ABM-2 | W | |
| 08h | Auto Breath Control Register 3 of ABM-2 | Set loop characters of ABM-2 | W | |
| 09h | Auto Breath Control Register 4 of ABM-2 | Set loop characters of ABM-2 | W | |
| 0Ah | Auto Breath Control Register 1 of ABM-3 | Set fade in and hold time for breath function of ABM-3 | W | |
| 0Bh | Auto Breath Control Register 2 of ABM-3 | Set the fade out and off time for breath function of ABM-3 | W | |
| 0Ch | Auto Breath Control Register 3 of ABM-3 | Set loop characters of ABM-3 | W | |
| 0Dh | Auto Breath Control Register 4 of ABM-3 | Set loop characters of ABM-3 | W | |
| 0Eh | Time Update Register | Update the setting of 02h ~ 0Dh registers | W | |
| 0Fh | SWy Pull-Up Resistor Selection Register | Set the pull-up resistor for SWy | W | |
| 10h | CSx Pull-Down Resistor Selection Register | Set the pull-down resistor for CSx | W | |
| 11h | Reset Register | Reset all register to POR state | R | |

Table 13 00h Configuration Register

| Bit | D7:D6 | D5:D3 | D2 | D1 | D0 |
|---------|-------|-------|-----|------|-----|
| Name | SYNC | - | OSD | B_EN | SSD |
| Default | 00 | 000 | 0 | 0 | 0 |

The Configuration Register sets operating mode of IS32FL3738.

When SYNC bits are set to “01”, the IS32FL3738 is configured as the master clock source and the SYNC pin will generate a clock signal distributed to the clock slave devices. To be configured as a clock slave device and accept an external clock input the slave device’s SYNC bits must be set to “10”.

When OSD set high, open/short detection will be trigger once, the user could trigger OS detection again by set OSD from 0 to 1.

When B_EN enable, those dots select working in ABM-x mode will start to run the pre-established timing. If it is disabled, all dots work in PWM mode. Following Figure 16 to enable the Auto Breath mode. When SSD is “0”, IS32FL3738 works in software shutdown mode and to normal operate the SSD bit should set to “1”.

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| | |
|-------------|---------------------------------|
| SYNC | Synchronize Configuration |
| 00/11 | High Impedance |
| 01 | Master |
| 10 | Slave |
| OSD | Open/Short Detection Enable Bit |
| 0 | Disable open/short detection |
| 1 | Enable open/short detection |
| B_EN | Auto Breath Enable |
| 0 | PWM Mode Enable |
| 1 | Auto Breath Mode Enable |
| SSD | Software Shutdown Control |
| 0 | Software shutdown |
| 1 | Normal operation |

| | |
|-----------|------------|
| T1 | T1 Setting |
| 000 | 0.21s |
| 001 | 0.42s |
| 010 | 0.84s |
| 011 | 1.68s |
| 100 | 3.36s |
| 101 | 6.72s |
| 110 | 13.44s |
| 111 | 26.88s |

| | |
|-----------|-------------|
| T2 | T2 Setting |
| 0000 | 0s |
| 0001 | 0.21s |
| 0010 | 0.42s |
| 0011 | 0.84s |
| 0100 | 1.68s |
| 0101 | 3.36s |
| 0110 | 6.72s |
| 0111 | 13.44s |
| 1000 | 26.88s |
| Others | Unavailable |

Table 14 01h Global Current Control Register

| Bit | D7:D0 |
|---------|-----------|
| Name | GCCx |
| Default | 0000 0000 |

The Global Current Control Register modulates all CS_x (x=1~8) DC current which is noted as I_{OUT} in 256 steps.

I_{OUT} is computed by the Formula (3):

$$I_{OUT} = \frac{840}{R_{EXT}} \times \frac{GCC}{256} \quad (3)$$

$$GCC = \sum_{n=0}^7 D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n, R_{EXT} is the external resistor of R_{SET} pin.

For example: if D7:D0 = 1011 0101,

$$I_{OUT} = \frac{2^0 + 2^2 + 2^4 + 2^5 + 2^7}{256} \times \frac{840}{R_{EXT}}$$

Table 15 02h, 06h, 0Ah Auto Breath Control Register 1 of ABM-x

| Bit | D7:D5 | D4:D1 | D0 |
|---------|-------|-------|----|
| Name | T1 | T2 | - |
| Default | 000 | 0000 | 0 |

Auto Breath Control Register 1 set the T1&T2 time in Auto Breath Mode.

Table 16 03h, 07h, 0Bh Auto Breath Control Register 2 of ABM-x

| Bit | D7:D5 | D4:D1 | D0 |
|---------|-------|-------|----|
| Name | T3 | T4 | - |
| Default | 000 | 0000 | 0 |

Auto Breath Control Register 2 set the T3&T4 time in Auto Breath Mode.

| | |
|-----------|------------|
| T3 | T3 Setting |
| 000 | 0.21s |
| 001 | 0.42s |
| 010 | 0.84s |
| 011 | 1.68s |
| 100 | 3.36s |
| 101 | 6.72s |
| 110 | 13.44s |
| 111 | 26.88s |

| | |
|-----------|-------------|
| T4 | T4 Setting |
| 0000 | 0s |
| 0001 | 0.21s |
| 0010 | 0.42s |
| 0011 | 0.84s |
| 0100 | 1.68s |
| 0101 | 3.36s |
| 0110 | 6.72s |
| 0111 | 13.44s |
| 1000 | 26.88s |
| 1001 | 53.76s |
| 1010 | 107.52s |
| Others | Unavailable |

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Table 17 04h, 08h, 0Ch Auto Breath Control Register 3 of ABM-x

| Bit | D7:D6 | D5:D4 | D3:D0 |
|---------|-------|-------|-------|
| Name | LE | LB | LTA |
| Default | 00 | 00 | 0000 |

Total loop times= LTA ×256 + LTB.

For example, if LTA=2, LTB=100, the total loop times is 256×2+100= 612 times.

For the counting of breathing times, do follow Figure 16 to enable the Auto Breath Mode.

If the loop start from T4,

T4->T1->T2->T3(1)->T4->T1->T2->T3(2)->T4->T1->... and so on.

If the loop not start from T4,

Tx->T3(1) ->T4->T1->T2->T3(2)->T4-> T1->... and so on.

If the loop ends at off state (End of T3), the LED will be off state at last. If the loop ends at on state (End of T1), the LED will run an extra T4&T1, which are not included in loop.

LE Loop End Time
 00 Loop end at off state (End of T3)
 01 Loop end at on state (End of T1)
 Others Unavailable

LB Loop Beginning Time
 00 Loop begin from T1
 01 Loop begin from T2
 10 Loop begin from T3
 11 Loop begin from T4

LTA 8-11 Bits Of Loop Times
 0000 Endless loop
 0001 1
 0010 2

 1111 15

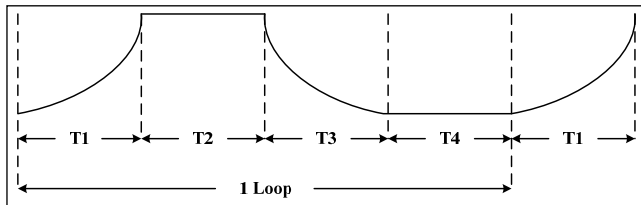


Figure 13 Auto Breathing Function

Table 18 05h, 09h, 0Dh Auto Breath Control Register 4 of ABM-x

| Bit | D7:D0 |
|---------|-----------|
| Name | LTB |
| Default | 0000 0000 |

Total loop times= LTA ×256 + LTB.

For example, if LTA=2, LTB=100, the total loop times is 256×2+100= 612 times.

LTB 0-7 Bits Of Loop Times
 0000 0000 Endless loop
 0000 0001 1
 0000 0010 2

 1111 1111 255

0Eh Time Update Register (02h~0Dh)

The data sent to the time registers (02h~0Dh) will be stored in temporary registers. A write operation of “0000 0000” data to the Time Update Register is required to update the registers (02h~0Dh). Please follow Figure 16 to enable the Auto Breath mode and update the time parameters.

Table 19 0Fh SWy Pull-Up Resistor Selection Register

| Bit | D7:D3 | D2:D0 |
|---------|-------|-------|
| Name | - | PUR |
| Default | 00000 | 000 |

Set pull-up resistor for SWy.

PUR SWy Pull-up Resistor Selection Bit
 000 No pull-up resistor
 001 0.5kΩ
 010 1.0kΩ
 011 2.0kΩ
 100 4.0kΩ
 101 8.0kΩ
 110 16kΩ
 111 32kΩ

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Table 20 10h CSx Pull-Down Resistor Selection Register

| Bit | D7:D3 | D2:D0 |
|---------|-------|-------|
| Name | - | PDR |
| Default | 00000 | 000 |

Set the pull-down resistor for CSx.

| PDR | CSx Pull-down Resistor Selection Bit |
|------------|--------------------------------------|
| 000 | No pull-down resistor |
| 001 | 0.5kΩ |
| 010 | 1.0kΩ |
| 011 | 2.0kΩ |
| 100 | 4.0kΩ |
| 101 | 8.0kΩ |
| 110 | 16kΩ |
| 111 | 32kΩ |

11h Reset Register

Once user read the Reset Register, IS32FL3738 will reset all the IS32FL3738 registers to their default value. On initial power-up, the IS32FL3738 registers are reset to their default values for a blank display.

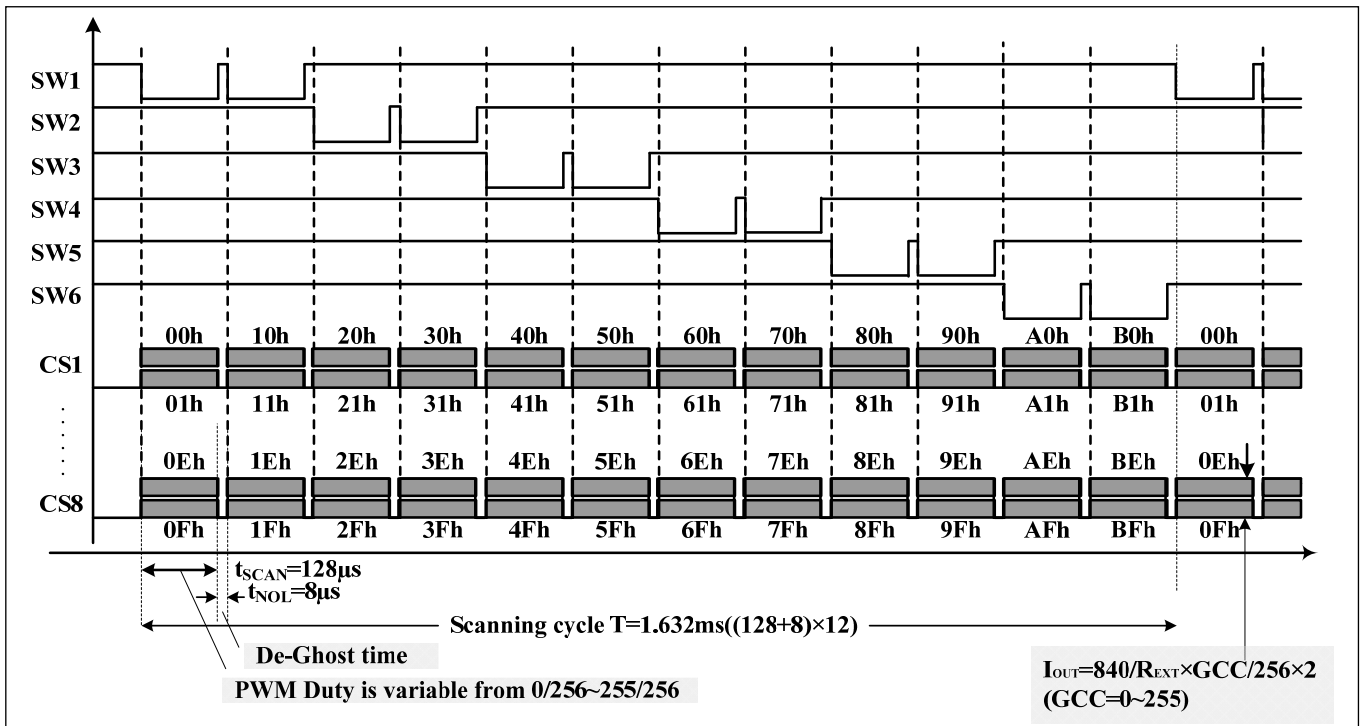


Figure 14 Scanning Timing

SCANNING TIMING

As shown in Figure 12, the SW1~SW6 is turned on by serial, LED is driven 8 by 8 within the SWy (x=1~6) on time (SWy, y=1~6) is sink and pull low when LED on), including the non-overlap blanking time during scan, the duty cycle of SWy (active low, y=1~6) is:

$$Duty = \frac{128\mu s}{(128\mu s + 8\mu s)} \times \frac{1}{6} \times \frac{1}{2} = \frac{1}{12.75} \quad (2)$$

Where 128μs is t_{SCAN} , the period of scanning and 8μs is t_{NOL} , the non-overlap time.

EXTERNAL RESISTOR (R_{EXT})

The output current for each CSx can be set by a single external resistor, R_{EXT} , as described in Formula (3).

$$I_{OUT} = \frac{840}{R_{EXT}} \times \frac{GCC}{256} \times 2 \quad (3)$$

GCC is Global Current Control Register (PG3, 01h) data showing in Table 14.

PWM CONTROL

After setting the I_{OUT} and GCC, the brightness of each LEDs (LED average current (I_{LED})) can be modulated with 512 steps by PWM Register, as described in Formula (1).

$$I_{LED} = \frac{\sum PWM}{512} \times I_{OUT} \times Duty \quad (1)$$

Where PWM is PWM Registers (PG1, 00h~BFh) data showing in Table 10.

For example, in Figure 1, 00h=0xff, 01h=0xff, 10h=0xff, 11h=0xff, GCC=255. R_{EXT} =20kΩ (I_{OUT} =84mA),

$$I_{LED-1A} = \frac{0xff + 0xff + 0xff + 0xff}{512} \times I_{OUT} \times \frac{1}{12.75} = 13.13mA$$

For example 2:

In Figure 1, 00h=0x80, 01h=0x80, 10h=0x80, 11h=0x00, GCC=255. R_{EXT} =20kΩ (I_{OUT} =84mA),

$$I_{LED-1A} = \frac{0x80 + 0x80 + 0x80 + 0x00}{512} \times I_{OUT} \times \frac{1}{12.75} = 4.94mA$$

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

LED AVERAGE CURRENT (I_{LED})

As described in Formula (1), the LED average current (I_{LED}) is effected by 3 factors:

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1. R_{EXT} , resistor which is connected RSET pin and GND. R_{EXT} sets the current of all CSx(x=1~8) based on Formula (3).
2. Global Current Control Register (PG3, 01h). This register adjusts all CSx (x=1~8) output currents by 256 steps as shown in Formula (3).
3. PWM Registers (PG1, 00h~BFh), every LED has an own PWM register. PWM Registers adjust individual LED average current by 512 steps as shown in Formula (1).

GAMMA CORRECTION

In order to perform a better visual LED breathing effect we recommend using a gamma corrected PWM value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting, but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS32FL3738 can modulate the brightness of the LEDs with 512 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

Table 21 32 Gamma Steps with 256 PWM Steps

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| C(0) | C(1) | C(2) | C(3) | C(4) | C(5) | C(6) | C(7) |
| 0 | 1 | 2 | 4 | 6 | 10 | 13 | 18 |
| C(8) | C(9) | C(10) | C(11) | C(12) | C(13) | C(14) | C(15) |
| 22 | 28 | 33 | 39 | 46 | 53 | 61 | 69 |
| C(16) | C(17) | C(18) | C(19) | C(20) | C(21) | C(22) | C(23) |
| 78 | 86 | 96 | 106 | 116 | 126 | 138 | 149 |
| C(24) | C(25) | C(26) | C(27) | C(28) | C(29) | C(30) | C(31) |
| 161 | 173 | 186 | 199 | 212 | 226 | 240 | 255 |

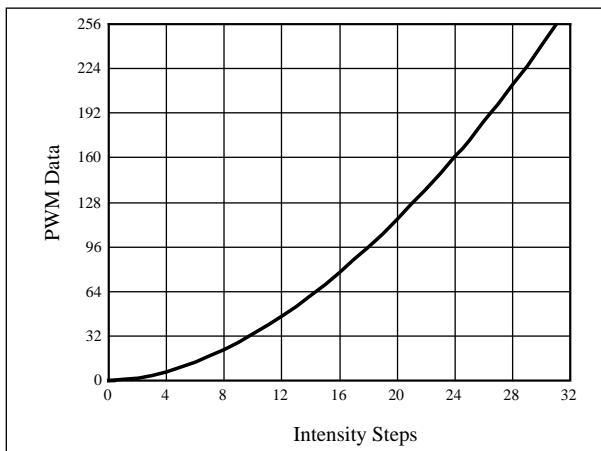


Figure 15 Gamma Correction (32 Steps)

Choosing more gamma steps provides for a more continuous looking breathing effect. This is useful for very long breathing cycles. The recommended

configuration is defined by the breath cycle T. When T=1s, choose 32 gamma steps, when T=2s, choose 64 gamma steps. The user must decide the final number of gamma steps not only by the LED itself, but also based on the visual performance of the finished product.

Table 22 64 Gamma Steps with 256 PWM Steps

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| C(0) | C(1) | C(2) | C(3) | C(4) | C(5) | C(6) | C(7) |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| C(8) | C(9) | C(10) | C(11) | C(12) | C(13) | C(14) | C(15) |
| 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 |
| C(16) | C(17) | C(18) | C(19) | C(20) | C(21) | C(22) | C(23) |
| 24 | 26 | 29 | 32 | 35 | 38 | 41 | 44 |
| C(24) | C(25) | C(26) | C(27) | C(28) | C(29) | C(30) | C(31) |
| 47 | 50 | 53 | 57 | 61 | 65 | 69 | 73 |
| C(32) | C(33) | C(34) | C(35) | C(36) | C(37) | C(38) | C(39) |
| 77 | 81 | 85 | 89 | 94 | 99 | 104 | 109 |
| C(40) | C(41) | C(42) | C(43) | C(44) | C(45) | C(46) | C(47) |
| 114 | 119 | 124 | 129 | 134 | 140 | 146 | 152 |
| C(48) | C(49) | C(50) | C(51) | C(52) | C(53) | C(54) | C(55) |
| 158 | 164 | 170 | 176 | 182 | 188 | 195 | 202 |
| C(56) | C(57) | C(58) | C(59) | C(60) | C(61) | C(62) | C(63) |
| 209 | 216 | 223 | 230 | 237 | 244 | 251 | 255 |

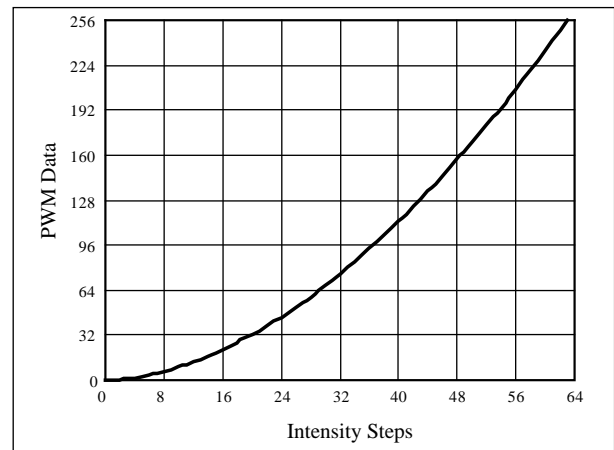


Figure 16 Gamma Correction (64 Steps)

Note: The data of 32 gamma steps is the standard value and the data of 64 gamma steps is the recommended value.

OPERATING MODE

Each dot of IS32FL3738 has two selectable operating modes, PWM Mode and Auto Breath Mode.

PWM Mode

By setting the Auto Breath Mode Register bits of the Page 2 (PG2, 00h~BFh) to "00", or disable the B_EN bit of Configure Register (PG3, 00h), the IS32FL3738 operates in PWM Mode. The brightness of each LED can be modulated with 512 steps by PWM registers. For example, if the data in PWM Register is "0000 0100", then the PWM is the fourth step.

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Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

Auto Breath Mode

By setting the B_EN bit of the Configuration Register (PG3, 00h) to "1", breath function enables. When set the B_EN bit to "0", breath function disables.

By setting the Auto Breath Mode Register bits of the Page 2 (PG2, 00h~BFh) to "01" (ABM-1), "10" (ABM-2) or "11" (ABM-3), the IS32FL3738 operates in Auto Breath Mode.

IS32FL3738 has three auto breath modes, Auto Breath Mode 1, Auto Breath Mode 2 and Auto Breath Mode 3. Each ABM has T1, T2, T3 and T4, as shown below:

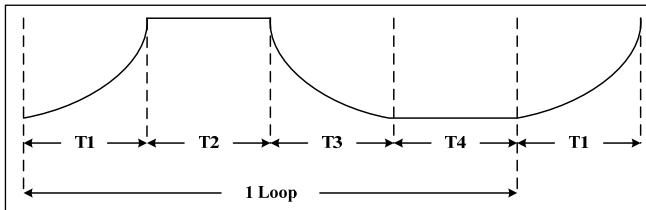


Figure 17 Auto Breathing Function

T1/T3 is variable from 0.21s to 26.88s, T2/T4 is variable from 0s to 26.88s, for each loop, the start point can be T1~T4 and the stop point can be on state (T2) and off state (T4), also the loop time can be set to 1~2¹² times or endless. Each LED can select ABM-1~ABM-3 to work.

The setting of ABM-1~ABM-3 (PG2, 02h~0Dh) need to write the 0Eh in PG3 to update before effective.

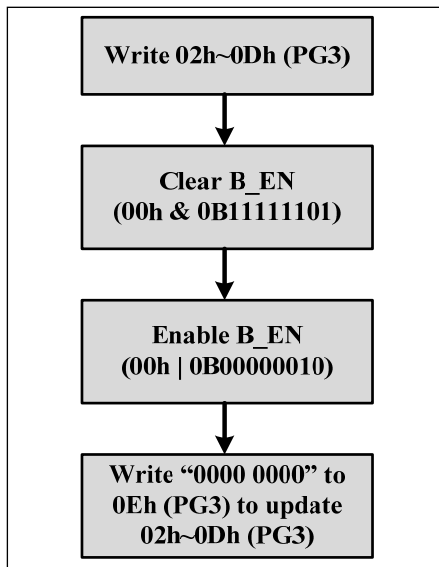


Figure 18 Enable Auto Breath mode

If not follow this flow, first loop's start point may be wrong

OPEN/SHORT DETECT FUNCTION

IS32FL3738 has open and short detect bit for each LED.

By setting the OSD bit of the Configuration Register (PG3, 00h) from "0" to "1", the LED Open Register and LED Short Register will start to store the open/short information and after at least 2 scanning cycle (3.264ms) the MCU can get the open/short information by reading the 18h~2fh/30h~47h, for those dots are turned off via LED On/Off Registers (PG0, 00h~17h), the open/short data will not get refreshed when setting the OSD bit of the Configuration Register (PG3, 00h) from "0" to "1".

The Global Current Control Register (PG3, 01h) need to set to 0x01 in order to get the right open/short data.

The detect action is one-off event and each time before reading out the open/short information, the OSD bit of the Configuration Register (PG3, 00h) need to be set from "0" to "1" (clear before set operation).

INTERRUPT CONTROL

IS32FL3738 has an INTB pin, by setting the Interrupt Mask Register (F0h), it can be the flag of LED open, LED short or the finish flag of ABM-1, ABM-2, and ABM-3.

For example, if the IO bit of the Interrupt Mask Register (F0h) set to "1", when LED open happens, the INTB will pull be pulled low and the OB bit of Interrupt Status Register (F1h) will store open status at the same time.

The INTB pin will be pulled high after reading the Interrupt Status Register (F1h) operation or it will be pulled high automatically after it stays low for 8ms (Typ.) if the IAC bit of Interrupt Mask Register (F0h) is set to "1". The bits of Interrupt Status Register (F1h) will be reset to "0" after INTB pin pulled high.

SYNCHRONIZE FUNCTION

SYNC bits of the Configuration Register (PG3, 00h) sets SYNC pin input or output synchronize clock signal. It is used for more than one part working synchronize. When SYNC bits are set to "01", SYNC pin output synchronize clock to synchronize other parts as master. When SYNC bits are set to "10", SYNC pin input synchronize clock and work synchronization with this input signal as slave. When SYNC bits are set to "00/11", SYNC pin is high impedance, and synchronize function is disabled. SYNC bit default state is "00" and SYNC pin is high impedance when power up.

DE-GHOST FUNCTION

The 'ghost' term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. A ghosting effect typically can occur when multiplexing LEDs. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

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To prevent this LED ghost effect, the IS32FL3738 has integrated pull-up resistors for each SWy (y=1~6) and pull-down resistors for each CSx (x=1~8). Select the right SWy pull-up resistor (PG3, 0Fh) and CSx pull-down resistor (PG3, 10h) which eliminates the ghost LED for a particular matrix layout configuration.

Typically, selecting the 32k Ω will be sufficient to eliminate the LED ghost phenomenon.

The SWy pull-up resistors and CSx pull-down resistors are active only when the CSx/SWy outputs are in the OFF state and therefore no power is lost through these resistors

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Configuration Register (PG3, 00h) to "0", the IS32FL3738 will operate in software shutdown mode. When the IS32FL3738 is in software shutdown, all current sources are switched off, so that the matrix is blanked. All registers can be operated. Typical current consume is 3 μ A.

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown, typical the current consume is 3 μ A.

The chip releases hardware shutdown when the SDB pin is pulled high. During hardware shutdown state Function Register can be operated.

If V_{CC} has risk drop below 1.75V but above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

LAYOUT

As described in external resistor (R_{EXT}), the chip consumes lots of power. Please consider below factors when layout the PCB.

1. The V_{CC} (PVCC, AVCC, VIO) capacitors need to close to the chip and the ground side should well connected to the GND of the chip.
2. R_{EXT} should be close to the chip and the ground side should well connect to the GND of the chip.
3. The thermal pad should connect to ground pins and the PCB should have the thermal pad too, usually this pad should have some via thru the PCB to other side's ground area to help radiate the heat. About the thermal pad size, please refer to the land pattern of each package.
4. The CSx pins maximum current is 84mA ($R_{EXT}=20k\Omega$), and the SWy pins maximum current is 672mA ($R_{EXT}=20k\Omega$), the width of the trace, SWy should have wider trace than CSx.
5. In the middle of SDA and SCL trace, a ground line is recommended to avoid the effect between these two lines.

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CLASSIFICATION REFLOW PROFILES

| Profile Feature | Pb-Free Assembly |
|---|----------------------------------|
| Preheat & Soak Temperature min (T _{sm}) Temperature max (T _{sm}) Time (T _{sm} to T _{sm}) (t _s) | 150°C 200°C 60-120 seconds |
| Average ramp-up rate (T _{sm} to T _p) | 3°C/second max. |
| Liquidous temperature (T _L) Time at liquidous (t _L) | 217°C 60-150 seconds |
| Peak package body temperature (T _p)* | Max 260°C |
| Time (t _p)** within 5°C of the specified classification temperature (T _c) | Max 30 seconds |
| Average ramp-down rate (T _p to T _{sm}) | 6°C/second max. |
| Time 25°C to peak temperature | 8 minutes max. |

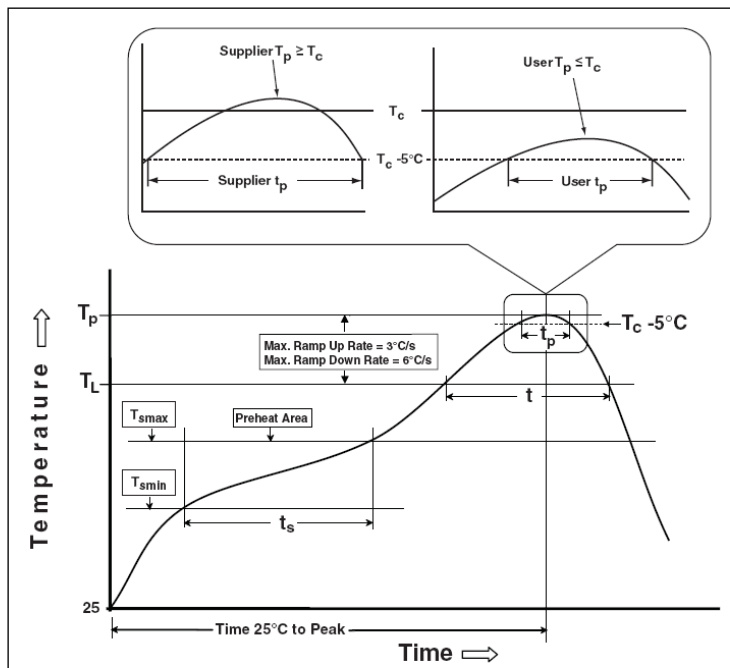
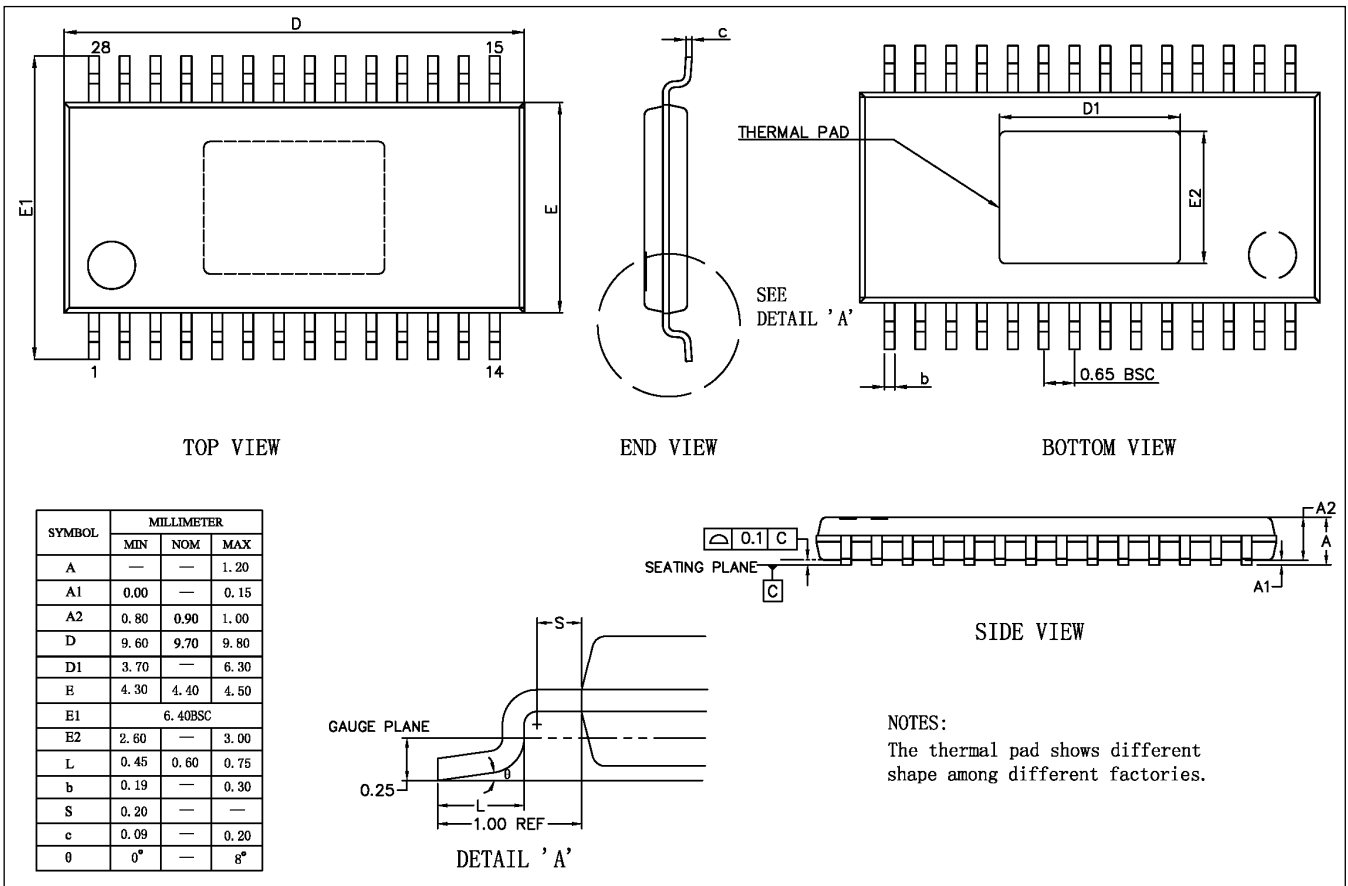


Figure 19 Classification Profile

IS32FL3738

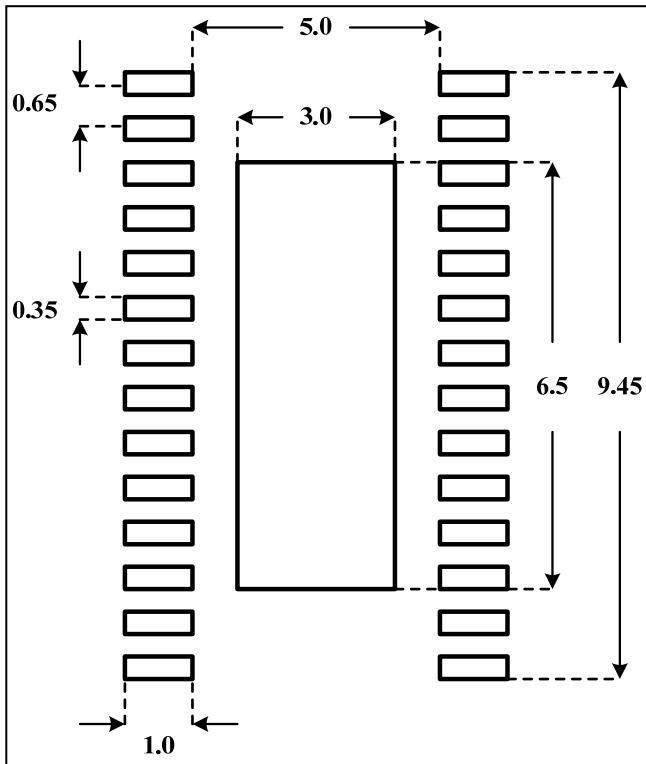
PACKAGE INFORMATION

eTSSOP-28



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RECOMMENDED LAND PATTERN



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.



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REVISION HISTORY

| Revision | Detail Information | Date |
|----------|---|------------|
| 0A | Initial release | 2016.06.28 |
| 0B | <ol style="list-style-type: none">1. Change the PWM 1024 level to 512 level, update Table 10 detail description and Formula (1)2. Update I2C READING OPERATIOON section and Figure 83. Correct some mistakes in REGISTER DEFINITION-2 table4. Update ESD value | 2017.01.18 |