SiI5293ANU Product Family Qualification Summary

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Dear Customer,

Enclosed is Lattice (Silicon Image) Semiconductor's SiI5293ANU Product Qualification Summary Report.

This report was created to assist you in the decision making process of selecting and using our products. The information contained in this report represents the entire qualification effort for this device family.

The information is drawn from an extensive qualification program of the wafer technology and packaging assembly processes used to manufacture our products. The program adheres to JEDEC Industry standards for qualification of the technology and device packaging. This program ensures you only receive product that meets the most demanding requirements for Quality and Reliability.

Your feedback is valuable to Lattice (Silicon Image). If you have suggestions to improve this report, or the data included, we encourage you to contact your Lattice (Silicon Image) representative.

Sincerely,

James M. Orr
Vice President,
Corporate Quality
Lattice Semiconductor Corporation

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INTRODUCTION

The Silicon Image SiI5293 device is the first automotive grade combined MHL/HDMI Receiver that supports Mobile High-Definition Link (MHL®), standard High Definition Multimedia Interface (HDMI™) and Silicon Image Auto-Link Technology (SALT).

The SiI5293 receiver can receive MHL/HDMI/SALT video input up to 1080p60 and 3D 1080p30. Efficient color space conversion receives RGB or YCbCr video data and sends either standard-definition or high-definition RGB or YCbCr formats.

The Silicon Image MHL® technology carries formatted video and audio from compatible transmitters, using only three signal lines, power, and ground (five pins total) compared to the 19 pins required for the standard HDMI™. The SALT™ uses two pairs of differential lines to transfer video, audio and CBUS commands. It does not support power supply compared to MHL.

The SiI5293 receiver is preprogrammed with High-bandwidth Digital Content Protection (HDCP) Keys and contains an integrated HDCP decryption engine for receiving protected audio and video content.
The MHL/HDMI/SALT core of the SiI5293 device uses the latest generation Transition Minimized Differential Signaling (TMDS™) core technology. With this solution, it facilitates automobile's display to support MHL and HDMI together. The SALT also can be used as interconnection between armrest interface cluster and head unit.

Features:

- MHL/HDMI/SALT/DVI-compatible input port
- Supports Consumer Electronics Control (CEC) interface for HDMI input
- The TMDS™ core runs at 25 MHz – 225 MHz
- Dynamic cable equalization automatically detects the equalization required for the incoming signal
- Supports all resolutions with pixel clock rates ranging from 25 MHz to 75 MHz in 24-bit mode for MHL input
- Supports up to1080p60 and 3D 1080p30 in Packed Pixel mode for MHL input
- Supports HDMI input formats up to 1080p30
- Supports HDMI input with DVI formats up to UXGA
- Supports SALT input/output up to 1080p30
- Supports HDCP decryption
- Low power less than 0.75 w
- AEC – Q100 compliant

LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Lattice Semiconductor's Reliability Monitor Program Procedure (Doc. #SiI-QA-0007). All product qualification plans are generated in conformance with Lattice Semiconductor's (Silicon Image) Qualification Procedure (Doc. # SiI-QA-0007) with failure analysis performed in conformance with Lattice Semiconductor's (Silicon Image) Failure Analysis Procedure (Doc. #SiI-QA-0045). Both documents are referenced in Lattice Semiconductor's (Silicon Image) Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office. Figure1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8D process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

Failure rates in this reliability report are expressed in FITs. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

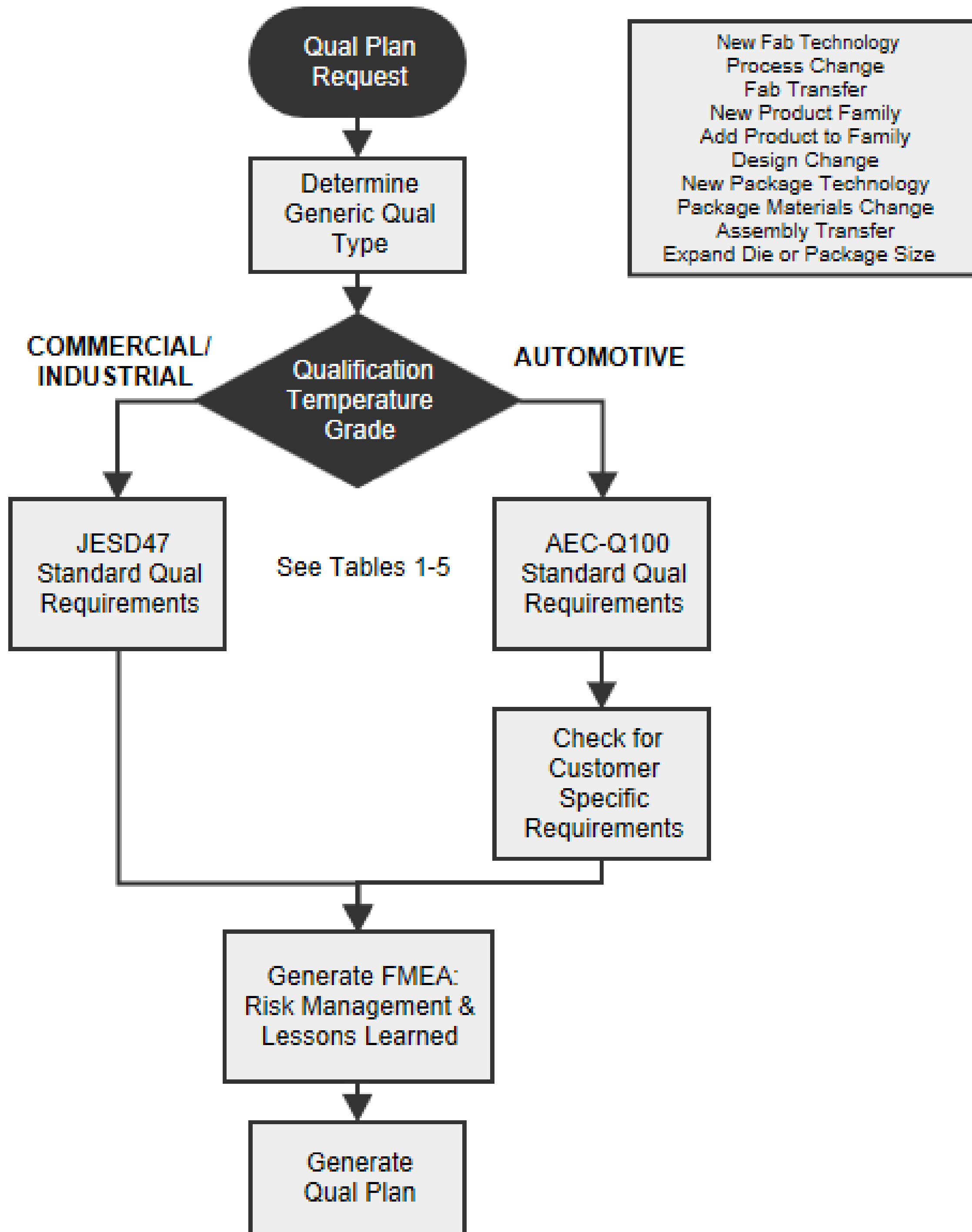
Product families are qualified based upon the requirements outlined in Table#1. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Lattice automotive products are qualified and characterized to the Automotive Electronics Council (AEC) testing requirements and methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice (Silicon Image) Reliability Monitor Report which can be obtained upon request.

Lattice (Silicon Image) Standard Product Qualification Process Flow

This diagram represents the standard qualification flow used by Lattice (Silicon Image) to qualify new Product Families. The target end market for the Product Family determines which flow options are used. The SiI5293ANU Product Family was qualified using the Automotive Option.

Figure1



Standard Qualification Testing

Table#1

TEST	STANDARD	TEST CONDITIONS
High Temperature Operating Life (HTOL)	JESD22-A108	125°C Ambient and max operating supplies
Early Life Failure Rate (ELFR)	AEC Q100-008	125°C Ambient and max operating supplies
Human Body Model ESD (HBM)	AEC-Q100-002	25°C (Technology/Device dependent Performance Targets)
Machine Body Model ESD (MM)	AEC-Q100-003	25°C (Technology/Device dependent Performance Targets)
Charged Device Model ESD (CDM)	AEC-Q100-011	25°C (Technology/Device dependent Performance Targets)
Latch-Up (LU)	AEC-Q100-004	Class II, +/-200mA trigger current and AMR operating supplies

QUALIFICATION DATA FOR SiI5293ANU PRODUCT

Product Family: SiI5293ANU

Packages offered: 72 QFN

Process Technology Fab: TSMC Fab.12

Process Technology Node: 55nm, 1P7M

Wafer Size: 12 inches

Die Size: X: 2.307mm; Y: 2.370mm

Product Life (HTOL) Data

High Temperature Operating Life (HTOL) Test:

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JESD22-A108D "Temperature, Bias, and Operating Life", a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at specified voltages as described in test conditions for each device type.

The Early Life Failure Rate (ELFR) test uses large sample sizes for a short duration (48hrs) HTOL stress to determine the infant mortality rate of a device family.

SiI5293ANU Early Life Results

Early Life Failure Rate Test (ELFR) Conditions:

Stress Duration: 48 hours

Stress Conditions: Max operating supplies, Ambient = 125°C

Method: AEC Q100-008

		48 hrs		
Rev. ID	Lot #	Rej	Qty	Note
0.3	NFU939.06	0	800	
0.3	NFU939.08	0	800	
0.3	NFU939.09	0	800	
		Total	2400	

SiI5293 Early Life Testing Device Hours = 115200
SiI5293 Result / Sample Size = 0 / 2400
SiI5293 PPM Rate = 381.8 (Parts Per Million)

SiI5293 HTOL (48 Hrs) Cumulative Result / Sample Size = 0 / 2400
Test Chip Cumulative Sample Size = 0 / 2400

Life Test (HTOL) Conditions:

Stress Duration: 168, 500, 1000 hours

Stress Conditions: Max operating supplies, Ambient = 125°C

Method: JESD22-A108

SiI5293ANU Product Life Results

		168hrs			500hrs			1000hrs		
Rev. ID	Lot #	Rej	Qty	Note	Rej	Qty	Note	Rej	Qty	Note
0.3	NFU939.06	0	80		0	80		0	80	
0.3	NFU939.08	0	80		0	80		0	80	
0.3	NFU939.09	0	80		0	80		0	80	
0.4	NSW959.2Q	0	80		0	80		0	80	
0.4	NSW959.3Q	0	80		0	80		0	80	
0.4	NSW959.4Q	0	80		0	80		0	80	
	Total	0	480		0	480		0	480	

SiI5293 Cumulative Life Testing Device Hours = 480,000
SiI5293 Result / Sample Size = 0 / 480
SiI5293 FIT Rate = 24.53 FIT
FIT Assumptions: CL=60%, AE=0.7eV, Tjref=55C

SiI5293 HTOL (168 Hrs) Cumulative Result / Sample Size = 0 / 480
SiI5293 HTOL (500 Hrs) Cumulative Result / Sample Size = 0 / 480
SiI5293 HTOL (1000 Hrs) Cumulative Result / Sample Size = 0 / 480
Test Chip Cumulative Sample Size = 0 / 480

ESD and Latch Up Data

Electrostatic Discharge-Human Body Model:

The SiI5293ANUproduct was tested per JESD22-A114F Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure.

All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

SiI5293ANU ESD-HBM Data

Rev. ID	Lot #	Test Result
0.3	NFU939.06	500V
0.4	NSW959.2Q	500V
0.3	NFU939.06	1000V
0.4	NSW959.2Q	1000V
0.3	NFU939.06	1500V

0.4	NSW959.2Q	1500V
0.3	NFU939.06	2000V
0.4	NSW959.2Q	2000V
0.3	NFU939.06	2500V
0.4	NSW959.2Q	2500V
0.3	NFU939.06	3000V
0.4	NSW959.2Q	3000V
0.3	NFU939.06	3500V
0.4	NSW959.2Q	3500V

HBM classification for Commercial/Industrial products, per ESD-HBM per AEC-Q100-002 REV-D, Class H2.
All HBM levels indicated are dual-polarity (±).
HBM worst-case performance is the package with the smallest RLC parasitic.

Electrostatic Discharge-Machine Model:

The SiI5293ANUproduct was tested per JESD22-A115C Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM) procedure.

All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

SiI5293ANU ESD-MM

Rev. ID	Lot #	Results
0.3	NFU939.06	50V
0.4	NSW959.2Q	50V
0.3	NFU939.06	100V
0.4	NSW959.2Q	100V
0.3	NFU939.06	150V
0.4	NSW959.2Q	150V
0.3	NFU939.06	200V
0.4	NSW959.2Q	200V

MM classification for Industrial products, per AEC-Q100-003 REV-E, Class M3.
All MM levels indicated are dual-polarity (±).
MM worst-case performance is the package with the smallest RLC parasitic.

Electrostatic Discharge-Charged Device Model:

The SiI5293ANUproduct family was tested per the JESD22-C101E, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure.

All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

SiI5293ANU ESD CDM

Rev. ID	Lot #	Results
0.3	NFU939.06	250V
0.4	NSW959.4Q	250V
0.3	NFU939.06	500V
0.4	NSW959.4Q	500V
0.3	NFU939.06	750V
0.4	NSW959.4Q	750V
0.3	NFU939.06	1000V
0.4	NSW959.4Q	1000V

CDM classification Industrial products, per AEC-Q100-011 Rev-B; Class C3B.
All CDM levels indicated are dual-polarity (±).
CDM worst-case performance is the package with the largest bulk capacitance.

Latch-Up:

The SiI5293ANUproduct was tested per the AEC-Q100-004 IC Latch-up Test procedure.
All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

SiI5293ANU Latch-up Data

Rev. ID	Lot #	Results
0.3	NFU939.06	200mA
0.4	NSW959.4Q	200mA

I-Test classification for Commercial/Industrial products, per AEC-Q100-004 REV-C, Class II (85°C room ambient).
All I-Test levels indicated are dual-polarity (±).
I-Test worst-case performance is the package with access to the most IOs.

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