MAX15062

60V, 300mA, Ultra-Small, High-Efficiency, Synchronous Step-Down DC-DC Converters

General Description

The MAX15062 high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a 4.5V to 60V input voltage range. The converter delivers output currents up to 300mA at output voltages of 3.3V (MAX15062A) and 5V (MAX15062B). The device operates over the -40°C to +125°C temperature range and is available in a compact 8-pin (2mm x 2mm) TDFN package. Simulation models are available.

The device employs a peak-current-mode control architecture with a MODE pin that can be used to operate the device in pulse-width modulation (PWM) or pulse-frequency modulation (PFM) control schemes. PWM operation provides constant frequency operation at all loads and is useful in applications sensitive to variable switching frequency. PFM operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. The low-resistance on-chip MOSFETs ensure high efficiency at full load and simplify the PCB layout.

To reduce input inrush current, the device offers an internal fixed soft-start. The device also incorporates an EN/UVLO pin that allows the user to turn on the part at the desired input-voltage level. An open-drain $\overline{\text{RESET}}$ pin can be used for output-voltage monitoring.

Applications

- Industrial Sensors and Process Control
- 4–20mA Current-Loop Powered Sensors
- HVAC and Building Control
- Automotive
- Battery-Powered Equipment
- Space-Constrained Applications
- High-Voltage LDO Replacement
- General-Purpose Point-of-Load

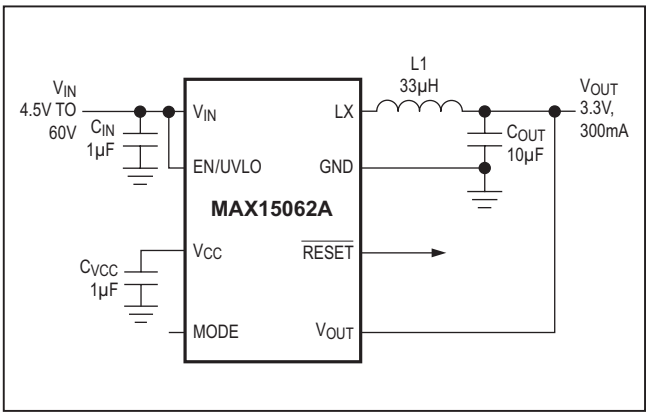
***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX15062.related.

Benefits and Features

- Eliminates External Components and Reduces Total Cost
  - No Schottky—Synchronous Operation for High Efficiency and Reduced Cost
  - Internal Compensation and Feedback Divider
  - Internal Soft-Start
  - All-Ceramic Capacitors, Ultra-Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4.5V to 60V Input Voltage Range
  - Fixed 3.3V and 5V Output Voltages
  - Delivers Up to 300mA
  - Configurable Between PFM and Forced-PWM Modes
- Reduces Power Dissipation
  - Peak Efficiency = 92%
  - PFM Feature for High Light-Load Efficiency
  - Shutdown Current = 2.2µA (typ)
- Operates Reliably in Adverse Industrial Environments
  - Hiccup-Mode Current Limit and Autoretry Startup
  - Built-In Output Voltage Monitoring with Open-Drain $\overline{\text{RESET}}$ Pin
  - Programmable EN/UVLO Threshold
  - Monotonic Startup into Prebiased Output
  - Overtemperature Protection
  - -40°C to +125°C Automotive/Industrial Temperature Range

Typical Operating Circuit



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Absolute Maximum Ratings

V_{IN} to GND ..... -0.3V to 70V
EN/UVLO to GND ..... -0.3V to 70V
LX to GND ..... -0.3V to V_{IN} + 0.3V
V_{CC}, V_{OUT}, $\overline{RESET}$ to GND ..... -0.3V to 6V
MODE to GND ..... -0.3V to V_{CC} + 0.3V
LX total RMS Current ..... ±800mA
Output Short-Circuit Duration ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
8-Pin TDFN (derate 6.2mW/NC above +70°C) 496mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics(Note 1)

TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....+162°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....+20°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 24V, V_{GND} = 0V, C_{IN} = C_{VCC} = 1µF, $V_{EN/UVLO}$ = 1.5V, LX = MODE = $\overline{RESET}$ = unconnected; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (VIN)						
Input Voltage Range	V_{IN}		4.5		60	V
Input Supply Current	I_{IN-SH}	$V_{EN/UVLO}$ = 0V, shutdown mode		2.2	4	µA
	$I_{IN-HIBERNATE}$	MODE = unconnected and V_{OUT} = 1.03 x $V_{OUT-REG}$		95	160	µA
	I_{IN-SW}	Normal switching mode, V_{IN} = 24V		2.5	4	mA
ENABLE/UVLO (EN/UVLO)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.19	1.215	1.24	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.06	1.09	1.15	
	$V_{EN-TRUESD}$	$V_{EN/UVLO}$ falling, true shutdown		0.75		
EN/UVLO Input Leakage Current	$I_{EN/UVLO}$	$V_{EN/UVLO}$ = 60V, T_A = +25°C			100	nA
LDO (V_{CC})						
V_{CC} Output Voltage Range	V_{CC}	6V < V_{IN} < 60V, 0mA < I_{VCC} < 10mA	4.75	5	5.25	V
V_{CC} Current Limit	$I_{VCC-MAX}$	V_{CC} = 4.3V, V_{IN} = 12V	13	30	50	mA
V_{CC} Dropout	V_{CC-DO}	V_{IN} = 4.5V, I_{VCC} = 5mA		0.15	0.3	V
V_{CC} UVLO	V_{CC-UVR}	V_{CC} rising	4.05	4.18	4.3	V
	V_{CC-UVF}	V_{CC} falling	3.7	3.8	3.95	

Electrical Characteristics (continued)

(V_{IN} = 24V, V_{GND} = 0V, C_{IN} = C_{VCC} = 1µF, $V_{EN/UVLO}$ = 1.5V, LX = MODE = $\overline{RESET}$ = unconnected; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER MOSFETs							
High-Side pMOS On-Resistance	R_{DS-ONH}	I_{LX} = 0.3A (sourcing)	T_A = +25°C		1.35	1.75	Ω
			T_A = T_J = +125°C			2.7	
Low-Side nMOS On-Resistance	R_{DS-ONL}	I_{LX} = 0.3A (sinking)	T_A = +25°C		0.45	0.55	Ω
			T_A = T_J = +125°C			0.9	
LX Leakage Current	I_{LX-LKG}	$V_{EN/UVLO}$ = 0V, V_{IN} = 60V, T_A = +25°C, V_{LX} = (V_{GND} + 1V) to (V_{IN} - 1V)		-1		+1	µA
SOFT-START (SS)							
Soft-Start Time	t_{SS}				4.1		ms
FEEDBACK (V_{OUT})							
V_{OUT} Input Bias Current	I_{VOUT}	T_A = +25°C			12	17	µA
OUTPUT VOLTAGE (V_{OUT})							
V_{OUT} Regulation Voltage	$V_{OUT-REG}$	MAX15062A		3.25	3.3	3.35	V
		MAX15062B		4.93	5	5.07	
V_{OUT} Threshold for Entering Hibernate Mode	$V_{OUT-HIBR}$	V_{OUT} rising		101	102.3	103.3	%
V_{OUT} Threshold for Exiting Hibernate Mode	$V_{OUT-HIBF}$	V_{OUT} falling		100	101.1	102.1	
CURRENT LIMIT							
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$			0.49	0.56	0.62	A
Runaway Current-Limit Threshold	$I_{RUNAWAY-LIMIT}$			0.58	0.66	0.73	A
Negative Current-Limit Threshold	$I_{SINK-LIMIT}$	MODE = GND		0.25	0.3	0.35	A
					0.01		mA
PFM Current Level	I_{PFM}				0.13		A
TIMING							
Switching Frequency	f_{SW}	V_{OUT} > $V_{OUT-HICF}$		465	500	535	kHz
Events to Hiccup After Crossing Runaway Current Limit					1		Cycles
V_{OUT} Undervoltage Trip Level to Cause Hiccup	$V_{OUT-HICF}$			62.5	64.5	66.5	%
Hiccup Timeout					131		ms
Minimum On-Time	t_{ON-MIN}				90	130	ns
Maximum Duty Cycle	D_{MAX}	V_{OUT} = 0.98 x $V_{OUT-REG}$		89	91.5	94	%
LX Dead Time					5		ns

Electrical Characteristics (continued)

(V_{IN} = 24V, V_{GND} = 0V, C_{IN} = C_{VCC} = 1µF, $V_{EN/UVLO}$ = 1.5V, LX = MODE = $\overline{RESET}$ = unconnected; T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

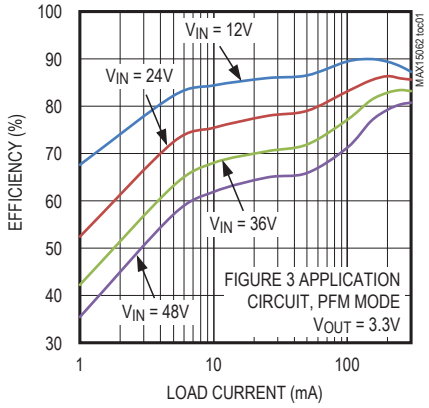
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RESET}$						
V_{OUT} Threshold for $\overline{RESET}$ Rising	$V_{OUT-OKR}$	V_{OUT} rising	94	95.5	97	%
V_{OUT} Threshold for $\overline{RESET}$ Falling	$V_{OUT-OKF}$	V_{OUT} falling	90.5	92	93.5	%
$\overline{RESET}$ Delay After V_{OUT} Reaches 95% Regulation				2		ms
$\overline{RESET}$ Output Level Low		$I_{\overline{RESET}}$ = 5mA			0.2	V
$\overline{RESET}$ Output Leakage Current		V_{OUT} = 1.01 x $V_{OUT-REG}$, T_A = +25°C			0.1	µA
MODE						
MODE Internal Pullup Resistor				500		kΩ
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold		Temperature rising		166		°C
Thermal-Shutdown Hysteresis				10		°C

Note 2: All the limits are 100% tested at T_A = +25°C. Limits over temperature are guaranteed by design.

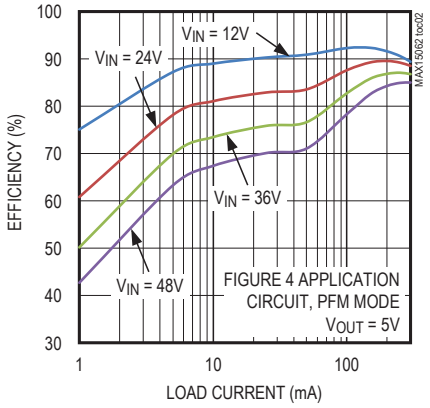
Typical Operating Characteristics

(V_{IN} = 24V, V_{GND} = 0V, C_{IN} = C_{VCC} = 1µF, $V_{EN/UVLO}$ = 1.5V, T_A = +25°C, unless otherwise noted.)

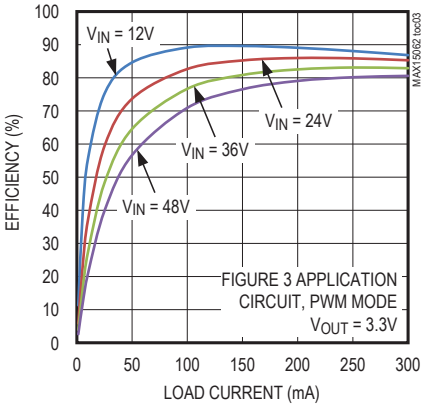
EFFICIENCY vs. LOAD CURRENT



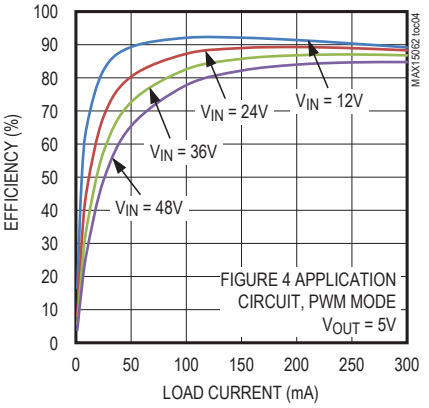
EFFICIENCY vs. LOAD CURRENT



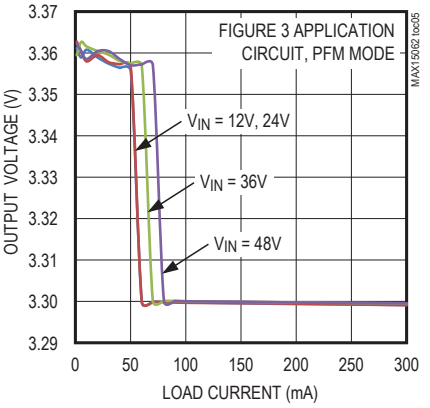
EFFICIENCY vs. LOAD CURRENT



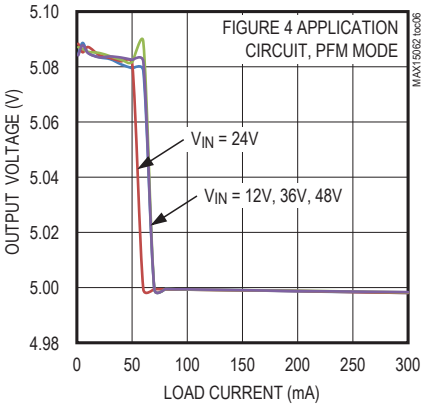
EFFICIENCY vs. LOAD CURRENT



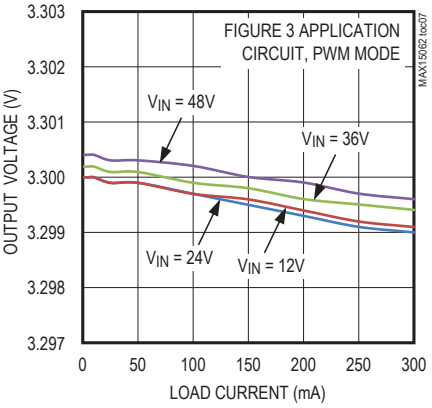
OUTPUT VOLTAGE vs. LOAD CURRENT



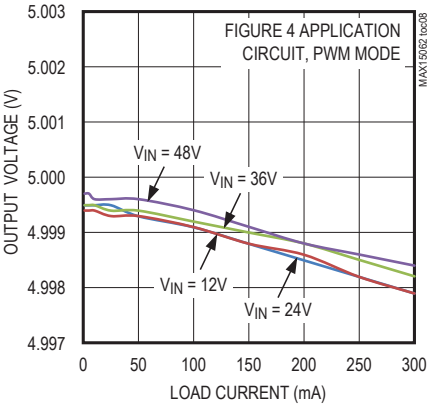
OUTPUT VOLTAGE vs. LOAD CURRENT



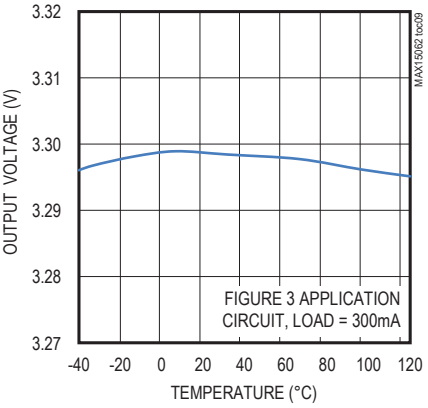
OUTPUT VOLTAGE vs. LOAD CURRENT



OUTPUT VOLTAGE vs. LOAD CURRENT



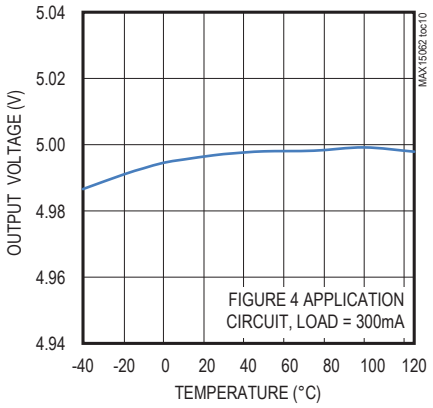
OUTPUT VOLTAGE vs. TEMPERATURE



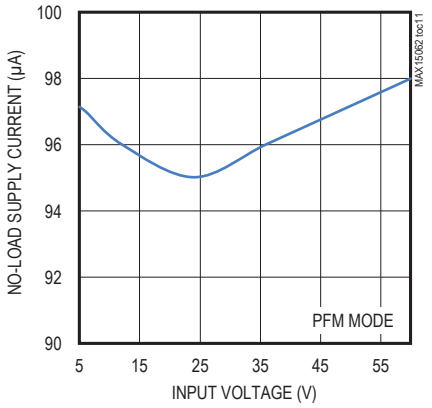
Typical Operating Characteristicsc (continued)

(V_{IN} = 24V, V_{GND} = 0V, C_{IN} = C_{VCC} = 1µF, $V_{EN/UVLO}$ = 1.5V, T_A = +25°C, unless otherwise noted.)

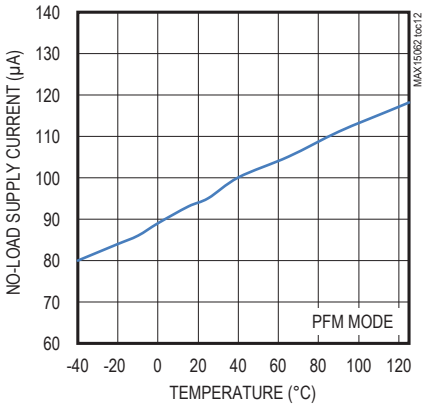
OUTPUT VOLTAGE vs. TEMPERATURE



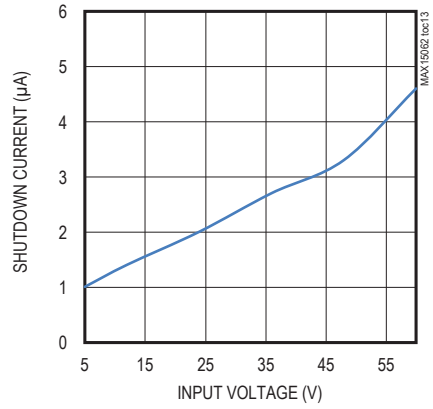
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



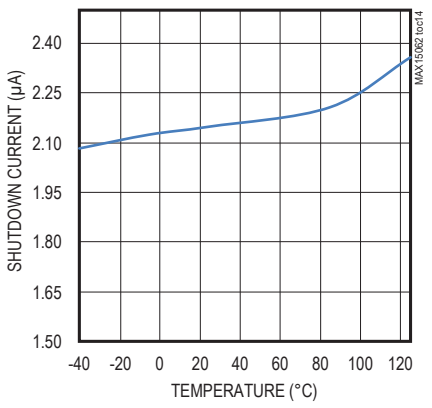
NO-LOAD SUPPLY CURRENT vs. TEMPERATURE



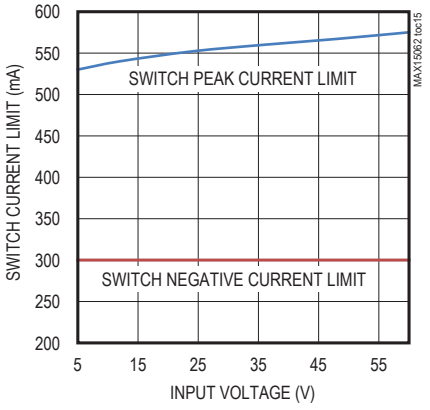
SHUTDOWN CURRENT vs. INPUT VOLTAGE



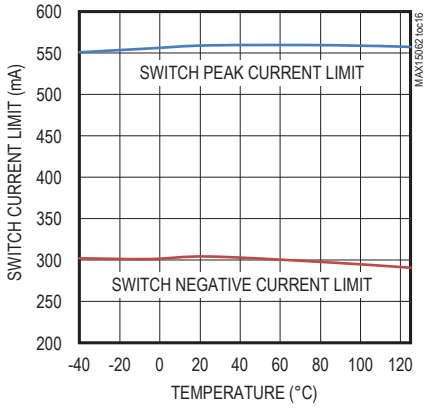
SHUTDOWN CURRENT vs. TEMPERATURE



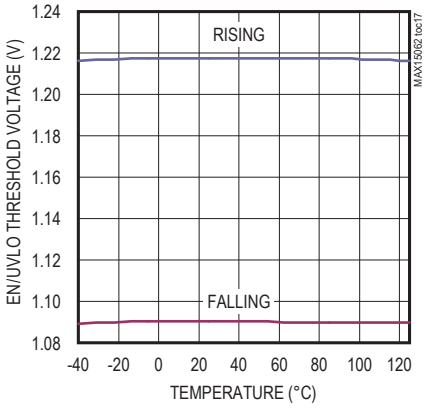
SWITCH CURRENT LIMIT vs. INPUT VOLTAGE



SWITCH CURRENT LIMIT vs. TEMPERATURE



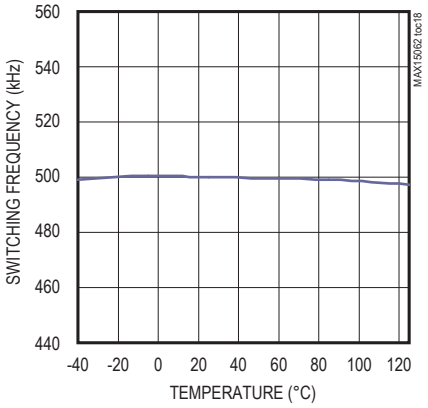
EN/UVLO THRESHOLD vs. TEMPERATURE



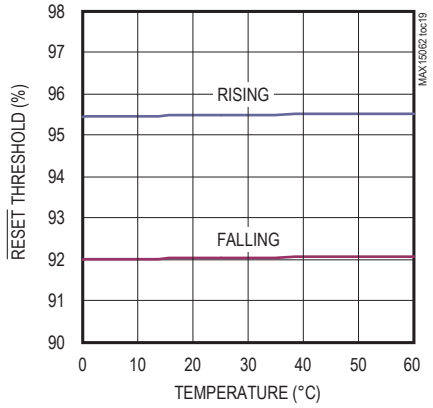
Typical Operating Characteristicsc (continued)

(V_{IN} = 24V, V_{GND} = 0V, C_{IN} = C_{VCC} = 1µF, $V_{EN/UVLO}$ = 1.5V, T_A = +25°C, unless otherwise noted.)

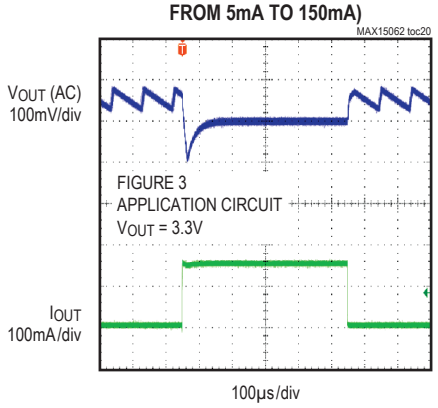
SWITCHING FREQUENCY vs. TEMPERATURE



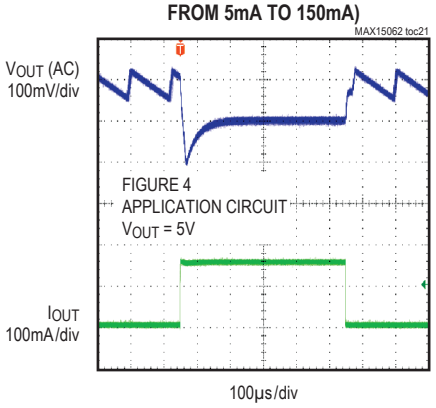
RESET THRESHOLD vs. TEMPERATURE



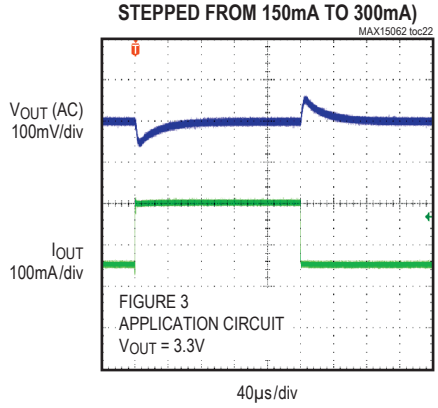
LOAD TRANSIENT RESPONSE, PFM MODE (LOAD CURRENT STEPPED FROM 5mA TO 150mA)



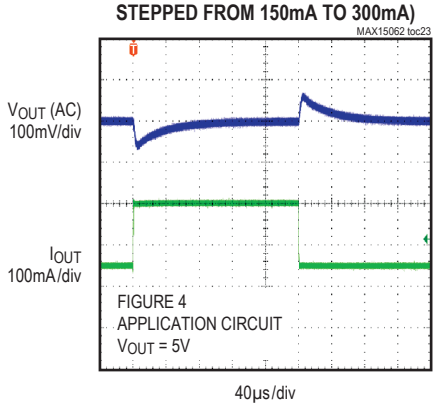
LOAD TRANSIENT RESPONSE, PFM MODE (LOAD CURRENT STEPPED FROM 5mA TO 150mA)



LOAD TRANSIENT RESPONSE, PFM OR PWM MODE (LOAD CURRENT STEPPED FROM 150mA TO 300mA)



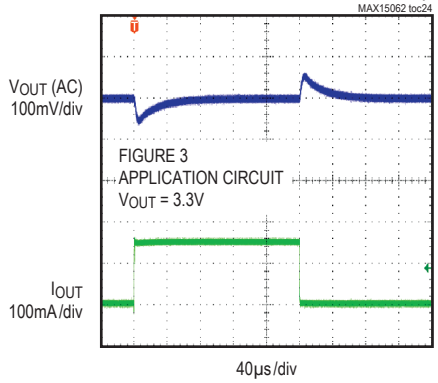
LOAD TRANSIENT RESPONSE, PFM OR PWM MODE (LOAD CURRENT STEPPED FROM 150mA TO 300mA)



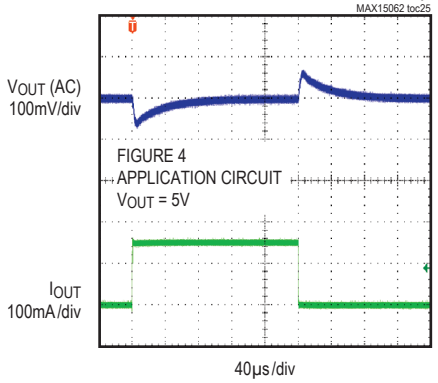
Typical Operating Characteristicsc (continued)

(V_{IN} = 24V, V_{GND} = 0V, C_{IN} = C_{VCC} = 1µF, $V_{EN/UVLO}$ = 1.5V, T_A = +25°C, unless otherwise noted.)

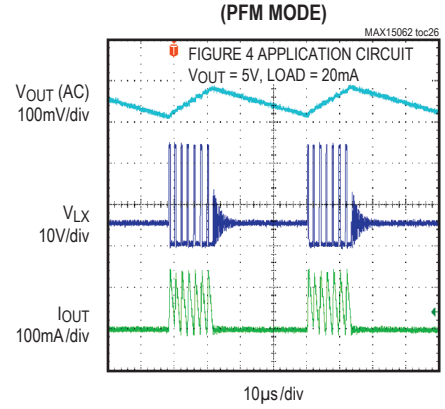
LOAD TRANSIENT RESPONSE, PWM MODE (LOAD CURRENT STEPPED FROM NO LOAD TO 150mA)



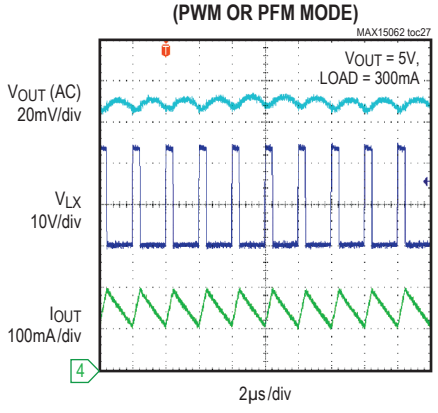
LOAD TRANSIENT RESPONSE, PWM MODE PWM mode (LOAD CURRENT STEPPED FROM NO LOAD TO 150mA)



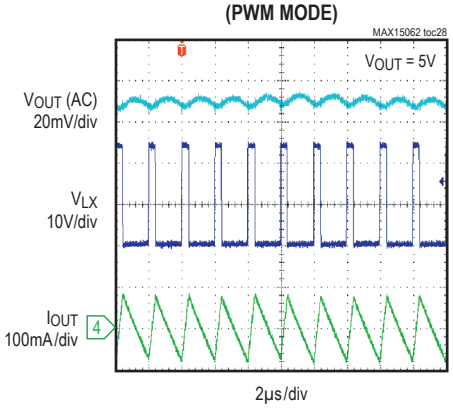
SWITCHING WAVEFORMS (PFM MODE)



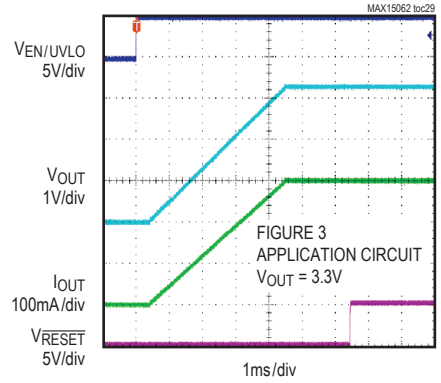
FULL-LOAD SWITCHING WAVEFORMS (PWM OR PFM MODE)



NO-LOAD SWITCHING WAVEFORMS (PWM MODE)



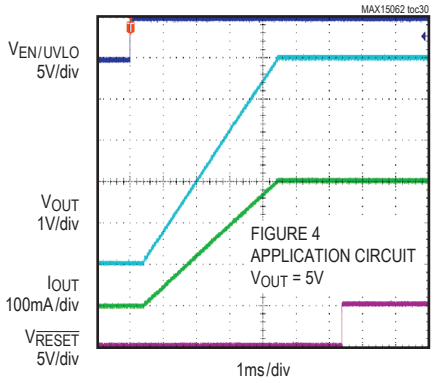
SOFT-START



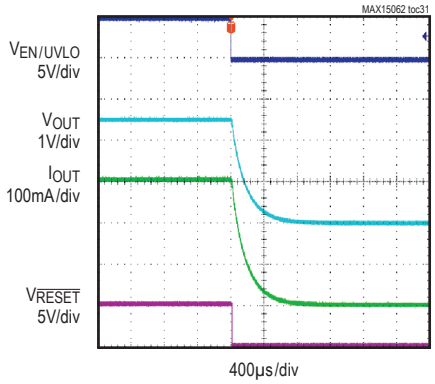
Typical Operating Characteristicsc (continued)

(V_{IN} = 24V, V_{GND} = 0V, C_{IN} = C_{VCC} = 1µF, $V_{EN/UVLO}$ = 1.5V, T_A = +25°C, unless otherwise noted.)

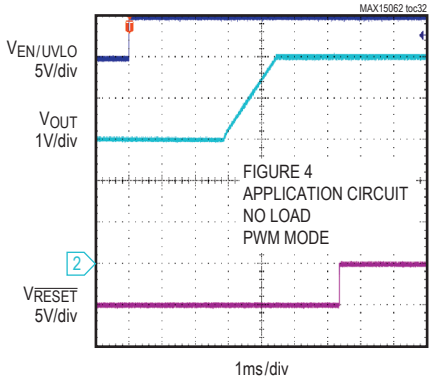
SOFT-START



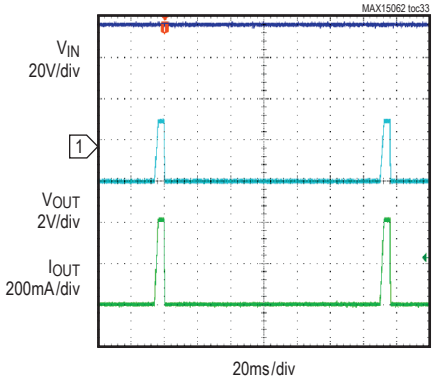
SHUTDOWN WITH ENABLE



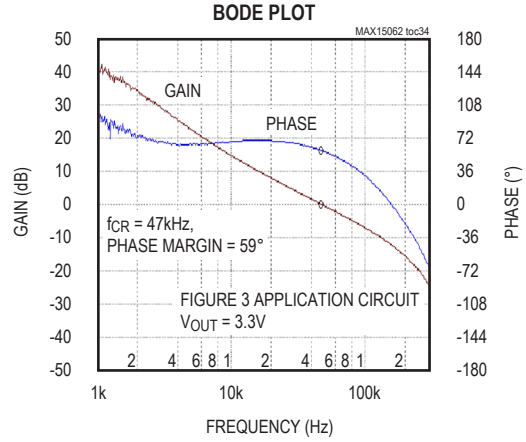
SOFT-START WITH 3V PREBIAS



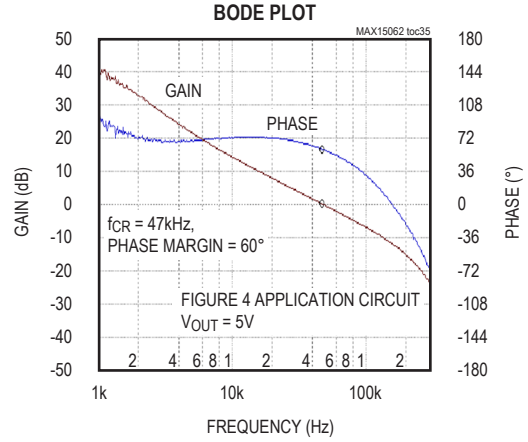
OVERLOAD PROTECTION



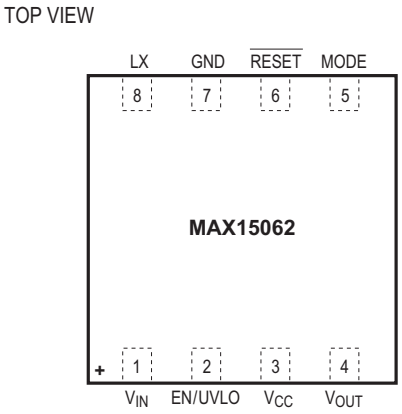
BODE PLOT



BODE PLOT



Pin Configuration

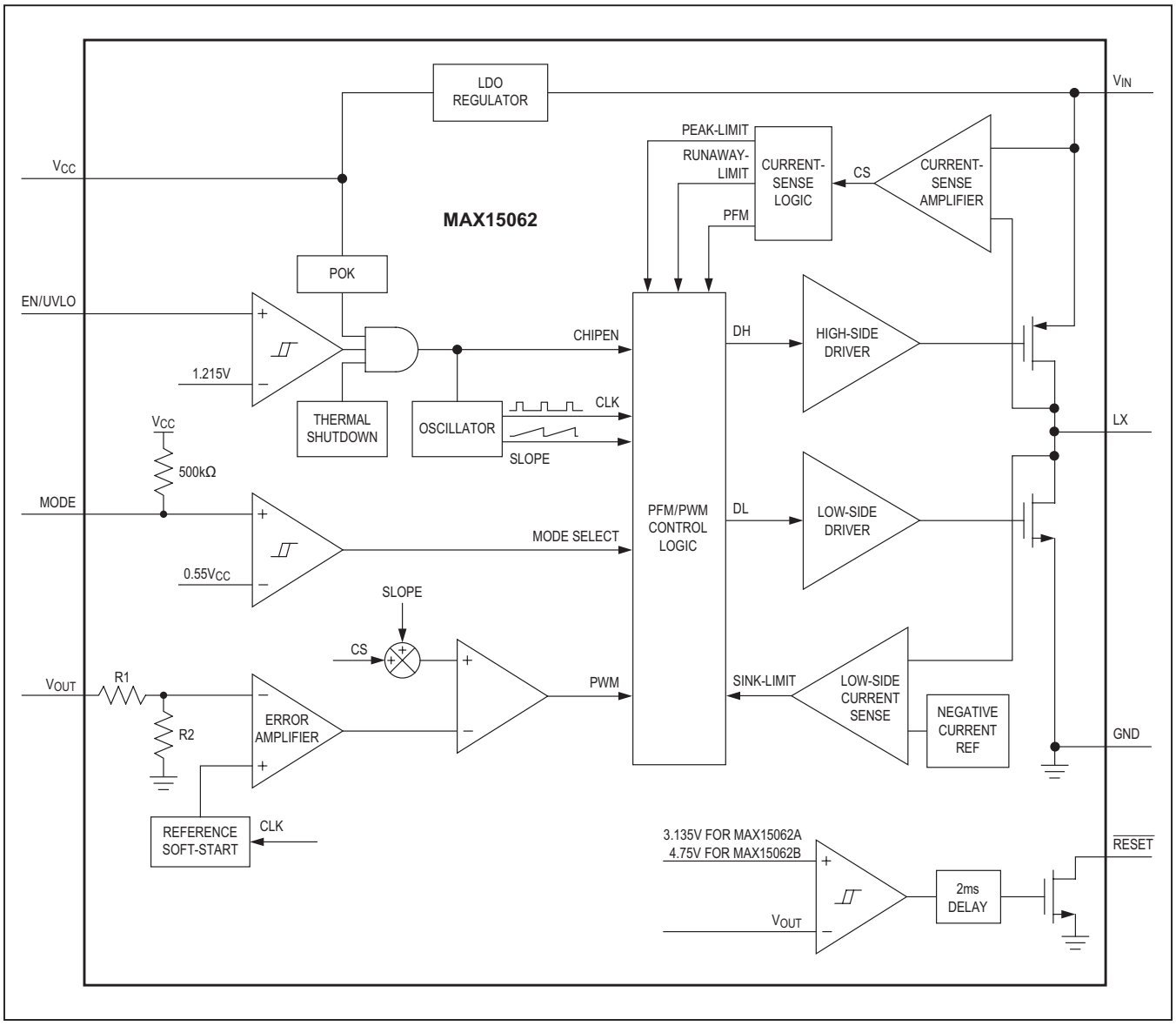


TDFN
(2mm x 2mm)

Pin Description

PIN	NAME	FUNCTION
1	V_{IN}	Switching Regulator Power Input. Connect a X7R 1µF ceramic capacitor from V_{IN} to GND for bypassing.
2	EN/UVLO	Active-High, Enable/Undervoltage-Detection Input. Pull EN/UVLO to GND to disable the regulator output. Connect EN/UVLO to V_{IN} for always-on operation. Connect a resistor-divider between V_{IN} and EN/UVLO to GND to program the input voltage at which the device is enabled and turns on.
3	V_{CC}	Internal LDO Power Output. Bypass V_{CC} to GND with a minimum 1µF capacitor.
4	V_{OUT}	Feedback Power Input. Connect V_{OUT} directly to the output.
5	MODE	PFM/PWM Mode Selection Input. Connect MODE to GND to enable the fixed-frequency PWM operation. Leave unconnected for light-load PFM operation.
6	$\overline{RESET}$	Open-Drain Reset Output. Pull up $\overline{RESET}$ to an external power supply with an external resistor. $\overline{RESET}$ goes low when V_{OUT} voltage drops below 92% of the set nominal regulated voltage. $\overline{RESET}$ goes high 2ms after the output voltage rises above 95% of its regulation value. See the *Electrical Characteristics* table for threshold values.
7	GND	Ground. Connect GND to the power ground plane. Connect all the circuit ground connections together at a single point. See the *PCB Layout Guidelines* section.
8	LX	Inductor Connection. Connect LX to the switched side of the inductor. LX is high impedance when the device is in shutdown.

Block Diagram



Detailed Description

The MAX15062 high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a wide 4.5V to 60V input voltage range. The converter delivers output currents up to 300mA at output voltages of 3.3V (MAX15062A) and 5V (MAX15062B). When EN/UVLO and V_{CC} UVLO are satisfied, an internal power-up sequence soft-starts the error-amplifier reference, resulting in a clean monotonic output-voltage soft-start independent of the load current. The V_{OUT} pin monitors the output voltage through an internal resistor-divider. $\overline{RESET}$ transitions to a high-impedance state 2ms after the output voltage reaches 95% of regulation. The device selects either PFM or forced-PWM mode depending on the state of the MODE pin at power-up. By pulling the EN/UVLO pin to low, the device enters the shutdown mode and consumes only 2.2µA (typ) of standby current.

DC-DC Switching Regulator

The device uses an internally compensated, fixed-frequency, current-mode control scheme (see the *Block Diagram*). On the rising edge of an internal clock, the high-side pMOSFET turns on. An internal error amplifier compares the feedback voltage to a fixed internal reference voltage and generates an error voltage. The error voltage is compared to a sum of the current-sense voltage and a slope-compensation voltage by a PWM comparator to set the on-time. During the on-time of the pMOSFET, the inductor current ramps up. For the remainder of the switching period (off-time), the pMOSFET is kept off and the low-side nMOSFET turns on. During the off-time, the inductor releases the stored energy as the inductor current ramps down, providing current to the output. Under overload conditions, the cycle-by-cycle current-limit feature limits the inductor peak current by turning off the high-side pMOSFET and turning on the low-side nMOSFET.

Mode Selection (MODE)

The logic state of the MODE pin is latched after V_{CC} and EN/UVLO voltages exceed respective UVLO rising thresholds and all internal voltages are ready to allow LX switching. If the MODE pin is unconnected at power-up, the part operates in PFM mode at light loads. If the MODE pin is grounded at power-up, the part operates in constant-frequency PWM mode at all loads. State changes on the MODE pin are ignored during normal operation.

PWM Mode Operation

In PWM mode, the inductor current is allowed to go negative. PWM operation is useful in frequency sensitive applications and provides fixed switching frequency at all loads. However, the PWM mode of operation gives lower efficiency at light loads compared to PFM mode of operation.

PFM Mode Operation

PFM mode operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak of 130mA every clock cycle until the output rises to 102.3% of the nominal voltage. Once the output reaches 102.3% of the nominal voltage, both high-side and low-side FETs are turned off and the part enters hibernate operation until the load discharges the output to 101.1% of the nominal voltage. Most of the internal blocks are turned off in hibernate operation to save quiescent current. After the output falls below 101.1% of the nominal voltage, the device comes out of hibernate operation, turns on all internal blocks, and again commences the process of delivering pulses of energy to the output until it reaches 102.3% of the nominal output voltage. The advantage of the PFM mode is higher efficiency at light loads because of lower quiescent current drawn from supply.

Internal 5V Linear Regulator

An internal regulator provides a 5V nominal supply to power the internal functions and to drive the power MOSFETs. The output of the linear regulator (V_{CC}) should be bypassed with a 1µF capacitor to GND. The V_{CC} regulator dropout voltage is typically 150mV. An undervoltage-lockout circuit that disables the regulator when V_{CC} falls below 3.8V (typ). The 400mV V_{CC} UVLO hysteresis prevents chattering on power-up and power-down.

Enable Input (EN/UVLO), Soft-Start

When EN/UVLO voltage is above 1.21V (typ), the device's internal error-amplifier reference voltage starts to ramp up. The duration of the soft-start ramp is 4.1ms, allowing a smooth increase of the output voltage. Driving EN/UVLO low disables both power MOSFETs, as well as other internal circuitry, and reduces V_{IN} quiescent current to below 2.2µA. EN/UVLO can be used as an input-voltage UVLO adjustment input. An external voltage-divider between V_{IN} and EN/UVLO to GND adjusts the input voltage at which the device turns on or turns off. If input UVLO programming is not desired, connect EN/UVLO to V_{IN} (see the *Electrical Characteristics* table for EN/UVLO rising and falling threshold voltages).

Reset Output ($\overline{RESET}$)

The device includes an output open-drain $\overline{RESET}$ output to monitor the output voltage. $\overline{RESET}$ goes high 2ms after the output rises above 95% of its nominal set value and pulls low when the output voltage falls below 92% of the set nominal regulated voltage. $\overline{RESET}$ asserts low during the hiccup timeout period.

Startup into a Prebiased Output

The device is capable of soft-start into a prebiased output, without discharging the output capacitor in both the PFM and forced-PWM modes. Such a feature is useful in applications where digital integrated circuits with multiple rails are powered.

Operating Input Voltage Range

The maximum operating input voltage is determined by the minimum controllable on-time and the minimum operating input voltage is determined by the maximum duty cycle and circuit voltage drops. The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{INMIN} = \frac{V_{OUT} + (I_{OUT} \times (R_{DCR} + 0.5))}{D_{MAX}} + (I_{OUT} \times 1.0)$$

$$V_{INMAX} = \frac{V_{OUT}}{t_{ONMIN} \times f_{SW}}$$

where V_{OUT} is the steady-state output voltage, I_{OUT} is the maximum load current, R_{DCR} is the DC resistance of the inductor, f_{SW} is the switching frequency (max), D_{MAX} is maximum duty cycle (0.92), and t_{ONMIN} is the worst-case minimum controllable switch on-time (130ns).

Overcurrent Protection/Hiccup Mode

The device is provided with a robust overcurrent protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit of 0.56A (typ). A runaway current limit on the high-side switch current at 0.66A (typ) protects the device under high input voltage, and short-circuit conditions when there is insufficient output voltage available to restore the inductor current that was built up during the on period of the step-down converter. One occurrence of the runaway current limit triggers a hiccup mode. In addition, if due to a fault condition, output voltage drops to 65% (typ) of its nominal value any time after soft-start is complete, hiccup mode is triggered. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 131ms. Once the hiccup timeout period expires, soft-start is attempted again. Hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

Thermal Overload Protection

Thermal overload protection limits the total power dissipation in the device. When the junction temperature exceeds +166°C, an on-chip thermal sensor shuts down the device, turns off the internal power MOSFETs, allowing the device to cool down. The thermal sensor turns the device on after the junction temperature cools by 10°C.

Applications Information

Inductor Selection

A low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions should be selected. The saturation current (I_{SAT}) must be high enough to ensure that saturation cannot occur below the maximum current-limit value ($I_{PEAK-LIMIT}$) of 0.56A (typ). See Table 1 to select the inductors for fixed 5V and 3.3V output voltage, 300mA load current applications.

Input Capacitor

Small ceramic capacitors are recommended for the device. The input capacitor reduces peak current drawn from the power source and reduces noise and voltage ripple on the input caused by the switching circuitry. A minimum of 1µF, X7R-grade capacitor in a package larger than 0805 is recommended for the input capacitor of the device to keep the input voltage ripple under 2% of the minimum input voltage, and to meet the maximum ripple-current requirements. See Table 2 to select the input capacitor for fixed 5V and 3.3V output voltage, 300mA load current applications.

Table 1. Inductor Selection

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (mA)	L (µH)	SUGGESTED PART NO.
4.5 to 60	3.3	300	33	Coilcraft LPS4018-333ML
5.5 to 60	5	300	47	Coilcraft LPS4018-473ML

Table 2. Input and Output Capacitor Selection

INPUT VOLTAGE RANGE (V_{IN})	V_{OUT} (V)	I_{OUT} (mA)	C_{IN}	C_{OUT}	SUGGESTED PART NO.	
					INPUT CAPACTIOR	OUTPUT CAPACTIOR
4.5V to 60V	3.3	300	1µF/1206/ X7R/100V	10µF/1206/ X7R/6.3V	Murata GRM31CR72A105KA01	Murata GRM31CR70J106KA01
5.5V to 60V	5	300	1µF/1206/ X7R/100V	10µF/1206/ X7R/6.3V	Murata GRM31CR72A105KA01	Murata GRM31CR70J106KA01

Output Capacitor

Small ceramic X7R-grade capacitors are sufficient and recommended for the device. The output capacitor has two functions. It filters the square wave generated by the device along with the output inductor. It stores sufficient energy to support the output voltage under load transient conditions and stabilizes the device's internal control loop. Usually the output capacitor is sized to support a step load of 50% of the maximum output current in the application, such that the output-voltage deviation is less than 3%. The device requires a minimum of 10µF capacitance for stability. Required output capacitance can be calculated from the following equation:

$$C_{OUT} = \frac{100 \times I_{STEP}}{V_{OUT} \times f_{SW}}$$

where I_{STEP} is the load current step, f_{SW} is the switching frequency, and V_{OUT} is the output voltage.

See Table 2 to select the output capacitor for fixed 5V and 3.3V output voltage, 300mA load current applications.

Setting the Input Undervoltage-Lockout Level

The devices offer an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from V_{IN} to GND (see Figure 1). Connect the center node of the divider to EN/UVLO.

Choose R1 to be 3.3MΩ max, and then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.215}{(V_{INU} - 1.215)}$$

where V_{INU} is the voltage at which the device is required to turn on.

Power Dissipation

Ensure that the junction temperature of the device does not exceed 125°C under the operating conditions specified for the power supply. At a particular operating condition, the power losses that lead to temperature rise of the part are estimated as follows:

$$P_{LOSS} = \left(P_{OUT} \times \left(\frac{1}{\eta} - 1\right)\right) - (I_{OUT}^2 \times R_{DCR})$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where P_{OUT} is the output power, E is the efficiency of power conversion, and R_{DCR} is the DC resistance of the output inductor. See the *Typical Operating Characteristics* for the power-conversion efficiency or measure the efficiency to determine the total power dissipation.

The junction temperature (T_J) of the device can be estimated at any ambient temperature (T_A) from the following equation:

$$T_J = T_A + (\theta_{JA} \times P_{LOSS})$$

where θ_{JA} is the junction-to-ambient thermal impedance of the package.

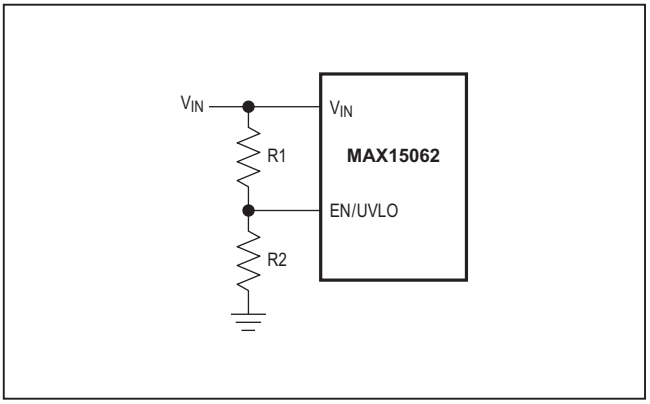


Figure 1. Adjustable EN/UVLO Network

PCB Layout Guidelines

Careful PCB layout (see Figure 2) is critical to achieve clean and stable operation. The switching power stage requires particular attention. Follow the guidelines below for good PCB layout.

- Place the input ceramic capacitor as close as possible to the V_{IN} and GND pins.
- Connect the terminal of the V_{CC} bypass capacitor to the GND pin with shortest possible trace or ground plane.
- Minimize the area formed by the LX pin and the inductor connection to reduce the radiated EMI.
- Place the V_{CC} decoupling capacitor as close as possible to the V_{CC} pin.
- Ensure that all feedback connections are short and direct.
- Route the high-speed switching node (LX) away from the V_{OUT}, $\overline{RESET}$, and MODE pins.

For a sample PCB layout that ensures the first-pass success, refer to the MAX15062 evaluation kit layouts available at **www.maximintegrated.com**.

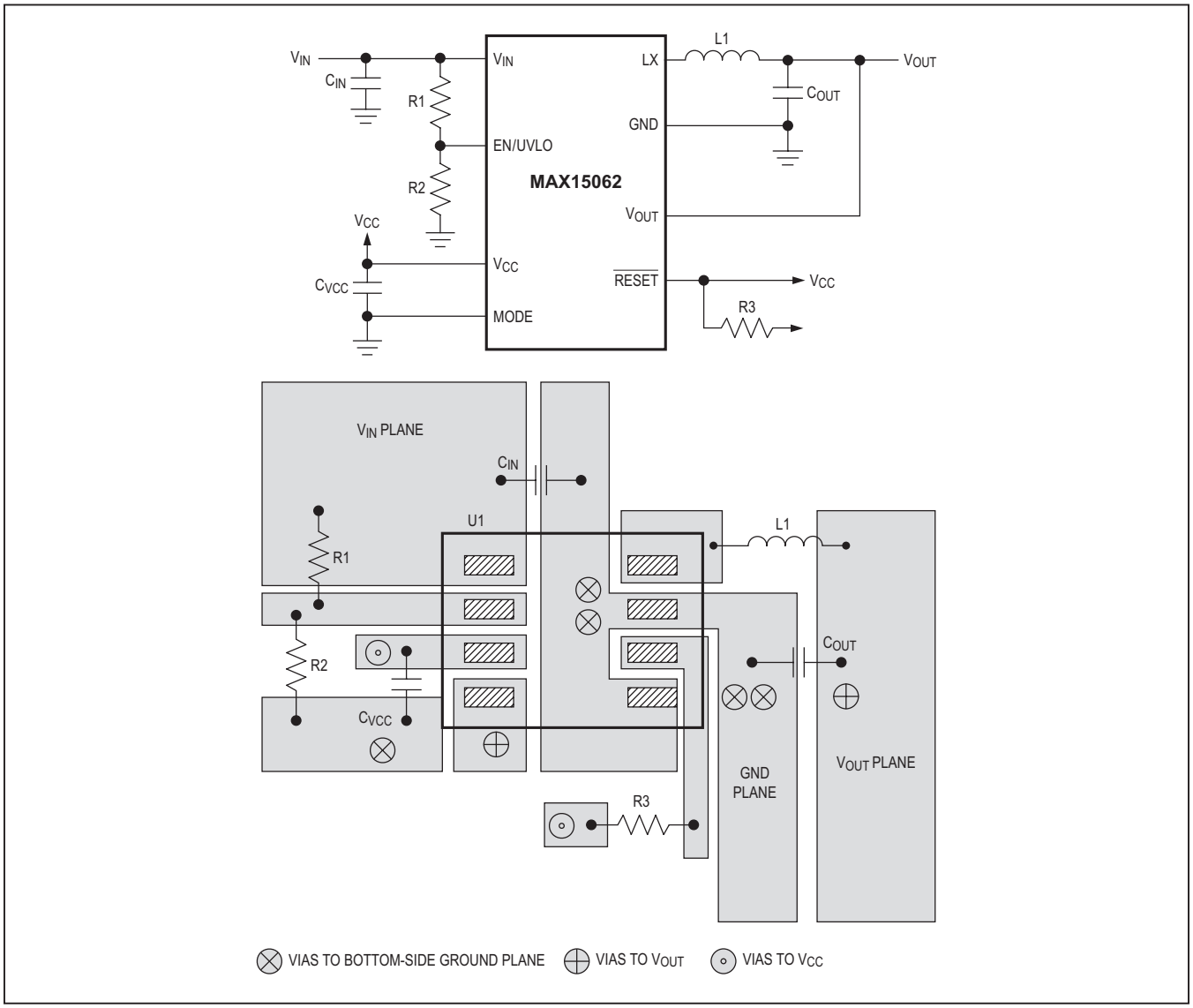


Figure 2. Layout Guidelines

Typical Application Circuits

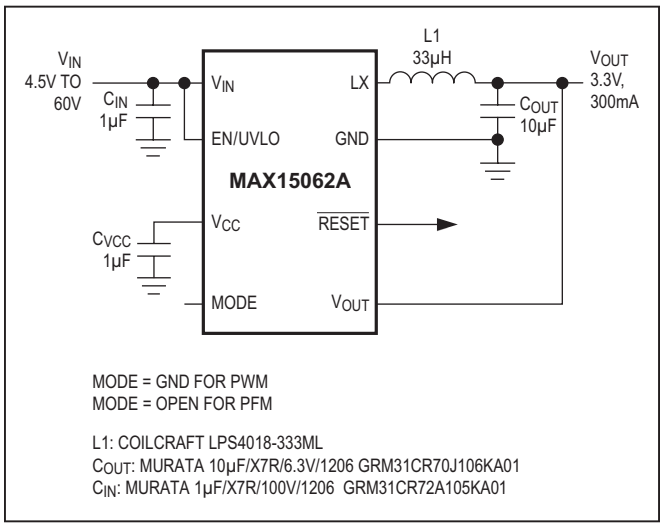


Figure 3. 3.3V, 300mA Step-Down Regulator

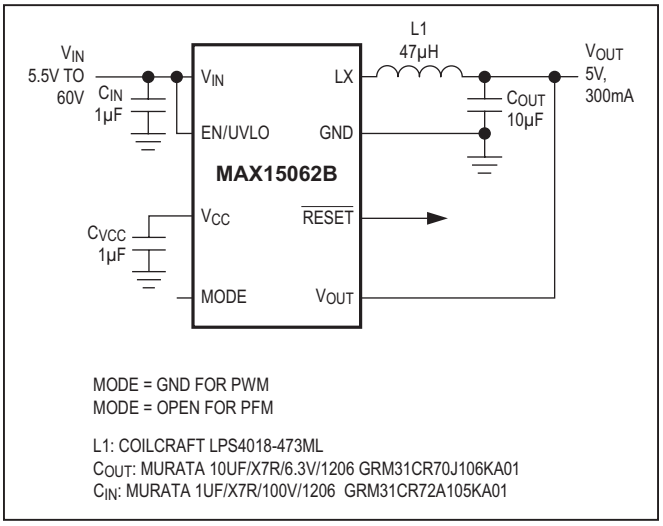


Figure 4. 5V, 300mA Step-Down Regulator

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	V_{OUT}
MAX15062AATA+	-40°C to +125°C	8 TDFN	3.3V
MAX15062BATA+	-40°C to +125°C	8 TDFN	5V

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 TDFN	T822CN+1	21-0487	90-0349

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/13	Initial release	—

