

# MAX15096/MAX15096A/ MAX15096D

# 2.7V to 18V, 6A Integrated Hot-Swap/Electronic Circuit Breaker

## General Description

The MAX15096/MAX15096A/MAX15096D ICs are integrated solutions for hot-swap applications requiring the safe insertion and removal of circuit line cards from a live backplane. They can also be used as electronics circuit breaker for hard drive and solid-state drive and fans. The devices integrate a hot-swap controller, 12m $\Omega$  (typ) power MOSFET, and an electronic circuit-breaker protection in a single package.

The devices are designed for protection of 2.7V to 18V supply voltages. These devices implement a foldback current limit during startup to control inrush current, lowering di/dt and keeping the MOSFET operating under safe operating area (SOA) conditions. After the startup cycle is complete, on-chip comparators provide VariableSpeed/BiLevel™ protection against short-circuit and overcurrent faults, and immunity against system noise and load transients. The load is disconnected in the event of a fault condition. The devices are factory calibrated to deliver accurate overcurrent protection with  $\pm 10\%$  accuracy. During a fault condition, PG goes low and the devices latch off (MAX15096) or automatic retry (MAX15096A); the output could also be discharged after a fault event (MAX15096D).

The devices feature an IN-to-OUT short-circuit detection before startup. The devices provide a power-MOSFET GATE pin to program the slew rate during startup by adding an external capacitor. The devices have an undervoltage/overvoltage input pin (UVOV) that can detect an undervoltage/overvoltage fault and disconnect the IN from the OUT. Additional features include internal overtemperature protection and a power-good output (PG).

The devices are available in a 16-bump, 2mm x 2mm wafer-level package (WLP) and are rated over the  $-40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$  extended temperature range.

## Benefits and Features

- Integration Reduces Solution size for Blade Servers and Other Space-Constrained Designs
  - Integrated 12m $\Omega$  (typ) Internal Power MOSFET
  - Programmable Overvoltage Protection and Undervoltage-Lockout Threshold
  - Power-Good and Fault Outputs
  - Analog Current Report Output without Need for External R<sub>SENSE</sub>
  - Thermal Protection
- Flexibility Enables Use in Many Unique Designs
  - 2.7V to 18V Operating Voltage Range
  - Programmable Inrush Current Control Under SOA Operation
  - Adjustable Circuit-Breaker Current/Current-Limit Threshold
  - Programmable Slew-Rate Control
  - Variable-Speed Circuit-Breaker Response
  - Latchoff or Automatic Retry Options
- Safety Features Ensure Accurate, Robust Protection
  - 6A (max) Load Current Capability
  - $\pm 10\%$  Circuit-Breaker Threshold Accuracy
  - IN-to-OUT Short-Circuit Detection
  - Open-Drain PG Output
  - Output Discharge After a Fault Event (MAX15096D Only)
  - Programmable Additional Delay (2 $\mu\text{s}$  max) to Fast-Comparator Response Time
  - Enable Input (EN)

## Applications

- Blade Servers
- Server I/O Cards
- RAID Systems
- Disk Drive Power
- Storage Applications
- Industrial Applications

*Ordering Information* appears at end of data sheet.

*VariableSpeed/BiLevel* is a trademark of Maxim Integrated Products, Inc.

### Absolute Maximum Ratings

V <sub>CC</sub> to GND .....	-0.3V to 20V
IN to GND.....	-0.3V to +20V
PG, PRSNT to GND .....	-0.3V to +20V
OUT to GND.....	-0.3V to (V <sub>IN</sub> + 0.3V)
GATE to OUT .....	-0.3V to +6V
EN, UVOV to GND .....	-0.3V to +6V
TIMER, CB to GND .....	-0.3V to (V <sub>REG</sub> + 0.3V)
REG to GND.....	-0.3V to min (+6V, (V <sub>CC</sub> + 0.3V))

Continuous Power Dissipation (T <sub>A</sub> = +70°C) 16-bump WLP (derate 20.4mW/°C above +70°C) ....	1633mW
Operating Temperature Range.....	-40°C to +105°C
Junction Temperature.....	+150°C
Storage Temperature Range.....	-60°C to +150°C
Lead Temperature (soldering, 10s) .....	+300°C
Soldering Temperature (reflow) .....	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ<sub>JA</sub>).....49°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

### Electrical Characteristics

(V<sub>IN</sub> = V<sub>CC</sub> = 2.7V to 18V, T<sub>A</sub> = T<sub>J</sub> = -40°C to +105°C, unless otherwise noted. Typical values are at V<sub>IN</sub> = 12V, R<sub>CB</sub> = 10.5kΩ, and T<sub>A</sub> = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>POWER SUPPLIES</b>							
V <sub>CC</sub> Operating Range	V <sub>CC</sub>		2.7		18	V	
IN Operating Range	V <sub>IN</sub>		2.7		18	V	
V <sub>CC</sub> Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> = 2.7V to 18V, enable		0.58	0.9	mA	
		V <sub>IN</sub> = V <sub>CC</sub> = 2.7V to 18V, disable		0.59		mA	
IN Supply Current	I <sub>IN</sub>	R <sub>CB</sub> = 41.2kΩ, no load		3.3	3.8	mA	
		R <sub>CB</sub> = 10.5kΩ, no load		1.3	1.8	mA	
V <sub>CC</sub> Default Undervoltage Lockout	V <sub>UVLO</sub>	V <sub>CC</sub> rising	2.35	2.5	2.65	V	
V <sub>CC</sub> Default Undervoltage-Lockout Hysteresis	V <sub>UVLO_HYS</sub>			0.1		V	
REG Regulator Voltage	V <sub>REG</sub>	No load, V <sub>CC</sub> > 4V	3	3.3	3.6	V	
UV Turn-On Threshold	V <sub>UV_TH</sub>	V <sub>UVOV</sub> rising	0.536	0.55	0.564	V	
UV Turn-On Threshold Hysteresis	V <sub>UV_HYS</sub>	V <sub>UVOV</sub> falling		50		mV	
OV Turn-On Threshold	V <sub>OV_TH</sub>	V <sub>UVOV</sub> rising	1.199	1.23	1.261	V	
OV Turn-On Threshold Hysteresis	V <sub>OV_HYS</sub>	V <sub>UVOV</sub> falling		50		mV	
UVOV Input Leakage Current	I <sub>LEAK</sub>	V <sub>UVOV</sub> = 0 to 5.5V	-1		+1	µA	
<b>CURRENT LIMIT</b>							
Circuit-Breaker Accuracy (Note 3)	I <sub>CB_TH</sub>	V <sub>IN</sub> = 12V	R <sub>CB</sub> = 41.2kΩ	5.4	6	6.6	A
			R <sub>CB</sub> = 10.5kΩ	1.14	1.27	1.40	
Circuit-Breaker Accuracy Deviation (Note 4)		R <sub>CB</sub> = 10.5kΩ to 21.5kΩ, compared to nominal current-limit value, V <sub>IN</sub> = V <sub>CC</sub> = 8V to 15V		-10		+10	%
		R <sub>CB</sub> = 21.5kΩ to 41.2kΩ, compared to nominal current-limit value		-10		+10	

**Electrical Characteristics (continued)**

( $V_{IN} = V_{CC} = 2.7V$  to  $18V$ ,  $T_A = T_J = -40^{\circ}C$  to  $+105^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{IN} = 12V$ ,  $R_{CB} = 10.5k\Omega$ , and  $T_A = +25^{\circ}C$ .) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Slow-Comparator Response Time (Note 5)	$t_{SCD}$	0.6% overcurrent		2.7		ms
		30% overcurrent		200		$\mu s$
CB Source Current	$I_{THCB\_NORM}$	In power-on mode		12		$\mu A$
Maximum Current Limit During Startup	$I_{LIM}$	(see Figure 2)		$0.5 \times I_{CB\_TH}$		A
Fast-Comparator Threshold	$I_{FC\_TH}$			$1.5 \times I_{CB\_TH}$		A
Fast-Comparator Response Time	$t_{FCD}$			200		ns
Additional Delay Time by TIMER	$t_{AFCD}$	$R_{TIMER} = \text{open}$		2		$\mu s$
Minimum CB Voltage Reference During Foldback (Note 6)	$V_{THCB\_MIN}$	$V_{IN} - V_{OUT} > 10V$ , $R_{CB} = 41.2k\Omega$		60		mV
Maximum CB Voltage Reference During Foldback (Note 6)	$V_{THCB\_MAX}$	$V_{IN} - V_{OUT} < 2V$ , $R_{CB} = 41.2k\Omega$		250		mV
<b>TIMING</b>						
Startup Maximum Time Duration	$t_{SU}$		43	52	61	ms
Autoretry Delay Time	$t_{RESTART}$	MAX15096A/MAX15096D only		3.4		s
Output Short Detection at Startup	$t_{SHORT}$		10.4	13.2	15.6	ms
<b>MOSFET</b>						
Total On-Resistance	$R_{ON}$	$T_A = +25^{\circ}C$		12	18	m $\Omega$
		$T_A = -40^{\circ}C$ to $+105^{\circ}C$			25	
GATE Charge Current	$I_{GATE}$		4.8	5.9	7.1	$\mu A$
<b>OUTPUTS</b>						
PG Output Low Voltage	$V_{OL}$	Low-impedance state, $I_{PG} = +5mA$			0.4	V
PG Output High-Leakage Current	$I_{OH}$	High-impedance state, $V_{PG} = 16V$			1	$\mu A$
<b>DISCHARGE</b>						
Discharge Current After PG Deasserted	$I_{DISCHARGE}$	$V_{OUT} < 7.1V$ (MAX15096D only)	50	100	160	mA
		$V_{OUT} \geq 7.1V$ to $18V$ (MAX15096D only)		$710mW/V_{OUT}$		
<b>PG THRESHOLD</b>						
PG Threshold	$V_{PG}$	$V_{IN} = 12V$		$0.9 \times V_{IN}$		V
PG Assertion Delay	$t_{PG}$	From $V_{OUT} > V_{PG}$ and $V_{GATE} - V_{OUT} > 3V$	12	16	20	ms
OUT-to-IN Short-Circuit Detection Threshold	$V_{IOSHT}$	Measured at $V_{OUT}$		$0.9 \times V_{IN}$		V
OUT Preload Threshold	$V_{PL}$	Measured at $V_{OUT}$		$0.5 \times V_{IN}$		V

### Electrical Characteristics (continued)

( $V_{IN} = V_{CC} = 2.7V$  to  $18V$ ,  $T_A = T_J = -40^{\circ}C$  to  $+105^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{IN} = 12V$ ,  $R_{CB} = 10.5k\Omega$ , and  $T_A = +25^{\circ}C$ .) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>INPUTS</b>						
Input Logic Threshold EN	$V_{EN\_TH}$	Rising	0.95	1	1.05	V
Threshold Hysteresis EN	$V_{EN\_TH\_HYS}$	Falling		50		mV
Input Logic Threshold $\overline{PRSNT}$	$V_{\overline{PRSNT}\_TH}$	Falling	0.92	0.97	1.02	V
Threshold Hysteresis $\overline{PRSNT}$	$V_{\overline{PRSNT}\_TH\_HYS}$	Rising		50		mV
EN Bias Current	$I_{EN\_BIAS}$	$V_{EN} = 0$ or $5.5V$			1	$\mu A$
$\overline{PRSNT}$ Input Bias Current	$I_{\overline{PRSNT}\_BIAS}$	$V_{\overline{PRSNT}} = 0$ or $18V$			1	$\mu A$
EN Deglitch Time	$t_{EN\_DEG}$			100		$\mu s$
$\overline{PRSNT}$ High-to-Low Deglitch Time	$t_{\overline{PRSNT}\_DEG}$			400		$\mu s$
<b>THERMAL SHUTDOWN</b>						
Thermal Shutdown	TSD	$T_J$ rising		150		$^{\circ}C$
Thermal Shutdown Hysteresis		$T_J$ falling		20		$^{\circ}C$

**Note 2:** All devices are 100% production tested at  $T_A = +25^{\circ}C$ . Limits over temperature are guaranteed by design.

**Note 3:**  $41.2k\Omega$  is the maximum allowed external resistance value to be connected at the CB pin to GND for safe operation. All devices are tested with  $10.5k\Omega$ , the parameter specified at  $R_{CB} = 41.2k\Omega$  is guaranteed by bench characterization and correlation, with respect to the tested parameter at  $R_{CB} = 10.5k\Omega$ . The formula that describes the relationship between  $R_{CB}$  and the circuit-breaker current threshold is:  $I_{CB} = R_{CB}/6510(\Omega/A) - 0.34A$ .

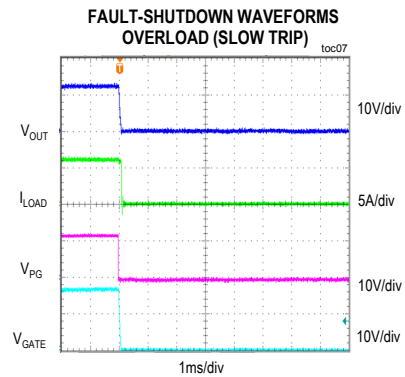
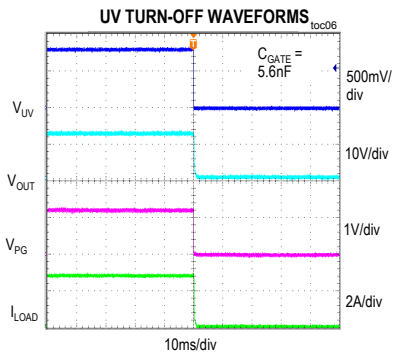
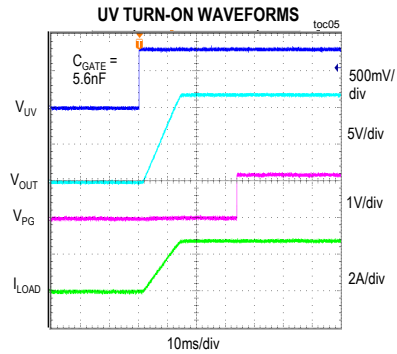
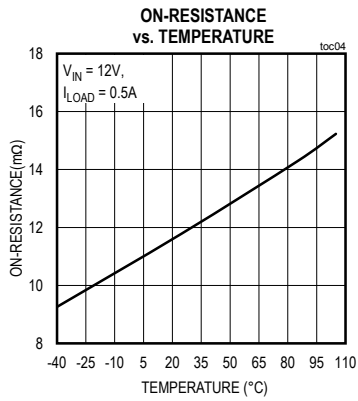
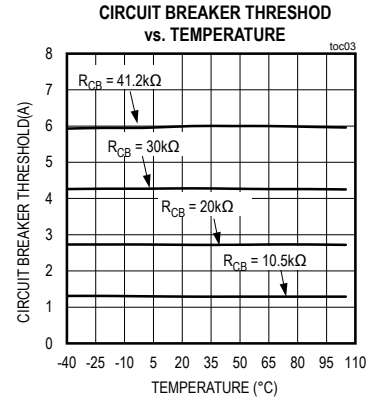
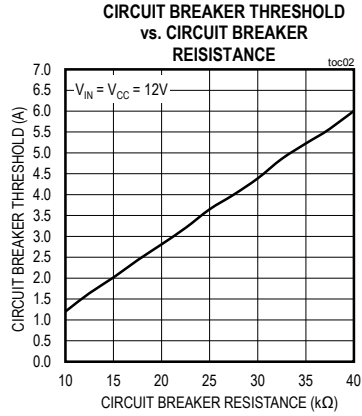
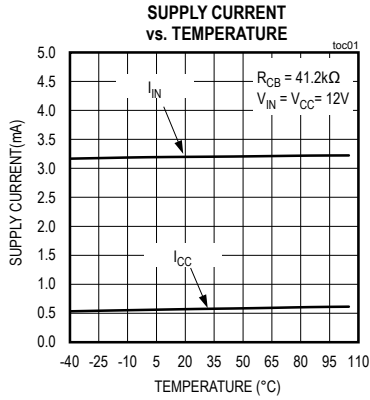
**Note 4:** Guaranteed by desing and not production tested.

**Note 5:** The current-limit slow-comparator response time is weighed against the amount of overcurrent so the higher the overcurrent condition, the faster the response time.

**Note 6:** Foldback is active during the startup phase so the internal power MOSFET operates within SOA.

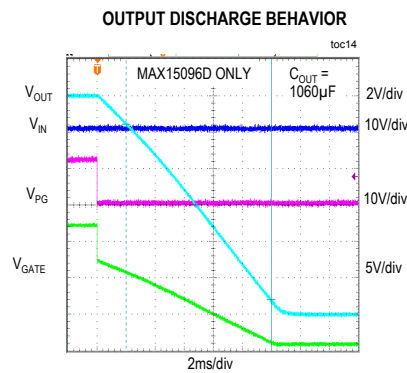
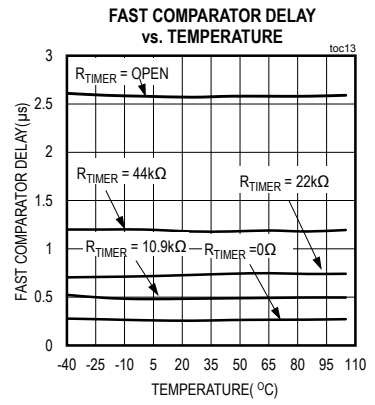
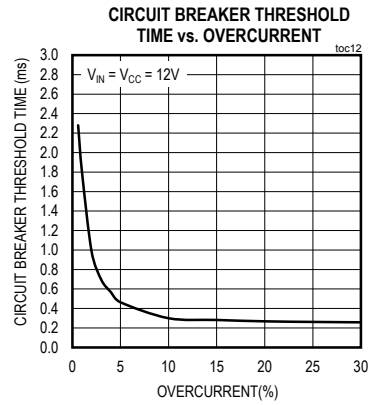
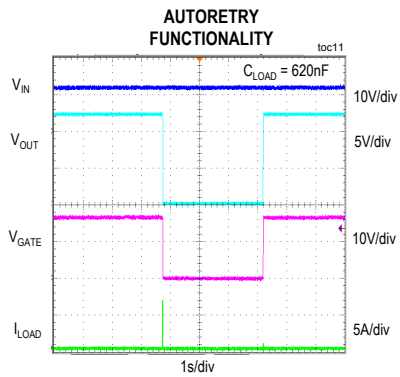
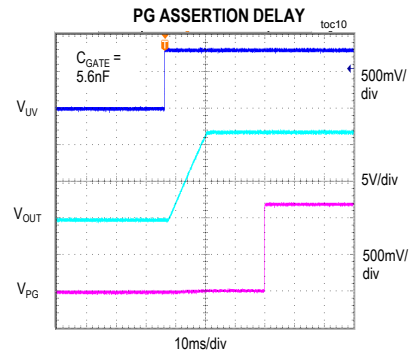
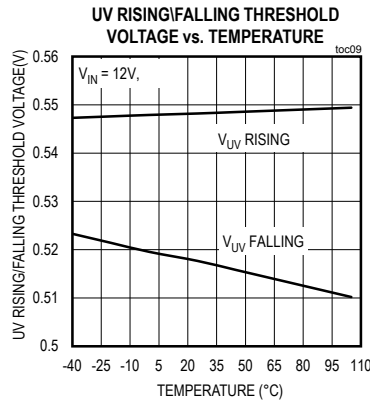
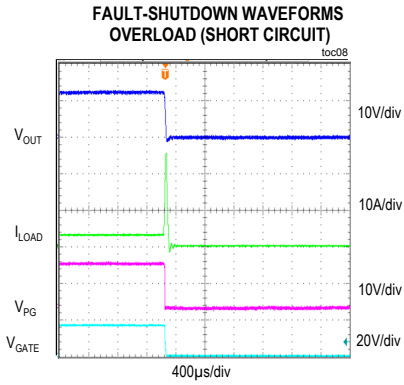
### Typical Operating Characteristics

( $V_{IN} = V_{CC} = 2.7V$  to  $18V$ ,  $T_A = T_J = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{IN} = 12V$ ,  $R_{CB} = 10.5k\Omega$ , and  $T_A = +25^{\circ}C$ .)

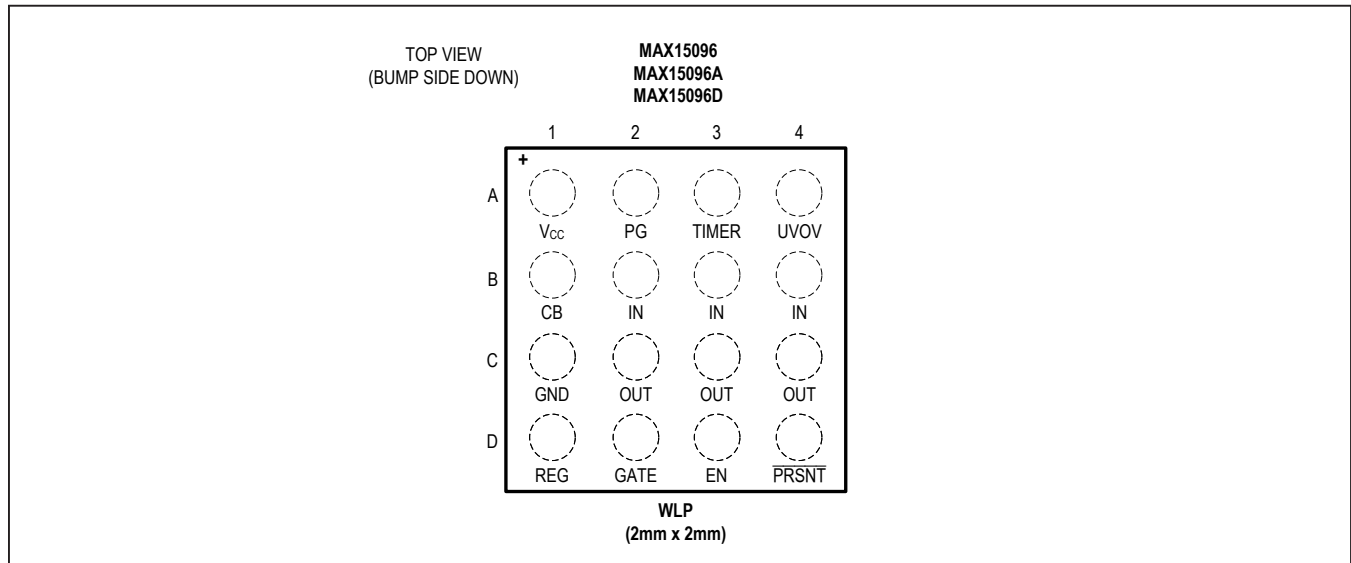


**Typical Operating Characteristics (continued)**

( $V_{IN} = V_{CC} = 2.7V$  to  $18V$ ,  $T_A = T_J = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{IN} = 12V$ ,  $R_{CB} = 10.5k\Omega$ , and  $T_A = +25^{\circ}C$ .)



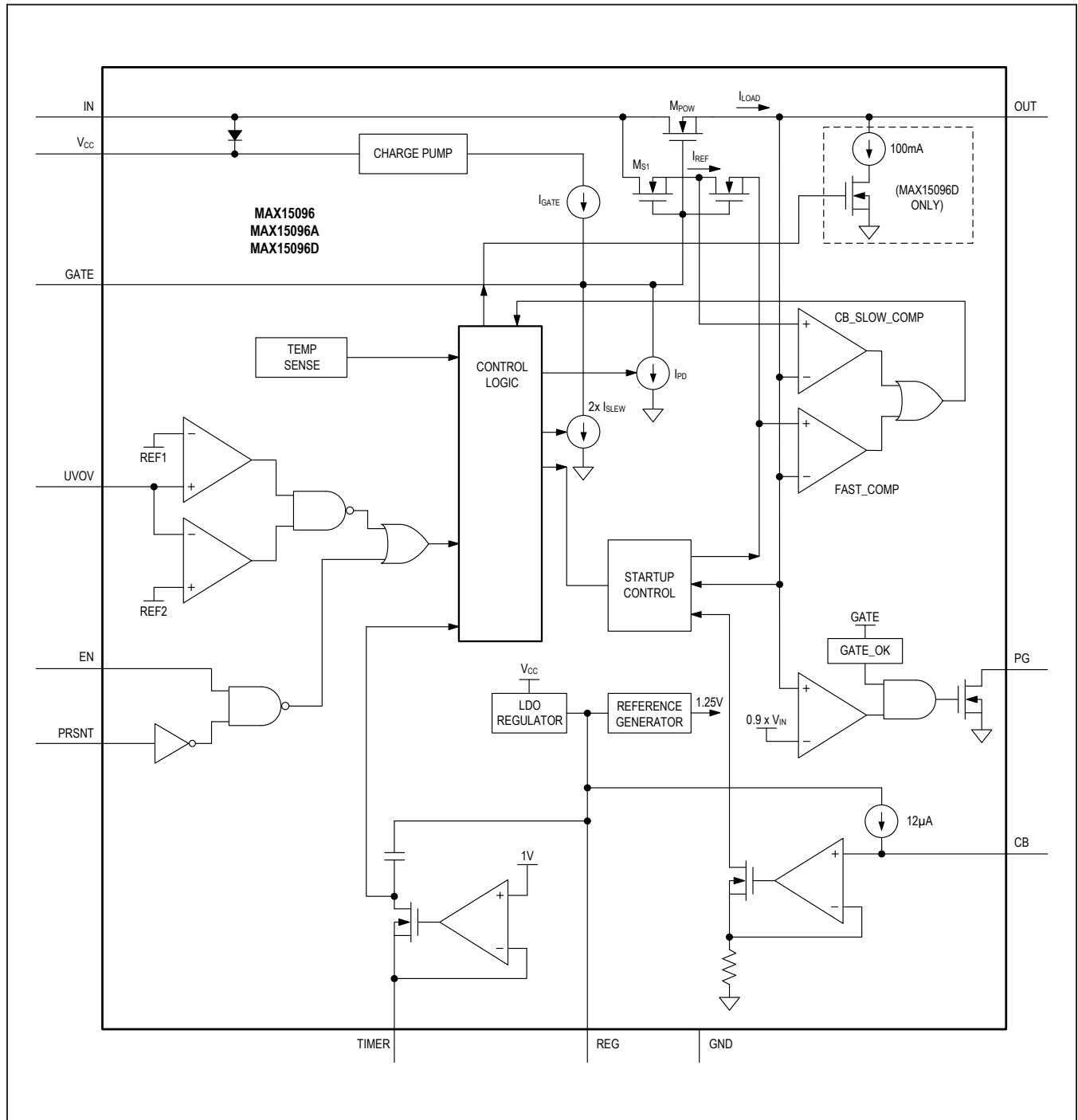
## Bump Configuration



## Bump Description

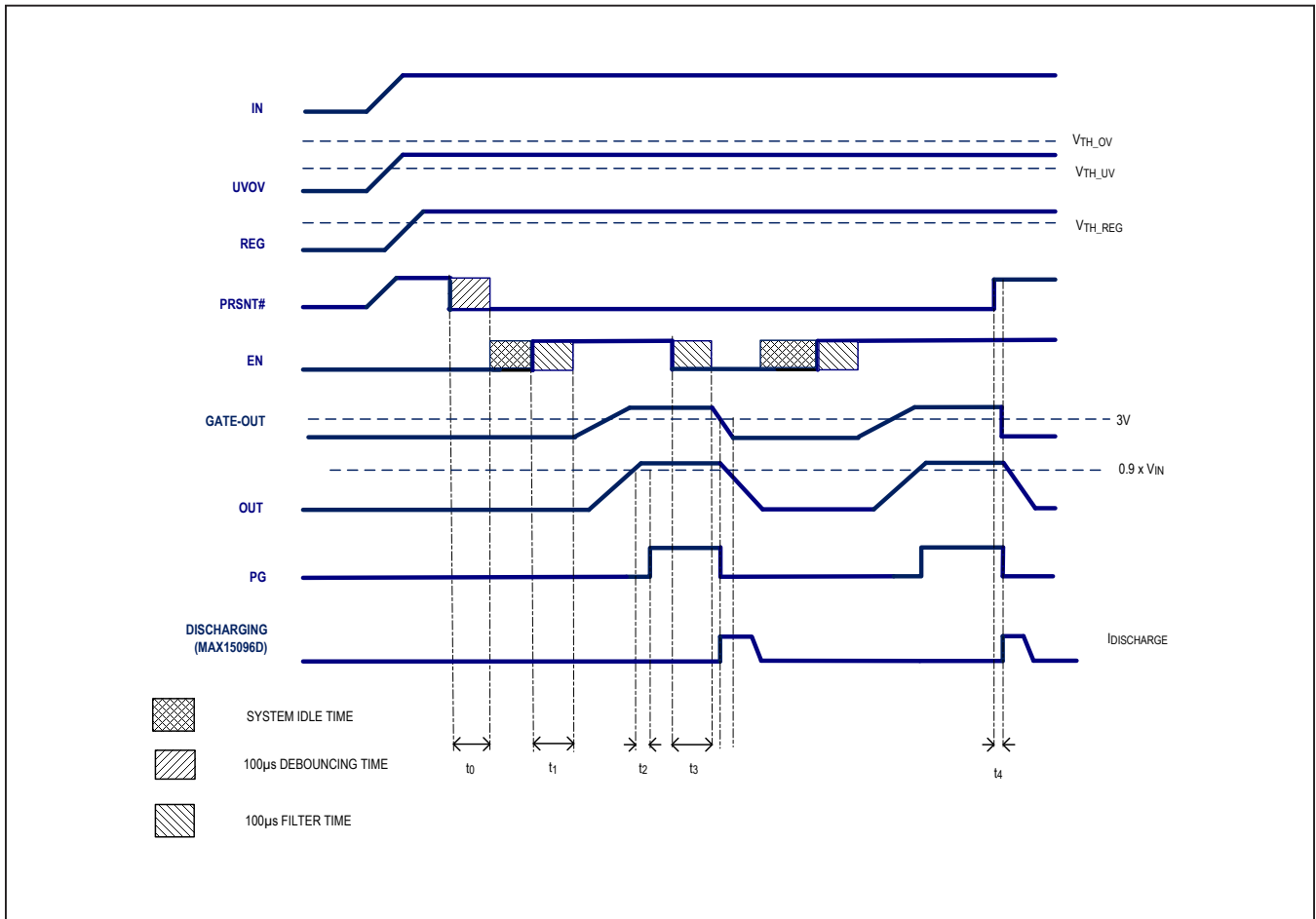
BUMP	NAME	FUNCTION
A1	V <sub>CC</sub>	Power-Supply Input. Connect V <sub>CC</sub> to a voltage between 2.7V and 18V. Connect a Schottky diode (or 10Ω resistor) from IN to V <sub>CC</sub> , and a 1μF bypass capacitor to GND to guarantee full operation in the event V <sub>IN</sub> collapses during a strong short from OUT to GND.
A2	PG	Power-Good Output. PG is an open-drain, active-high output. PG pulls low until the internal power MOSFET is fully enhanced.
A3	TIMER	Timing Input. Connect a resistor from TIMER to GND to program the maximum time the part is allowed to remain in current limit. See the <i>TIMER</i> section. If TIMER is not connected, the parasitic capacitance between TIMER and GND must be less than 10pF.
A4	UVOV	Undervoltage and Overvoltage Threshold Pin. UVOV sets the under/overvoltage threshold. See the <i>Setting the Undervoltage/Overvoltage Threshold</i> section.
B1	CB	Current-Limit Threshold Set. Connect a resistor from CB to GND to set the circuit-breaker threshold. Maximum value of 41.2kΩ can be accepted for safe operation. Having the CB pin connected to GND sets the circuit-breaker threshold at 0A.
B2–B4	IN	Supply Voltage Input. IN is connected to the drain of the internal 12mΩ (typ) MOSFET. Bypass IN with a transient voltage-suppressor diode to GND for clamping inductive kick transients in the case of fast output short circuit to GND.
C1	GND	Ground
C2–C4	OUT	Load Output. Source of the internal power MOSFET.
D1	REG	Internal Regulator Output. Bypass to ground with a 1μF capacitor. Do not power external circuitry using the REG output.
D2	GATE	Gate of Internal MOSFET. During startup, a 5.9μA (typ) current is sourced to enhance the internal MOSFET with a 10V/ms slew rate. Connect an external capacitance from GATE to GND to reduce the output slew rate during startup.
D3	EN	Active-High Enable Comparator Input. Pulling EN high enables the output if PR $\overline$ SNT is held low.
D4	PR $\overline$ SNT	Active-Low Present-Detect Logic Input. Pulling PR $\overline$ SNT to GND enables the output if EN is high.

Block Diagram





### Timing Diagram



**Table 1. Timing**

TIMING PARAMETER	MIN	TYP	MAX	UNITS
$t_0$	—	400	—	µs
$t_1$	—	100	—	µs
$t_2$	12	16	20	ms
$t_3$	—	100	—	µs
$t_4$	—	0.5	—	µs

## Detailed Description

### Enable Logic and Undervoltage/Overvoltage-Lockout Threshold

The supply output can become active only after all the following events have occurred:

- IN is within the UVOV window
- $V_{CC}$  is above its UVLO threshold
- EN meets its enable threshold for more than 100 $\mu$ s
- $\overline{PRSNT}$  is low for more than 400 $\mu$ s

The MAX15096 devices enable the outputs as shown in Table 1. The devices are ready to drive the output when the  $V_{CC}$  supply rises above the  $V_{UVLO}$  threshold. The devices turn on the output when  $V_{CC} > V_{UVLO}$ ,  $V_{UVOV}$  is higher than 0.55V ( $V_{UV\_TH}$ ) and less than 1.23V ( $V_{OV\_TH}$ ). The devices turn off the output when  $V_{UVOV}$  falls below (0.55V -  $V_{UV\_HYS}$ ) or  $V_{UVOV}$  rises above

1.23V. An external resistive divider from IN to UVOV and ground provide the flexibility to select the undervoltage/overvoltage-lockout threshold to the desired value. See Figure 1 and the [Setting the Undervoltage/Overvoltage Threshold](#) section in the [Applications Information](#) section.

### Startup

Once the devices' output is enabled, the device provides controlled application of power to the load. The voltage at OUT begins to rise at approximately 10V/ms default until the programmed circuit-breaker current level is reached, while the devices actively limit the inrush current at the circuit-breaker setting. An external capacitance connected to the GATE pin allows the user to program the slew rate to a value lower than the default. The inrush current can be programmed by appropriate selection of  $R_{CB}$ . During startup, a foldback current limit is active to protect the internal MOSFET to operate within safe operating area. (Figure 2).

**Table 2. Output Enable Truth Table**

POWER SUPPLY	PRECISION ANALOG INPUT		OUT
	UVP	OVP	
$V_{CC} > V_{UVLO}$	$V_{UVOV} > V_{UV\_TH}$	$V_{UVOV} < V_{OV\_TH}$	On
$V_{CC} < V_{UVLO}$	X	X	Off
X	$V_{UVOV} < (V_{UV\_TH} - V_{UV\_HYS})$	X	Off
X	X	$V_{UVOV} > V_{OV\_TH}$	Off

X = Don't care.

$V_{UV\_TH} = 0.55V$  (typ).

$V_{OV\_TH} = 1.23V$  (typ).

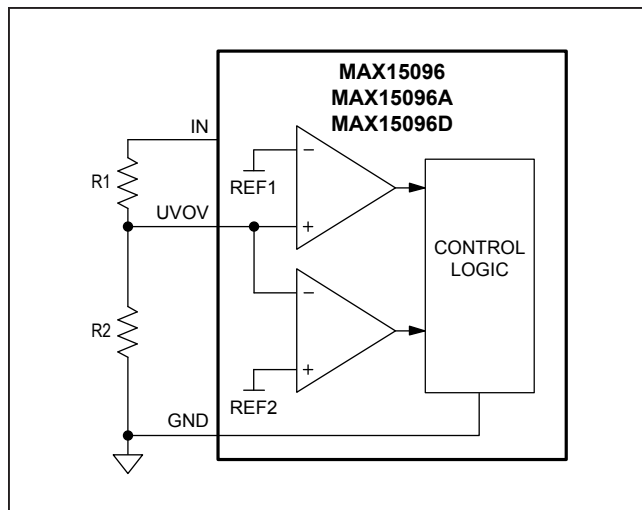


Figure 1. Undervoltage/Overvoltage Threshold Setting

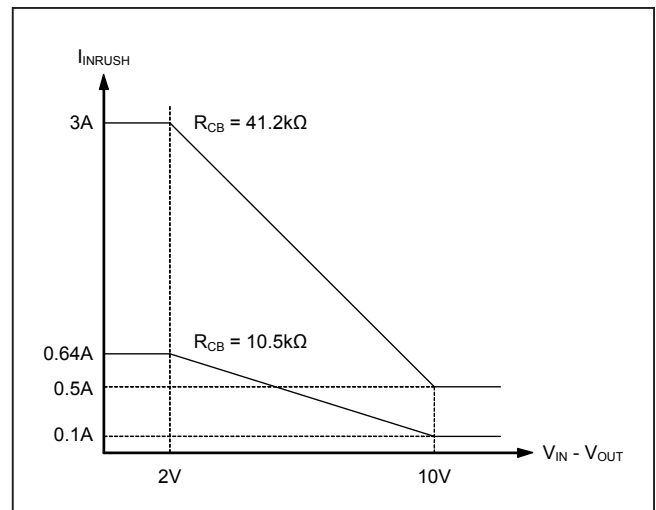


Figure 2. Startup Inrush Current Foldback Characteristics

An internal 52ms (typ) timer starts counting when the device enters startup phase. The devices complete startup phase and enter normal operation mode if the voltage at OUT rises above the preload threshold ( $0.9 \times V_{IN}$ ) and  $(V_{GATE} - V_{OUT}) > 3V$ . An open-drain power-good output (PG) goes high impedance 16ms after the startup successfully completes. The thermal-protection circuit is always active and the internal MOSFET is immediately turned off so thermal-shutdown threshold condition can be reached.

If the startup is not successful because the output is shorted or the load is too high (OUT voltage  $< 1V$ ), the devices turn off the hot-swap switch after the output short detection at startup  $t_{SHORT}$  (13.2ms) elapses.

### VariableSpeed/BiLevel-Fault Protection

VariableSpeed/BiLevel-fault protection incorporates comparators with different thresholds and response times to monitor the load current (Figure 3). Protection is provided in normal operation (after the startup period has expired) by discharging the MOSFET gate in response to a fault condition. During a fault condition, the MAX15096A enters an autoretry mode while the MAX15096 latches off (see the [Autoretry and Latchoff Fault Management](#) section).

### Enable Input (EN)

The devices allow for enabling the MOSFET in an active-high configuration. When all other enabling conditions are verified and the EN pin is at a logic-high level, the MOSFET is enabled. Similarly, when the EN pin is at a logic-low level, the MOSFET is disabled.

### Charge Pump

An integrated charge pump provides the gate-drive voltage for the internal power MOSFET. The charge pump generates the proper gate-drive voltage above  $V_{IN}$  to fully enhance the internal power MOSFET and guarantee low  $R_{ON}$  operation during normal state condition.

During startup, the internal charge pump drives the GATE of the MOSFET with a  $5.9\mu A$  current to enhance the internal MOSFET with 10V/ms slew rate. Connect an external capacitor ( $C_{GATE}$ ) from GATE to GND to reduce the output slew rate during startup.  $C_{GATE}$  can be calculated according to the formula below:

$$C_{GATE} = (I_{GATE} \times \Delta t) / \Delta V_{GATE}$$

where  $I_{GATE}$  is  $5.9\mu A$  (typ),  $\Delta t$  is the desired slew rate time, and the 5V of  $\Delta V_{GATE}$  is the voltage at the gate of the internal MOSFET at turn-on.

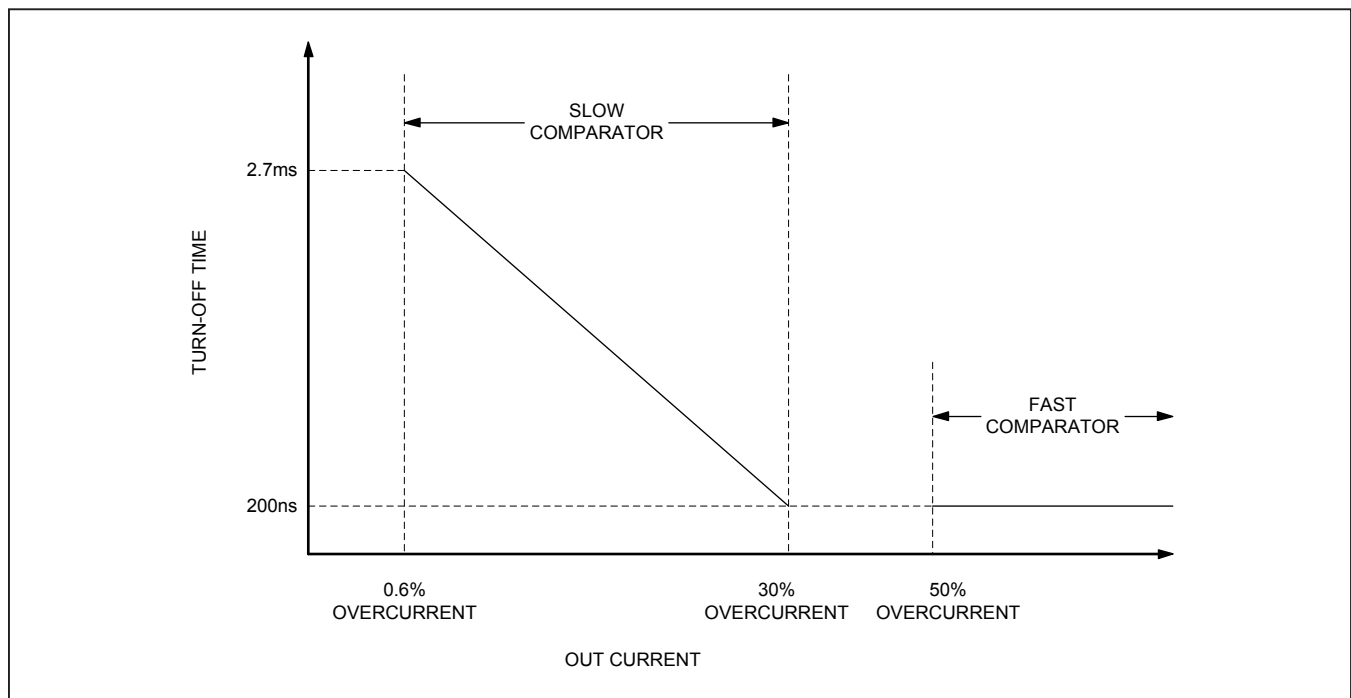


Figure 3. VariableSpeed/BiLevel Response

### Circuit-Breaker Comparator and Current Limit

The current through the internal power MOSFET is compared to a circuit-breaker threshold. An external resistor between CB and ground sets this threshold according to the following formula:

$$I_{CB} = (R_{CB}/6501)(A/\Omega) - 0.34A$$

where  $I_{CB}$  is in amps and  $R_{CB}$  (the resistor between CB and ground) is in ohms.

The circuit-breaker comparator is designed so that the load current can exceed the threshold for some amount of time before tripping. The time delay varies inversely with the overdrive above the threshold. The greater the overcurrent condition, the faster the response time, allowing the devices to tolerate load transients and noise near the circuit-breaker threshold. The maximum allowed external resistor value is 41.2k $\Omega$ , which corresponds to a 6A CB threshold setting. Programming the CB threshold to a value higher than 6A could cause unsafe operating conditions, resulting in damage to the device.

The devices also feature catastrophic short-circuit protection. During normal operation, if OUT is shorted directly to ground, a fast protection circuit forces the gate of the internal MOSFET to discharge quickly and disconnect the output from the input.

### Autoretry and Latchoff Fault Management

During a fault condition, the devices turn off the internal MOSFET, disconnecting the output from the input. The MAX15096A enters an autoretry mode and restarts after  $t_{RESTART}$  (3.4s typ.) time delay elapses.

The MAX15096 latches off and remains off until the enable logic is cycled off and on after a certain delay. The delay prevents the latchoff device to restart and operate with unsafe power-dissipation duty cycle. See the *Timing* diagram and [Table 1](#) for delay values.

### Latchoff Reset

The latchoff could be reset if any one of the following happens:

- $V_{CC}$  is below its UVLO threshold
- EN is disabled for longer than 100 $\mu$ s
- UV is triggered

- $\overline{PRSNT}$  goes above its threshold
- OV is triggered

### Power-Good (PG) Delay

The devices feature an open-drain, power-good output that asserts after  $t_{PG}$  delay, indicating that OUT voltage has reached  $(0.9 \times V_{IN})$  voltage and  $(V_{GATE} - V_{OUT}) > 3V$ .

### REG

The devices include a linear regulator that outputs 3.3V at REG. REG provides power to the internal circuit blocks of the devices and must not be loaded externally (except a resistor > 50k $\Omega$  connected from REG to EN). REG requires a 1 $\mu$ F capacitor to ground for proper operation.

### Output Discharging

The discharge FET is active when the output is disabled or under fault event. In this event, the hot-swap is off and the output is on the way down. The discharging is triggered after the main FET has completely turned off.

The maximum output capacitance is approximately 1000 $\mu$ F. The voltage could be up to 18V. Ideally, it discharges the output capacitor in constant power mode (710mW typ) to ensure the voltage rail is below 0.3V within 2s or less time.

### TIMER

Connect a resistor from the TIMER pin to the GND pin to program the fast-trip response time. This time is the sum of the internal fast-comparator propagation delay (less than 200ns typ) plus an additional delay set by the external resistor connected from TIMER to ground. Choosing different resistance values, it is possible to change the value of additional delay. If the TIMER pin is connected to REG, the total response time is less than 200ns (typ).

Additional delay is disabled also during the startup phase or after a short-circuit event ( $V_{OUT} < 90\% V_{IN}$ ). Be careful about additional delay settings related to a short event.

Additional delay can be calculated using the following formula:

$$\text{Additional\_Delay } (\mu\text{s}) = R_{\text{TIMER}} (\text{k}\Omega) \times 22.9E-03$$

Maximum additional delay time is set to 2 $\mu$ s. [Table 3](#) provides additional delay settings.

**Table 3. Additional Delay Settings**

OPTION	R <sub>TIMER</sub> (kΩ)	RESPONSE TIME (μs)
1	Open	2
2	86.6	2
3	43.2	1
4	21.5	0.5
5	11	0.25
6	0	0.050

**Table 4. Setting the Undervoltage/Overvoltage Thresholds**

OPTION	R1 TABLE (kΩ) R2 = 10kΩ	OVP	UVP
1	133	17.6	7.9
2	127	16.9	7.5
3	118	15.7	7.0
4	115	15.4	6.9
5	113	15.1	6.8
6	107	14.4	6.4
7	102	13.8	6.2
8	49.9	7.4	3.3
9	46.4	6.9	3.1
10	43.2	6.5	2.9
11	39.2	6.1	2.7
12	33.2	5.3	2.4

### Thermal Protection

The devices enter a thermal shutdown mode in the event of overheating caused by excessive power dissipation or high ambient temperature. When the junction temperature exceeds  $T_J = +150^{\circ}\text{C}$  (typ), the internal thermal protection circuitry turns off the internal power MOSFET. The devices recover from thermal shutdown mode once the junction temperature drops by  $20^{\circ}\text{C}$  (typ).

### IN-to-OUT Short-Circuit Protection

At startup, after all the input conditions are satisfied (UV, OV,  $V_{UVLO}$ ), the devices immediately check for IN-to-OUT short-circuit faults. If  $V_{OUT}$  is greater than 90% of

$V_{IN}$ , the internal MOSFET cannot be turned on, then the MAX15096A autoretries in  $t_{RESTART}$  (3.4s typ), while the MAX15096 latches off.

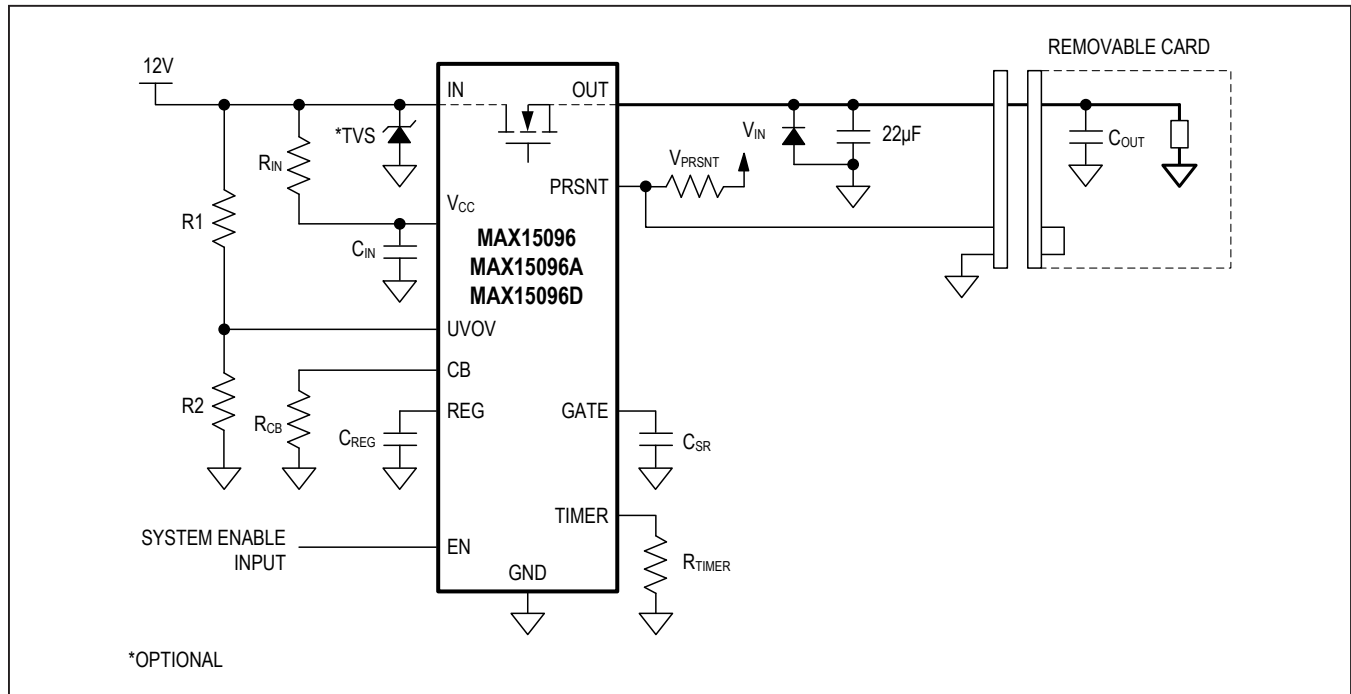
If  $V_{OUT}$  is in the range from 50% to 90% of  $V_{IN}$ , then the internal MOSFET still cannot be turned on after  $t_{SU}$  time elapses. The MAX15096A autoretries in  $t_{RESTART}$ , while the MAX15096 latches off.

## Applications Information

### Setting the Undervoltage/Overvoltage Threshold

See [Table 4](#) for options.

### Typical Application Circuit



### Wafer-Level Packaging (WLP) Applications Information

For the latest application details on WLP construction, dimensions, tape carrier information, printed-circuit board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to Application Note 1891: *Wafer-Level Packaging (WLP) and Its Applications*—available on Maxim’s website at [www.maximintegrated.com/wlp](http://www.maximintegrated.com/wlp).

### Ordering Information

PART	TEMP RANGE (°C)	PIN-PACKAGE	FAULT MANAGEMENT
MAX15096GWE+	-40 to +105	16 WLP	Latchoff
MAX15096AGWE+	-40 to +105	16 WLP	Autoretry
MAX15096DGWE+*	-40 to +105	16 WLP	Autoretry

+Denotes a lead (Pb)-free/RoHS-compliant package.

\*Future product—contact factory for availability.

### Chip Information

PROCESS: BICMOS

### Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 WLP	W162J2Z+1	<a href="#">21-0200</a>	Refer to <a href="#">Application Note 1891</a>

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/14	Initial release	—
1	8/14	Replaced TOCs 1, 3, 4, 9, and 13	5, 6
2	1/15	Updated <i>Benefits and Features</i> section	1

For information on other Maxim Integrated products, visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

*Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.*