



# ±15V, 128-Tap, Low-Drift Digital Potentiometers

MAX5436-MAX5439

## General Description

The MAX5436-MAX5439 are 128-tap high-voltage ( $\pm 5V$  to  $\pm 15V$ ) digital potentiometers in packages that are half the size of comparable devices in 8-pin SO. They perform the same function as mechanical potentiometers, but replace the mechanics with a simple digital interface. The digital logic is powered by a separate single  $+2.7V$  to  $+5.25V$  supply voltage ( $V_{CC}$ ). The resistor string uses its own analog supplies ( $V_{DD}$  and  $V_{SS}$ ) that require  $V_{DD} - V_{SS}$  to be greater than  $9V$  and less than  $31.5V$ . This allows for greater flexibility in voltage ranges that can be used with these devices. Examples of analog supply ranges include not only dual voltages of  $\pm 5V$  to  $\pm 15V$ , but single-supply voltages, such as  $+10V$ ,  $+15V$ ,  $+30V$ ,  $-30V$ , and more, as long as the ranges of  $V_{DD} - V_{SS}$  and  $V_{CC} - V_{SS}$  are met.

The MAX5437/MAX5439 include an on-chip, high-voltage, uncommitted amplifier, providing additional reductions in board space and cost. Other features include low  $35\text{ppm}/^{\circ}\text{C}$  end-to-end and  $5\text{ppm}/^{\circ}\text{C}$  ratio-metric resistor temperature coefficients, a 3-wire SPI™/QSPI™/MICROWIRE™-compatible serial interface, and a power-on reset to midscale.

The MAX5436/MAX5438 are available in 10-pin  $\mu\text{MAX}$  packages. The MAX5437/MAX5439 are available in 14-pin TSSOP package. Each device is guaranteed over the extended temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

## Applications

- LCD Screen Contrast Adjustment
- Data-Acquisition Systems
- Mechanical Potentiometer Replacement
- Low-Drift Programmable Gain Amplifier
- Audio Volume Control

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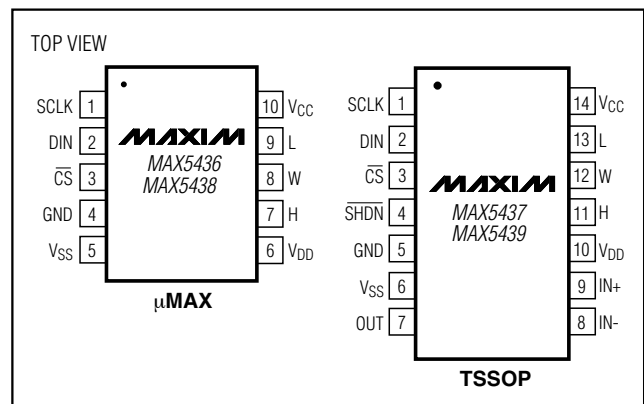
## Features

- ◆ **+10V to +30V Single-Supply Operation**
- ◆ **-28V to -10V Single Negative Supply Operation**
- ◆  **$\pm 5V$  to  $\pm 15V$  Dual-Supply Operation**
- ◆ **128 Tap Positions**
- ◆ **Uncommitted High-Voltage Amplifier (MAX5437/MAX5439)**
- ◆ **Low Temperature Coefficient**  
 **$35\text{ppm}/^{\circ}\text{C}$  (End-to-End)**  
 **$5\text{ppm}/^{\circ}\text{C}$  (Ratiometric)**
- ◆ **Small-Footprint Packages**  
**10-Pin  $\mu\text{MAX}$  (MAX5436/MAX5438)**  
**14-Pin TSSOP (MAX5437/MAX5439)**
- ◆ **Glitchless Switching Between the Resistor Taps**
- ◆ **3-Wire SPI/QSPI/MICROWIRE-Compatible Serial Interface**
- ◆  **$50\text{k}\Omega/100\text{k}\Omega$  End-to-End Resistances**
- ◆ **Power-On Reset: Wiper Goes to Midscale (Position 64)**

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	RESISTANCE (k $\Omega$ )
MAX5436EUB	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	10 $\mu\text{MAX}$	50
MAX5437EUD	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	14 TSSOP	50
MAX5438EUB	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	10 $\mu\text{MAX}$	100
MAX5439EUD	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	14 TSSOP	100

## Pin Configurations



# ±15V, 128-Tap, Low-Drift Digital Potentiometers

## ABSOLUTE MAXIMUM RATINGS

V <sub>DD</sub> to GND, V <sub>SS</sub> = GND	-0.3V to +34V	Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
V <sub>SS</sub> to GND, V <sub>DD</sub> = GND	-34V to +0.3V	10-Pin μMAX (derate 6.94mW/°C above +70°C)	556mW
V <sub>DD</sub> to V <sub>SS</sub>	-0.3V to +34V	14-Pin TSSOP (derate 9.1mW/°C above +70°C)	727mW
V <sub>DD</sub> to V <sub>CC</sub>	-6.3V to +28.75V	Operating Temperature Range	-40°C to +85°C
V <sub>CC</sub> to V <sub>SS</sub>	-0.3V to +34V	Junction Temperature	+150°C
V <sub>CC</sub> to GND	-0.3V to +6V	Storage Temperature Range	-65°C to +150°C
DIN, SCLK, CS, SHDN	-0.3V to (V <sub>CC</sub> + 0.3V)	Lead Temperature (soldering, 10s)	+300°C
H, L, W, IN+, IN-, OUT	(V <sub>SS</sub> - 0.3V) to (V <sub>DD</sub> + 0.3V)		
Maximum Continuous Current into H, L, and W			
MAX5436-MAX5439	±1mA		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = +15V, V<sub>SS</sub> = -15V, V<sub>CC</sub> = +5V, V<sub>H</sub> = V<sub>DD</sub>, V<sub>L</sub> = V<sub>SS</sub>, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC PERFORMANCE (Voltage-Divider Mode)</b>						
Resolution	2 <sup>N</sup>		128			Taps
Integral Nonlinearity	INL	(Note 1)			±1	LSB
Differential Nonlinearity	DNL	(Note 1)			±1	LSB
End-to-End Resistor Tempco	TC <sub>R</sub>			35		ppm/°C
Ratiometric Resistor Tempco				5		ppm/°C
Full-Scale Error		R <sub>H</sub> L = 50kΩ (MAX5436/MAX5437)		-0.3		LSB
Zero-Scale Error		R <sub>H</sub> L = 50kΩ (MAX5436/MAX5437)		+0.3		LSB
Full-Scale Error		R <sub>H</sub> L = 100kΩ (MAX5438/MAX5439)		-0.15		LSB
Zero-Scale Error		R <sub>H</sub> L = 100kΩ (MAX5438/MAX5439)		+0.15		LSB
<b>DC PERFORMANCE (Variable-Resistor Mode)</b>						
Resolution	2 <sup>N</sup>		128			Taps
Integral Nonlinearity	INL	(Note 2)			±1	LSB
Differential Nonlinearity	DNL	(Note 2)			±1	LSB
<b>DC PERFORMANCE (Resistor Characteristics)</b>						
Wiper Resistance	W <sub>R</sub>	(Note 3)		0.9	2	kΩ
Wiper Capacitance	W <sub>C</sub>	Midscale		6		pF
End-to-End Resistance	R <sub>H</sub> L	MAX5438/MAX5439	75	100	125	kΩ
		MAX5436/MAX5437	37.5	50	62.5	
<b>DIGITAL INPUTS</b>						
Input High Voltage		V <sub>CC</sub> = 4.75V to 5.25V (Note 4)	2.4			V
Input Low Voltage		V <sub>CC</sub> = 4.75V to 5.25V			0.8	V

# ±15V, 128-Tap, Low-Drift Digital Potentiometers

MAX5436-MAX5439

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +15V$ ,  $V_{SS} = -15V$ ,  $V_{CC} = +5V$ ,  $V_H = V_{DD}$ ,  $V_L = V_{SS}$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage		$V_{CC} = 2.7V$ to $3.6V$	2.0			V
Input Low Voltage		$V_{CC} = 2.7V$ to $3.6V$			0.6	V
Input Leakage Current					±1.0	μA
Input Capacitance				5.0		pF
<b>DYNAMIC CHARACTERISTICS (Analog)</b>						
Wiper -3dB Bandwidth	BW <sub>W</sub>	$R_{HL} = 50k\Omega$ , midscale, $V_H = 1.5V_{P-P}$ , $C_{WIPER} = 20pF$ , voltage-divider mode		400		kHz
		$R_{HL} = 100k\Omega$ , midscale, $V_H = 1.5V_{P-P}$ , $C_{WIPER} = 20pF$ , voltage-divider mode		200		
Wiper Settling Time	t <sub>IL</sub>	$C_{WIPER} = 20pF$ , code 1 to code 127, settle to 0.5LSB		5		μs
<b>AMPLIFIER CHARACTERISTICS (Analog)</b>						
Input Bias Current	I <sub>B</sub>			15		nA
Input Offset Voltage	V <sub>OS</sub>			±6		mV
Offset-Voltage Temperature Drift	V <sub>OSD</sub>			10		μV/°C
Input Offset Current	I <sub>OS</sub>			2		nA
Unity-Gain Bandwidth	UBW <sub>A</sub>	$C_{LOAD} = 250pF$		100		kHz
Slew Rate	SR			0.25		V/μs
Large-Signal Voltage Gain	A <sub>VO</sub>	$R_{LOAD} = 100k\Omega$ , $V_{OUT} = \pm 14V$		100		V/mV
Input Noise	V <sub>N</sub>	f = 1kHz		110		nV/√Hz
Input Compliance	CMR <sub>I</sub>		$V_{SS} + 1$		$V_{DD} - 2$	V
Output Compliance	CMR <sub>O</sub>	$I_{LOAD} = \pm 5mA$	$V_{SS} + 1$		$V_{DD} - 1$	V
DC CMRR	CMRR			68		dB
DC PSRR	PSRR			70		dB
<b>TIMING CHARACTERISTICS (Digital)</b> (Note 5, Figure 3)						
SCLK Clock Frequency	f <sub>CLK</sub>		0		10	MHz
SCLK Clock Period	t <sub>CP</sub>		100			ns
SCLK Pulse Width High	t <sub>CH</sub>		40			ns
SCLK Pulse Width Low	t <sub>CL</sub>		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t <sub>CSS</sub>		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t <sub>CSH</sub>		10			ns
DIN Setup Time	t <sub>DS</sub>		40			ns
DIN Hold Time	t <sub>DH</sub>		0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	t <sub>CSD</sub>		10			ns
$\overline{CS}$ Rise to SCLK Rise Hold	t <sub>CS1</sub>		40			ns
$\overline{CS}$ Pulse Width High	t <sub>CSW</sub>		100			ns
<b>POWER SUPPLIES</b>						
Positive Analog Supply Voltage	V <sub>DD</sub>		0		31.5	V
Negative Analog Supply Voltage	V <sub>SS</sub>		-28.8		0	V

# ±15V, 128-Tap, Low-Drift Digital Potentiometers

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +15V$ ,  $V_{SS} = -15V$ ,  $V_{CC} = +5V$ ,  $V_H = V_{DD}$ ,  $V_L = V_{SS}$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Supply Separation	$V_{DS}$	$V_{DD} - V_{SS}$	9.0		31.5	V
Digital Supply Voltage	$V_{CC}$		2.70		5.25	V
Digital Supply to Negative Analog Supply Separation	$V_{CS}$	$V_{CC} - V_{SS}$	2.7		31.5	V
Power-On Reset Threshold	POR			1.6		V
Digital Supply Current	$I_{CC}$	(Note 4)		30	50	$\mu A$
Positive Analog Supply Current	$I_{DD}$	MAX5436/MAX5438 $\overline{SHDN} = GND$ for MAX5437/MAX5439		30	60	$\mu A$
		$\overline{SHDN} = V_{CC}$		105	215	
Negative Analog Supply Current	$I_{SS}$	MAX5436/MAX5438 $\overline{SHDN} = GND$ for MAX5437/MAX5439		55	110	$\mu A$
		$\overline{SHDN} = V_{CC}$		130	250	

**Note 1:** The DNL and INL are measured with the potentiometer configured as a voltage-divider with  $H = V_{DD}$  and  $L = V_{SS}$ . The wiper terminal is unloaded.

**Note 2:** The DNL and INL are measured with the potentiometer configured as a variable resistor.  $H$  is unconnected and  $L = V_{SS}$ . The wiper terminal is driven with a source current of  $80\mu A$  for the  $50k\Omega$  configuration and  $40\mu A$  for the  $100k\Omega$  configuration.

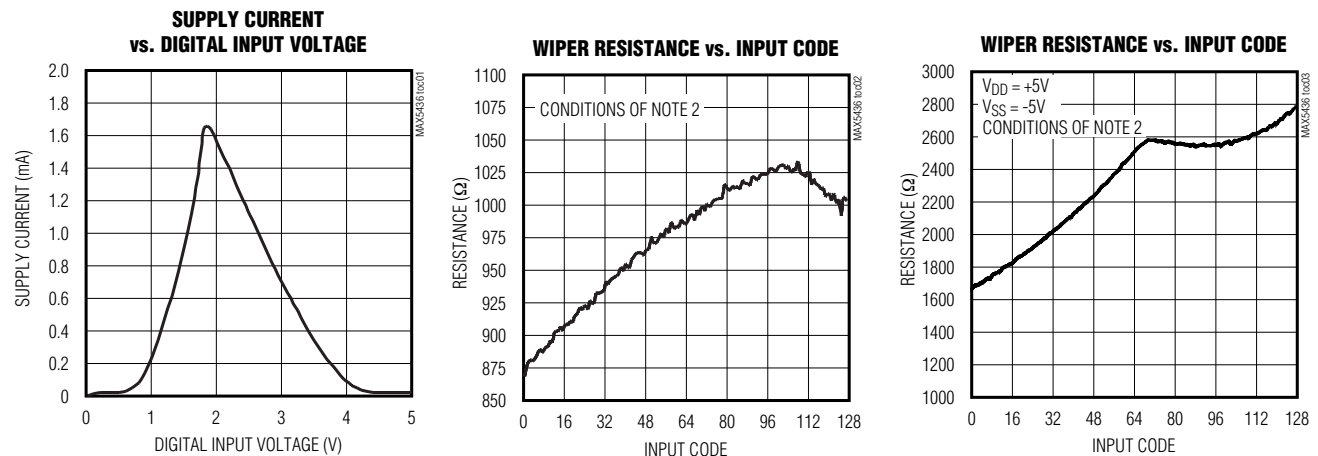
**Note 3:** The wiper resistance is measured assuming the source currents given in Note 2.

**Note 4:** The device draws current in excess of the specified supply current when the digital inputs are driven with voltages between  $(V_{CC} - 0.5V)$  and  $(GND$  to  $5V)$ . See Supply Current vs. Digital Input Voltage in the *Typical Operating Characteristics* section.

**Note 5:** Guaranteed by design and characterization.

## Typical Operating Characteristics

( $V_{DD} = +15V$ ,  $V_{SS} = -15V$ ,  $V_{CC} = +5V$ ,  $V_H = V_{DD}$ ,  $V_L = V_{SS}$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.)



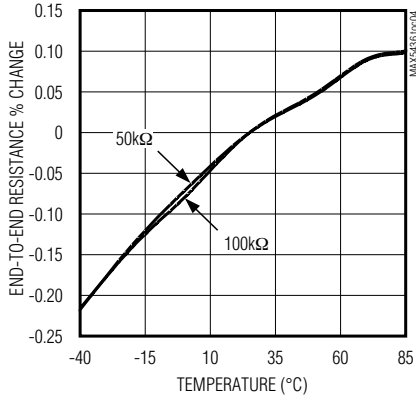
# ±15V, 128-Tap, Low-Drift Digital Potentiometers

MAX5436-MAX5439

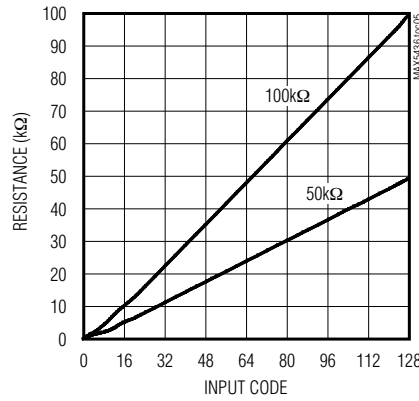
## Typical Operating Characteristics (continued)

( $V_{DD} = +15V$ ,  $V_{SS} = -15V$ ,  $V_{CC} = +5V$ ,  $V_H = V_{DD}$ ,  $V_L = V_{SS}$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

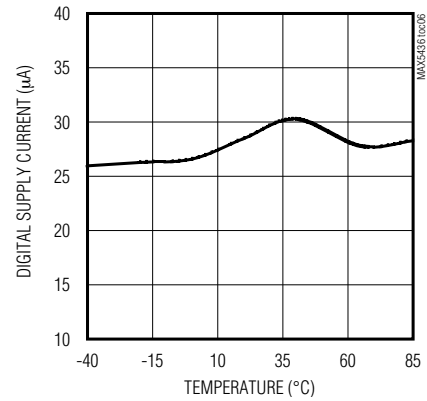
**END-TO-END RESISTANCE % CHANGE vs. TEMPERATURE**



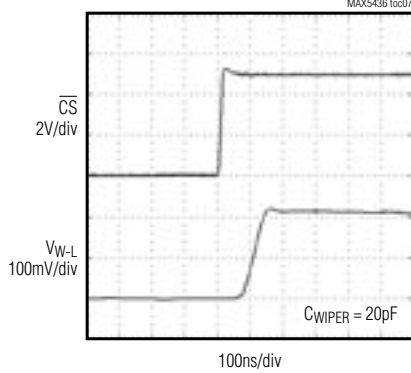
**W-TO-L RESISTANCE CHANGE vs. INPUT CODE**



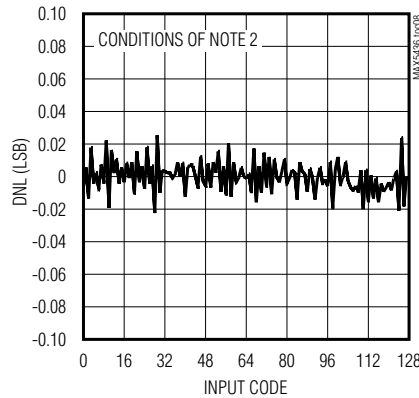
**DIGITAL SUPPLY CURRENT vs. TEMPERATURE**



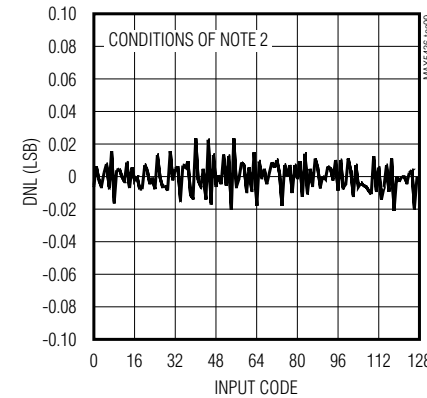
**MIDSCALE SWITCHING TRANSIENT (CODE 63 TO CODE 64)**



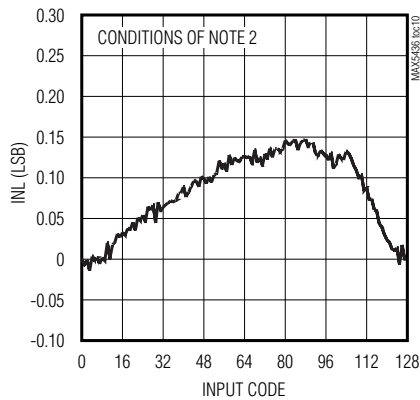
**VARIABLE-RESISTOR DNL vs. INPUT CODE (50kΩ)**



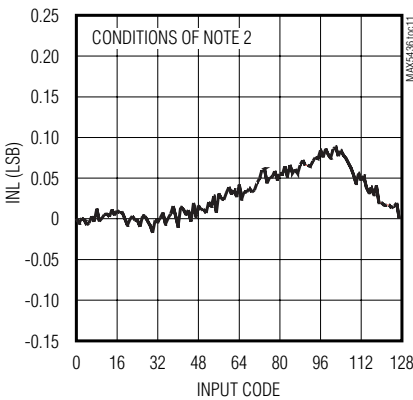
**VARIABLE-RESISTOR DNL vs. INPUT CODE (100kΩ)**



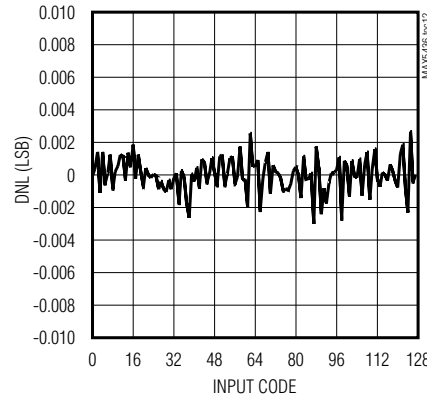
**VARIABLE-RESISTOR INL vs. INPUT CODE (50kΩ)**



**VARIABLE-RESISTOR INL vs. INPUT CODE (100kΩ)**



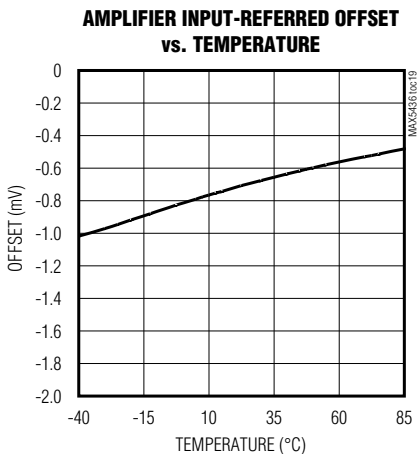
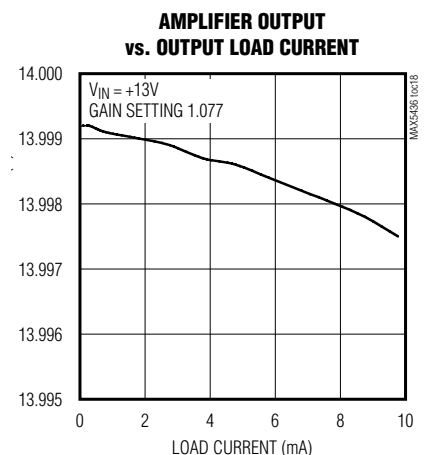
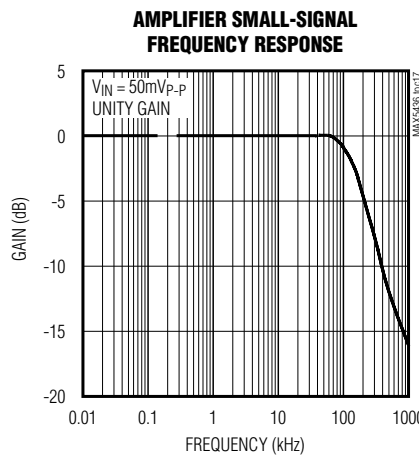
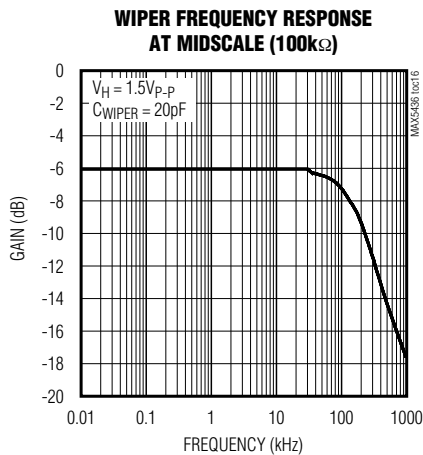
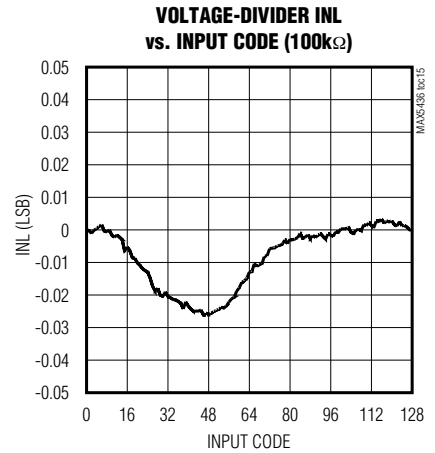
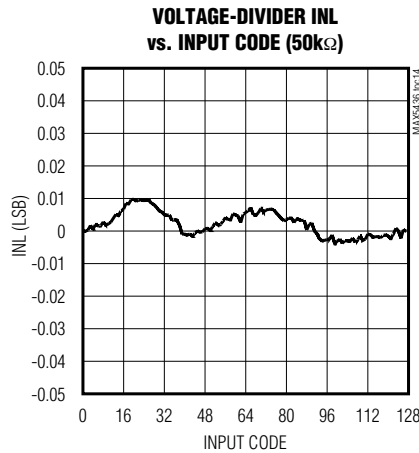
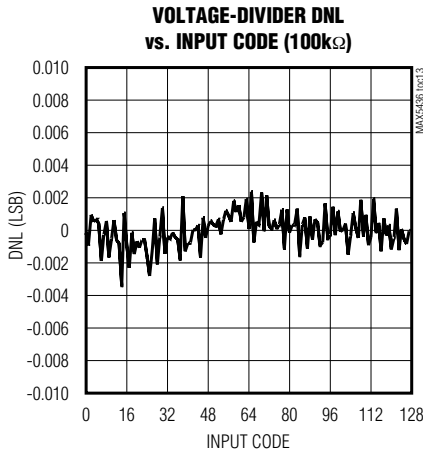
**VOLTAGE-DIVIDER DNL vs. INPUT CODE (50kΩ)**



# ±15V, 128-Tap, Low-Drift Digital Potentiometers

## Typical Operating Characteristics (continued)

( $V_{DD} = +15V$ ,  $V_{SS} = -15V$ ,  $V_{CC} = +5V$ ,  $V_H = V_{DD}$ ,  $V_L = V_{SS}$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



# ±15V, 128-Tap, Low-Drift Digital Potentiometers

**MAX5436-MAX5439**

## Pin Description

PIN		NAME	DESCRIPTION
MAX5436/ MAX5438	MAX5437/ MAX5439		
1	1	SCLK	Serial Clock Input
2	2	DIN	Serial Data Input
3	3	$\overline{\text{CS}}$	Chip Select
—	4	$\overline{\text{SHDN}}$	Amplifier Shutdown
4	5	GND	Analog and Digital Ground
5	6	V <sub>SS</sub>	Negative Analog Supply. Bypass with a 0.1μF capacitor to GND.
—	7	OUT	Amplifier Output
—	8	IN-	Amplifier Negative Input
—	9	IN+	Amplifier Positive Input
6	10	V <sub>DD</sub>	Positive Analog Supply. Bypass with a 0.1μF capacitor to GND.
7	11	H	High Terminal of Resistor
8	12	W	Wiper Terminal of Resistor
9	13	L	Low Terminal of Resistor
10	14	V <sub>CC</sub>	Digital Supply. Bypass with a 0.1μF capacitor to GND.

## Detailed Description

### Digital Interface Operation

The MAX5436–MAX5439 use a 3-wire SPI/QSPI/MICROWIRE-compatible serial data interface to control the wiper position. This write-only interface contains three inputs: chip select ( $\overline{\text{CS}}$ ), data in (DIN), and serial clock (SCLK). When  $\overline{\text{CS}}$  is taken low, data from DIN is synchronously loaded into the serial shift register on the rising edge of each SCLK pulse (Figure 2). The 8-bit data word requires 8 clock pulses to input the serial data. Note that the first bit of the data word, D7, is unused and should be ignored. Therefore, the second rising edge of SCLK loads the MSB. After all the data bits have been shifted in, they are latched into the potentiometer control register when  $\overline{\text{CS}}$  transitions from low to high, the wiper position is then updated. Note that if  $\overline{\text{CS}}$  is not kept low during the entire data stream, the data will be corrupted and the device will need to be reloaded.

## Applications Information

### Power-Up Sequencing

The MAX5436–MAX5439 have been designed so that any of the supplies can turn on first without causing any unwanted crowbar currents to flow. Note that both digital and analog supplies are required to power up the wiper and uncommitted amplifier (MAX5437/MAX5439 only).

### Adjustable Gain Amplifier

The MAX5436/MAX5438 are used with the MAX427 to make a digitally adjustable gain circuit as shown in Figure 4. The normal feedback resistor is replaced with the MAX5436/MAX5438 in a variable-resistor configuration so that the gain of the circuit can be digitally controlled. The MAX5437/MAX5439 can use the internal high-voltage amplifier to make this digitally adjustable gain circuit.

### LCD Biasing Control Applications

The MAX5436–MAX5439 are ideal for LCDs that require separate voltage for contrast control in addition to the main supply voltage. Figure 5a shows the MAX5436–MAX5439 being used for LCD contrast control along with the MAX629, which provides the LCD supply voltage. A similar circuit with an additional buffer circuit is shown in Figure 5b.

# ±15V, 128-Tap, Low-Drift Digital Potentiometers

DATA WORD							
D7	D6	D5	D4	D3	D2	D1	D0
Don't Care	(MSB)						(LSB)
<b>First Bit Loaded</b>							<b>Last Bit Loaded</b>

Figure 1. Serial Data Format

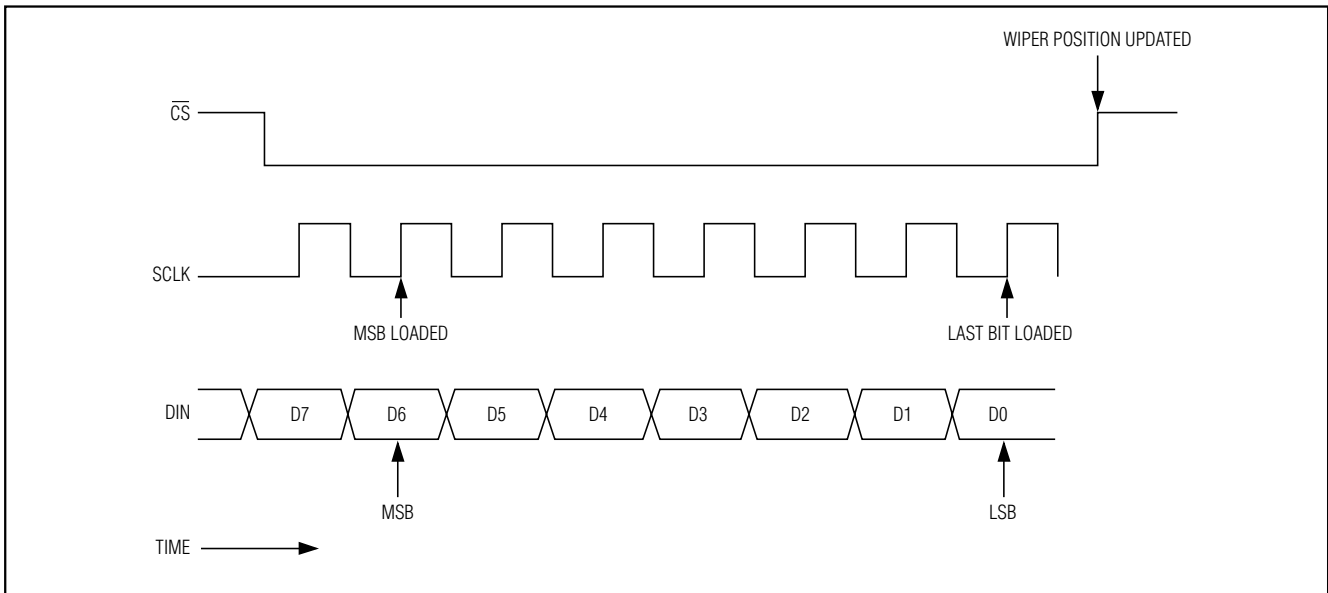


Figure 2. Serial Interface Timing Diagram

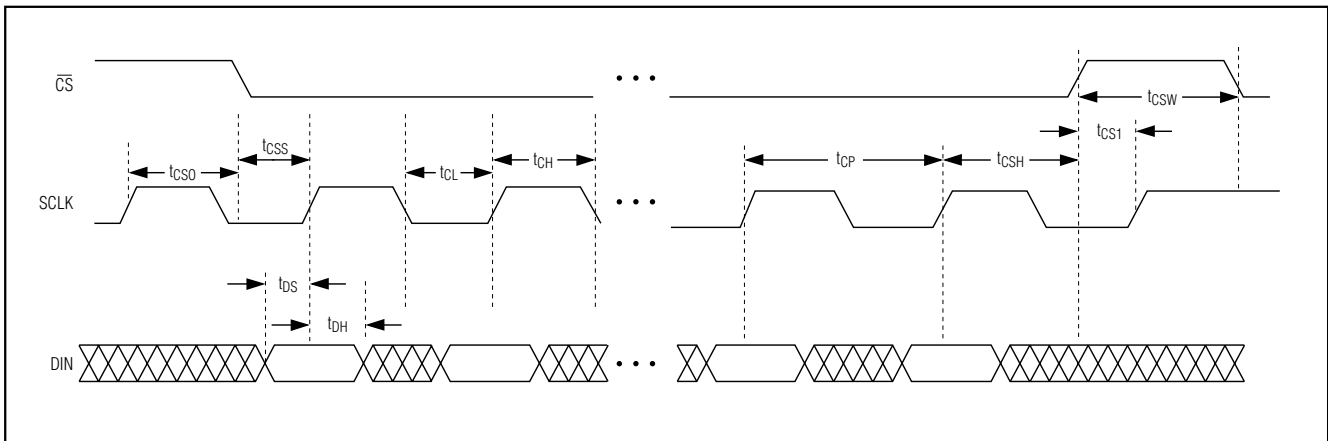


Figure 3. Detailed Serial-Interface Timing Diagram



# ±15V, 128-Tap, Low-Drift Digital Potentiometers

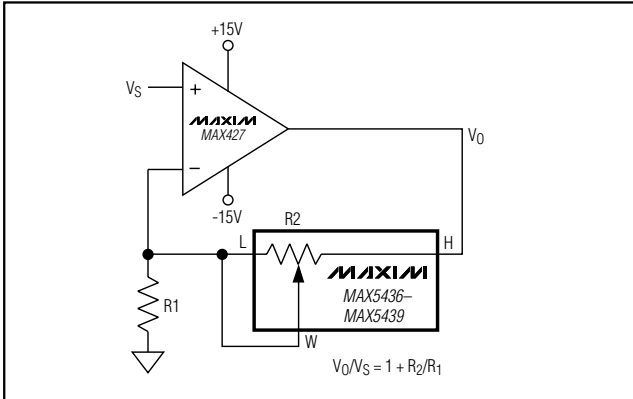


Figure 4. Noninverting Amplifier

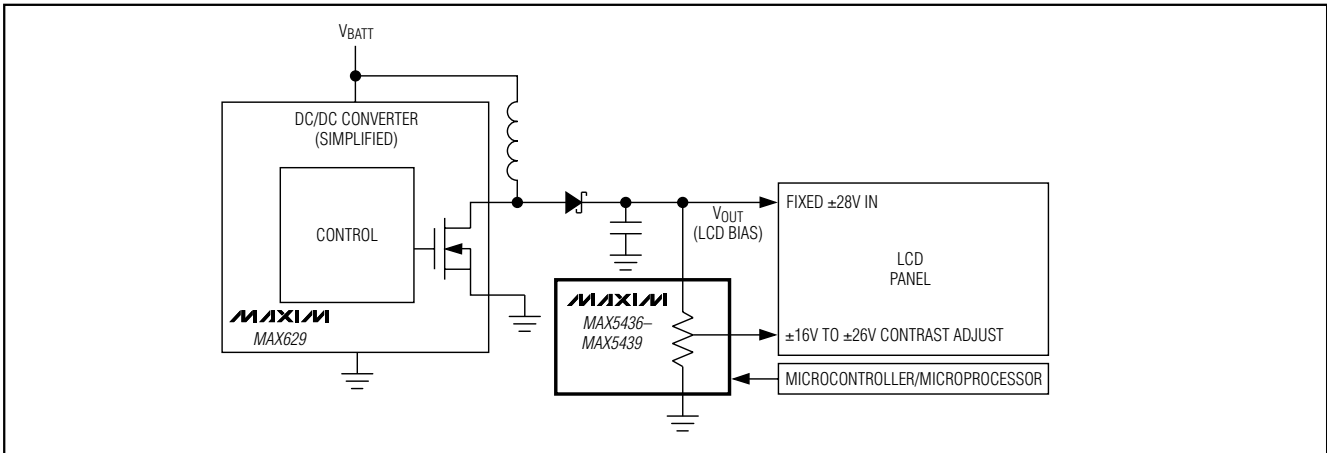


Figure 5a. Simplified LCD Contrast Control Circuit

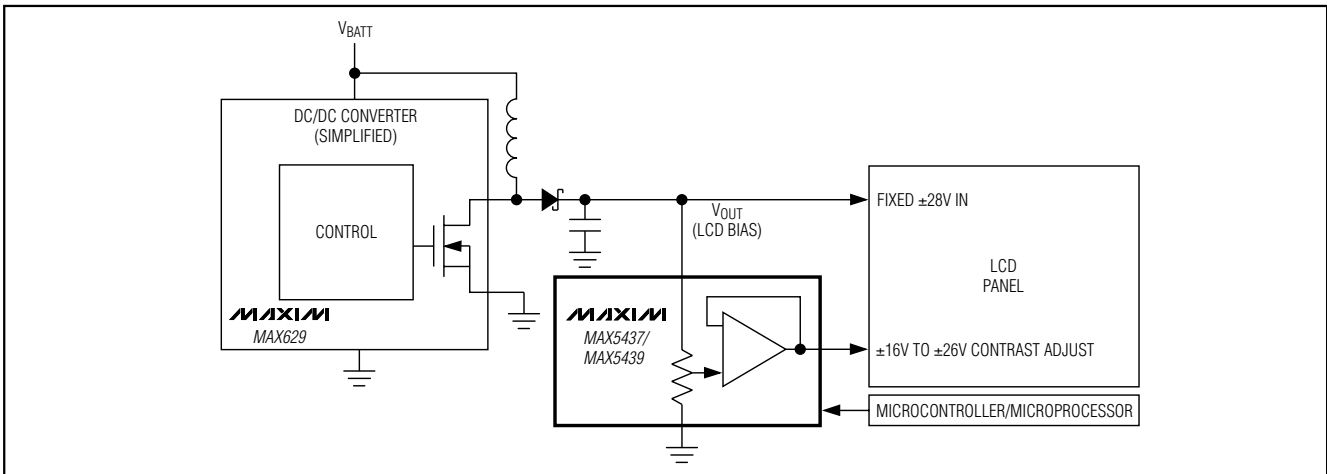
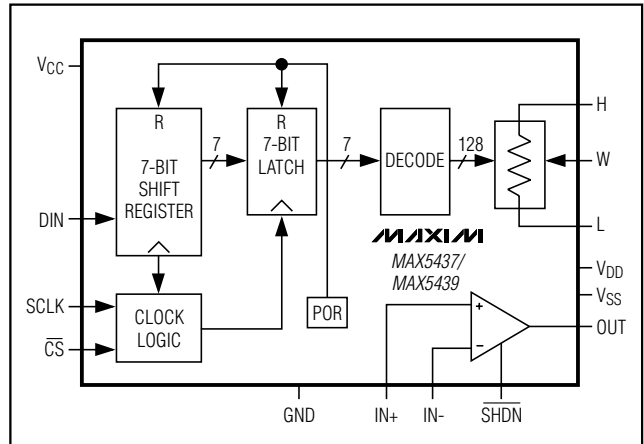
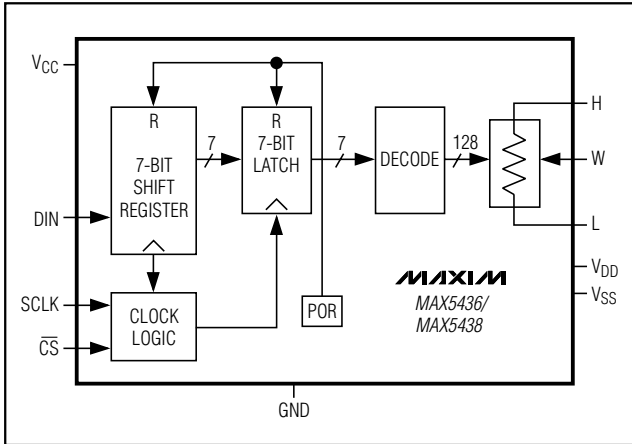


Figure 5b. Simplified LCD Contrast Control Circuit with Buffer

# ±15V, 128-Tap, Low-Drift Digital Potentiometers

## Functional Diagrams



## Chip Information

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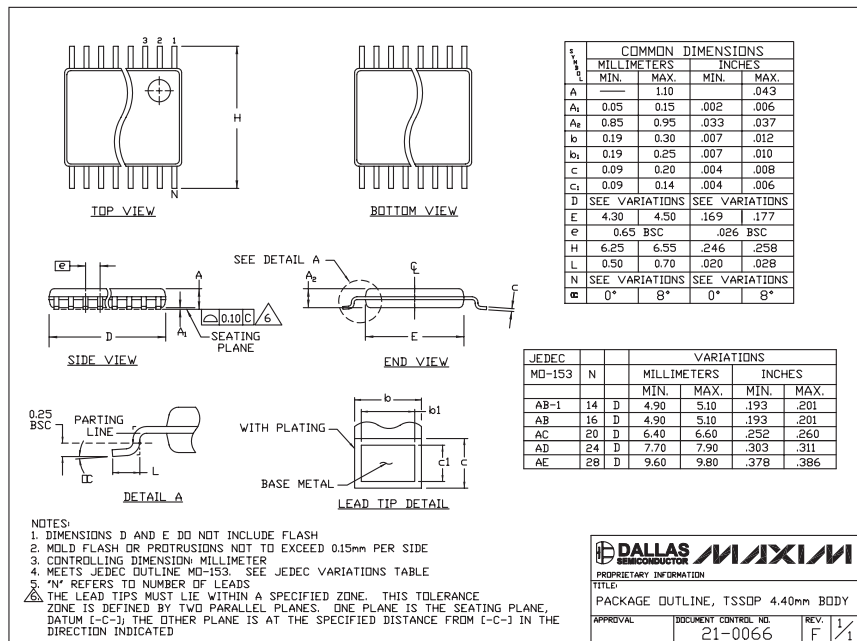
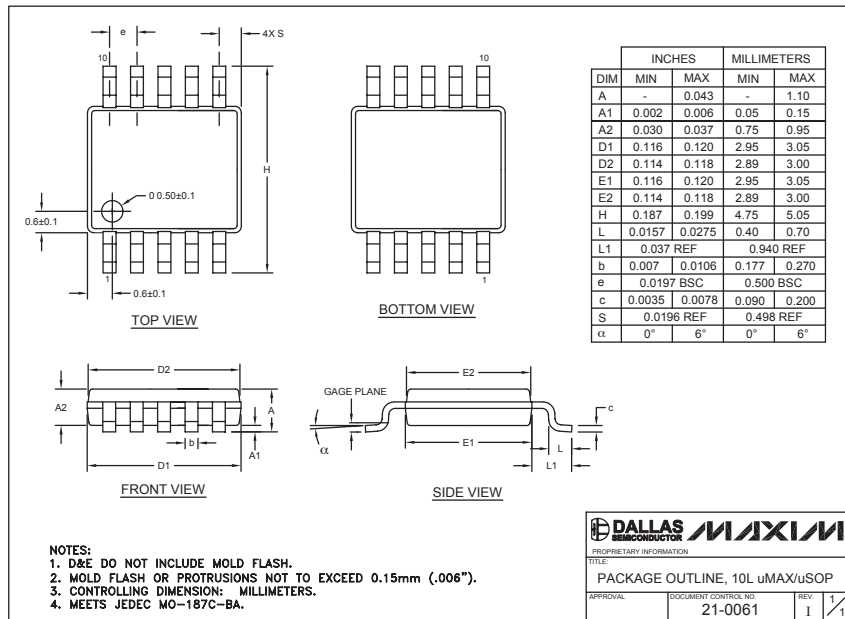
PROCESS: BiCMOS

# ±15V, 128-Tap, Low-Drift Digital Potentiometers

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX5436-MAX5439



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