SAMB11-MR210CA/MR510CA

Ultra Low Power BLE 4.1 Module

DATASHEET

Description

The Atmel® SAMB11-MR210CA is an ultra-low power Bluetooth® SMART (BLE 4.1) module with Integrated MCU, Transceiver, Modem, MAC, PA, TR Switch, and Power Management Unit (PMU). It is a standalone Cortex®-M0 applications processor with embedded Flash memory and BLE connectivity.

The qualified Bluetooth Smart protocol stack is stored in dedicated ROM, the firmware includes L2CAP service layer protocols, Security Manager, Attribute protocol (ATT), Generic Attribute Profile (GATT), and the Generic Access Profile (GAP). Additionally, application profiles such as Proximity, Thermometer, Heart Rate, Blood Pressure, and many others are supported and included in the protocol stack.

The module contains all circuitry required including a ceramic high gain antenna, 26MHz crystal, and PMU circuitry. The customer simply needs to place the module on the board, provide power and a 32KHz Real Time Clock or crystal.

Features

- Complies with Bluetooth V4.1, ETSI EN 300 328 and EN 300 440 Class 2, FCC CFR47 Part 15, ARIB STD-T66, and TELEC
- Bluetooth Certification
  - QD ID Controller (see declaration D028678)
  - QD ID Host (see declaration D028679)
- 2.4GHz transceiver and Modem
  - -95dBm/-93dBm programmable receiver sensitivity
  - -20 to +3dBm programmable TX output power
  - Integrated T/R switch
  - Single wire antenna connection
- ARM® Cortex®-M0 32-bit processor
  - Single wire Debug (SWD) interface
  - 4-channel DMA controller
  - Brown out detector and Power On Reset
  - Watch Dog Timer
- Memory
  - 128kB embedded RAM (96kB available for application)
  - 128kB embedded ROM
  - 256kB Flash
- Hardware Security Accelerators
  - AES-128
  - SHA-256

- Peripherals
  - 23 digital and three wake-up GPIO with 96kΩ Internal Pullup resistors, four Mixed Signal GPIO
  - 2x SPI (Master/Slave)
  - 2x I^2C (Master/Slave)
  - 2x UART
  - 1x SPI Flash
  - 3-axis quadrature decoder
  - 4x Pulse Width Modulation (PWM), three General Purpose Timers, and one Wake up Timer
  - Four channel 11-bit ADC
- Clock
  - Integrated 26MHz oscillator
  - 26MHz crystal oscillator
  - Fully integrated sleep oscillator
- Ultra-low power
  - Less than 1.15µA (8K RAM retention and RTC running)
  - 3.2mA peak TX current (0dBm, 3.6V)
  - 5.0mA peak RX current (3.6V, -95dBm sensitivity)
- Integrated Power management
  - 1.8 - 4.3V input range for PMU
  - 2.3 - 3.6V input range for I/O (limited by Flash memory)
  - Fully integrated Buck DC-DC converter

Table of Contents

1 Ordering Information

Ordering code	Package	Description
ATSAMB11-MR210CA	22 x 15mm	Chip Antenna
ATSAMB11-MR510CA	22 x 15mm	Chip Antenna

The ATSAMB11-MR510CA module is identical to ATSAMB11-MR210CA regarding the module footprint and functionality. The ATSAMB11-MR510CA also includes the capability of hardware encryption.

2 Package Information

Table 2-1. ATSAMB11-MR210/MR510 Module Information (1)

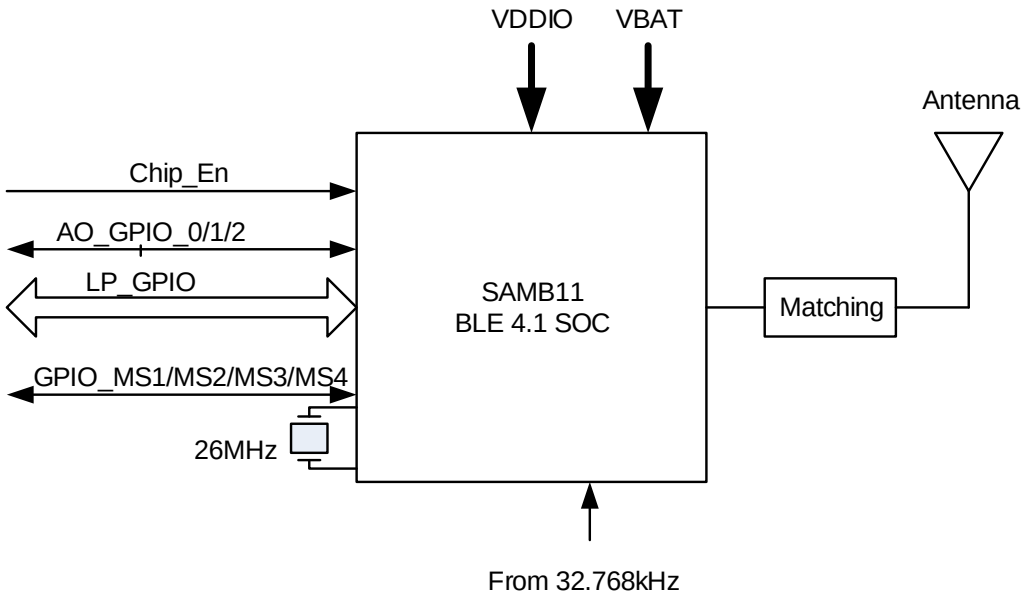
Parameter	Value	Units	Tolerance
Package Size	22.88 X 15.36	mm	
Pad Count	40		
Total Thickness	~2.1	mm	
Pad Pitch	.9002		
Pad Width	.500		
Exposed Pad size	4.4 x 4.4		

Note: 1. For details, see Package Drawing in Section 4.3.

3 Block Diagram

Figure 3-1 shows the block diagram of the SAMB11-MR210CA/MR510 module.

Figure 3-1. Block Diagram

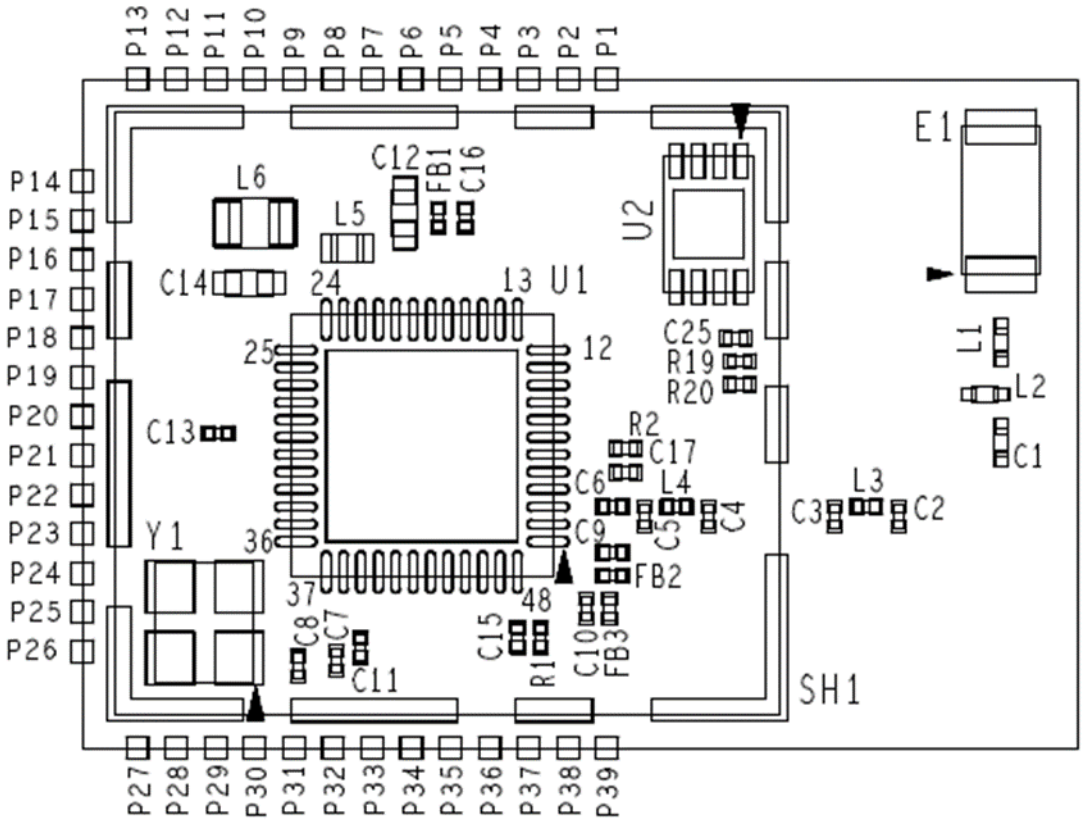


4 Pin Out Information

4.1 Pin Assignment

Figure 4-1 shows the module top view and pin numbering.

Figure 4-1. Top View



4.2 Pin Description

Table 4-1. Pin Description

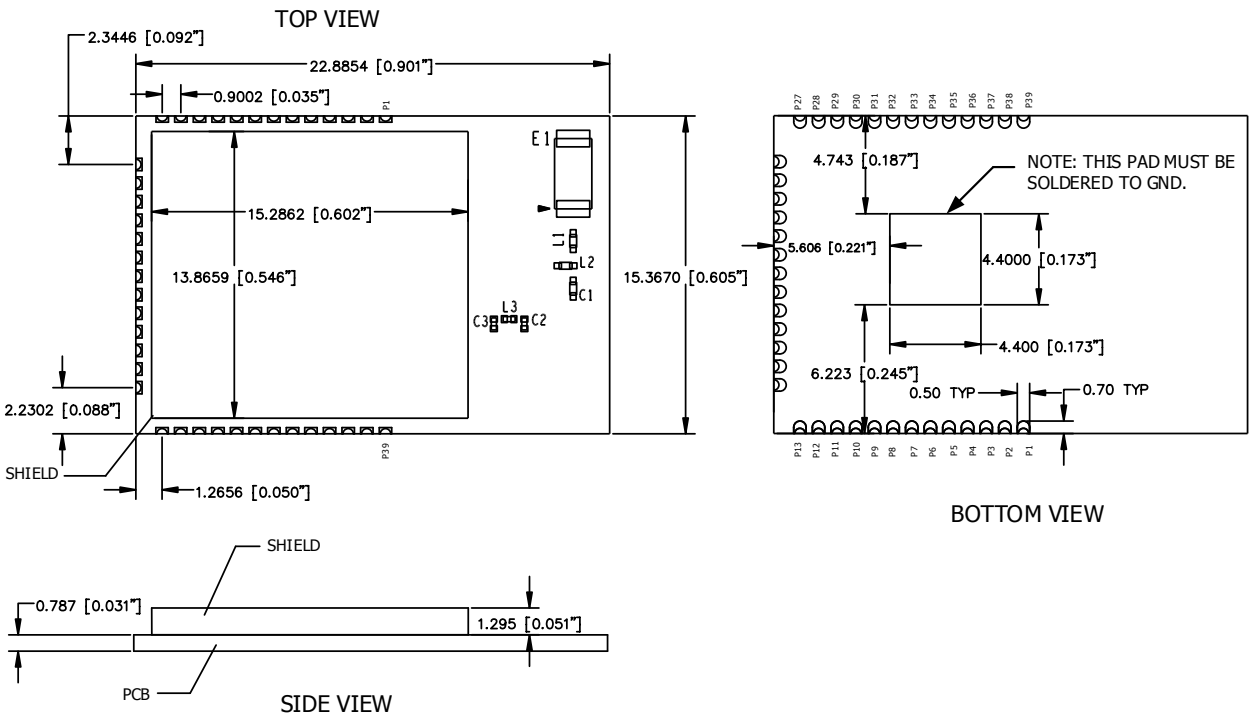
#	Name	Type	Description	Notes
1	Ground	Power	Ground Pin. Connect to PCB ground	
2	LP_GPIO_0	I/O	Used for Single Wire Debug Clock	Debug interface pin. Connect to a header or test point.
3	LP_GPIO_1	I/O	Used for Single Wire Debug Data	Debug interface pin. Connect to a header or test point.
4	VBAT	Power	Power Supply Pin for the on chip Power Management Unit (PMU). Connect to a 1.8V – 4.3V power supply.	
5	LP_GPIO_2	I/O	General Purpose I/O	Default function is Host UART RXD
6	LP_GPIO_3	I/O	General Purpose I/O	Default function is Host UART TXD
7	LP_GPIO_4	I/O	General Purpose I/O	Default function is Host UART CTS
8	LP_GPIO_22	I/O	General Purpose I/O	
9	LP_GPIO_23	I/O	General Purpose I/O	

#	Name	Type	Description	Notes
10	LP_GPIO_5	I/O	General Purpose I/O	Default function is Host UART RTS
11	LP_GPIO_6	I/O	General Purpose I/O	Default function is Debug UART RXD
12	LP_GPIO_7	I/O	General Purpose I/O	Default function is Debug UART TXD
13	LP_GPIO_8	I/O	General Purpose I/O	Default function is I2C_SDA
14	Ground	Power	Ground Pin. Connect to PCB ground	
15	LP_GPIO_9	I/O	General Purpose I/O	Default function is I2C_SCL
16	LP_GPIO_10	I/O	General Purpose I/O	Default function is SPI_SCK
17	LP_GPIO_11	I/O	General Purpose I/O	Default function is SPI_MOSI
18	LP_GPIO_12	I/O	General Purpose I/O	Default function is SPI_SSN
19	LP_GPIO_13	I/O	General Purpose I/O	Default function is SPI_MISO
20	GPIO_MS1	I/O	Mixed Signal I/O	Configurable to be a GPIO or ADC input
21	GPIO_MS2	I/O	Mixed Signal I/O	Configurable to be a GPIO or ADC input
22	Chip_En	Con-trol	Chip Enable. A high level turns on the On Chip PMU and enables oper-ation of the device. Low disables the device and turns off the PMU.	Control this pin with a host GPIO. If not used, tie to VDDIO.
23	GPIO_MS3	I/O	Mixed Signal I/O	Configurable to be a GPIO or ADC input
24	GPIO_MS4	I/O	Mixed Signal I/O	Configurable to be a GPIO or ADC input
25	RTC_CLKP		Positive Pin for Real Time Clock Crystal	Connect to a 32KHz Crystal
26	Ground	Power	Ground Pin. Connect to PCB ground.	
27	RTC_CLKN		Negative Pin for Real Time Clock Crystal	Connect to a 32KHz Crystal
28	AO_GPIO_0	I/O	Always on GPIO_0. Can be used to wake up the device from sleep. Can also be used as a general purpose I/O.	
29	AO_GPIO_1	I/O	Always on GPIO_0. Can be used to wake up the device from sleep. Can also be used as a general purpose I/O.	
30	AO_GPIO_2	I/O	Always on GPIO_0. Can be used to wake up the device from sleep. Can also be used as a general purpose I/O.	
31	LP_GPIO_14	I/O	General Purpose I/O	Default function is Debug I2C_SDA
32	VDDIO	Power	Power Supply Pin for the I/O pins. Connect to a 2.3V – 3.6V power supply.	I/O supply can be less than or equal to VBAT
33	LP_GPIO_15	I/O	General Purpose I/O	Default function is Debug I2C_SCL
34	LP_GPIO_16	I/O	General Purpose I/O	
35	LP_GPIO_17	I/O	General Purpose I/O	
36	LP_GPIO_18	I/O	General Purpose I/O	
37	LP_GPIO_19	I/O	General Purpose I/O	
38	LP_GPIO_20	I/O	General Purpose I/O	
39	Ground	Power	Ground Pin. Connect to PCB ground.	
40	Paddle	Power	Center Ground Paddle	Connect to inner PCB ground plane with an array of vias

4.3 Module Outline Drawing

Figure 4-2 shows the bottom view of the module and the module dimensions. All dimensions are in millimeters.

Figure 4-2. Module Dimensions (millimeters)



5 Electrical Specifications

5.1 Absolute Maximum Ratings

Table 5-1. SAMB11-MR210CA Absolute Maximum Ratings

Symbol	Characteristic	Min.	Max.	Unit
VDDIO	I/O Supply Voltage	-0.3	4.6	V
VBAT	Battery Supply Voltage	-0.3	5.0	V
V_{IN} (1)	Digital Input Voltage	-0.3	VDDIO	V
V_{AIN} (2)	Analog Input Voltage	-0.3	1.5	V
V_{ESDHBM} (3)	ESD Human Body Model	-1000, -2000 (see notes below)	+1000, +2000 (see notes below)	V
T_A	Storage Temperature	-65	150	°C
	Junction Temperature		125	°C

Note:
1. V_{IN} corresponds to all the digital pins.
2. V_{AIN} corresponds to the following analog pins: RFIO.
3. For V_{ESDHBM}, each pin is classified as Class 1, or Class 2, or both:
   - The Class 1 pins include all the pins (both analog and digital)
   - The Class 2 pins include all digital pins only
   - V_{ESDHBM} is ±1kV for Class1 pins. V_{ESDHBM} is ±2kV for Class2 pins

5.2 Recommended Operating Conditions

Table 5-2. SAMB11-MR210CA Recommended Operating Conditions

Symbol	Characteristic	Min.	Typ.	Max.	Units
VDDIO	I/O Supply Voltage Low Range	2.3	3.3	4.3	V
VBAT	Battery Supply Voltage	1.8 (1)	3.6	4.3	V
	Operating Temperature	-40		85	˚C

Note: 1. VBAT supply must be greater than or equal to VDDIO.

5.3 Restrictions for Power States

When VDDIO is off (either disconnected or at ground potential), a voltage must not be applied to the device pins. This is because each pin contains an ESD diode from the pin to the VDDIO supply. This diode will turn on when a voltage higher than one diode-drop is supplied to the pin. This in turn will try to power up the part through the VDDIO supply.

If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than 0.3V below ground to any pin.

5.4 Power-up Sequence

The power-up/down sequence for ATSAMB1-MR210A is shown in Figure 5-1. The timing parameters are provided in Table 5-3.

Figure 5-1. Power-up Sequence

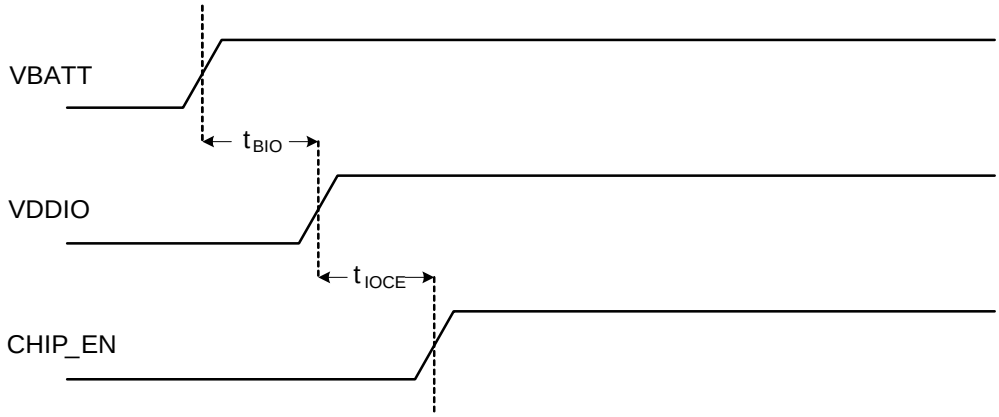


Table 5-3. Power-Up Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t_{BIO}	0		ms	VBAT rise to VDDIO rise	VBAT and VDDIO can rise simultaneously or can be tied together
t_{IOCE}	0			VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating

5.5 RTC Pins

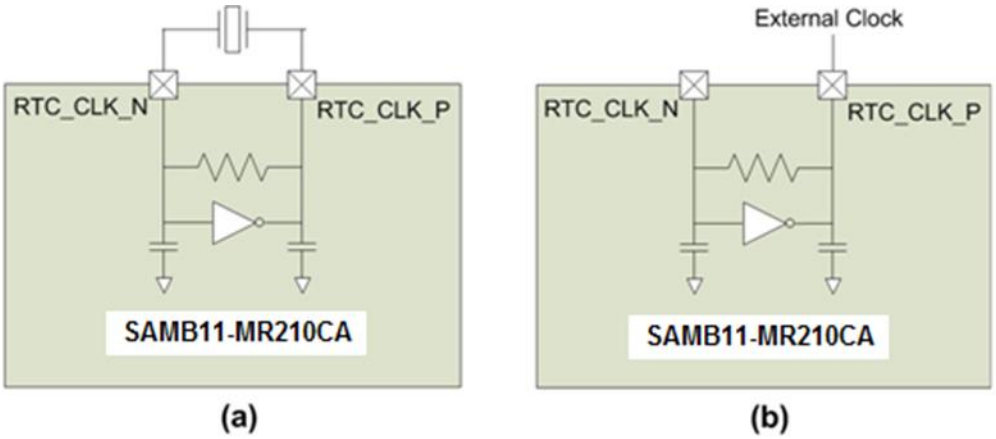
Module pins 25 and 27 (RTC_CLKP and RTC_CLKN, respectively) are used for a 32.768kHz crystal. To be compliant with the BLE specifications for connection events, the frequency accuracy of this clock has to be within ±500ppm. Because of the high accuracy of the 32.768kHz crystal oscillator clock (±25ppm), the power consumption can be minimized by leaving radio circuits in low power sleep mode for as long as possible until they need to wake up for the next connection timed event.

The block diagram in Figure 5-2(a) shows how the internal low frequency Crystal Oscillator (XO) is connected to the external crystal.

Typically, the crystal should be chosen to have a load capacitance of 7pF to minimize the oscillator current. The SAMB11 device has switchable on chip capacitance that can be used to adjust the total load the crystal sees to meet its load capacitance specification. Refer to the SAMB11 datasheet for more information.

Alternatively, if an external 32.768kHz clock is available, it can be used to drive the RTC_CLKP pin instead of using a crystal. The XO has 5.625F internal capacitance on the RTC_CLKP pin. To bypass the crystal oscillator an external signal capable of driving 5.625pF can be applied to the RTC_CLK_P terminal as shown in Figure 5-2(b). This signal must be 1.2V maximum. RTC_CLK_N must be left unconnected when driving an external source into RTC_CLK_P.

Figure 5-2. SAMB11 XO Connections to Low Frequency Crystal Oscillator



(a) Crystal oscillator is used (b) Crystal oscillator is bypassed

Table 5-4. SAMB11-MR210CA 32.768kHz External Clock Specification

Parameter	Min.	Typ.	Max.	Unit.	Comments
Oscillation frequency		32.768		kHz	Must be able to drive 6pF load @ desired frequency
VinH	0.7		1.2	V	High level input voltage
VinL	0		0.2	V	Low level input voltage
Stability – Temperature	-250		+250	ppm	

6 Characteristics

6.1 Device States

Table 6-1. SAMB11-MR210CA Device States

Device State	CHIP_EN	VDDIO	$I_{VBAT\ (typical)}$	$I_{VDDIO\ (typical)}$	Remark
BLE_On_Transmit	On	On	3.0mA	0.2µA	VBAT = 3.6V
BLE_On_Receive	On	On	4.2mA	0.2µA	VBAT = 3.6V
Ultra Low Power	On	On	1.25µA	0.1µA	With 8KB retention memory, BLE Timer and RTC enabled
Power_Down	GND	On	<0.05µA	<0.05µA	Chip Enable Off

6.2 Receiver Performance

Table 6-2. SAMB11-MR210CA Receiver Performance

Parameter	Unit	Min.	Typ.(1)	Max.
Frequency	MHz	2,402	-	2,480
Sensitivity (max. RX Gain setting)	dBm		-95	
Maximum Receive Signal Level	dBm		0	
CCI	dB		13	
ACI (N±1)	dB		0	
N+2 Blocker (Image)	dB		-20	
N-2 Blocker	dB		-30	
N+3 Blocker (Adj. Image)	dB		-32	
N-3 Blocker	dB		-44	
N±4 or greater	dB	-45		
Intermod (N+3, N+6)	dBm		-33	
OOB (2GHz<f<2.399GHz)	dBm		-10	
OOB (f<2GHz)	dBm		-10	

Note: 1. Expected values for production silicon.

All measurements performed at 3.6V VBAT and 25°C, with tests following Bluetooth V4.1 standard tests.

6.3 Transmitter Performance

Table 6-3. SAMB11-MR210CA Transmitter Performance

Parameter	Unit	Min.	Typ.	Max.
Frequency	MHz	2,402		2,480
Output Power Range	dBm	-20		3.5
Output Power	dBm	-55		
In-band Spurious (N±2)	dBm		-40	
In-band Spurious (N±3)	dBm		-50	
2nd Harmonic Pout	dBm		-45	
Frequency Dev	kHz		250	

All measurements performed at 3.6V VBAT and 25°C, with tests following Bluetooth V4.1 standard tests.

Average advertising current for connectable beacon with full payload (37-byte packet) is targeted to be 9.7µA. The average advertising current is based on automatic advertising from the ROM with RTC 32kHz, BLE sleep timers, and 8KB memory retention. IDRAM1 and IDRAM2 are OFF. External Peripherals and debug clocks are turned OFF. VBAT is set to 3.6V. This advertising current will be enabled on a future SDK release. For current SDK based advertising current, see errata Chapter 13.

7 Application Schematic

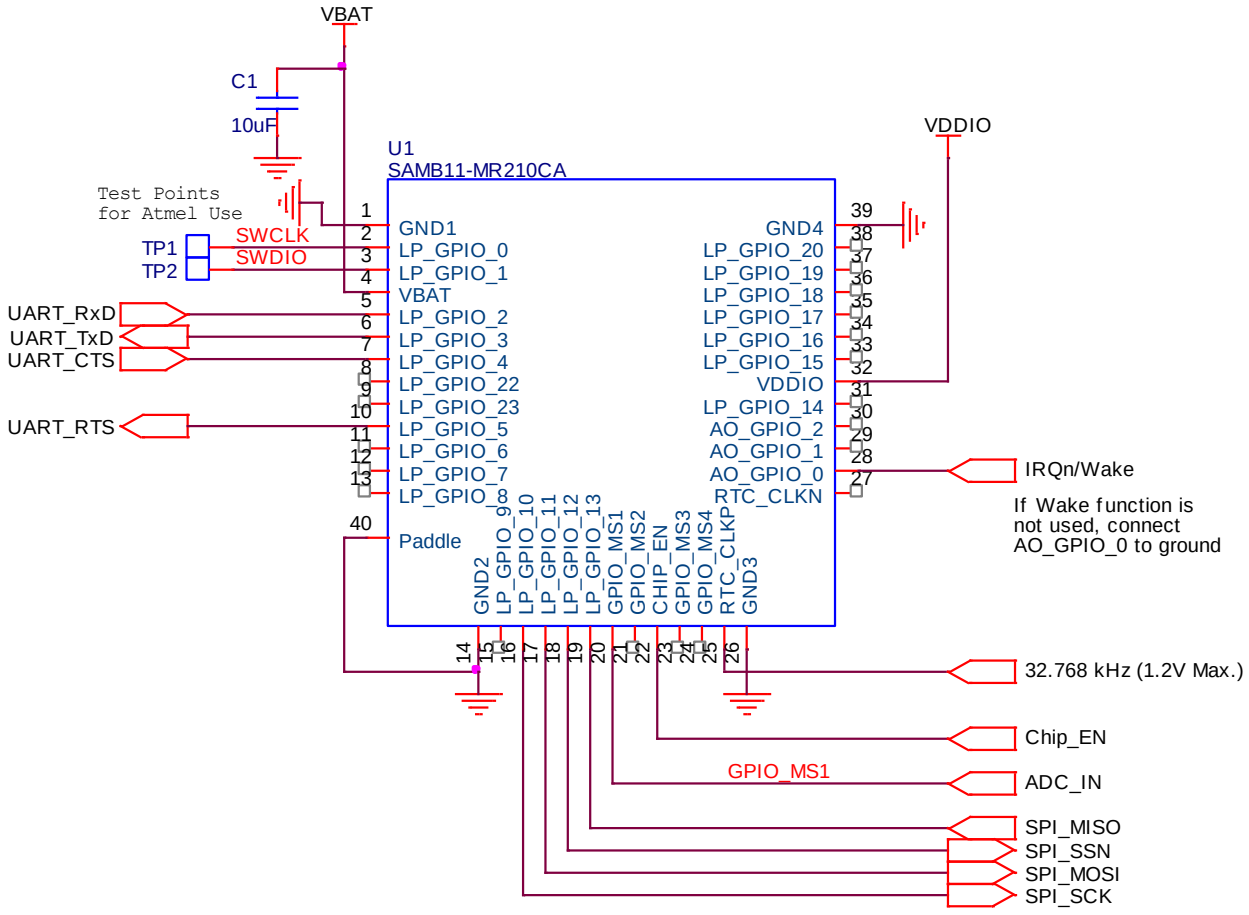
The SAMB11-MR210/MR510CA modules are fully self-contained. To use the module, just provide VBAT and VDDIO supplies. Figure 7-1 and Figure 7-2 shows a typical design using the SAMB11-MR210/MR510CA modules. The schematic shows several host interfaces: UART, I^2C, and SPI as well as an input to the ADC on the GPIO_MS1 pin. A user can choose the interface(s) required for their application. If a 32.768kHz Real Time Clock is not available in the system, a 32.768KHz crystal can be used. Section 7.2 shows a design using a crystal for the Real Time Clock. The crystal should be specified with a load capacitance, C_L=7pF and a total frequency error of 200ppm. Table 7-1 shows the BOM for the application schematics.

Note: The UART RTS and UART CTS are used for hardware flow control; they MUST be connected to the host MCU UART and enabled for the UART interface to be functional.

Module design information such as module schematics can be obtained under an NDA from Atmel.

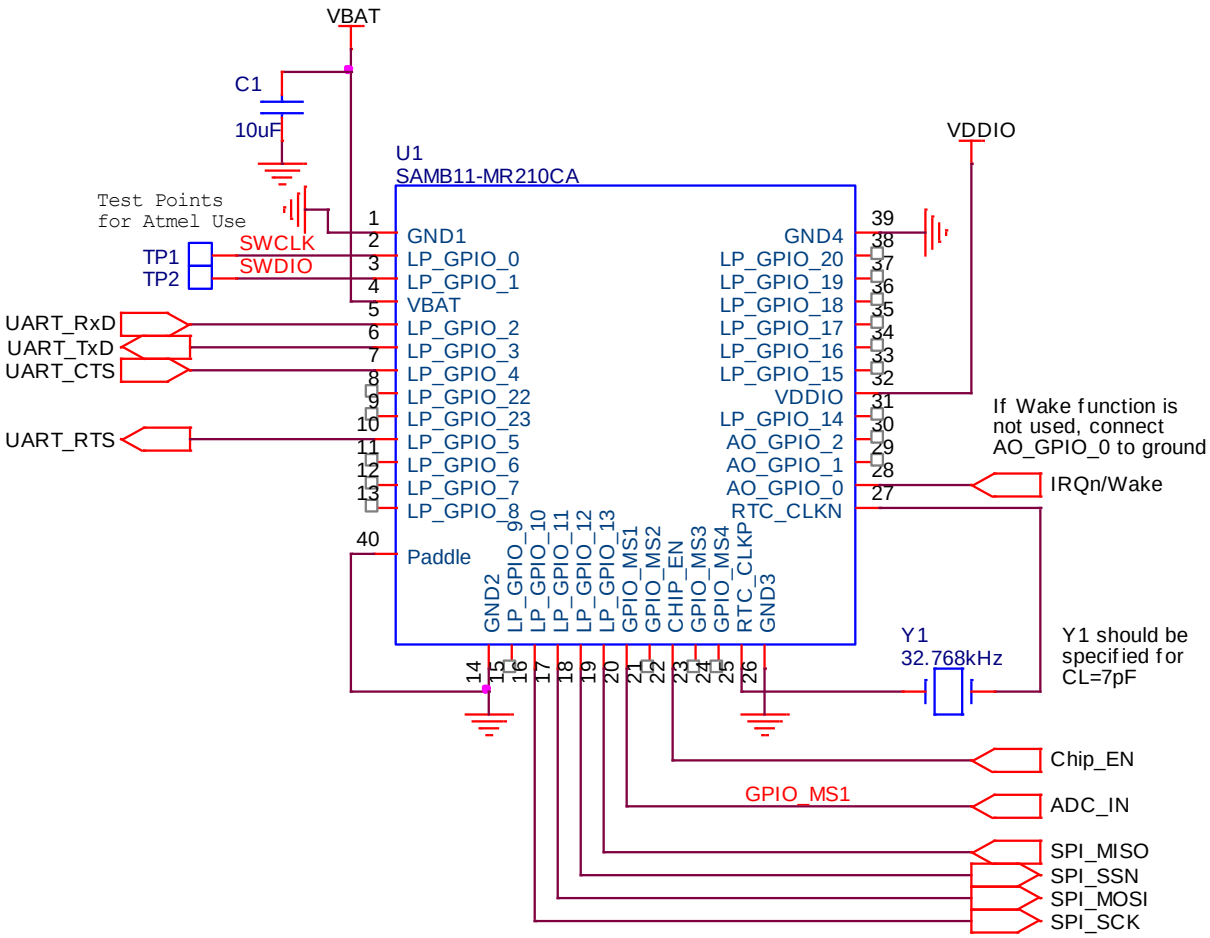
7.1 Application Schematic

Figure 7-1. Application Schematic



7.2 Applications Schematic with 32.768kHz Crystal

Figure 7-2. Application Schematic with 32.768kHz Crystal



7.3 Application Schematic BOM

Table 7-1. Application Schematic BOM

Item	Qty.	Ref.	Value	Description	Manufacturer	Part #
1	1	C1	10µF	CAP,CER,10µF,20%,X5R,0603,6.3V	Panasonic	ECI-1VB0I106M
2	2	TP1, TP2		Test point		
3	1	U1	SAMB11-MR210CA	Module, BLE, SAMB11	Atmel	SAMB11-MR210CA
4	1	Y1	32.768KHz	XTAL, 32.768KHz, ±20ppm, -40 to +85°C, CL=7pF, 2 lead, SM	ECS	ECS-.327-7-34B-TR

8 Placement and Routing Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance:

- The board should have a solid ground plane. The center ground pad of the device must be solidly connected to the ground plane by using a 3x3 grid of vias. Each ground pin of the module should have a ground via placed either in the pad or right next to the pad going down to the ground plane.
- When the module is placed on the motherboard, a provision for the antenna must be made. There should be nothing under the portion of the module which contains the antenna. This means the antenna should not be placed directly on top of the motherboard PCB. This can be accomplished by, for example, placing the module at the edge of the board such that the module edge with the antenna extends beyond the main board edge by 6.5mm. Alternatively, a cut out in the motherboard can be provided under the antenna. The cutout should be at least 22mm x 6.5mm. Ground vias spaced 2.5mm apart should be placed all around the perimeter of the cutout. No large components should be placed near the antenna.
- Keep away from antenna, as far as possible, large metal objects to avoid electromagnetic field blocking
- Do not enclose the antenna within a metal shield
- Keep any components which may radiate noise or signals within the 2.4GHz – 2.5GHz frequency band far away from the antenna or better yet, shield those components. Any noise radiated from the main board in this frequency band will degrade the sensitivity of the module.

8.1 Power and Ground

Dedicate one layer as a ground plane. Make sure that this ground plane does not get broken up by routes. Power can route on all layers except the ground layer. Power supply routes should be heavy copper fill planes to insure the lowest possible inductance. The power pins of the module should have a via directly to the power plane as close to the pin as possible. Decoupling capacitors should have a via right next to the capacitor pin and this via should go directly down to the power plane – that is to say, the capacitor should not route to the power plane through a long trace. The ground side of the decoupling capacitor should have a via right next to the pad which goes directly down to the ground plane. Each decoupling capacitor should have its own via directly to the ground plane and directly to the power plane right next to the pad. The decoupling capacitors should be placed as close to the pin that it is filtering as possible.

9 Interferers

One of the biggest problems with RF receivers is poor performance due to interferers on the board radiating noise into the antenna or coupling into the RF traces going to input LNA. Care must be taken to make sure that there is no noisy circuitry placed anywhere near the antenna or the RF traces. All noise generating circuits should also be shielded so they do not radiate noise that is picked up by the antenna.

10 Reflow Profile Information

This section provides guidelines for reflow processes in getting the Atmel module soldered to the customer's design.

10.1 Storage Conditions

10.1.1 Moisture Barrier Bag Before Opened

A moisture barrier bag must be stored in a temperature of less than 30°C with humidity under 85% RH.

The calculated shelf life for the dry-packed product shall be 12 months from the date the bag is sealed.

10.1.2 Moisture Barrier Bag Open

Humidity indicator cards must be blue, <30%.

10.2 Stencil Design

The recommended stencil is laser-cut, stainless-steel type with thickness of 100µm to 130µm and approximately a 1:1 ratio of stencil opening to pad dimension. To improve paste release, a positive taper with bottom opening 25µm larger than the top can be utilized. Local manufacturing experience may find other combinations of stencil thickness and aperture size to get good results.

10.3 Baking Conditions

This module is rated at MSL level 3. After sealed bag is opened, no baking is required within 168 hours so long as the devices are held at ≤30°C/60% RH or stored at <10% RH.

The module will require baking before mounting if:

- The sealed bag has been open for >168 hours
- Humidity Indicator Card reads >10%
- SIPs need to be baked for 8 hours at 125°C

10.4 Soldering and Reflow Condition

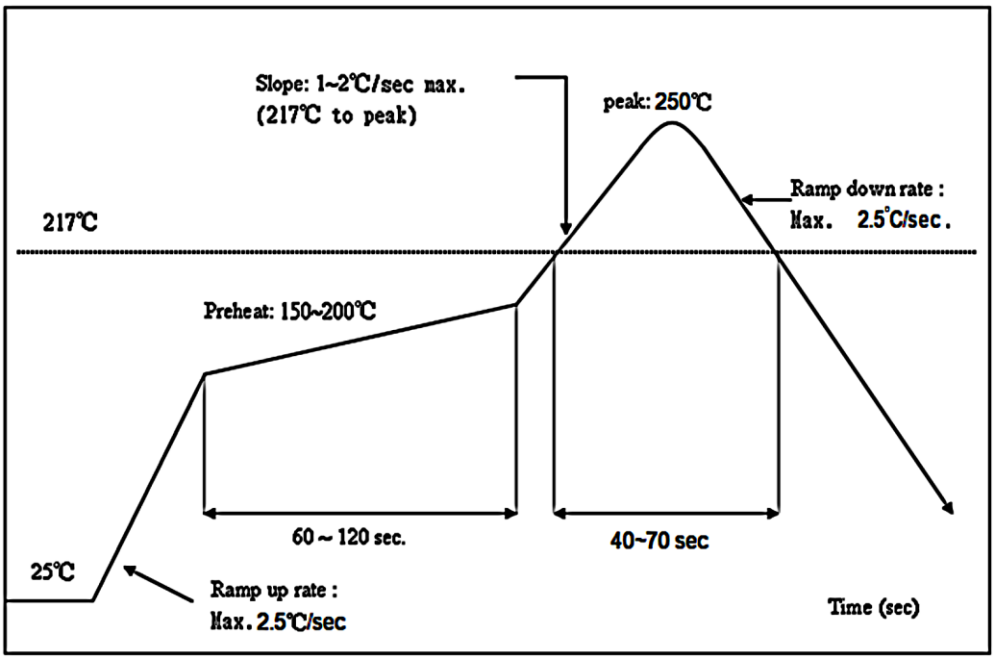
10.4.1 Reflow Oven

It is strongly recommended that a reflow oven equipped with more heating zones and Nitrogen atmosphere be used for lead-free assembly. Nitrogen atmosphere has shown to improve the wet-ability and reduce temperature gradient across the board. It can also enhance the appearance of the solder joints by reducing the effects of oxidation.

The following bullet items should also be observed in the reflow process:

- Some recommended pastes include NC-SMQ® 230 flux and Indalloy® 241 solder paste made up of 95.5 Sn/3.8 Ag/0.7 Cu or SENJU N705-GRN3360-K2-V Type 3, no clean paste.
- Allowable reflow soldering times: 2 times based on the following reflow soldering profile (see Figure 10-1).
- Temperature profile: Reflow soldering shall be done according to the following temperature profile (see Figure 10-1).
- Peak temperature: 250°C.

Figure 10-1. Solder Reflow Profile



11 Reference Documentation and Support

11.1 Reference Documents

Atmel offers a set of collateral documentation to ease integration and device ramp. The following table list documents available on Atmel web or integrated into development tools.

Table 11-1. Reference Documents

Title	Content
Datasheet	This document
SAMB11 SOC Preliminary Datasheet	Data sheet for the SAMB11 SOC contained on this module
SW Design Guide	Integration guide with clear description of: High level Arch, overview on how to write a networking application, list all API, parameters and structures. Features of the device, SPI/handshake protocol between device and host MCU, with flow/sequence/state diagram, timing.
SW Programmer guide	Explain in details the flow chart and how to use each API to implement all generic use cases (e.g. start AP, start STA, provisioning, UDP, TCP, http, TLS, p2p, errors management, connection/transfer recovery mechanism/state diagram) - usage and sample application note

For a complete listing of development-support tools and documentation, visit http://www.atmel.com/, or contact the nearest Atmel field representative.

12 Certifications

12.1 Agency Compliance

The ATSAMB11-MR210CA has been tested and certified to meet the compliance for the following agencies:

- Bluetooth 4.1 – The SAMB11-MR210 utilizes the ATBTLC1000 Bluetooth die for Bluetooth operation. Refer to these QD ID reference numbers for Bluetooth certifications.
  - QD ID Controller (see declaration D028678)
  - QD ID Host: (see declaration D028679)
- FCC
  - FCC ID: 2ADHKSAMB11
    - CFR47 Part 15
- ETSI
  - EN 300 328
  - EN 300 400 Class 2
- ARIB
  - STD-T66
- TELEC

13 Errata

Issue: In the ATSAMB11 Datasheet, the measured advertisement current for the cases listed in Table 6-3 will be higher than what is reported.

SDK5.0 does not resemble the same conditions where Table 6-3 has been measured.

For example:

- The power and timing parameters in the SDK5.0 release have not been fully optimized to their final values
- IDRAM1 and IDRAM2 are always enabled/retained for ROM patches and application development
- SDK5.0 enables clocks to different peripheral blocks to allow easier application development
- Continuous access to the SWD debug interface is needed. Therefore, debug clocks cannot be turned OFF.

A small sample measurement has been performed they show the following results:

Measurement condition:

- 1-sec adverting interval
- 37 byte advertising payload
- Connectable beacon
- Advertising on 3 channels (37,38,39)
- VBAT and VDDIO are set to 3.3V

Average advertising current: 13.65µA

Average sleep current between beacons: 2.00µA

With VBAT set to 3.6V, the average advertising current under the same conditions is 12.67µA.

14 Document Revision History

Doc Rev.	Date	Comments
42498C	02/2016	Some minor corrections in text and layout. 1. Added text referring to SAMB11-MR510CA devices. 2. Updated Module drawing in Figure 4-2. 3. Updated schematic information in Section 7 and added revised Application schematic figures to Figure 7-1 and Figure 7-2. 4. Revised Reflow Profile Section 10.
42498B	02/2016	1. Changed pins in Table 4-1 to add UART flow control. 2. Added UART flow control requirement in Chapter 7. 3. Updated Application Schematics in Chapter 7. 4. Added Agency certifications in Chapter 12. 5. Added full module drawing in Figure 4-2. 6. Revised Table 6-1 to remove footnote that is no longer applicable. 7. Added application Schematic BOM in Table 7-1. 8. Clearer reference schematic for SAMB11-MR210 in Figure 7.1. 9. Clearer BOM for SAMB11-MR210 in Figure 7-2. 10. Added reference schematic in Figure 7-3. 11. Added BOM for SAMB11-MR510 in Figure 7-4. 12. Added comment to Table 6-3. 13. Added Errata (Chapter 13).
42498A	09/2015	Initial document release.

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Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**