

# GDDR5 SGRAM

## EDW4032BABG – 8 Meg x 32 I/O x 16 banks, 16 Meg x 16 I/O x 16 banks

### Features

- $V_{DD} = V_{DDQ} = 1.6V/1.55V/1.5V \pm 3\%$  and  $1.35V \pm 3\%$
- Data rate: 6.0 Gb/s, 7.0 Gb/s, 8.0 Gb/s (MAX)
- 16 internal banks
- Four bank groups for  $t_{CCDL} = 3 t_{CK}$
- 8n-bit prefetch architecture: 256-bit per array read or write access for x32; 128-bit for x16
- Burst length (BL): 8 only
- Programmable CAS latency: 6–27
- Programmable WRITE latency: 3–7
- Programmable CRC READ latency: 1–3
- Programmable CRC WRITE latency: 8–14
- Programmable EDC hold pattern for CDR
- Precharge: Auto option for each burst access
- Auto refresh and self refresh modes
- Refresh cycles: 16,384 cycles/32ms
- Interface: Pseudo open drain (POD-15) compatible outputs: 40Ω pull-down, 60Ω pull-up
- On-die termination (ODT): 60Ω or 120Ω (NOM)
- ODT and output driver strength auto calibration with external resistor ZQ pin: 120Ω
- Programmable termination and driver strength off-sets
- Selectable external or internal  $V_{REF}$  for data inputs; programmable offsets for internal  $V_{REF}$
- Separate external  $V_{REF}$  for address/command inputs
- $T_C = 0^\circ\text{C}$  to  $+95^\circ\text{C}$
- x32/x16 mode configuration set at power-up with EDC pin
- Single-ended interface for data, address, and command
- Quarter data rate differential clock inputs CK\_t, CK\_c for address and commands
- Two half data rate differential clock inputs, WCK\_t and WCK\_c, each associated with two data bytes (DQ, DBI\_n, EDC)
- DDR data (WCK) and addressing (CK)
- SDR command (CK)
- Write data mask function via address bus (single/double byte mask)
- Data bus inversion (DBI) and address bus inversion (ABI)
- Input/output PLL on/off mode
- Duty cycle corrector (DCC) for data clock (WCK)
- Digital RAS lockout

- Address training: Address input monitoring via DQ pins
- WCK2CK clock training: Phase information via EDC pins
- Data read and write training via read FIFO (FIFO depth = 6)
- Read FIFO pattern preloaded by LDFF command
- Direct write data load to read FIFO by WRTR command
- Consecutive read of read FIFO by RDTR command
- Read/write data transmission integrity secured by cyclic redundancy check (CRC-8)
- Read/write EDC on/off mode
- Low power modes
- RDQS mode on EDC pin
- On-die temperature sensor with readout
- Automatic temperature sensor controlled self refresh rate
- Vendor ID, FIFO depth and density info fields for identification
- Mirror function with MF pin
- Boundary scan function with SEN pin

### Options<sup>1</sup>

### Marking

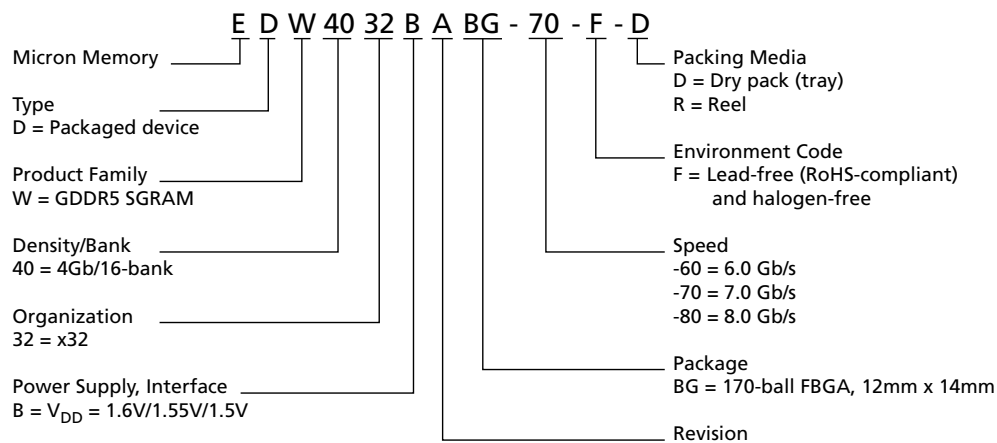
- |  |      |
|--|------|
| • Organization   |      |
| – Density  | 40   |
| – 128 Meg x 32 (words x bits)                                      | 32   |
| • FBGA package   |      |
| – 170-ball (12mm x 14mm)   | BG   |
| • Package environment code   |      |
| – Lead- and halogen-free (RoHS-compliant)                          | -F   |
| • Package media  |      |
| – Dry pack (tray)  | -D   |
| – Reel   | -R   |
| • Timing – maximum data rate                                       |      |
| – 6.0 Gb/s, 5.0 Gb/s   | -60  |
| – 7.0 Gb/s, 6.0 Gb/s   | -70  |
| – 8.0 Gb/s, 6.0 Gb/s   | -80  |
| • Operating temperature  |      |
| – Commercial ( $0^\circ\text{C} \leq T_C \leq +95^\circ\text{C}$ ) | None |
| • Revision   | A    |

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on <http://www.micron.com> for available offerings.

**Table 1: Addressing**

Parameter	256 Meg x 16	128 Meg x 32
Configuration	16 Meg x 16 x 16 banks	8 Meg x 32 x 16 banks
Refresh count	16K/32ms	16K/32ms
Refresh period	1.9µs	1.9µs
Row addressing	A[13:0]	A[13:0]
Bank addressing	BA[3:0]	BA[3:0]
Column addressing	A[6:0]	A[5:0]
Auto precharge	A8	A8
Page size	2KB	2KB

**Figure 1: Part Numbering**



## FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron’s web site: <http://www.micron.com>.

## Ball Assignments and Descriptions

**Figure 2: 170-Ball FBGA – MF = 0 (Top View)**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	V <sub>SSQ</sub>	DQ1	V <sub>SSQ</sub>	DQ0	NC					V <sub>REFD</sub>	DQ8	V <sub>SSQ</sub>	DQ9	V <sub>SSQ</sub>
B	V <sub>DDQ</sub>	DQ3	V <sub>DDQ</sub>	DQ2	V <sub>SS</sub>					V <sub>SS</sub>	DQ10	V <sub>DDQ</sub>	DQ11	V <sub>DDQ</sub>
C	V <sub>SSQ</sub>	EDC0	V <sub>SSQ</sub>	V <sub>SSQ</sub>	V <sub>DD</sub>					V <sub>DD</sub>	V <sub>SSQ</sub>	V <sub>SSQ</sub>	EDC1	V <sub>SSQ</sub>
D	V <sub>DDQ</sub>	DBI0_n	V <sub>DDQ</sub>	WCK01_t	WCK01_c					V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DBI1_n	V <sub>DDQ</sub>
E	V <sub>SSQ</sub>	DQ5	V <sub>SSQ</sub>	DQ4	V <sub>DDQ</sub>					V <sub>DDQ</sub>	DQ12	V <sub>SSQ</sub>	DQ13	V <sub>SSQ</sub>
F	V <sub>DDQ</sub>	DQ7	V <sub>DDQ</sub>	DQ6	V <sub>SSQ</sub>					V <sub>SSQ</sub>	DQ14	V <sub>DDQ</sub>	DQ15	V <sub>DDQ</sub>
G	V <sub>DD</sub>	V <sub>DDQ</sub>	RAS_n	V <sub>DD</sub>	V <sub>SS</sub>					V <sub>SS</sub>	V <sub>DD</sub>	CS_n	V <sub>DDQ</sub>	V <sub>DD</sub>
H	V <sub>SS</sub>	V <sub>SSQ</sub>	V <sub>DDQ</sub>	A10, A0	A9, A1					BA3, A3	BA0, A2	V <sub>DDQ</sub>	V <sub>SSQ</sub>	V <sub>SS</sub>
J	MF	RESET_n	CKE_n	ABI_n	A12, A13					SEN	CK_c	CK_t	ZQ	V <sub>REFC</sub>
K	V <sub>SS</sub>	V <sub>SSQ</sub>	V <sub>DDQ</sub>	A8, A7	A11, A6					BA1, A5	BA2, A4	V <sub>DDQ</sub>	V <sub>SSQ</sub>	V <sub>SS</sub>
L	V <sub>DD</sub>	V <sub>DDQ</sub>	CAS_n	V <sub>DD</sub>	V <sub>SS</sub>					V <sub>SS</sub>	V <sub>DD</sub>	WE_n	V <sub>DDQ</sub>	V <sub>DD</sub>
M	V <sub>DDQ</sub>	DQ31	V <sub>DDQ</sub>	DQ30	V <sub>SSQ</sub>					V <sub>SSQ</sub>	DQ22	V <sub>DDQ</sub>	DQ23	V <sub>DDQ</sub>
N	V <sub>SSQ</sub>	DQ29	V <sub>SSQ</sub>	DQ28	V <sub>DDQ</sub>					V <sub>DDQ</sub>	DQ20	V <sub>SSQ</sub>	DQ21	V <sub>SSQ</sub>
P	V <sub>DDQ</sub>	DBI3_n	V <sub>DDQ</sub>	WCK23_t	WCK23_c					V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DBI2_n	V <sub>DDQ</sub>
R	V <sub>SSQ</sub>	EDC3	V <sub>SSQ</sub>	V <sub>SSQ</sub>	V <sub>DD</sub>					V <sub>DD</sub>	V <sub>SSQ</sub>	V <sub>SSQ</sub>	EDC2	V <sub>SSQ</sub>
T	V <sub>DDQ</sub>	DQ27	V <sub>DDQ</sub>	DQ26	V <sub>SS</sub>					V <sub>SS</sub>	DQ18	V <sub>DDQ</sub>	DQ19	V <sub>DDQ</sub>
U	V <sub>SSQ</sub>	DQ25	V <sub>SSQ</sub>	DQ24	NC					V <sub>REFD</sub>	DQ16	V <sub>SSQ</sub>	DQ17	V <sub>SSQ</sub>

(Top view)



Note: 1. Balls shown with a heavy, solid outline are off in x16 mode.

**Figure 3: 170-Ball FBGA – MF = 1 (Top View)**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	V <sub>SSQ</sub>	DQ25	V <sub>SSQ</sub>	DQ24	NC					V <sub>REFD</sub>	DQ16	V <sub>SSQ</sub>	DQ17	V <sub>SSQ</sub>
B	V <sub>DDQ</sub>	DQ27	V <sub>DDQ</sub>	DQ26	V <sub>SS</sub>					V <sub>SS</sub>	DQ18	V <sub>DDQ</sub>	DQ19	V <sub>DDQ</sub>
C	V <sub>SSQ</sub>	EDC3	V <sub>SSQ</sub>	V <sub>SSQ</sub>	V <sub>DD</sub>					V <sub>DD</sub>	V <sub>SSQ</sub>	V <sub>SSQ</sub>	EDC2	V <sub>SSQ</sub>
D	V <sub>DDQ</sub>	DBI3_n	V <sub>DDQ</sub>	WCK23_t	WCK23_c					V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DBI2_n	V <sub>DDQ</sub>
E	V <sub>SSQ</sub>	DQ29	V <sub>SSQ</sub>	DQ28	V <sub>DDQ</sub>					V <sub>DDQ</sub>	DQ20	V <sub>SSQ</sub>	DQ21	V <sub>SSQ</sub>
F	V <sub>DDQ</sub>	DQ31	V <sub>DDQ</sub>	DQ30	V <sub>SSQ</sub>					V <sub>SSQ</sub>	DQ22	V <sub>DDQ</sub>	DQ23	V <sub>DDQ</sub>
G	V <sub>DD</sub>	V <sub>DDQ</sub>	CAS_n	V <sub>DD</sub>	V <sub>SS</sub>					V <sub>SS</sub>	V <sub>DD</sub>	WE_n	V <sub>DDQ</sub>	V <sub>DD</sub>
H	V <sub>SS</sub>	V <sub>SSQ</sub>	V <sub>DDQ</sub>	A8, A7	A11, A6					BA1, A5	BA2, A4	V <sub>DDQ</sub>	V <sub>SSQ</sub>	V <sub>SS</sub>
J	MF	RESET_n	CKE_n	ABI_n	A12, A13					SEN	CK_c	CK_t	ZQ	V <sub>REFC</sub>
K	V <sub>SS</sub>	V <sub>SSQ</sub>	V <sub>DDQ</sub>	A10, A0	A9, A1					BA3, A3	BA0, A2	V <sub>DDQ</sub>	V <sub>SSQ</sub>	V <sub>SS</sub>
L	V <sub>DD</sub>	V <sub>DDQ</sub>	RAS_n	V <sub>DD</sub>	V <sub>SS</sub>					V <sub>SS</sub>	V <sub>DD</sub>	CS_n	V <sub>DDQ</sub>	V <sub>DD</sub>
M	V <sub>DDQ</sub>	DQ7	V <sub>DDQ</sub>	DQ6	V <sub>SSQ</sub>					V <sub>SSQ</sub>	DQ14	V <sub>DDQ</sub>	DQ15	V <sub>DDQ</sub>
N	V <sub>SSQ</sub>	DQ5	V <sub>SSQ</sub>	DQ4	V <sub>DDQ</sub>					V <sub>DDQ</sub>	DQ12	V <sub>SSQ</sub>	DQ13	V <sub>SSQ</sub>
P	V <sub>DDQ</sub>	DBI0_n	V <sub>DDQ</sub>	WCK01_t	WCK01_c					V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DBI1_n	V <sub>DDQ</sub>
R	V <sub>SSQ</sub>	EDC0	V <sub>SSQ</sub>	V <sub>SSQ</sub>	V <sub>DD</sub>					V <sub>DD</sub>	V <sub>SSQ</sub>	V <sub>SSQ</sub>	EDC1	V <sub>SSQ</sub>
T	V <sub>DDQ</sub>	DQ3	V <sub>DDQ</sub>	DQ2	V <sub>SS</sub>					V <sub>SS</sub>	DQ10	V <sub>DDQ</sub>	DQ11	V <sub>DDQ</sub>
U	V <sub>SSQ</sub>	DQ1	V <sub>SSQ</sub>	DQ0	NC					V <sub>REFD</sub>	DQ8	V <sub>SSQ</sub>	DQ9	V <sub>SSQ</sub>

(Top view)



Note: 1. Balls shown with a heavy, solid outline are off in x16 mode.

**Table 2: 170-Ball FBGA Ball Descriptions**

Symbol	Type	Description
A[13:0]	Input	<b>Address inputs:</b> Provide the row address for ACTIVE commands. A[5:0] (A6) provide the column address and A8 defines the auto precharge bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A8 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A8 LOW, bank selected by BA[3:0]) or all banks (A8 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command and the data bits during LDFF commands. A[12:8] are sampled with the rising edge of CK_t and A[7:0], A13 are sampled with the rising edge of CK_c.
ABI_n	Input	<b>Address bus inversion:</b> Reduces the power requirements on address pins by limiting the number of address lines driving LOW to 5. ABI_n is enabled by the corresponding ABI mode register bit.
BA[3:0]	Input	<b>Bank address inputs:</b> Define the bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA[3:0] define which mode register is loaded during the MODE REGISTER SET command. BA[3:0] are sampled with the rising edge of CK_t.
CK_t, CK_c	Input	<b>Clock:</b> CK_t and CK_c are differential clock inputs. Command inputs are latched on the rising edge of CK_t. Address inputs are latched on the rising edge of CK_t and the rising edge of CK_c. All latencies are referenced to CK_t. CK_t and CK_c are externally terminated.
WCK01_t, WCK01_c/ WCK23_t, WCK23_c	Input	<b>Data Clocks:</b> WCK_t and WCK_c are differential clocks used for write data capture and read data output. WCK01_t and WCK01_c are associated with DQ[15:0], DBI0_n, DBI1_n, EDC0, and EDC1. WCK23_t and WCK23_c are associated with DQ[31:16], DBI2_n, DBI3_n, EDC2, and EDC3. WCK clocks operate at nominally twice the CK clock frequency.
CKE_n	Input	<b>Clock enable:</b> CKE_n enables (registered LOW) and disables (registered HIGH) internal circuitry and clocks on the device. The specific circuitry that is enabled/disabled is dependent upon the device configuration and operating mode. Taking CKE_n HIGH provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE_n is synchronous for power-down entry and exit and for self refresh entry. CKE_n must be maintained LOW throughout read and write accesses. Input buffers (excluding CKE_n) are disabled during SELF REFRESH operation. The value of CKE_n latched at power-up with RESET_n going HIGH determines the termination value of the address and command inputs.
CS_n	Input	<b>Chip select:</b> CS_n enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS_n is registered HIGH, but internal command execution continues. CS_n is considered part of the command code.
MF	Input	<b>Mirror function:</b> V <sub>DDQ</sub> CMOS input. Must be tied to V <sub>DDQ</sub> or V <sub>SS</sub> .
RAS_n, CAS_n, WE_n	Input	<b>Command inputs:</b> RAS_n, CAS_n, and WE_n (along with CS_n) define the command being entered.
RESET_n	Input	<b>Reset:</b> RESET_n is an active LOW CMOS input referenced to V <sub>SS</sub> . A full chip reset may be performed at any time by pulling RESET_n LOW. With RESET_n LOW all ODTs are disabled.
SEN	Input	<b>Scan enable:</b> V <sub>DDQ</sub> CMOS input. Must be tied to V <sub>SS</sub> when not in use.

**Table 2: 170-Ball FBGA Ball Descriptions (Continued)**

Symbol	Type	Description
DQ[31:0]	I/O	<b>Data input/output:</b> Bidirectional 32-bit data bus.
DBI[3:0]_n	I/O	<b>Data bus inversion:</b> Reduces the DC power consumption and supply noise induced jitter on data pins. DBI0_n is associated with DQ[7:0], DBI1_n with DQ[15:8], DBI2_n with DQ[23:16], and DBI3_n with DQ[31:24].
EDC[3:0]	Output	<b>Error detection code:</b> The calculated CRC data is transmitted on these pins. In addition, these pins drive a hold pattern when idle and can be used as an RDQS function. EDC0 is associated with DQ[7:0], EDC1 with DQ[15:8], EDC2 with DQ[23:16], and EDC3 with DQ[31:24].
V <sub>DD</sub>	Supply	<b>Power supply:</b> 1.6V/1.55V/1.5V ±3% and 1.35V ±3%.
V <sub>DDQ</sub>	Supply	<b>DQ power supply:</b> 1.6V/1.55V/1.5V ±3% and 1.35V ±3%. Isolated on the device for improved noise immunity.
V <sub>REFC</sub>	Supply	<b>Reference voltage for control and address:</b> V <sub>REFC</sub> must be maintained at all times (including self refresh) for proper device operation.
V <sub>REFD</sub>	Supply	<b>Reference voltage for data:</b> V <sub>REFD</sub> must be maintained at all times (including self refresh) for proper device operation.
V <sub>SS</sub>	Supply	Ground.
V <sub>SSQ</sub>	Supply	<b>DQ ground:</b> Isolated on the device for improved noise immunity.
ZQ	Reference	<b>External reference ball for impedance calibration:</b> This ball is tied to an external 120Ω resistor (ZQ), which is tied to V <sub>SSQ</sub> .
NC	–	<b>No connect:</b> These balls should be left unconnected (the ball has no connection to the device or to other balls).

