

GSMDB2116S

20V N+P Dual Channel MOSFETs

Product Description

These N+P dual Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for high efficiency fast switching applications.

Features

- N-Channel
20V, 5A, $R_{DS(ON)}=40m\Omega@V_{GS}=4.5V$
- P-Channel
-20V, -4.7A, $R_{DS(ON)}=95m\Omega@V_{GS}=-4.5V$
- Fast switching
- Suit for -1.8V/1.8V Gate Drive Applications
- Green Device Available
- DFN2X2-6L package design

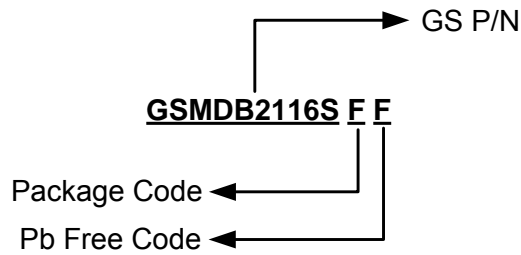
Applications

- Notebook
- Load Switch
- Networking
- Hand-held Instruments

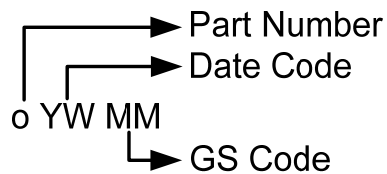
Packages & Pin Assignments

GSMDB2116SFF (DFN2X2-6L)	
<p style="text-align: center;">Top Views</p>	
Pin	Description
1	Source 1
2	Gate 1
3	Drain 2
4	Source 2
5	Gate 2
6	Drain 1

Ordering Information



Marking Information



Part Number	Package	Part Marking	Quantity
GSMDB2116SFF	DFN2X2-6L	oYWMM	3000pcs

Absolute Maximum Ratings

T_C=25°C Unless otherwise noted

Symbol	Parameter	Typical		Unit	
		N-Channel	P-Channel		
V _{DS}	Drain-Source Voltage	20	-20	V	
V _{GS}	Gate-Source Voltage	±10	±10	V	
I _D	Continuous Drain Current (T _J =150°C)	T _C =25°C	5	-4.7	A
		T _C =100°C	4.1	-3.9	
I _{DM}	Pulsed Drain Current (Note 1)	15.2	-10	A	
P _D	Power Dissipation	T _C =25°C	1.56	1.56	W
		Derate above 25°C	0.01	0.01	W/°C
T _J	Operating Junction Temperature Range	-55 to +150		°C	
T _{STG}	Storage Temperature Range	-55 to +150		°C	
R _{θJA}	Thermal Resistance-Junction to Ambient	80		°C/W	
R _{θJC}	Thermal Resistance-Junction to Case	15		°C/W	

Note 1: Repetitive Rating: Pulsed width limited by maximum junction temperature.

Electrical Characteristics (N-Channel)

T_J=25°C Unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	20			V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =1mA		0.02		V/°C
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	0.3	0.6	1.0	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient			-2		mV/°C
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±10V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V			1	uA
		V _{DS} =16V, V _{GS} =0V, T _J =125°C			10	
I _S	Continuous Source Current	V _G =V _D =0V, Force Current			5	A
I _{SM}	Pulsed Source Current				10	
R _{DS(on)}	Drain-Source On-Resistance	V _{GS} =4.5V, I _D =3A		30	40	mΩ
		V _{GS} =2.5V, I _D =2A		42	55	
		V _{GS} =1.8V, I _D =1.5A		55	70	
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =2A		4.4		S
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =1A			1	V
Dynamic						
Q _g	Total Gate Charge (Note 2,3)	V _{DS} =10V, V _{GS} =4.5V, I _D =3A		5.8	10	nC
Q _{gs}	Gate-Source Charge (Note 2,3)			0.6	1.5	
Q _{gd}	Gate-Drain Charge (Note 2,3)			1.5	3	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		315	600	pF
C _{oss}	Output Capacitance			50	80	
C _{rss}	Reverse Transfer Capacitance			40	60	
t _{d(on)}	Turn-On Time (Note 2,3)	V _{DD} =10V, I _D =1A, V _{GS} =4.5V, R _G =25Ω		2.9	6	ns
t _r				8.4	16	
t _{d(off)}	Turn-Off Time (Note 2,3)			19.2	38	
t _f				5.6	12	

Note 2: The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.

Note 3: Essentially independent of operating temperature.

Electrical Characteristics (P-Channel)

T_J=25°C Unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-20			V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA		-0.01		V/°C
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-0.3	-0.6	-1.0	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient			3		mV/°C
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±10V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-20V, V _{GS} =0V			-1	μA
		V _{DS} =-16V, V _{GS} =0V, T _J =125°C			-10	
I _S	Continuous Source Current	V _G =V _D =0V, Force Current			-4.7	A
I _{SM}	Pulsed Source Current				-9.4	
R _{DS(on)}	Drain-Source On-Resistance	V _{GS} = -4.5V, I _D = -3A		80	95	mΩ
		V _{GS} = -2.5V, I _D = -2A		109	125	
		V _{GS} = -1.8V, I _D = -1A		148	161	
g _{FS}	Forward Transconductance	V _{DS} =-10V, I _D =-1A		2.2		S
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =-1A			-1	V
Dynamic						
Q _g	Total Gate Charge (Note 2,3)	V _{DS} =-10V, V _{GS} =-4.5V, I _D =-2A		4.8	10	nC
Q _{gs}	Gate-Source Charge (Note 2,3)			0.5	1	
Q _{gd}	Gate-Drain Charge (Note 2,3)			1.9	4	
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz		350	510	pF
C _{oss}	Output Capacitance			65	95	
C _{rss}	Reverse Transfer Capacitance			50	75	
t _{d(on)}	Turn-On Time (Note 2,3)	V _{DD} =-10V, I _D =-1A, V _{GS} =-4.5V, R _G =25Ω		3.5	7	ns
t _r				12.6	24	
t _{d(off)}	Turn-Off Time (Note 2,3)			32.6	62	
t _f				8.4	16	

Note 2: The data tested by pulsed, pulse width ≤ 300μs, duty cycle ≤ 2%.

Note 3: Essentially independent of operating temperature.

Typical Performance Characteristics (N-Channel)

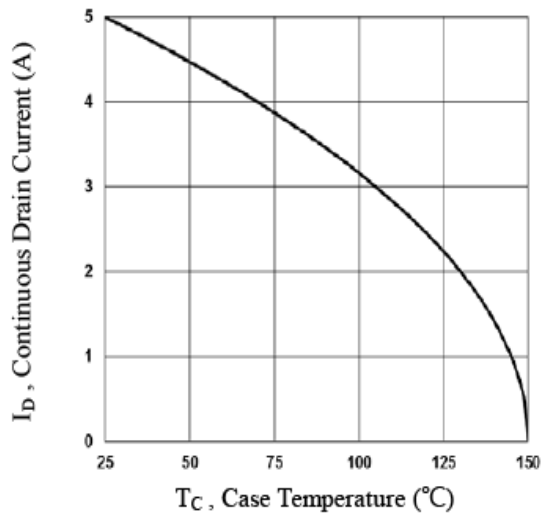


Fig.1 Continuous Drain Current vs. T_C

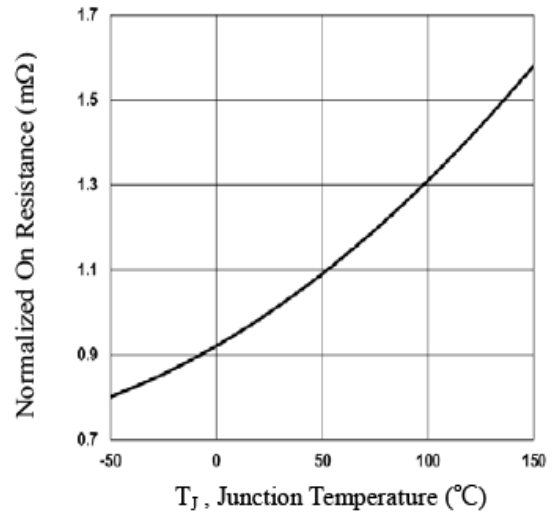


Fig.2 Normalized RDSON vs. T_J

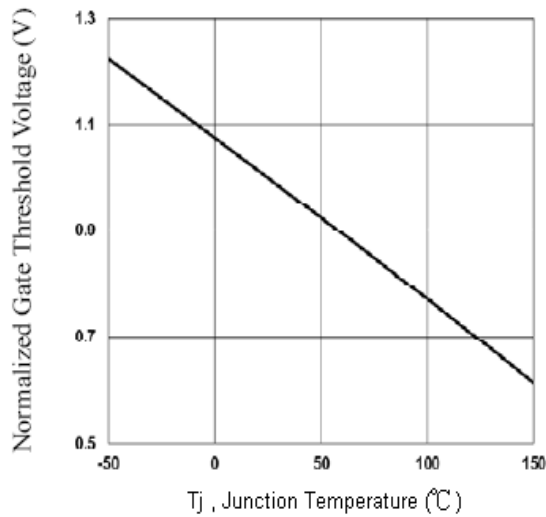


Fig.3 Normalized V_{th} vs. T_J

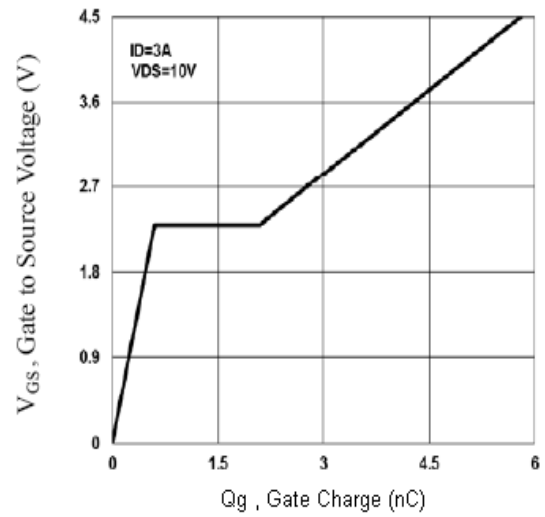


Fig.4 Gate Charge Waveform

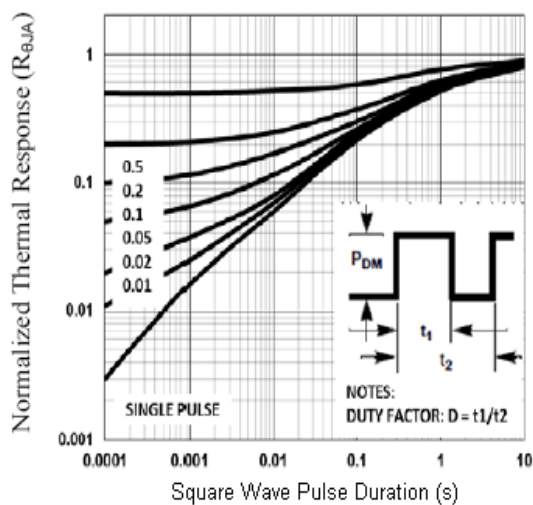


Fig.5 Normalized Transient Impedance

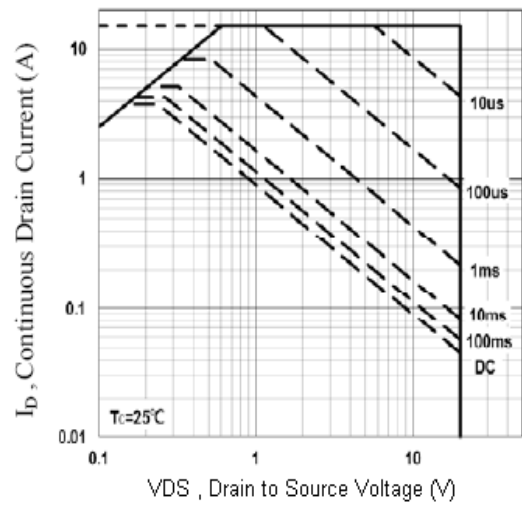
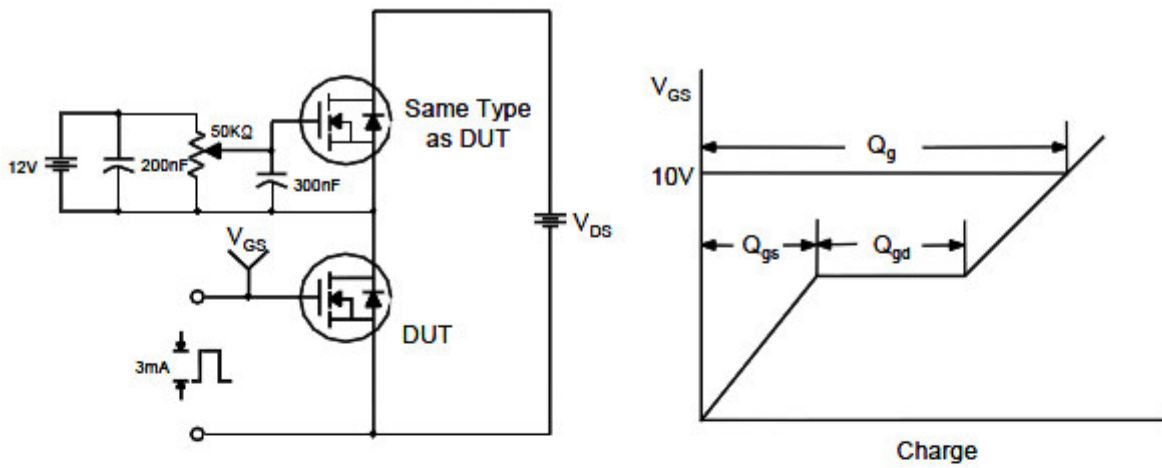


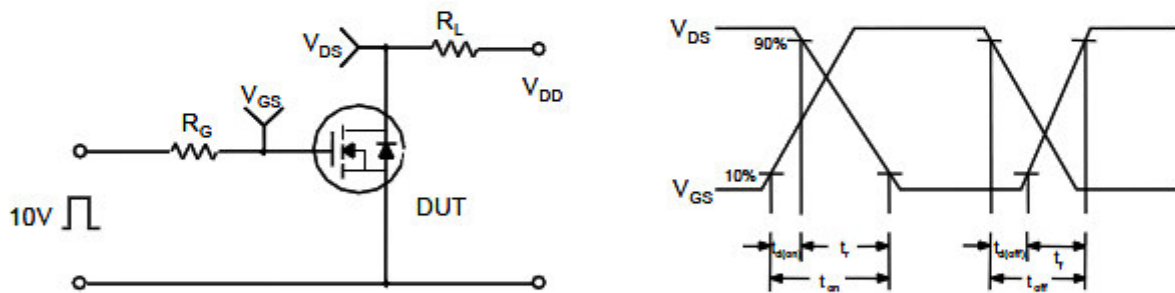
Fig.6 Maximum Safe Operation Area

Typical Performance Characteristics (N-Channel)

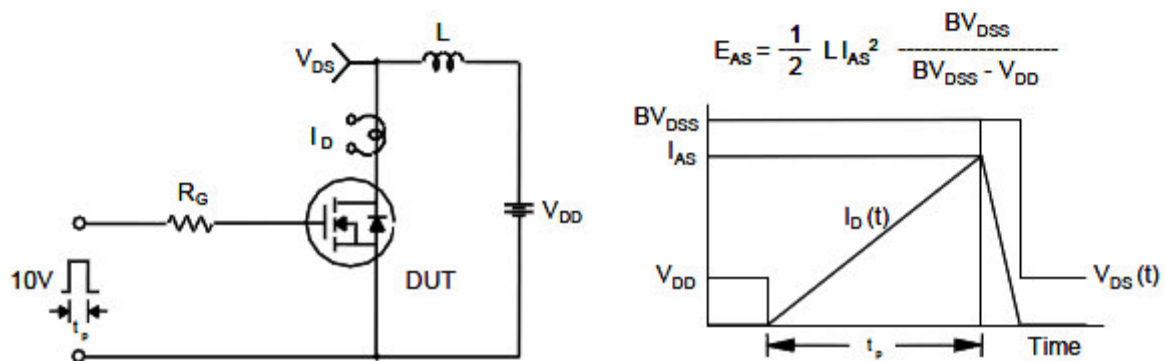
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Typical Performance Characteristics (P-Channel)

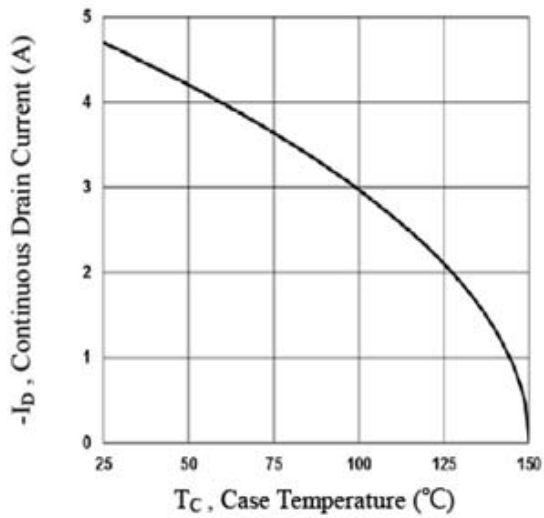


Fig.7 Continuous Drain Current vs. T_C

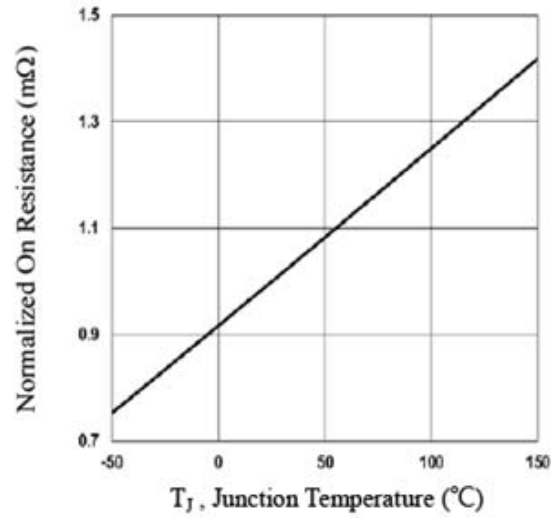


Fig.8 Normalized $R_{DS(on)}$ vs. T_J

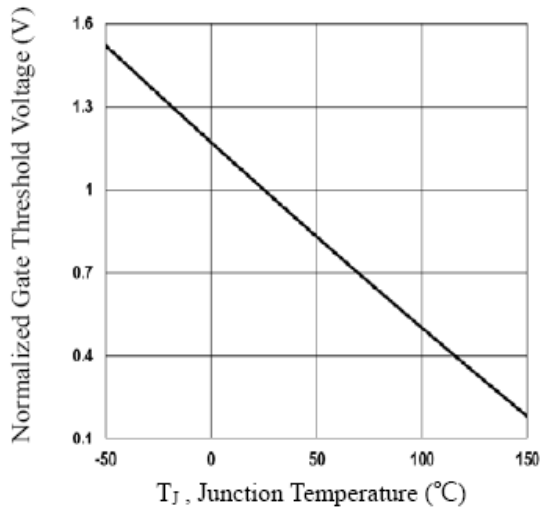


Fig.9 Normalized V_{th} vs. T_J

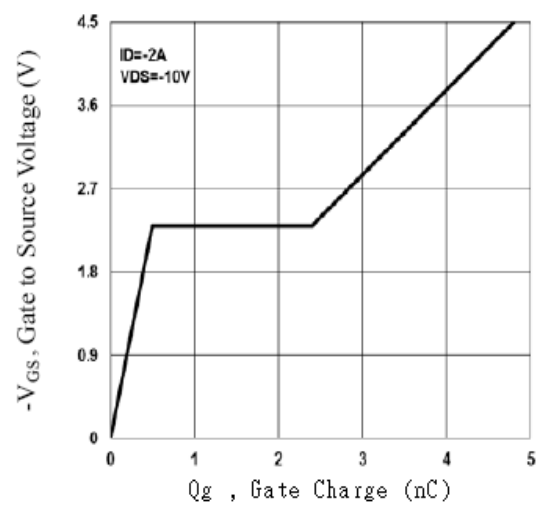


Fig.10 Gate Charge Waveform

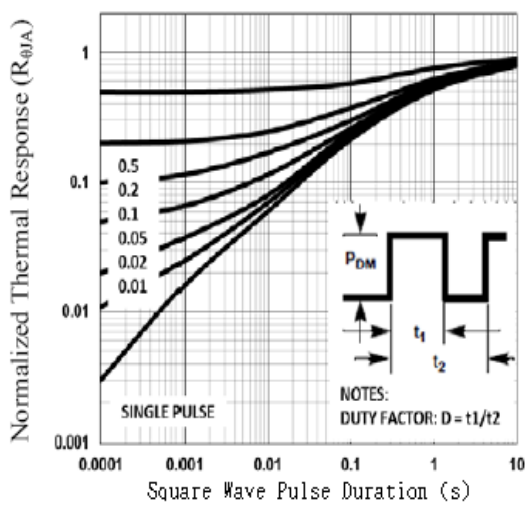


Fig.11 Normalized Transient Impedance

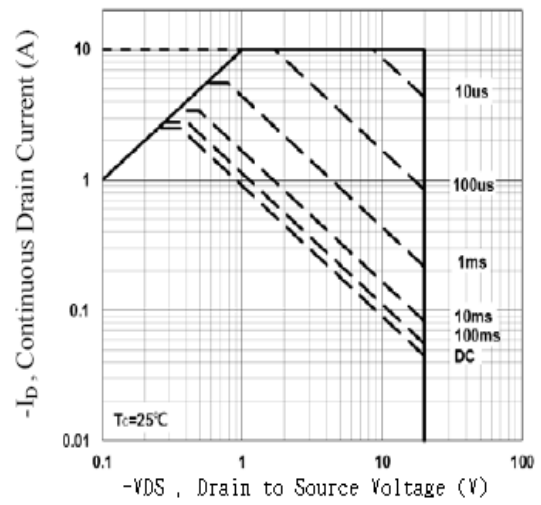
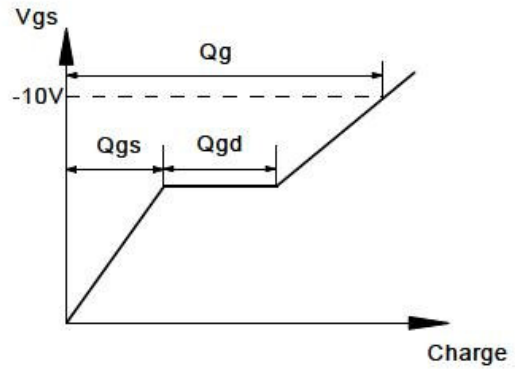
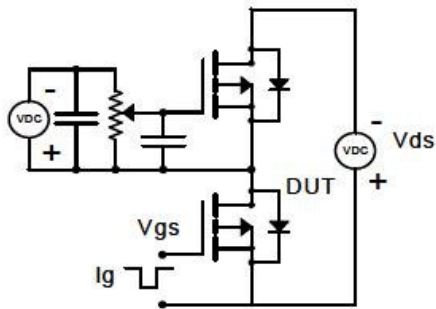


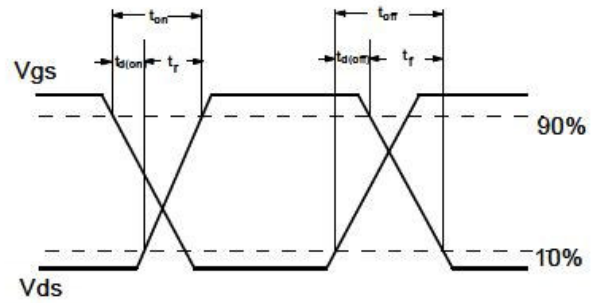
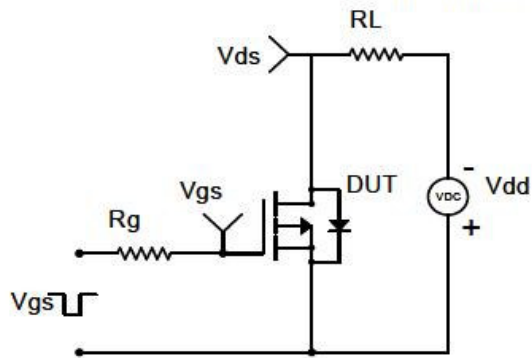
Fig.12 Maximum Safe Operation Area

Typical Performance Characteristics (P-Channel)

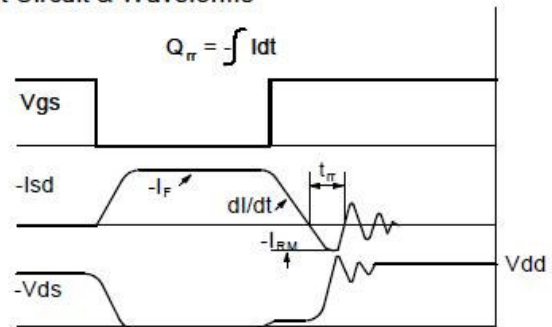
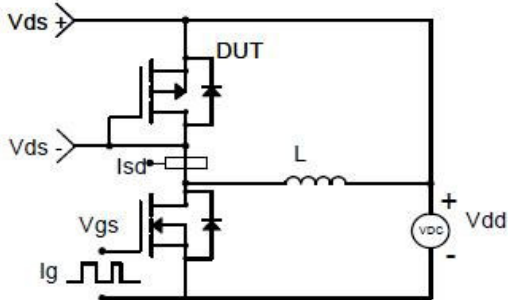
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

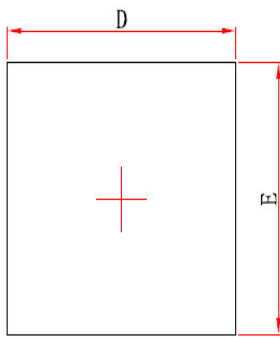


Diode Recovery Test Circuit & Waveforms

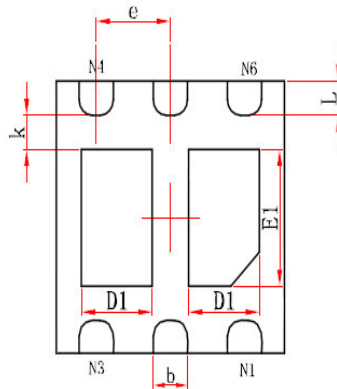


Package Dimension

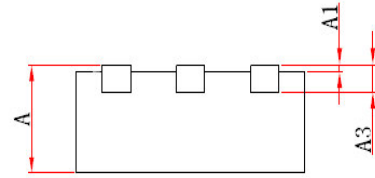
DFN2X2-6L



Top View



Bottom View



Side View




Dimensions




SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203 (REF)		0.008 (REF)	
D	1.924	2.076	0.076	0.082
E	1.924	2.076	0.076	0.082
D1	0.520	0.720	0.020	0.028
E1	0.900	1.100	0.035	0.043
k	0.200 (MIN)		0.008 (MIN)	
b	0.250	0.350	0.010	0.014
e	0.650 (TYP)		0.026 (TYP)	
L	0.174	0.326	0.007	0.013



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