



N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A) ^d	Q _g (Typ.)			
100	0.063 at V _{GS} = 10 V	6.8	9 nC			
100	0.084 at $V_{GS} = 6 \text{ V}$	5.8	9110			

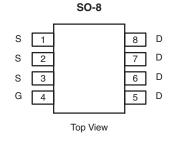
FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFET
- 100 % UIS Tested

RoHS COMPLIANT HALOGEN FREE

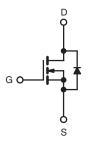
APPLICATIONS

- High Frequency Boost Converter
- LED Backlight for LCD TV



Ordering Information: Si4100DY-T1-E3 (Lead (Pb)-free)

Si4100DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V _{DS}	100	V		
Gate-Source Voltage		V_{GS}	± 20	V	
	T _C = 25 °C		6.8		
Continuous Drain Current (T ₁ = 150 °C)	T _C = 70 °C	1_	5.4		
Continuous Brain Current (1) = 130 °C)	T _A = 25 °C	I _D	4.4 ^{a, b}		
	T _A = 70 °C		3.5 ^{a, b}	Α	
Pulsed Drain Current		I _{DM}	20	A	
Continuous Source-Drain Diode Current	T _C = 25 °C	l _a	5		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	2.1 ^{a, b}		
Single Avalanche Current	I _ 0.1 mH	I _{AS}	19		
Single Avalanche Energy L = 0.1 mH		E _{AS}	18	mJ	
	T _C = 25 °C		6		
Maximum Dawar Dissination	T _C = 70 °C	P _D	3.8	w	
Maximum Power Dissipation	T _A = 25 °C	LD	2.5 ^{a, b}	VV	
	T _A = 70 °C		1.6 ^{a, b}		
Operating Junction and Storage Temperature	T _J , T _{stg}	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^{b, c}	t ≤ 10 s	R_{thJA}	37	50	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	17	21	0/ * *		

Notes

- a. Surface Mounted on 1" x 1" FR4 board.
- b. t = 10 s.
- c. Maximum under Steady State conditions is 85 °C/W.
- d. $T_C = 25$ °C.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 050 A		120		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 9			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	2		4.5	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1		
Zero Gate Voltage Drain Current		$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α	
		V _{GS} = 10 V, I _D = 4.4 A		0.051	0.063		
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 6 \text{ V}, I_D = 3.8 \text{ A}$		0.069	0.084	Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 4.4 A		10		S	
Dynamic ^b				l	l	<u> </u>	
Input Capacitance	C _{iss}			600		pF	
Output Capacitance	C _{oss}	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		90			
Reverse Transfer Capacitance	C _{rss}			50			
	Q _g	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 4.4 \text{ A}$		13.5	20		
Total Gate Charge				9	13.5	nC	
Gate-Source Charge	Q_{gs}	$V_{DS} = 50 \text{ V}, V_{GS} = 6 \text{ V}, I_{D} = 4.4 \text{ A}$		3			
Gate-Drain Charge	Q_{gd}			4.6			
Gate Resistance	R_{g}	f = 1 MHz		1		Ω	
Turn-On Delay Time	t _{d(on)}			15	25		
Rise Time	t _r	V_{DD} = 50 V, R_L = 14.3 Ω		12	20		
Turn-Off Delay Time	t _{d(off)}	$I_D\cong 3.5$ A, V_{GEN} = 6 V, R_g = 1 Ω		12	20		
Fall Time	t _f			10	15		
Turn-On Delay Time	t _{d(on)}			10	15	ns -	
Rise Time	t _r	V_{DD} = 50 V, R_L = 14.3 Ω		12	20		
Turn-Off Delay Time	t _{d(off)}	$I_D\cong 3.5$ A, V_{GEN} = 10 V, R_g = 1 Ω		15	25		
Fall Time	t _f			10	15		
Drain-Source Body Diode Characteristi	cs					•	
Continuous Source-Drain Diode Current	I _S	$T_C = 25 ^{\circ}C$			5	Δ	
Pulse Diode Forward Current	I _{SM}				20	А	
Body Diode Voltage	V _{SD}	I _S = 3.5 A, V _{GS} = 0 V		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			45	70	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = 3.5 A, dI/dt = 100 A/μs, T _J = 25 °C		80	120	nC	
Reverse Recovery Fall Time	t _a	i _F = 3.3 A, αί/αι = 100 A/μs, 1 _J = 25 °C		33		ns	
Reverse Recovery Rise Time	t _b			12			

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing.

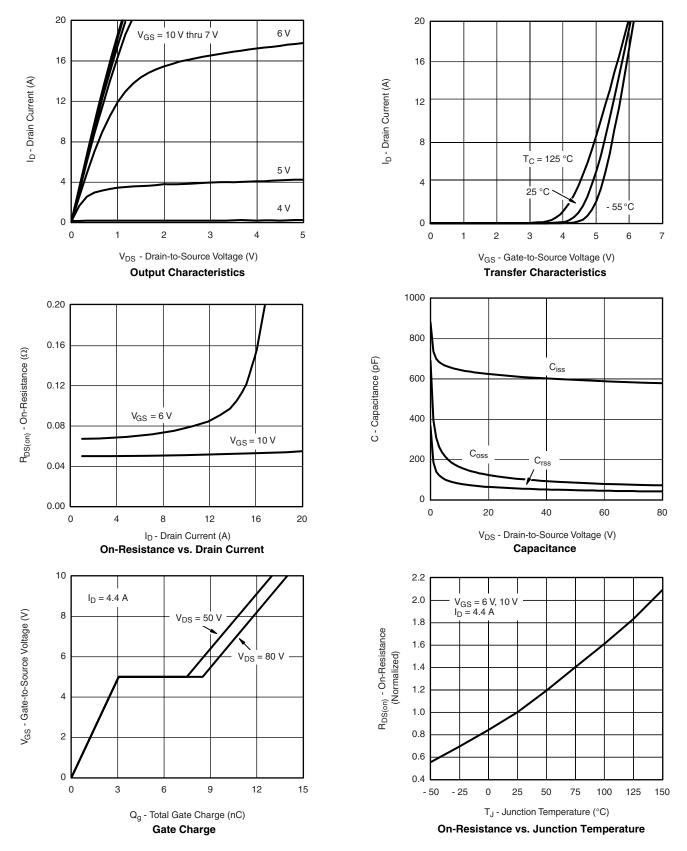
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





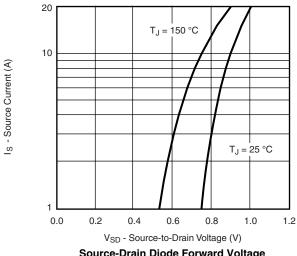


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

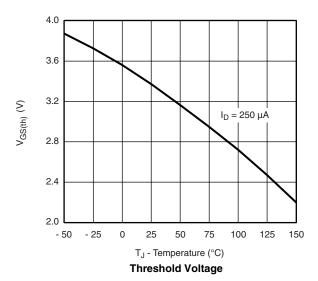


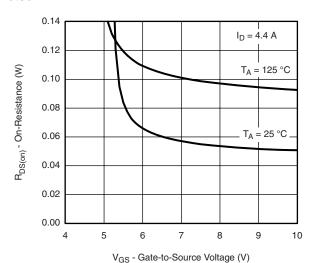
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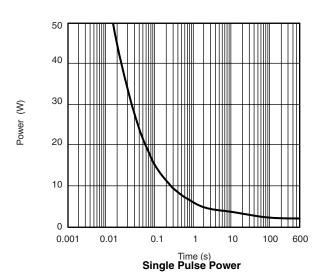


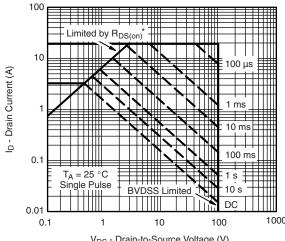
Source-Drain Diode Forward Voltage





On-Resistance vs. Gate-to-Source Voltage





V_{DS} - Drain-to-Source Voltage (V) * V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

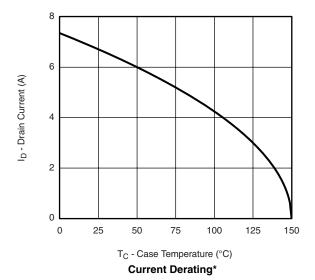
Safe Operating Area, Junction-to-Ambient

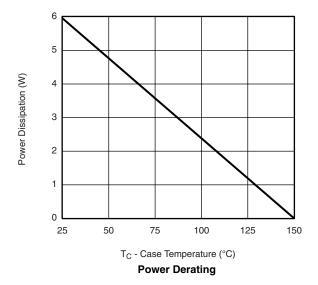






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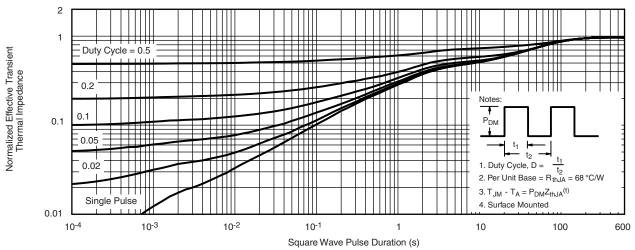


^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

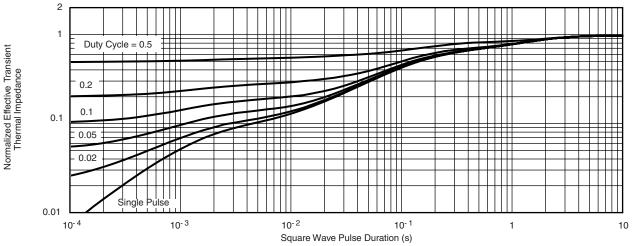
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INCHES			
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050	0.050 BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
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RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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