

DESCRIPTION

The MP2005 is a micropower, ultra low-dropout LDO linear regulator. It has a 1.0V to 5.5V input voltage range and can regulate the output voltage from as low as 0.5V. The MP2005 can supply up to 800mA of load current with a typical dropout voltage of 90mV. It requires a bias supply (2.7V to 5.5V) separate from V_{IN} to run the internal reference and LDO drive circuitry. The output current comes directly from the input voltage supply for high efficiency regulation. The 0.5V internal reference voltage allows the output to be programmed to a wide range of voltages (0.5V to 4V).

A low bias current of 100 μ A makes the MP2005 ideal for use in battery-powered applications. The bias supply V_{BIAS} can be directly applied from the battery while V_{IN} is powered from the high efficiency buck regulator (or other secondary supply). This reduces output noise and the size of the decoupling capacitor.

Other features of MP2005 include thermal overload and current limit protection, stability with ultra low ESR ceramic capacitors as low as 1 μ F, and fast transient response. The MP2005 is available in a 8-pin QFN (2mm x 3mm) package.

FEATURES

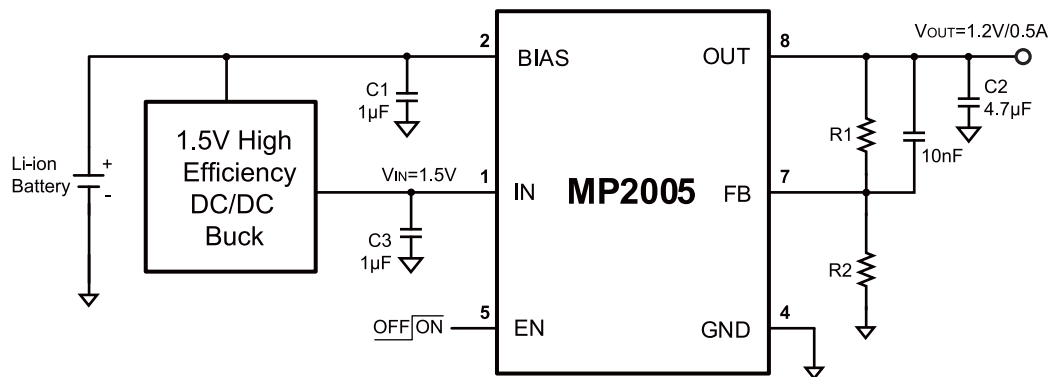
- Wide 1.0V to 5.5V Input Voltage Range
- Stable with 1 μ F Ceramic Capacitor
- Ultra-Low Dropout (ULDO) voltage: 90mV@800mA
- 2% Accurate Output Voltage
- Adjustable Output Range of 0.5V to 4V
- High PSRR
 - 65dB at 1KHz
 - 48dB at 1MHz
- Better Than 0.0005%/mA Load Regulation
- Stable With Low-ESR Output Capacitors
- Low 100 μ A Ground Current
- Internal Thermal Protection
- Current Limit Protection
- 1 μ A Typical Quiescent Current at Shutdown

APPLICATIONS

- Low Current Regulators
- Low Power Handheld Devices
- Battery Powered Systems
- Cellular Phones
- Portable Electronic Equipment
- Post Regulation for Switching Power Supplies
- Power Supplies

"MPS" and "The Future of Analog IC Technology" are Registered Trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION



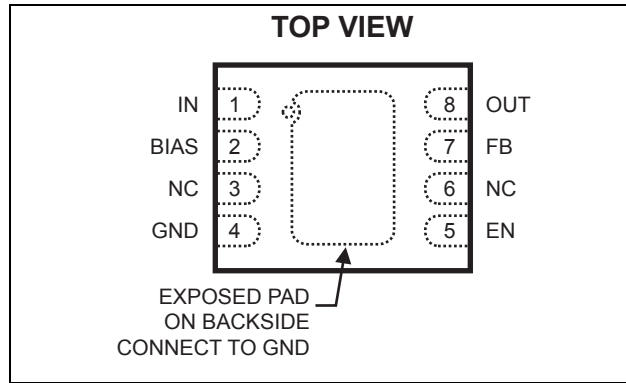
ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T _A)
MP2005DD	QFN8 (2mm x 3mm)	N3	–40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP2005DD–Z)

For RoHS compliant packaging, add suffix –LF (e.g. MP2005DD–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

V _{BIAS} , V _{IN} to GND.....	–0.3V to +6V
FB, EN to GND	–0.3V to 6V
OUT	–0.3V to 6V
Continuous Power Dissipation (T _A = +25°C) ⁽²⁾	2.3W
Junction Temperature	150°C
Lead Temperature	260°C
Storage Temperature	–65°C to +150°C

Recommended Operating Conditions ⁽³⁾

Input Voltage V _{IN}	1.0V to 5.5V
Input Voltage V _{BIAS}	2.7V to 5.5V
Output Voltage	0.5V to 4.0V
Load Current.....	800mA Maximum
Operating Temperature.....	–40°C to +85°C

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}
QFN8 (2mm x 3mm).....	55.....	12... °C/W

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 1.5V$, $V_{BIAS} = 3.6V$, $V_{OUT} = 1.2V$, $C2 = 4.7\mu F$, $C3 = 1\mu F$, $T_A = +25^\circ C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} Operating Voltage			1.0		5.5	V
V_{BIAS} Operating Voltage			2.7		5.5	V
V_{IN} Operating Current		$V_{OUT} = 1.2V$		4	10	μA
V_{BIAS} Operating Current		$I_{OUT} = 10\mu A$, $V_{OUT} = 1.2V$		100	150	μA
FB Regulation Voltage		$I_{OUT} = 1mA$ to 800mA	0.490	0.500	0.510	V
		$-40^\circ C \leq T_A \leq +85^\circ C$, $V_{OUT} = 0.5V$	0.487	0.500	0.512	
Dropout Voltage		$I_{OUT} = 800mA$, $V_{BIAS} = 3.6V$		70	90	mV
V_{IN} Line Regulation		$I_{OUT} = 1mA$, $V_{IN} = 1.0V$ to 5.5V $V_{BIAS} = 3.6V$, $V_{OUT} = 0.5V$		0.002		%/V
V_{BIAS} Line Regulation		$I_{OUT} = 100mA$, $V_{BIAS} = 2.7V$ to 5.5V $V_{OUT} = 0.5V$, $V_{IN} = 1.5V$		0.04		%/V
Load Regulation		$I_{OUT} = 1mA$ to 800mA		0.0005		%/mA
PSRR		$V_{IN} > V_{OUT} + 0.5V$, $C2 = 10\mu F$, $V_{IN(AC)} = 100mV$, $f = 1MHz$		48		dB
EN Input High Voltage			1.3			V
EN Input Low Voltage					0.8	V
EN Input Bias Current		$V_{EN} = 1.2V$	-1		+1	μA
Thermal Protection				155		$^\circ C$
Thermal Protection Hysteresis				30		$^\circ C$
GND Current		$I_{LOAD} = 500mA$		110	150	μA

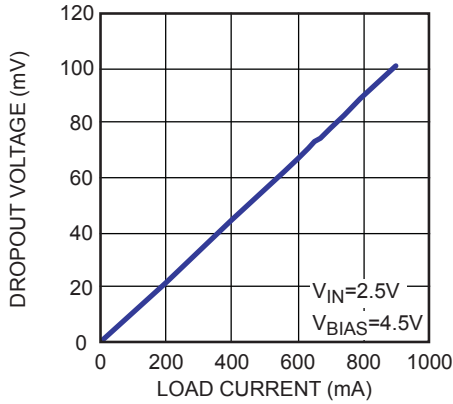
PIN FUNCTIONS

Pin #	Name	Description
1	IN	Power Source Input. Bypass IN to GND with a 1 μF or greater capacitor.
2	BIAS	Bias Voltage. Bypass to GND with a 1 μF capacitor (or greater)
3, 6	NC	No Connect.
4	GND	Ground.
5	EN	Enable Input. Drive EN high to turn on the MP2005, drive EN low to turn it off. For automatic startup, connect EN to Bias.
7	FB	Feedback Input. Connect a resistive voltage divider from OUT to FB to set the output voltage. OUT feedback threshold is 0.5V.
8	OUT	Regulator Output. OUT is the output of the linear regulator. Bypass OUT to GND with a 1 μF or greater capacitor.

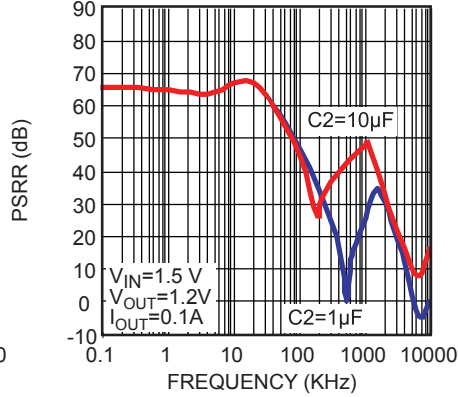
TYPICAL PERFORMANCE CHARACTERISTICS

$C1=C3=2.2\mu\text{F}$, $C2=4.7\mu\text{F}$, $V_{\text{EN}}=V_{\text{BIAS}}=3.6\text{V}$, $T_{\text{A}}=25^{\circ}\text{C}$, unless otherwise noted

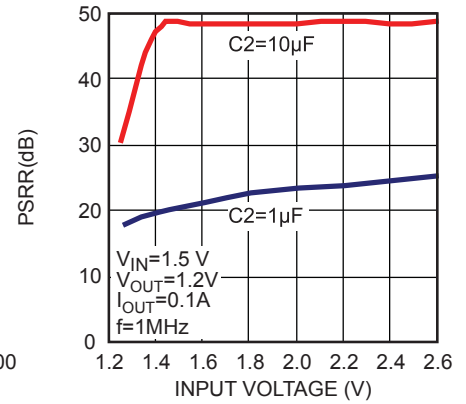
Voltage Dropout



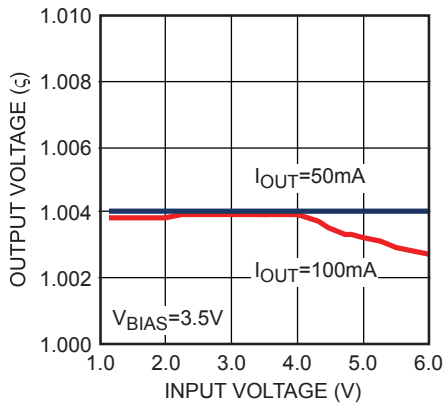
PSRR vs. Frequency



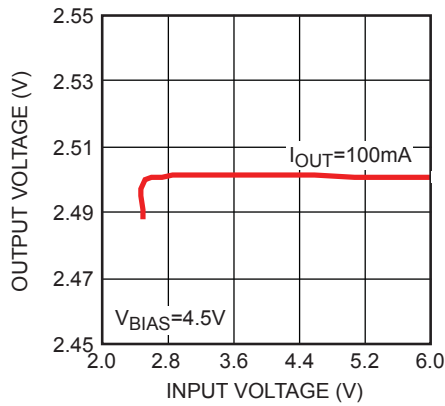
PSRR vs. V_{IN}



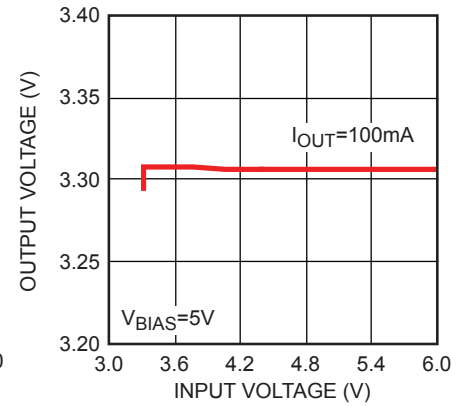
Line Regulation



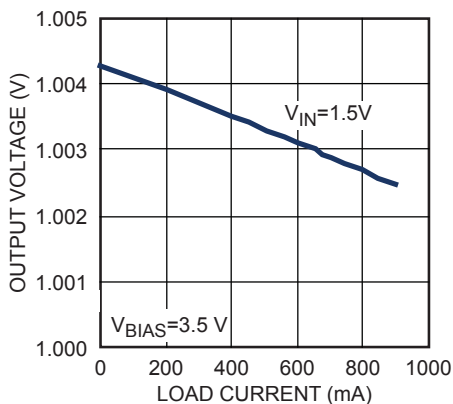
Line Regulation



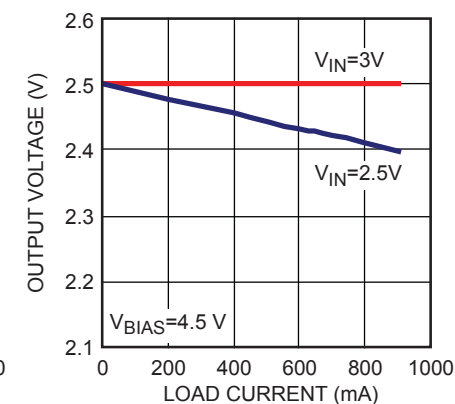
Line Regulation



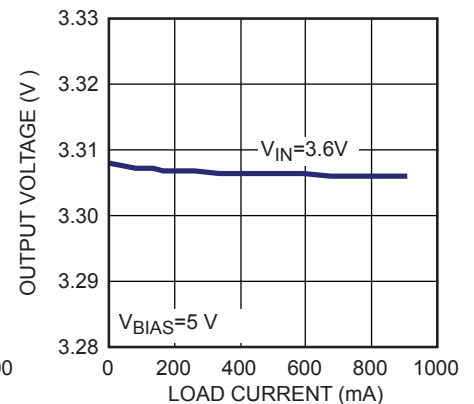
Load Regulation

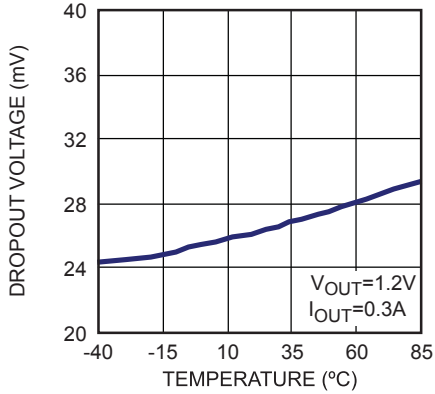
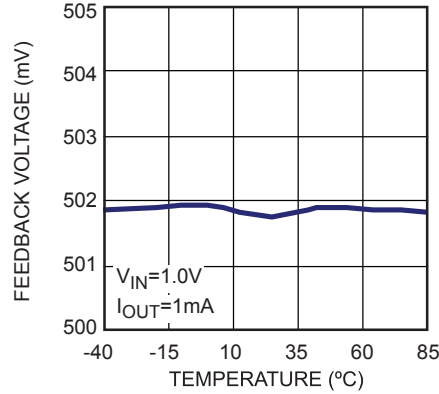
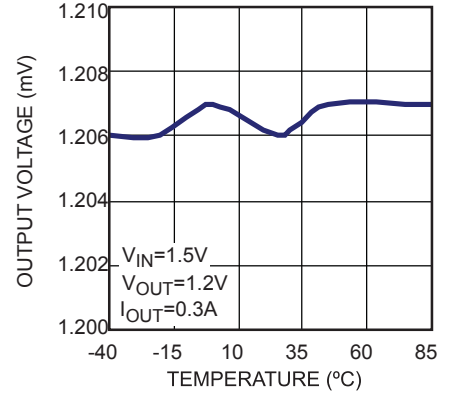
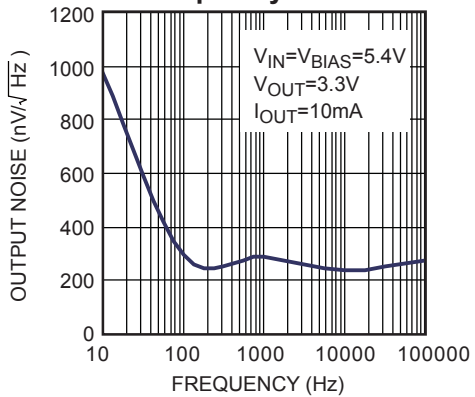


Load Regulation

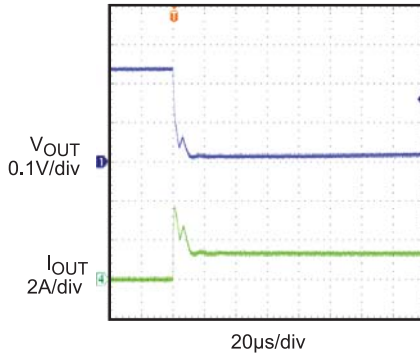


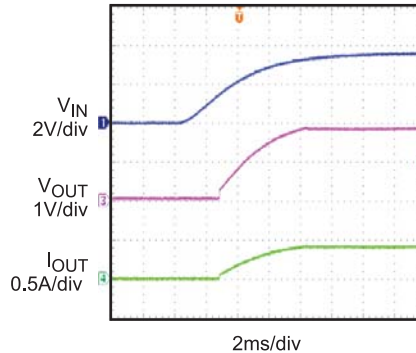
Load Regulation

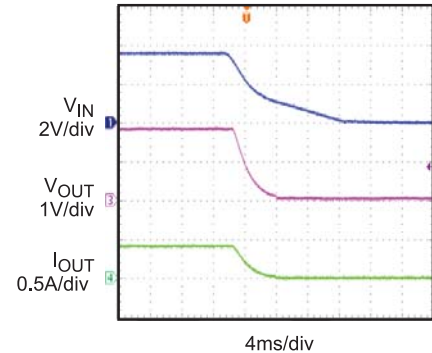


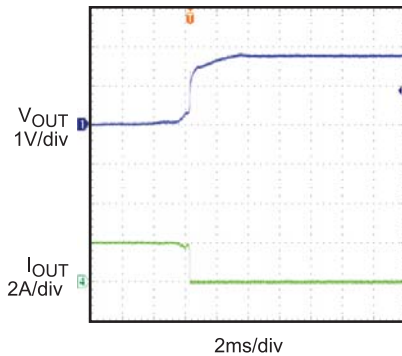
TYPICAL PERFORMANCE CHARACTERISTICS (continued)
C1=C3=2.2uF, C2=4.7uF, $V_{EN}=V_{BIAS}=3.6V$, $T_A=25^\circ C$, unless otherwise noted
Dropout Voltage vs. Temperature

Feedback Voltage vs. Temperature

Output Voltage vs. Temperature

Output Noise vs. Frequency


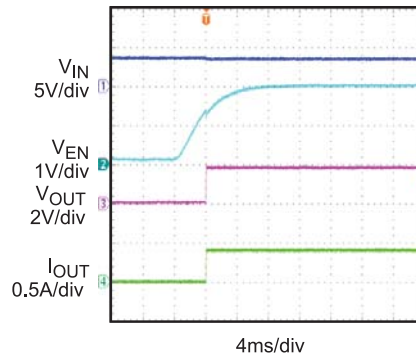
TYPICAL PERFORMANCE CHARACTERISTICS (continued)
C1=C3=2.2uF, C2=4.7uF, V_{EN}=V_{BIAS}=3.6V, V_{IN}=3.6V, T_A=25°C, unless otherwise noted
Short Circuit

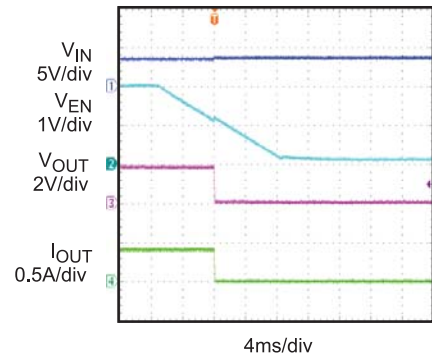
 V_{IN}=2V, V_{OUT}=1.8V

Power Rump Up

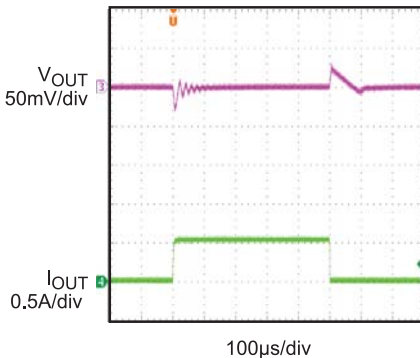
 V_{OUT}=1.8V, I_{OUT}=420mA,
with Resistor Load

Power Rump Down

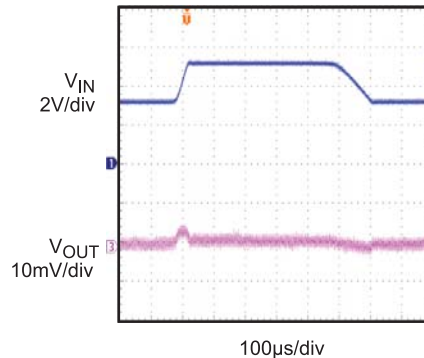
 V_{OUT}=1.8V, I_{OUT}=420mA
with Resistor Load

Short Circuit Recovery

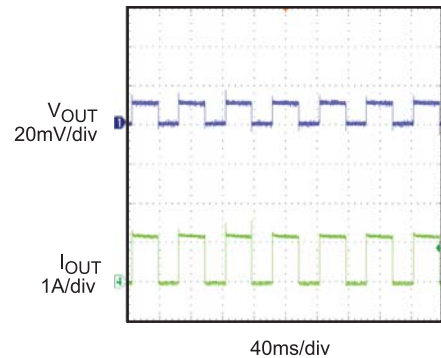
 V_{IN}=2V, V_{OUT}=1.8V

Enable Turn On

 V_{OUT}=1.8V, I_{OUT}=400mA
with Resistor Load

Enable Turn Off

 V_{OUT}=1.8V, I_{OUT}=400mA
with Resistor Load

Load Transient

 V_{BIAS}=2.9V, V_{OUT}=1.2V, V_{IN}=1.5V,
I_{OUT}=20mA to 600mA,
with Resistor Load

Line Transient

 V_{IN}=3.5V to 5.2V, V_{OUT}=1.2V,
I_{OUT}=100mA
with Resistor Load

Thermal Protection

 V_{OUT}=1.8V, I_{OUT}=1A
with Resistor Load


BLOCK DIAGRAM

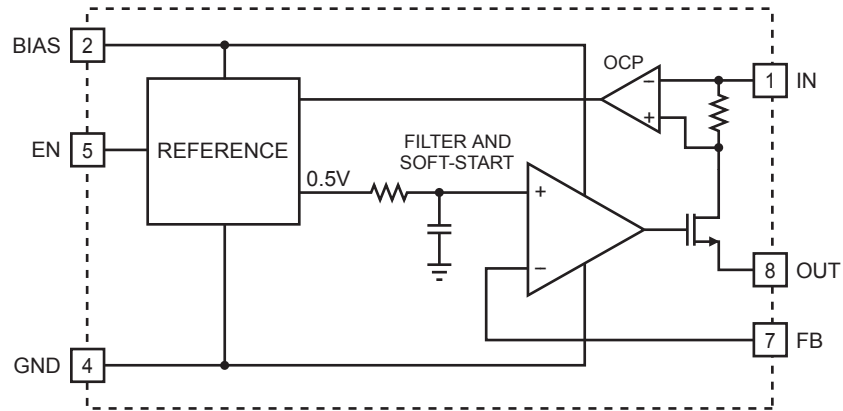


Figure 1—Block Diagram of Super Low Dropout Regulator

APPLICATION INFORMATION

Setting the Output Voltage

The MP2005 has an adjustable output voltage, set by using a resistive voltage divider from the output voltage to FB pin. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \frac{R2}{R1 + R2}$$

Where V_{FB} is the feedback threshold voltage ($V_{FB} = 0.5V$), and V_{OUT} is the output voltage.

Thus the output voltage is:

$$V_{OUT} = 0.5 \times \frac{R1 + R2}{R2}$$

$R2$ can be as high as 100k Ω , but a typical value is 10k Ω . Using that value, $R1$ is determined by:

$$R1 = R2 \times \left(\frac{V_{OUT} - V_{FB}}{V_{FB}} \right)$$

For example, for a 1.8V output voltage, $R2$ is 10k Ω , and $R1$ is 26k Ω . You can select a standard 26k Ω ($\pm 1\%$) resistor for $R1$.

The following table lists the selected $R1$ for various output voltages.

Table 1—Adjustable Output Voltages R1 Values

V_{OUT} (V)	$R1$ (k Ω)	$R2$ (k Ω)
1.25	15	10
1.5	20	
1.8	26	
2	30	
2.5	40	
2.8	46	
3	50	
3.3	56	
4	70	

Bias Input

The bias input is designed for low drop application. The bias pin must be at least 2.7V, and at least 1.5V higher than the output. If V_{IN} supply voltage meets these requirements, the bias pin can be tied to V_{IN} .

Feed Forward Capacitor

For stability, it needs a 10nF capacitor parallel with $R1$. The ceramic type capacitor, will provide the best performance.

PCB Layout Guide

PCB layout is very important to achieve good regulation, ripple rejection, transient response and thermal performance. It is highly recommended to duplicate EVB layout for optimum performance.

If change is necessary, please follow these guidelines and take Figure 2 for reference.

- 1) Input and output bypass ceramic capacitors are suggested to be put close to the IN Pin and OUT Pin respectively.
- 2) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
- 3) Connect IN, OUT and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

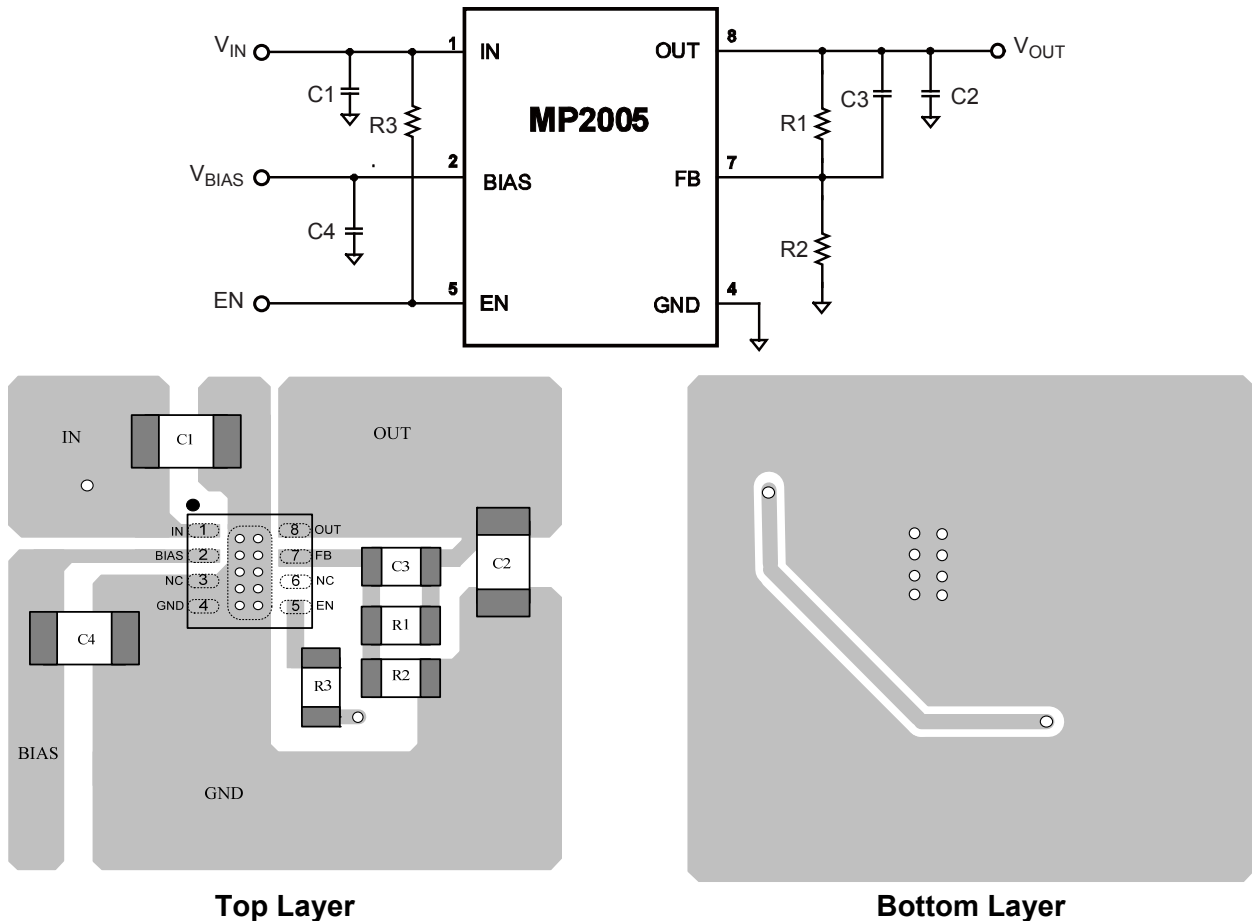
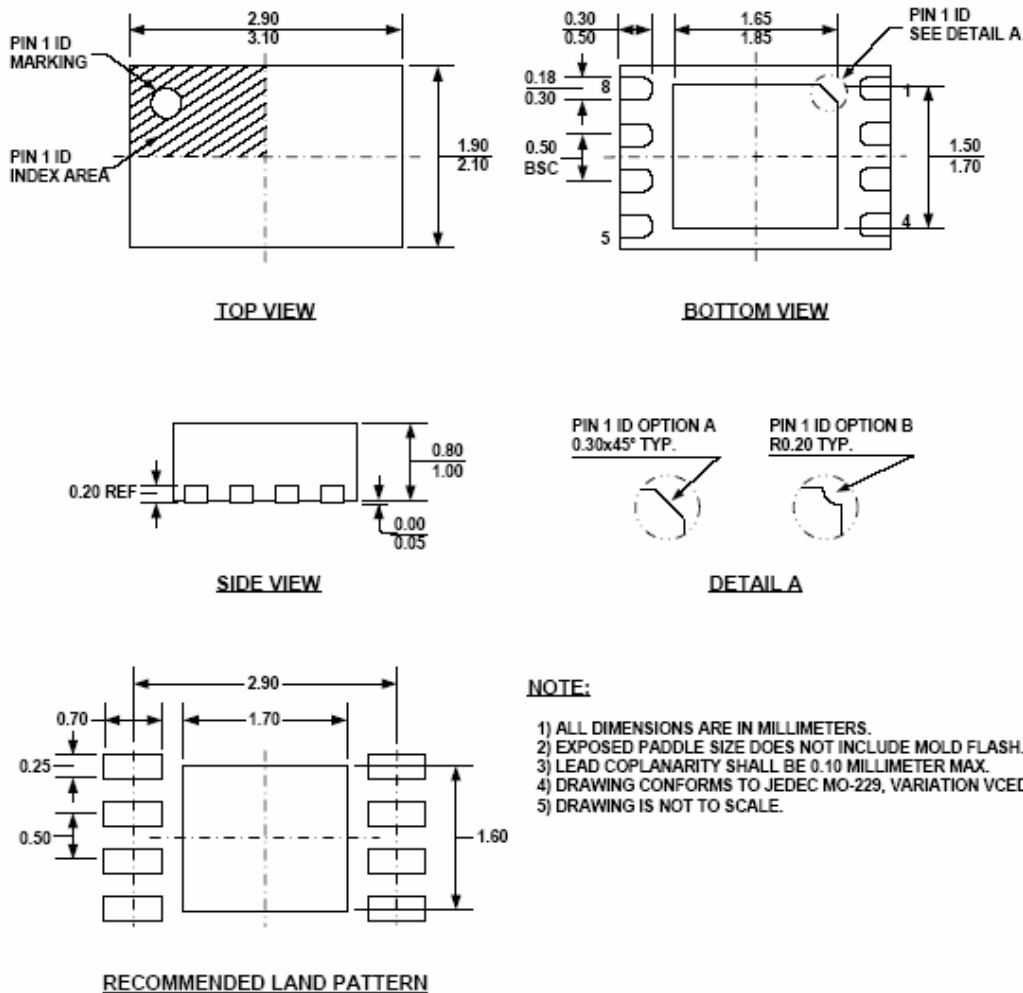


Figure 2—PCB Layout

PACKAGE INFORMATION

QFN8 (2mm x 3mm)



NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VCED-2.
- 5) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.