# MP2188

## Dual 3A, 5.5V, 1.2MHz, COT Synchronous Step-Down Switchers With Auto Output Discharge

The Future of Analog IC Technology

## DESCRIPTION

The MP2188 is a monolithic, step-down, switch-mode dual converter with internal power MOSFETs. It can achieve up to 3A continuous output current from a 2.5V–to-5.5V input voltage with excellent load and line regulation. The output voltages of two channels are 1.1V and 1.8V respectively.

The constant-on-time control scheme provides fast transient response and eases loop stabilization. Fault condition protections include cycle-by-cycle current limiting and thermal shutdown.

The MP2188 is available in small 2.2mmx2.6mm QFN-16 package and requires only a minimal number of readily available standard external components.

The MP2188 is ideal for a wide range of applications including high-performance DSPs, FPGAs, smartphones, portable instruments, and DVD drivers.

## FEATURES

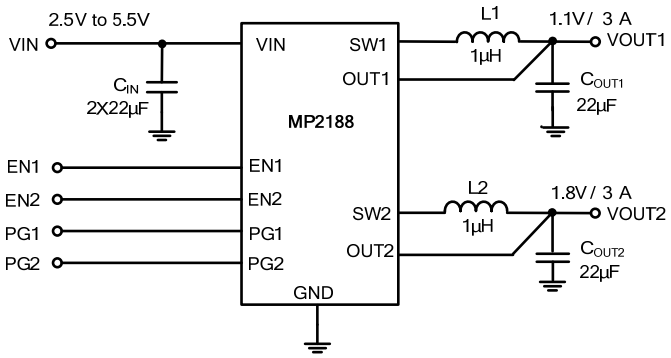
- Wide 2.5V-to-5.5V Operating Input Range
- Fixed Output Voltages: 1.1V & 1.8V
- Adjustable Output Voltage from 0.8V by external FB Resistor
- 100% Duty Cycle in Dropout
- Up to 3A Output Current
- Low IQ: 80μA
- 60mΩ and 30mΩ Internal Power MOSFET Switches
- Default 1.2MHz Switching Frequency
- EN and Power-Good for Power Sequencing
- Cycle-by-Cycle Over-Current Protection
- Auto Discharge at Power-Off
- Short-Circuit Protect with Hiccup Mode
- Stable with Low-ESR Output Ceramic Capacitors
- Available in a 2.2mm x 2.6mm QFN-16 Package

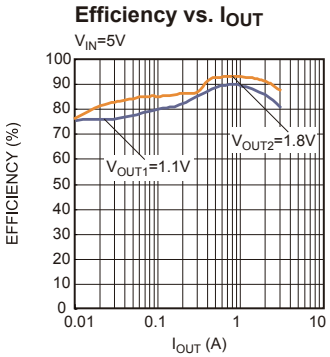
## APPLICATIONS

- Solid State Drives(SSD)
- Low Voltage I/O System Power
- Handheld/Battery-powered Systems
- Wireless/Networking Cards



## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|---|---|---|
| MP2188GQA | QFN-16(2.2mmx2.6mm) | *See Below* |

* For Tape & Reel, add suffix –Z (e.g. MP2188GQA–Z);

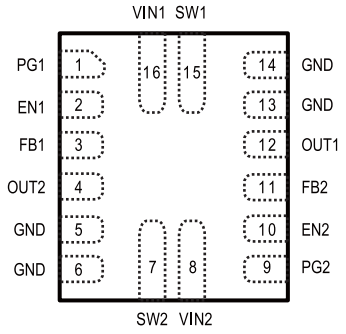
## TOP MARKING

AKJ
YWW
LLL

AKJ: product code of MP2188GQA;
Y: year code;
WW: week code:
LLL: lot number;

## PACKAGE REFERENCE

**TOP VIEW**




**QFN-16**

## ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage $V_{IN}$ ..... 6V
$V_{SW}$ ..... (-3V for < 10ns & -5V for <5ns) to 6.5V (7V for <10ns & 9V for <5ns)
All Other Pins .....-0.3V to +6 V
Junction Temperature .....150°C
Lead Temperature .....260°C
Continuous Power Dissipation ($T_A$ = 25°C) (2)
…….. ..... 1.67W
Storage Temperature..... -65°C to +150°C

## *Recommended Operating Conditions* (3)

Supply Voltage $V_{IN}$ .....2.5V to 5.5V
Output Voltage $V_{OUT}$..... 0.8V to $D_{max}$*$V_{IN}$
Operating Junction Temp. ($T_J$). -40°C to +125°C

## *Thermal Resistance* (4) $\theta_{JA}$ $\theta_{JC}$

| | | | |
|---|---|---|---|
| QFN-16 (2.2mm x 2.6mm) | 75 | 16 | °C/W |

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 5V, $T_J$=-40°C to +125°C, typical value is tested at $T_J$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Internal Feedback Voltage | $V_{FB}$ | 2.5V ≤ $V_{IN}$ ≤ 5.5V, $T_J$=25°C | -1.5% | 0.600 | +1.5% | V/% |
| | | | -2% | | +2% | |
| Fixed Output Voltage | Vo | 1.1V rail, $T_J$=25°C | -1.5% | 1.1 | +1.5% | V/% |
| | | 1.8V rail, $T_J$=25°C | -1.5% | 1.8 | +1.5% | |
| PFET Switch ON Resistance | $R_{DSON\_P}$ | | | 60 | | mΩ |
| NFET Switch ON Resistance | $R_{DSON\_N}$ | | | 30 | | mΩ |
| Switch Leakage | | $V_{EN1\ or\ 2}$ = 0V, $V_{IN}$ = 5V<br>$V_{SW1\ or\ 2}$ = 0V and 5V, $T_J$=25°C | | 0.1 | 2 | μA |
| PFET Current Limit(5) | | | 4.7 | 5.3 | | A |
| ON Time | $t_{ON}$ | $V_{IN}$=5V, $V_{OUT1}$ =1.1V | | 183 | | ns |
| | | $V_{IN}$=5V, $V_{OUT\ 2}$=1.8V | | 300 | | |
| Switching frequency | $f_s$ | $V_{IN}$=5V, $V_{OUT1}$ =1.1V, $I_{OUT1}$ =1A<br>$V_{IN}$=5V, $V_{OUT2}$ =1.8V, $I_{OUT2}$ =1A, $T_J$=25°C | -20% | 1200 | +20% | kHz |
| Minimum OFF Time | $t_{MIN-OFF}$ | | | 50 | | ns |
| Soft-Start Time | $t_{SS-ON}$ | | | 1.3 | | ms |
| Soft-Stop Time | $t_{SS-OFF}$ | | | 1 | | ms |
| Power-Good Upper Trip Threshold | $PG_H$ | FB voltage with respect to the regulation | | +10% | | % |
| Power-Good Lower Trip Threshold | $PG_L$ | | | -10% | | % |
| Power-Good Delay | $PG_D$ | | | 110 | | μs |
| Power-Good Sink Current Capability | $V_{PG-L}$ | Sink 1mA | | | 0.4 | V |
| Power Good Logic High Voltage | $V_{PG-H}$ | $V_{IN}$=5V | 4.9 | | | V |
| Power Good Internal Pull-Up Resistor | $R_{PG}$ | | | 500 | | kΩ |
| Under-Voltage Lockout Threshold Rising | | | 2.0 | 2.2 | 2.4 | V |
| Under-Voltage Lockout Threshold Hysteresis | | | | 150 | | mV |
| EN Input Logic Low Voltage | | | | | 0.4 | V |
| EN Input Logic High Voltage | | | 1.2 | | | V |
| EN Input Current | | $V_{EN1\ or\ 2}$=2V | | 2 | | μA |
| | | $V_{EN1\ or\ 2}$=0V | | 0.1 | | μA |
| Supply Current (Shutdown) | | $V_{EN1\ or\ 2}$=0V | | 0.1 | | μA |
| Supply Current (Quiescent) | | $V_{EN}$=2V, $V_{IN}$=3.6V, Both channel on | | 80 | | μA |
| Thermal Shutdown (6) | | | | 150 | | °C |
| Thermal Hysteresis (6) | | | | 30 | | °C |

**Notes:**

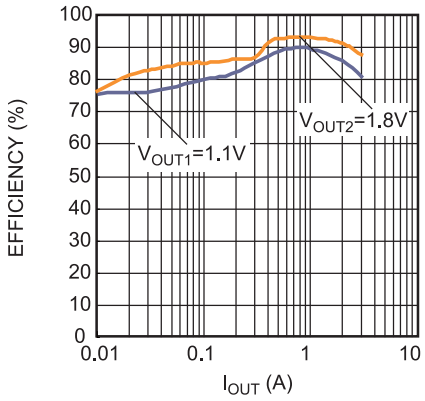
5) Guaranteed by engineering sample characterization.

6) Guaranteed by design.

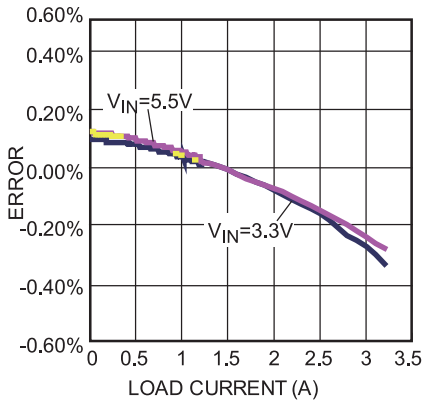
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 5V, $V_{OUT1}$ = 1.1V, $V_{OUT2}$ = 1.8V, L = 1.0µH, $C_{OUT}$=22µF, $T_A$ = 25°C, unless otherwise noted.**

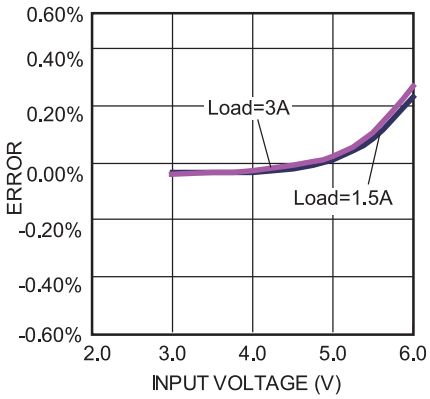
### Efficiency vs. $I_{OUT}$



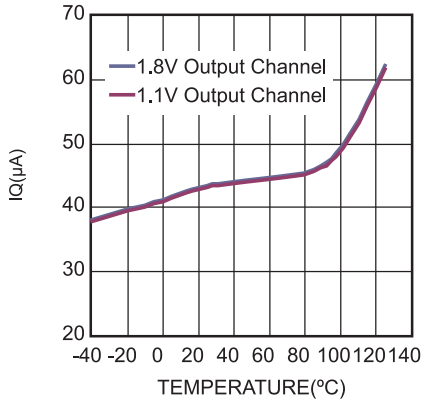

### Load Regulation



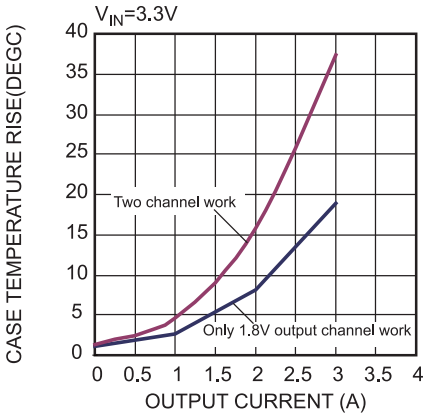

### Line Regulation



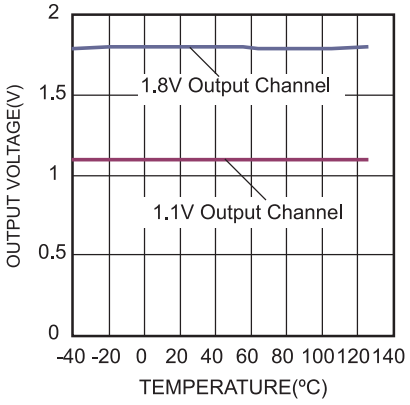

### Quiescent Current vs. Temperature



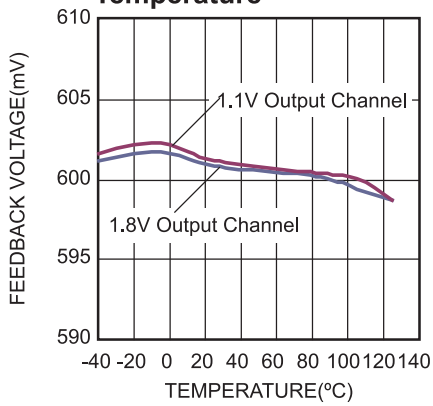

### Case Temperature Rise (Tcase-Tambient) vs. $I_{OUT}$




### Output Voltage vs. Temperature



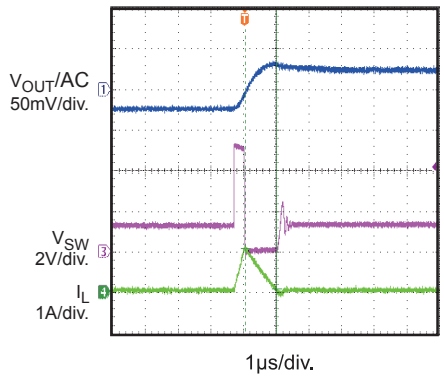

### Feedback Voltage vs. Temperature



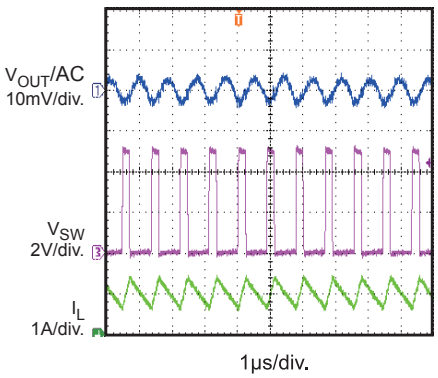
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5V, $V_{OUT1}$ = 1.1V, $V_{OUT2}$ = 1.8V, L = 1.0µH, $C_{OUT}$=22µF, $T_A$ = 25°C, unless otherwise noted.**

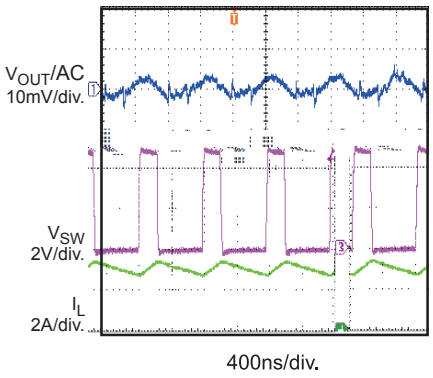
### Output Ripple
$I_{OUT}$=0A



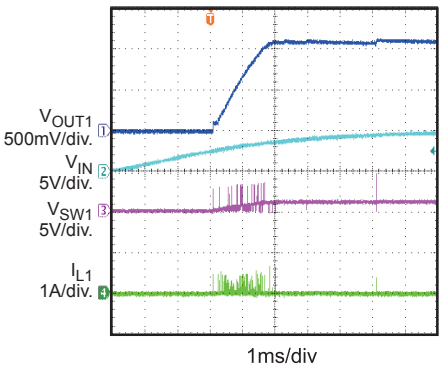

### Output Ripple
$I_{OUT}$=1A



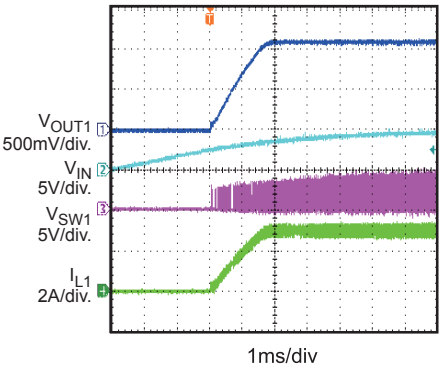

### Output Ripple
$I_{OUT}$=3A



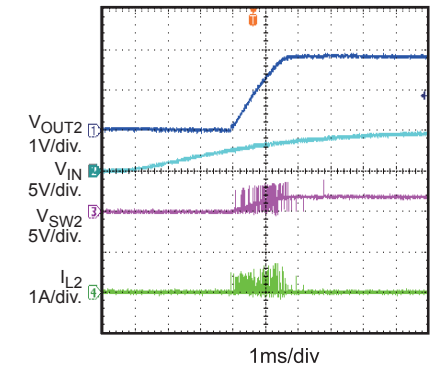

### VIN Power On
$V_{OUT1}$=1.1V, $I_{OUT1}$=0A



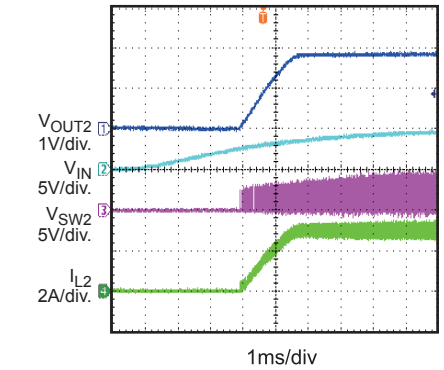

### VIN Power On
$V_{OUT1}$=1.1V, $I_{OUT1}$=3A



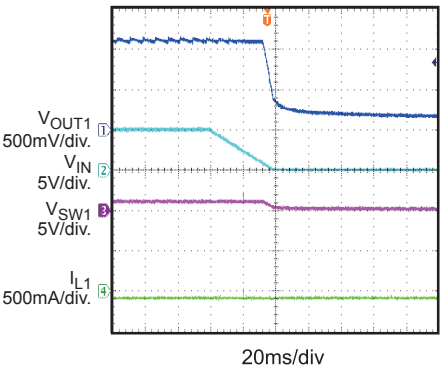

### VIN Power On
$V_{OUT2}$=1.8V, $I_{OUT2}$=0A



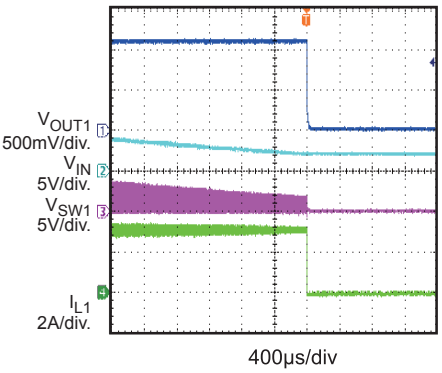

### VIN Power On
$V_{OUT2}$=1.8V, $I_{OUT2}$=3A




### VIN Power Off
$V_{OUT1}$=1.1V, $I_{OUT1}$=0A



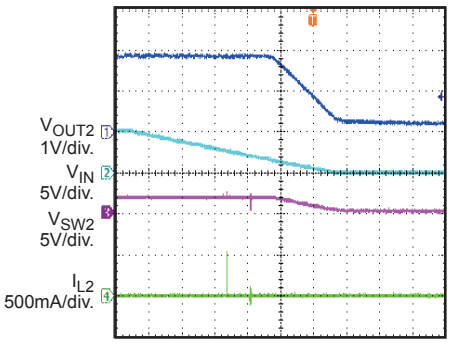

### VIN Power Off
$V_{OUT1}$=1.1V, $I_{OUT1}$=3A



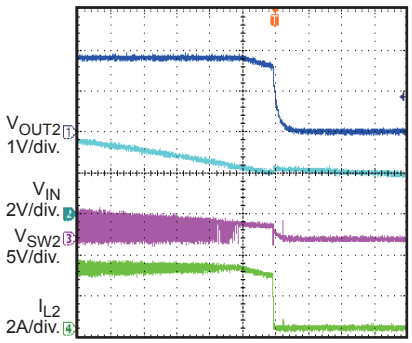
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5V, $V_{OUT1}$ = 1.1V, $V_{OUT2}$ = 1.8V, L = 1.0µH, $C_{OUT}$=22µF, $T_A$ = 25°C, unless otherwise noted.**

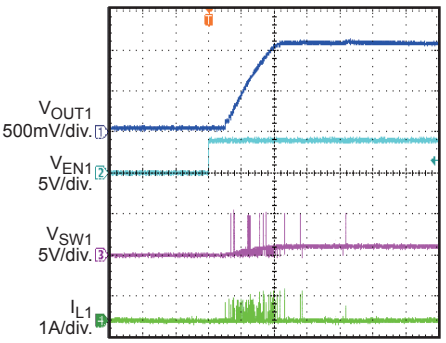
### VIN Power Off
$V_{OUT2}$=1.8V, $I_{OUT2}$=0A



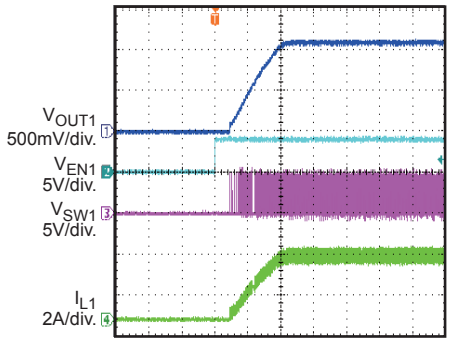

### VIN Power Off
$V_{OUT2}$=1.8V, $I_{OUT2}$=3A



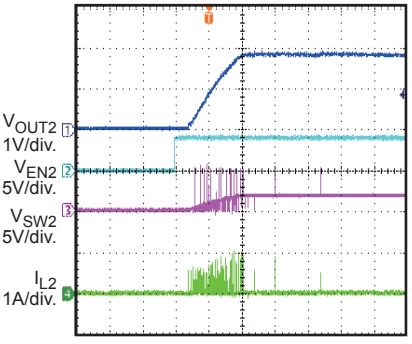

### EN ON
$V_{OUT1}$=1.1V, $I_{OUT1}$=0A



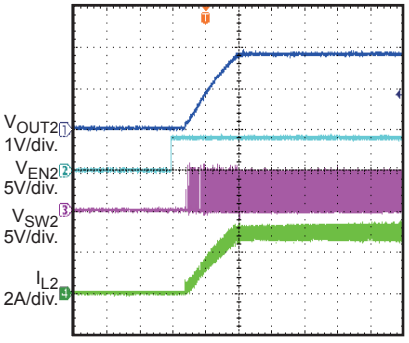

### EN ON
$V_{OUT1}$=1.1V, $I_{OUT1}$=3A



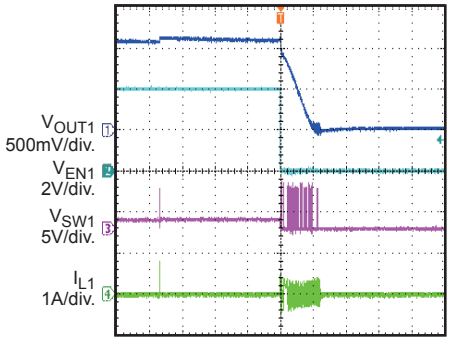

### EN ON
$V_{OUT2}$=1.8V, $I_{OUT2}$=0A



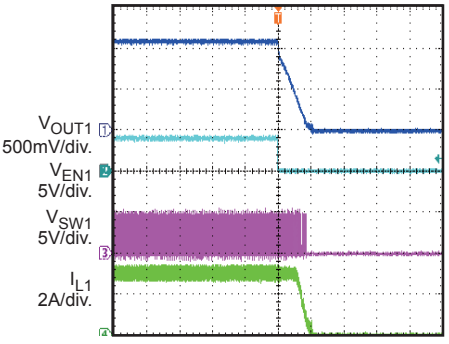

### EN ON
$V_{OUT2}$=1.8V, $I_{OUT2}$=3A



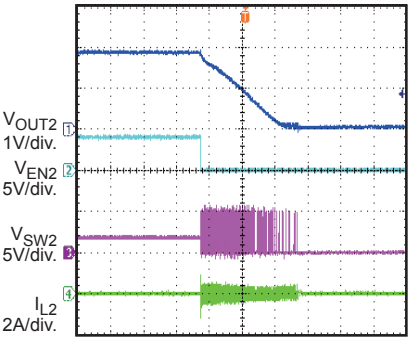

### EN OFF
$V_{OUT1}$=1.1V, $I_{OUT1}$=0A




### EN OFF
$V_{OUT1}$=1.1V, $I_{OUT1}$=3A




### EN OFF
$V_{OUT2}$=1.8V, $I_{OUT2}$=0A

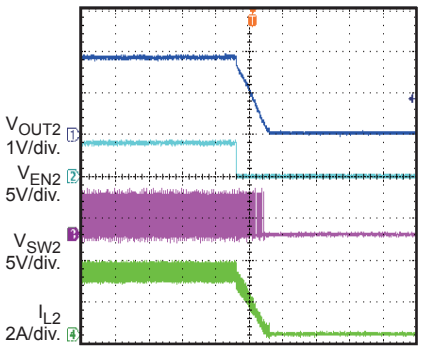


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5V, $V_{OUT1}$ = 1.1V, $V_{OUT2}$ = 1.8V, L = 1.0µH, $C_{OUT}$=22µF, $T_A$ = 25°C, unless otherwise noted.**

**EN OFF**

$V_{OUT2}$=1.8V, $I_{OUT2}$=3A



## PIN FUNCTION

| QFN16 Pin # | Name | Description |
|---|---|---|
| 1 | PG1 | Power Good Indicator of channel 1. The output of this pin is an open drain with an internal pull up resistor to IN. PG1 is pulled up to VIN1 when the FB1 voltage is within 10% of the regulation level. If the FB1 voltage is out of that regulation range, it is LOW. |
| 2 | EN1 | On/Off Control of channel 1. |
| 3 | FB1 | Internal FB point of channel 1. Floating FB1 PIN will get pre-set fixed output voltage. |
| 4 | OUT2 | Input Sense of channel 2. For output voltage sense. |
| 5, 6, 13, 14 | GND | Power Ground. |
| 7 | SW2 | Switch Output of channel 2. |
| 8 | VIN2 | Supply Voltage of channel 2. The MP2188 operates from a +2.5V-to-+5.5V unregulated input. |
| 9 | PG2 | Power Good Indicator of channel 2. The output of this pin is an open drain with an internal pull up resistor to IN. PG2 is pulled up to VIN2 when the FB2 voltage is within 10% of the regulation level. If the FB2 voltage is out of that regulation range, it is LOW. |
| 10 | EN2 | On/Off Control of channel 2. |
| 11 | FB2 | Internal FB point of channel 2. Floating FB2 PIN will get pre-set fixed output voltage. |
| 12 | OUT1 | Input Sense of channel 1. For output voltage sense. |
| 15 | SW1 | Switch Output of channel 1. |
| 16 | VIN1 | Supply Voltage of channel 1. The MP2188 operates from a +2.5V-to-+5.5V unregulated input. |

# FUNCTIONAL BLOCK DIAGRAM

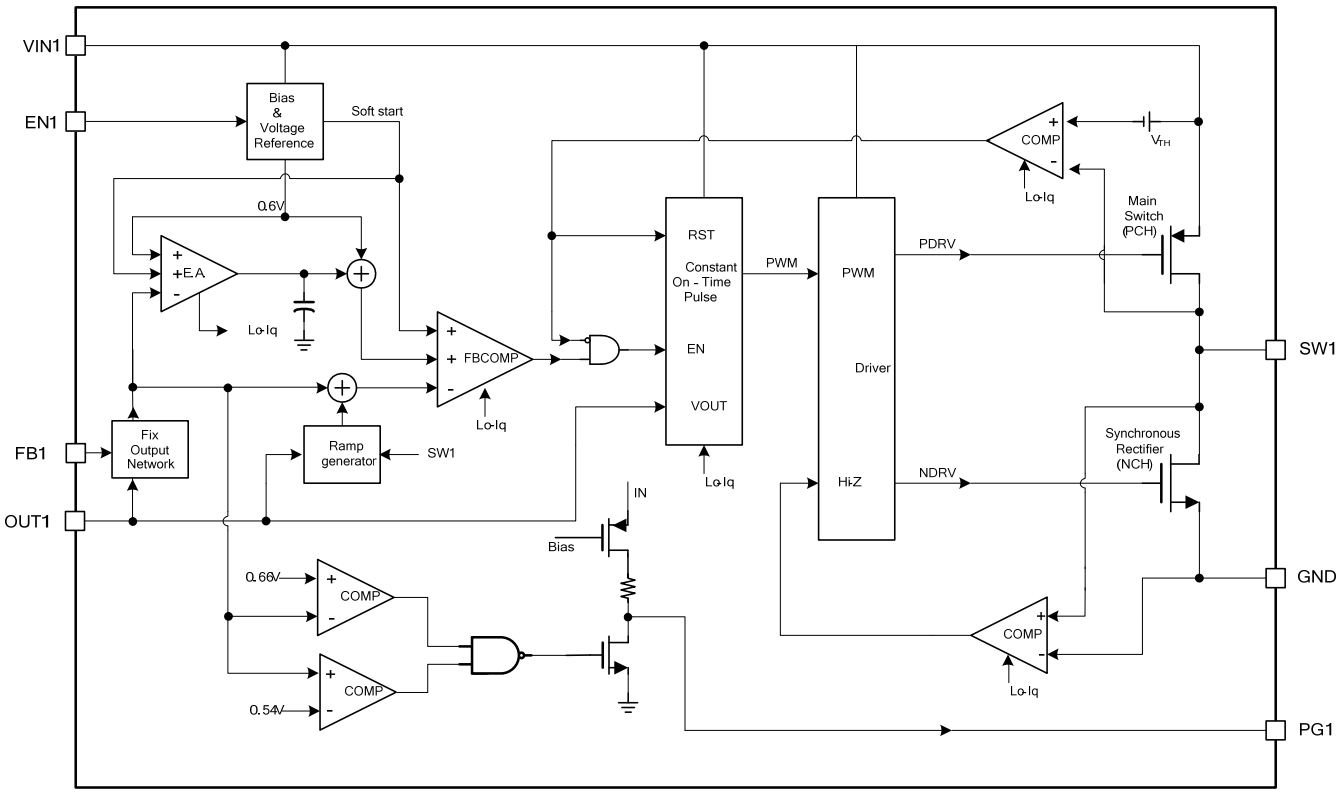



**Figure 1: Functional Block Diagram**
**(Only Channel 1 Included, Channel 2 is the same)**

## OPERATION

The MP2188 uses constant on-time control with input voltage feed-forward to stabilize the switching frequency over its full input range. At light load, the MP2188 employs proprietary control over the low-side MOSFET (LS-FET) and inductor current to eliminate ringing on switching node and improve efficiency. The output voltages are fixed. The output voltages of two channels are 1.1V and 1.8V respectively.

### Constant-On–Time Control

When compared to fixed-frequency PWM control, constant-on–time control offers advantages including simpler control loop and faster transient response. By using input voltage feed-forward, the MP2188 maintains a nearly constant switching frequency across the entire input and output voltage range. The on-time of the switching pulse can be estimated as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.833\mu s$$

To prevent inductor current runaway during the load transient, the MP2188 has a fixed minimum off time of 50ns. However, this minimum off time limit does not affect the operation of the MP2188 in steady state in any way.

### Light-Load Operation

Under light-load conditions, the MP2188 uses a proprietary control scheme to save power and improve efficiency: it gradually ramps down the LS-FET current to its minimum instead of turning off the LS-FET immediately when the inductor current starts to reverse. The gradual current drop avoids ringing at the switching node that always occurs in discontinuous conduction mode (DCM) operation.

There is a zero current cross detect circuit (ZCD) to judge if the inductor current starts to reverse. When the inductor current touch ZCD threshold, the low side switch will start to be turned off.

The DCM mode happens only after low side switch turned off by ZCD circuit. Considering the ZCD circuit propagation time, the typical delay is 30ns. It means the inductor current still fall after the ZCD is trigger during this delay. If the inductor current falling slew rate is fast (Output voltage is high or close to input Voltage), the low side MOSFET is turned off at the moment inductor current may be negative. This phenomena will cause MP2188 cannot enter DCM operation. If the DCM mode is required, the off time of low side MOSFET in CCM should be longer than 60ns. It means the maximum duty is 92% to guarantee DCM mode at light load. For example, Vin is 3.4V and Vo is 3.3V, the off time in CCM is 24.5ns. It is difficult to enter DCM at light load. And using smaller inductor can improve it and make it enter DCM easily.

### Enable

When the input voltage exceeds the under-voltage lockout (UVLO) threshold—typically 2.2V—the MP2188 can be enabled by pulling the EN pin higher than 1.2V. Leaving EN pin floating or grounded will disable the MP2188. There is an internal 1MΩ resistor from the EN pin to ground.

### Soft-Start/Stop

MP2188 has a built-in soft-start that ramps up the output voltage at a constant slew rate that avoids overshooting at startup. The soft-start time is typically about 1.3ms. When disabled, the MP2188 ramps down the internal reference voltage to allow the load to linearly discharge the output.

### Power GOOD Indictor

MP2188 has an open drain with a 500kΩ pull-up resistor pin for power good (PG) indication. When the FB pin is within ±10% of the regulatory voltage (0.6V), the PG pin is pulled up to VIN by the internal resistor. If the FB pin voltage is outside the ±10% window, the PG pin is pulled to ground by an internal MOSFET. The MOSFET has a maximum $R_{dson}$ of less than 100Ω.

### Current limit

The MP2188 has a 5.3A minimum current limit for the high side switch (HS-FET). When the HS-FET hits its current limit, MP2188 enters

hiccup mode until the current drops to prevent the inductor current from rising and possibly damaging the components.

**Short Circuit and Recovery**

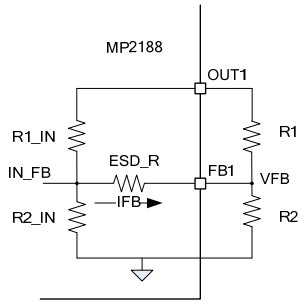
The MP2188 also enters short-circuit protection (SCP) mode when it hits the current limit, and tries to recover from the short circuit by entering hiccup mode. In SCP, the MP2188 disables the output power stage, discharges a soft-start capacitor, and then enacts a soft-start procedure. If the short-circuit condition still holds after soft-start ends, the MP2188 repeats this operation until the short circuit ceases and output rises back to regulation level.

# APPLICATION INFORMATION

## COMPONENT SELECTION

### Setting the Output Voltage

The MP2188 output voltage of the two channels can be changed with external feedback resistors. The feedback resistors cannot be too large considering the internal divider resistors. Choose external feedback resistors <20kΩ:




Using below formulas to set the new output voltages:

$$I_{FB} = \frac{V_{OUT} - V_{CH}}{R1\_IN}$$

$$V_{FB} = 0.6 - I_{FB} \times ESD\_R$$

$$R_1 = \frac{V_{OUT} - V_{FB}}{V_{FB} - I_{FB} \times R_2} \times R_2$$

Where, $V_{CH}$ is the pre-set fixed output voltage of each channel.
For channel 1: $V_{CH}$=1.1V, R1_IN =214.58kOhm, ESD_R=3.59kOhm.
For channel 2: $V_{CH}$=1.8V, R1_IN =227.61kOhm, ESD_R=4.28kOhm.

To mask internal resistor well, the adjustable $V_{OUT}$ is recommended to set higher than 0.8V. Table 1 lists the recommended resistors values for common output voltage.

**Table 1: Resistor Values for Common Output Voltages**

| $V_{OUT}$(V) | 1.1V output channel | | 1.8V output channel | |
|---|---|---|---|---|
| | R1(kΩ) | R2(kΩ) | R3(kΩ) | R4(kΩ) |
| 1.2 | 3.01 | 3 | 3 | 3 |
| 1.5 | 4.7 | 3 | 4.3 | 3 |
| 1.8 | 6.34 | 3 | 6.2 | 3 |
| 2.5 | 10.5 | 3 | 10 | 3 |
| 3.3 | 15.4 | 3 | 14.7 | 3 |

### Selecting the Inductor

A 0.82μH to 4.7μH inductor is recommended for most applications. For highest efficiency, chose an inductor with a DC resistance less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where $\Delta I_L$ is the inductor ripple current.

Choose an inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

### Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR values and small temperature coefficients. For most applications, a 22μF capacitor is sufficient. For higher output voltage, use 47μF to improve system stability.

Since the input capacitor absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at VIN = $2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor whose RMS current rating is greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, use a small high-quality ceramic capacitor (0.1μF), placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

**Selecting the Output Capacitor**

The output capacitor ($C_{OUT}$) maintains the output DC voltage. Use ceramic capacitors. Low-ESR capacitors keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_S \times C_{OUT}})$$

Where L is the inductor value and $R_{ESR}$ is the equivalent series resistance of the output capacitor.

Using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system.

**PCB Recommendation of MP2188**

Proper layout of the switching power supplies is very important, and sometimes critical for proper operation. For high-frequency switching converters, poor layout could lead to poor line or load regulation and stability issues.
The high current paths (GND, IN, and SW) should be placed very close to the device using short, direct, and wide traces. The input capacitor needs to be as close as possible to the IN and GND pins. The external feedback resistors should be placed next to the FB pin. Keep the switching node SW short and away from the feedback network.
For MP2188 PCB layout, there are two recommended layouts for selecting. Figure 2 (refer to schematic figure 4) shows symmetric PCB layout. If the layout is space limited, and has to be asymmetric, a ferrite bead (The Impedance should >220mΩ@100MHz) is suggested to separate the two input of each channel. Figure 3 (refer to schematic figure 5) shows asymmetric PCB layout.

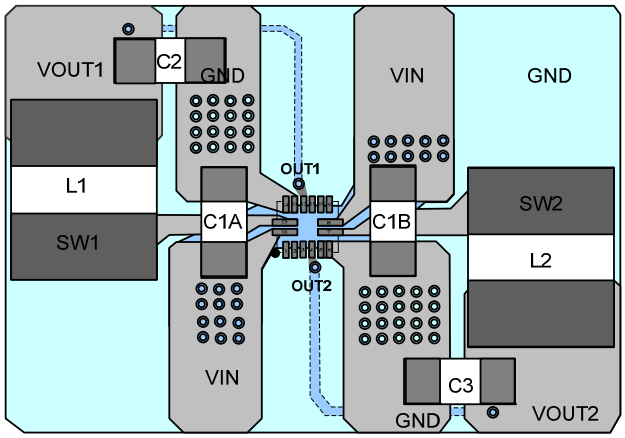



**Figure 2: symmetric PCB layout**

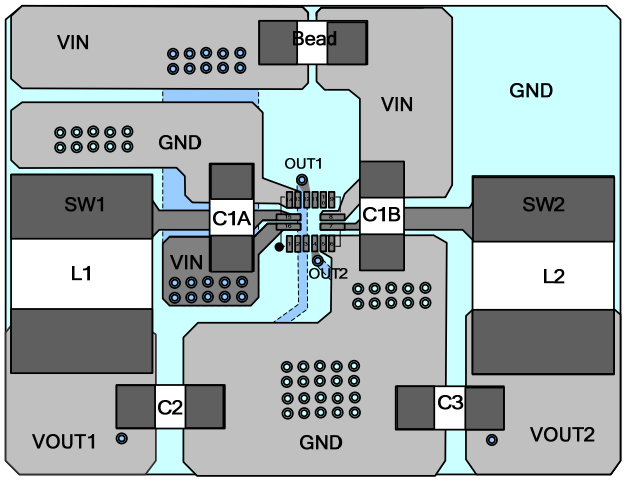



**Figure 3: asymmetric PCB layout**

### Design Example

Below is a design example following the application guidelines for the specifications:

**Table 2: Design Example**

| | |
|---|---|
| $V_{IN}$ | 5V |
| $V_{OUT1}$ | 1.1V |
| $V_{OUT2}$ | 1.8V |
| $I_{OUT1}$=$I_{OUT2}$ | 3A |

The detailed application schematic is shown in Figure 4. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

# TYPICAL APPLICATION CIRCUITS

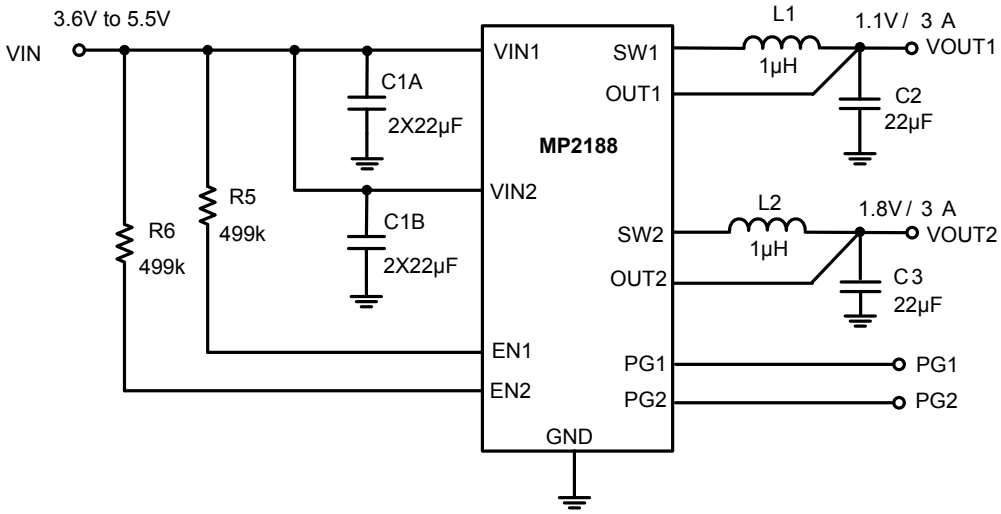



**Figure 4: MP2188 Typical Application Circuit with Symmetric PCB Layout**

Note: Low $V_{IN}$ application may need more input capacitors

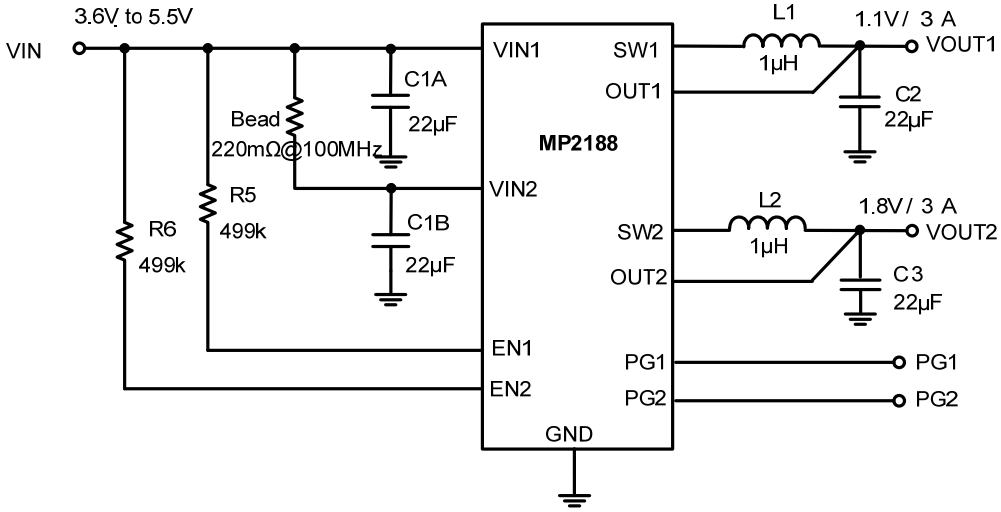
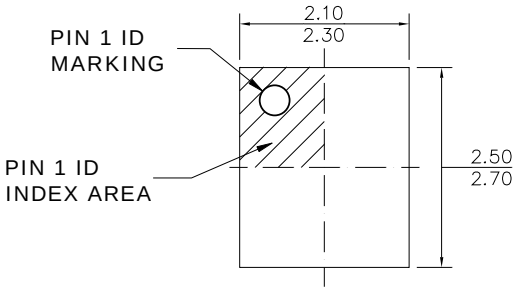



**Figure 5: MP2188 Typical Application Circuit with Asymmetric PCB Layout**

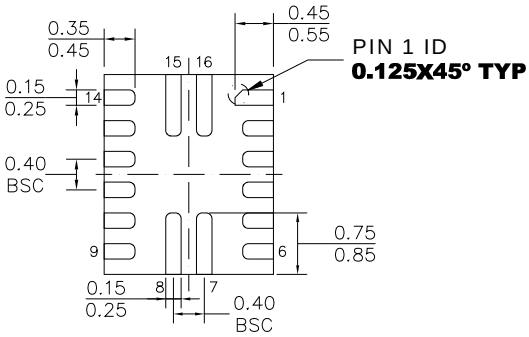
Note: Low $V_{IN}$ application may need more input capacitors

# PACKAGE INFORMATION

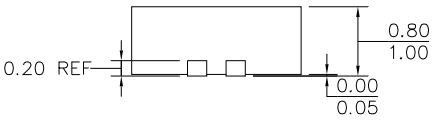
## QFN-16 (2.2mm x 2.6mm)



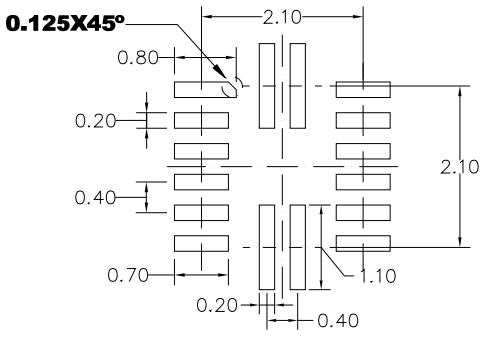

TOP VIEW




BOTTOM VIEW




SIDE VIEW




NOTE:

**1) ALL DIMENSIONS ARE IN MILLIMETERS.**
**2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.**
**3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.**
**4) JEDEC REFERENCE IS MO-220.**
**5) DRAWING IS NOT TO SCALE.**