MP8001, MP8001A

15W Power Over Ethernet PoE Powered Device (PD) Controller

The Future of Analog IC Technology

DESCRIPTION

The MP8001/MP8001A are IEEE 802. 3 af POE compliant Powered Device (PD) controllers. they include detection and classification modes as well as a 100V output pass device having a temperature compensated current limit over the specified temperature range. Thermal protection is built in to accommodate both transient and/or overload conditions, shutting the part down and protecting the input source as well as the output load depending on the particular fault conditions. Inrush current limiting is included to slowly charge the input capacitor without interruption due to die heating, a problem encountered without the current limit foldback feature.

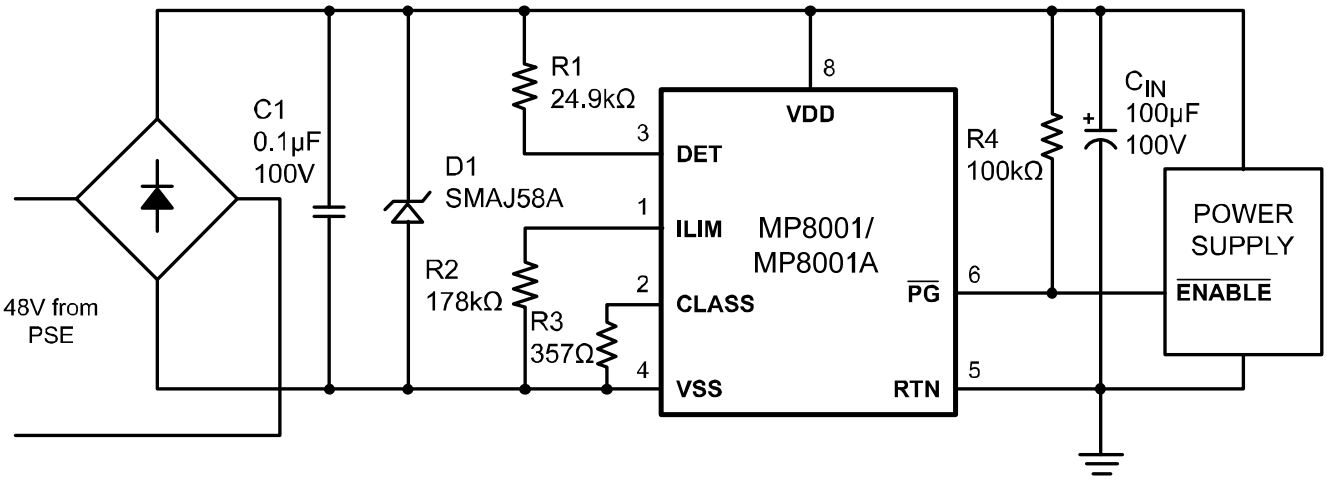
FEATURES

- Meets IEEE 802. 3 af Specifications
- 100V, 1Ω Integrate DMOS Device
- 420mA Current Limit for MP8001
  810mA Current Limit for MP8001A
- Open Drain Power Good Output
- SOIC-8 Package

APPLICATIONS

- VoIP Telephones
- Network Cards
- Security Camera Systems
- Safety Backup Power
- Remote Internet Power

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking	Free Air Temperature (T_A)
MP8001DS*	SOIC-8	MP8001DS	-40°C to +85°C
MP8001ADS**	SOIC-8	MP8001A	-40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP8001DS–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP8001DS–LF–Z)

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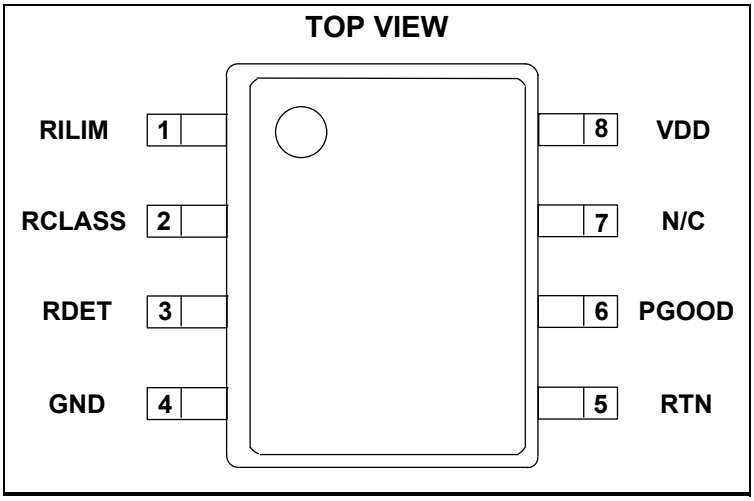
PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{DD}, RTN ..... -0.3V to +100V
PG, DET .....-0.3V to +57V
I_{LIM} .....-0.3V to +7V
CLASS .....-0.3V to +12V
Continuous Power Dissipation(T_A = +25°C) (2)
.....1.19W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....0V to 57V
Output Current I_{OUT} ..... 0 to 0.4A
Operating Temperature..... -40°C to +85°C
Junction Temperature..... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
SOIC-8	105	50	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{DD} = 48V, all voltages with respect to V_{SS}, V_{SS} = 0V; R_{DET} = 26.1kΩ, R_{CLASS} = 4.42KΩ, R_{ILIM} =178kΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition		Min	Typ	Max	Units
Detection							
Detection on	V_{DET_ON}	V_{DD}=V_{RTN}=V_{PG}=1.9V			1.9		V
Detection off	V_{DET_OFF}	V_{DD}=V_{RTN}=V_{PG}=11V			11		V
Detection on/off Hysteresis	V_{DET_H}	Falling below 11V on Threshold			0.2		V
DET Leakage Current	V_{DET_LK}	V_{DET}=V_{VDD}=57V, Measure I_{DET}			0.1	5	µA
Detection Current	I_{DET}	V_{VDD}=V_{RTN} R_{DET}=26.1kΩ, Measure I_{VDD}+I_{RTN}+I_{DET}	V_{DD}= 3V	135	140	145	µA
			V_{DD}= 10.1V	405	420	435	µA
Classification							
V_{CLASS} Output Voltage	V_{CL}	Over a Load Range of 1mA to 41.2 mA		9.6	10	10.3	V
Classification Current	I_{CLASS}	R_{CLASS}=4420Ω, 13≤V_{VDD}≤21V (guar by V_{CL})		2.2	2.4	2.8	mA
		R_{CLASS}=953Ω, 13≤V_{VDD}≤21V (guar by V_{CL})		10.3	10.6	11.3	
		R_{CLASS}=549Ω, 13≤V_{VDD}≤21V (guar by V_{CL})		17.7	18.3	19.5	
		R_{CLASS}=357Ω, 13≤V_{VDD}≤21V (guar by V_{CL})		27.1	28	29.5	
		R_{CLASS}=255Ω, 13≤V_{VDD}≤21V (guar by V_{CL})		38	39.4	41.2	
Classification Lower Threshold	V_{CL_ON}	Regulator Turns on, V_{VDD} Rising		10.2	11.3	13	V
Classification Upper Threshold	V_{CU_OFF}	Regulator Turns off, V_{VDD} Rising		21	21.9	23	V
	V_{CU_H}	Hysteresis			0.4		V
IC Supply Current during Classification	I_{IN_CLASS}	V_{DD} = 17.5V, CLASS Floating, RTN Tied to VSS			300	500	µA
Leakage Current	$I_{LEAKAGE}$	V_{CLASS} = 0 V, V_{VDD} = 57V				1	µA
Pass Device							
On Resistance	$R_{DS(ON)}$	I_{RTN}=300mA			1.0	1.2	Ω
Leakage Current	I_{SW_LK}	V_{VDD}=V_{RTN}=57V			1	15	µA
Current Limit	I_{LIMIT}	V_{RTN}=1V	MP8001	380	420	460	mA
			MP8001A	720	810	900	mA
Inrush Limit	I_{INRUSH}	V_{RTN}=2V, R_{ILM}=178kΩ	MP8001	120	150	180	mA
			MP8001A	290	330	370	mA
PG							
Latch off Voltage Threshold Rising(5)		V_{RTN} Rising		9.5	10	10.5	V
Latch off Voltage Threshold Falling(5)		V_{RTN} Falling			1.2		V
PG Deglitch(5)		Delay Rising and Falling PDG		75	150	225	µs
Output Low Voltage		I_{PG} = 400 µA			0.12	0.4	V

ELECTRICAL CHARACTERISTICS (*continued*)

V_{DD} = 48V, all voltages with respect to V_{SS}, V_{SS} = 0V; R_{DET} = 26.1kΩ, R_{CLASS} = 4.42KΩ, R_{ILIM} =178kΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Leakage Current		V_{PG} = 57 V, V_{RTN} = 0 V		0.1	1	µA
UVLO						
Voltage at V_{VDD}		V_{VDD} Rising (including 1.4V Diode drop)	38	40	42	V
		V_{VDD} Falling (including 1.4V Diode drop)	30.2	31.5	32.8	
Thermal Shutdown						
Thermal Shut down Temperature	T_{RISE}	Temperature Rising	135			ºC
Hysteresis	T_{HYS}			40		ºC
Thermal Shut down Counter(5)	T_{COUNT}	Events Prior to Latch off		8		counts
Thermal Counter Reset Voltage(5)	V_{CRST}	Must Drop below Classification Range		10.8		V
Bias Current						
Operating Current	$I_{Q(VDD)}$	V_{DD} = 48V, Pins 5, 6 Floating Measure I_{VDD}		240	450	µA

Notes:

5) Guaranteed by Design.

PIN FUNCTIONS

Pin #	Name	Description
1	ILIM	Startup I_{LIM} Value Set (optional at this point).
2	CLASS	Classification Resistor.
3	DET	26.1kΩ Detection Resistor.
4	VSS	Negative Power Supply Terminal.
5	RTN	Powered Device Negative Power Terminal.
6	PG	Power Good Indicator.
7	NC	No Connect. Possible post-package trim input.
8	VDD	Positive Power Supply Terminal.

OPERATION

The MP8001/MP8001A operate in the manner described here and in the IEEE 802.3af Powered Device (PD) Specifications. These devices (along with the power sourcing element (PSE)) operate as a safety device to supply potentially lethal voltages only when the power sourcing element recognizes a unique, tightly specified resistance at the end of an unknown length of Ethernet cable.

A 26.1kΩ resistance is presented as a load to the PSE in Detection Mode, when the PSE applies two “safe” voltages of less than 10.1V each while measuring the change in current drawn in order to determine the load resistance. If the PSE “sees” the correct load, then it may either further increase the applied voltage to enter the “classification” range of operation or switch on the nominal 48V power to the load.

The classification mode can further specify to the PSE the expected load range of the device under power so that the PSE can intelligently distribute power to as many loads as possible (within its maximum current capabilities). If a classification resistance is not present, the PD load is assumed to be the maximum of approximately 13 Watts. The classification mode is active between 14.5V and 20.5V.

The main power switch will pass a limited current above 31V, charging the external DC-to-DC converter’s input capacitor in a controlled manner. The charging will continue until the controlled current drops below the either an externally programmed limiting level or 420mA/810mA, depending upon the Rlim current setting resistor. The main power switch is internally thermally protected to 135°C by reducing the output current using a foldback technique. The required power dissipation of the IC drops from the allowed peak value of 24W (420mA x 57V) to 0.18W ($(420mA)^2$ x R_{ON}) during the normal operation at turn-on. The minimum allowed capacitance of 5µF will charge in 500µs. A larger capacitor will take a proportionally longer time to charge due to the constant current charging method. If a capacitor that is too large will overheat the part and force it into thermal shutdown. The IC will reattempt charging for a number of cycles but ultimately will be shut down until the input voltage from the PSE is recycled. This is the way the IC protects itself under overload and/or shorted conditions.

BLOCK DIAGRAM

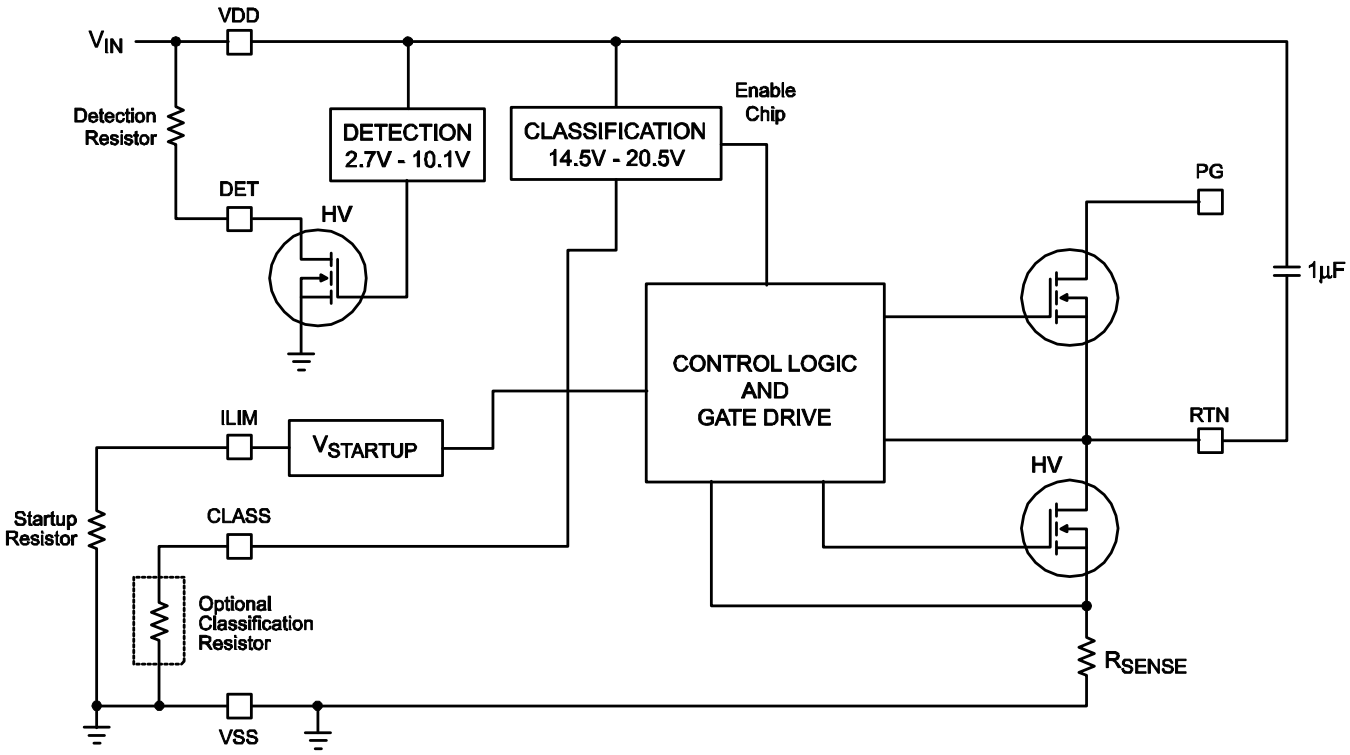
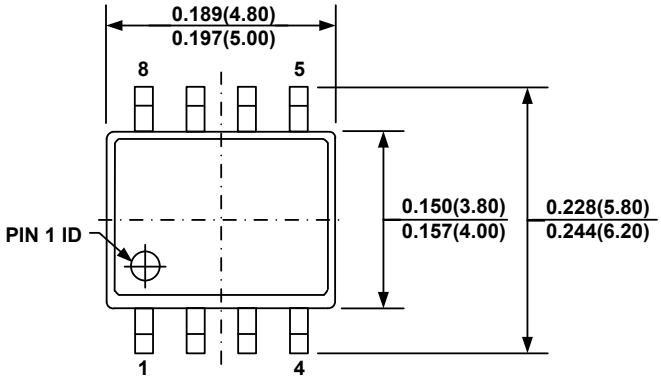


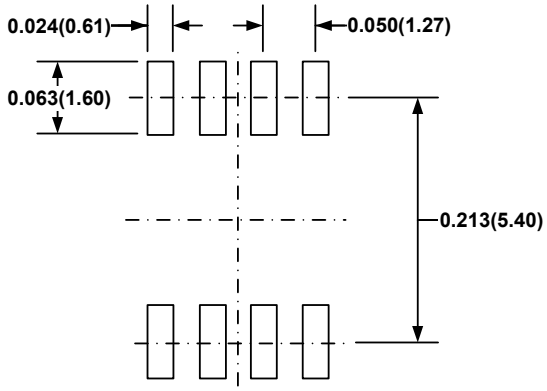
Figure 1—PD Block Diagram

PACKAGE INFORMATION

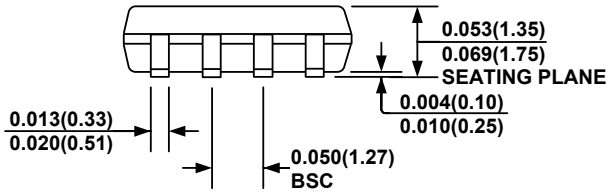
SOIC-8



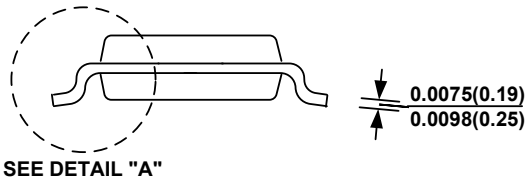
TOP VIEW



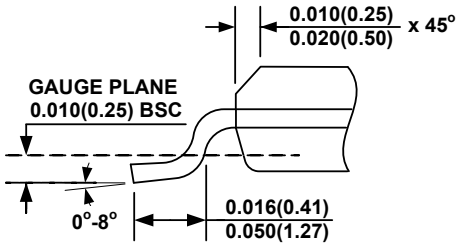
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.