MP86981

20A, 27V Intelli-Phase Solution (Single IC with Integrated HS/LS FETs and Driver)

The Future of Analog IC Technology

DESCRIPTION

The MP86981 is a monolithic Half Bridge with built in internal power MOSFETs and gate drivers. It achieves 20A continuous output current over a wide input supply range.

Integration of the Driver and MOSFETs results in high efficiency due to optimal dead time control and parasitic inductance reduction.

The MP86981 is a Monolithic IC approach to drive up to 20A per phase. This very small 5x5 QFN can be used from 100KHz to 1MHz operation.

This device is designed to work with tri state output controller.

The MP86981 is ideal for notebook applications where efficiency and small size are a premium.

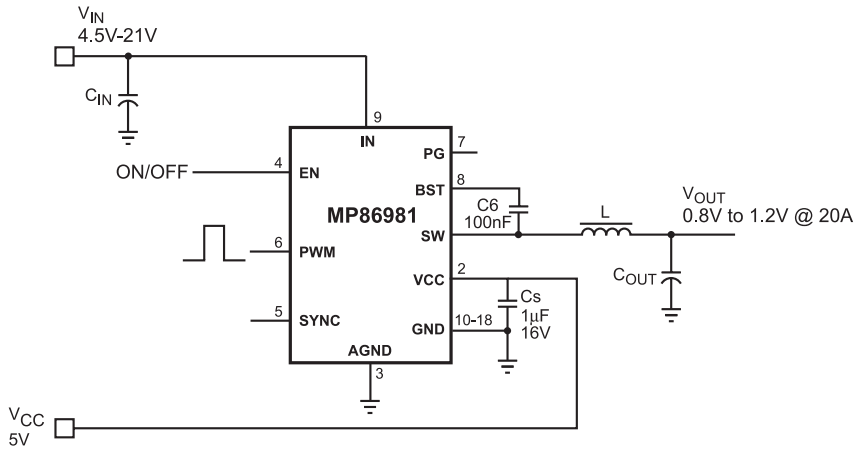
FEATURES

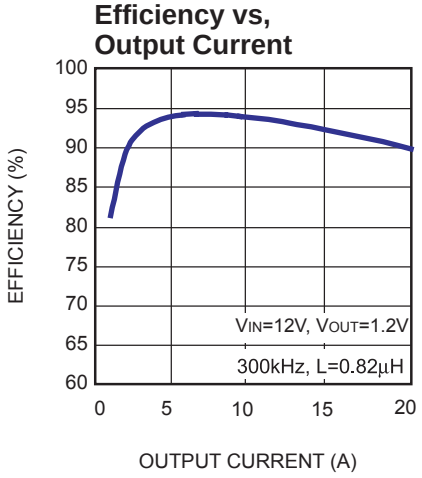
- Wide 4.5V to 21V Operating Input Range
- 20A Output Current
- Simple Logic Interface(5.0V)
- Synchronous Gate Driver Delivers up to 95% Efficiency
- Operation from 100KHz to 1MHz
- Accepts 3-state PWM Input
- Thermal Shutdown
- Used for multi phase operation
- Available in a 5mm x 5mm QFN Package

APPLICATIONS

- Power modules
- Notebook, Core Voltage
- Graphic Card Core Regulators

TYPICAL APPLICATION



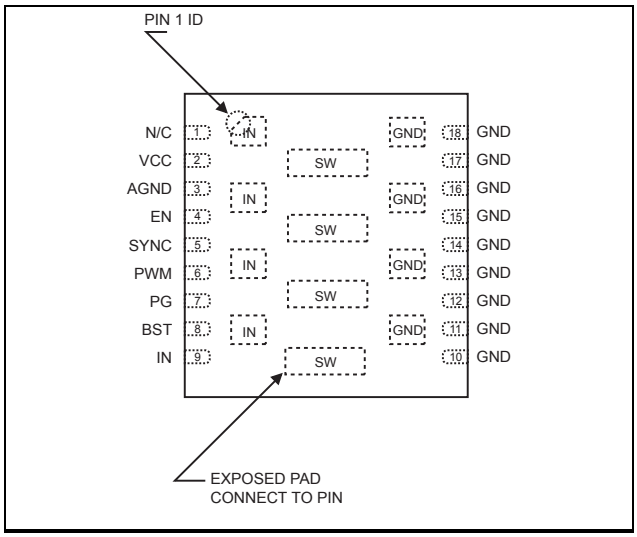


ORDERING INFORMATION

Part Number*	Package	Top Marking	Temperature
MP86981DU	5x5 QFN	MP86981DU	–40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP86981DU–Z); For RoHS compliant packaging, add suffix –LF (e.g. MP86981DU–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 27V
V_{SW} ..... –0.3V to V_{IN} + 0.3V
V_{BS} ..... V_{SW} + 6V
All Other Pins ..... –0.3V to +6V
Continuous Power Dissipation (T_A = +25°C)(2) 3.5W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 4.5V to 21V
Operating Temperature ..... –40°C to +85°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
5x5 QFN	36	8 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on approximately 4" square of 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
I_{CC} Standby	I_{CC_Stdby}	V_{CC} =5V, PWM=EN=LO		230	300	uA
I_{IN} (Shutdown)	$I_{IN\ (Off)}$	V_{CC} = 0V			5	uA
I_{IN} Standby	I_{IN_Stdby}	V_{CC} =5V, PWM=EN=LO	40	70	100	uA
Rise Time (5)		I_{OUT} = 20A		5	8	ns
Fall Time(5)		I_{OUT} = 20A		3	6	ns
PWM to SW Delay Rising	T_{dh}	PWM to SW		20		ns
PWM to SW Delay Falling	T_{dl}	PWM to SW		38		ns
Minimum On-Time				40		ns
Dead-Time Rising(5)				5	8	ns
Dead-Time Falling(5)				5	8	ns
Under Voltage Lockout Threshold Rising				3.7	4.2	V
Under Voltage Lockout Threshold Hysteresis				470		mV
Thermal Shutdown Rising				160		°C
SYNC Pull-Up Current	I_{SYNC}	SYNC=0V		-14		µA
SYNC Logic High Voltage			2			V
SYNC Logic Low Voltage					0.4	V
EN Input Low Voltage					0.4	V
En Input High Voltage			2			V
Power Good Rds(on)		EN=0V		20		Ω
PWM Input						
Input Current	I_{PWM}	V_{PWM}=5V		90		µA
		V_{PWM}=0V		-90		µA
PWM Tri-State Rising Threshold		V_{CC}=5V		1.7		V
PWM Tri-State Falling Threshold		V_{CC}=5V		3.5		V
Tri-State Shutdown Holdoff Time	t_{TSSHD}	V_{CC}=5V, Temperature=25°C		80		ns
UG/LG Three-State Propagation Delay	t_{PTS}			20		ns
USW Turn-Off Propagation Delay	t_{PDUL}	V_{CC}=5V		35		ns
LSW Turn-Off Propagation Delay	t_{PDLL}	V_{CC}=5V		16		ns
USW Turn-On Propagation Delay	t_{PDUH}	V_{CC}=5V		26		ns
LSW Turn-On Propagation Delay	t_{PDLH}	V_{CC}=5V		48		ns
Diode Emulation Delay	$t_{DE\ delay}$			85		ns

Notes:

5) Guaranteed by design.

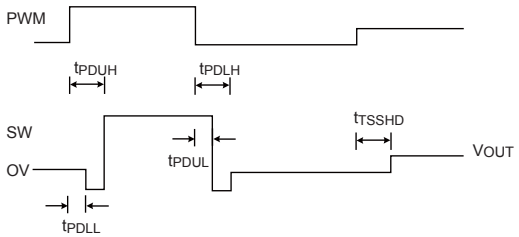


Figure 1—Timing Diagram

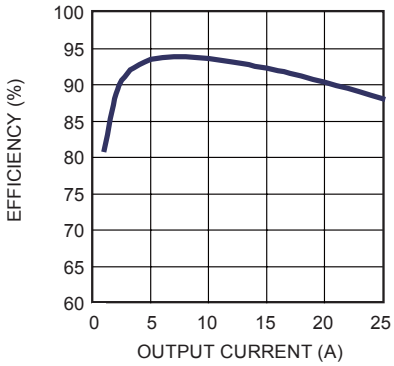
PIN FUNCTIONS

Pin #	Name	Description
1	NC	Not Connected.
2	VCC	BG Driver Bias Supply. Decouple with a 1µF ceramic capacitor.
3	AGND	Signal Ground.
4	EN	On/Off Control. A LOW places SW into high impedance state.
5	SYNC	An open enables Lower Synchronous Switch. Pull down low puts Low Switch into Diode Emulation mode.
6	PWM	Pulse Width Modulation Control. Accepts three state input. Force PWM to midstate or open to place SW into high impedance state.
7	PG	Power Good. Open drain output is low impedance to ground until internal supplies are good.
8	BST	Bootstrap. This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between SW and BST pins to form a floating supply across the power switch driver.
9 Exposed Pad	IN	Supply Voltage. C_{IN} is needed to prevent large voltage spikes from appearing at the input.
10–18 Exposed Pad	GND	Power Ground.
Exposed Pad	SW	Switch Output. These pins are fused together.

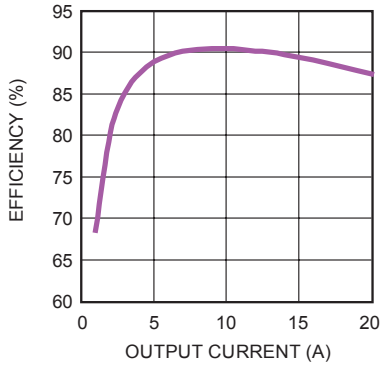
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{CC} = 5V, V_{OUT} = 1.2V, T_A = +25°C, unless otherwise noted.

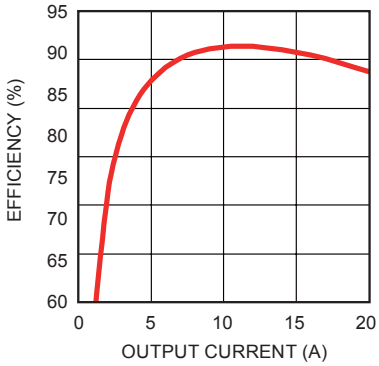
Efficiency vs. Output Current
300kHz, L=0.82uH



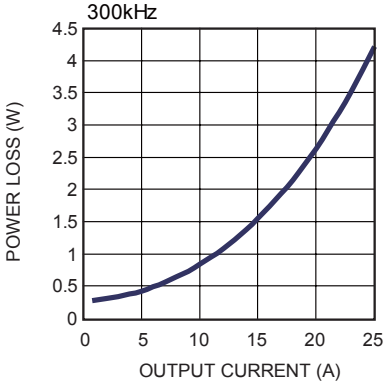
Efficiency vs. Output Current
600kHz, L=0.44uH



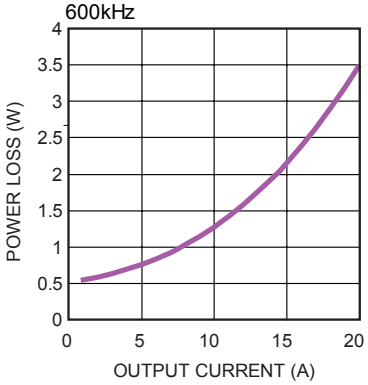
Efficiency vs. Output Current
1MHz, L=0.27uH



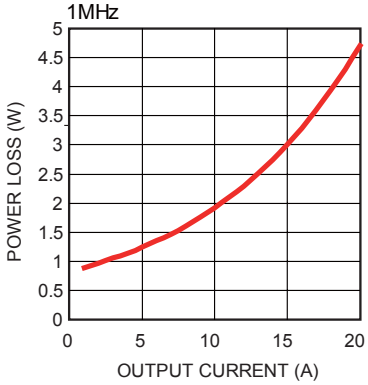
Power Loss vs. Output Current
300kHz



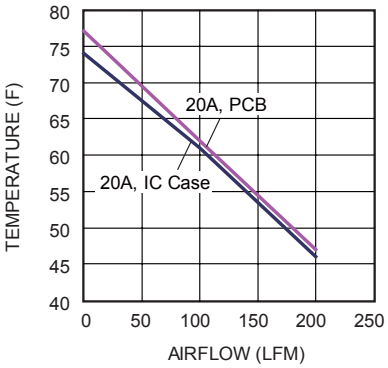
Power Loss vs. Output Current
600kHz



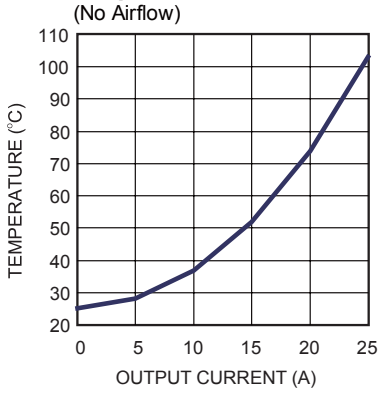
Power Loss vs. Output Current
1MHz



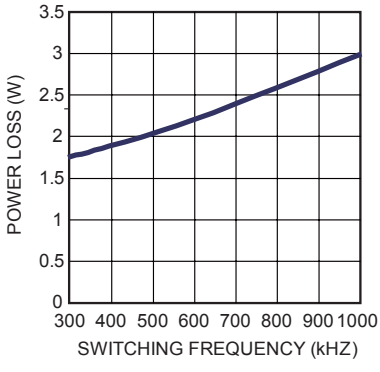
Temperature vs. Airflow



Temperature vs. Output Current
(No Airflow)



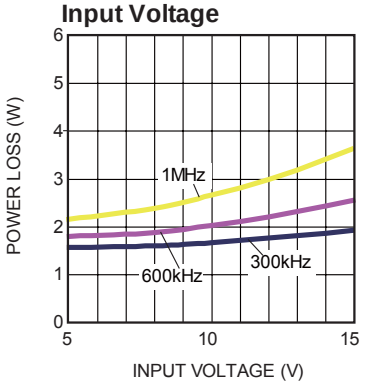
Power Loss vs. Switching Frequency



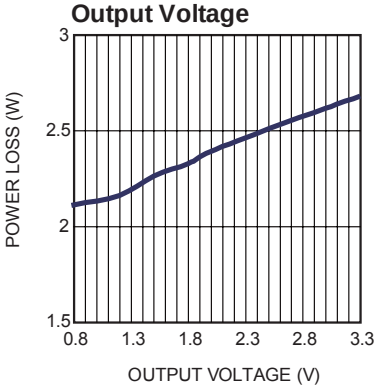
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{CC} = 5V, V_{OUT} = 1.2V, T_A = +25ºC, unless otherwise noted.

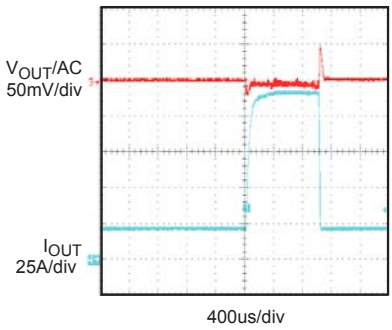
Power Loss vs . Input Voltage



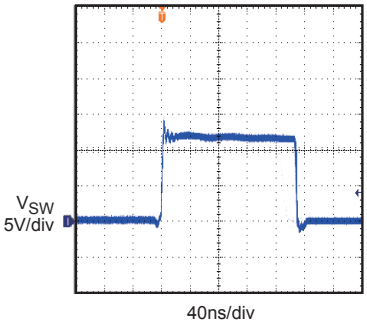
Power Loss vs . Output Voltage



SOA Waveform



Output Waveform



OPERATION

The MP86981 is a 20A Half Bridge driver ideally suited for Multi-Phase Buck regulators.

When the EN transitions from Low to High, the internal voltage regulators are enabled. Once both the V_{CC} and V_{BST} signals are sufficiently high and Thermal Shutdown is not tripped, the operation begins.

To allow M2, the lower DMOS, to enter Diode Emulation, the SYNC pin is driven Low.

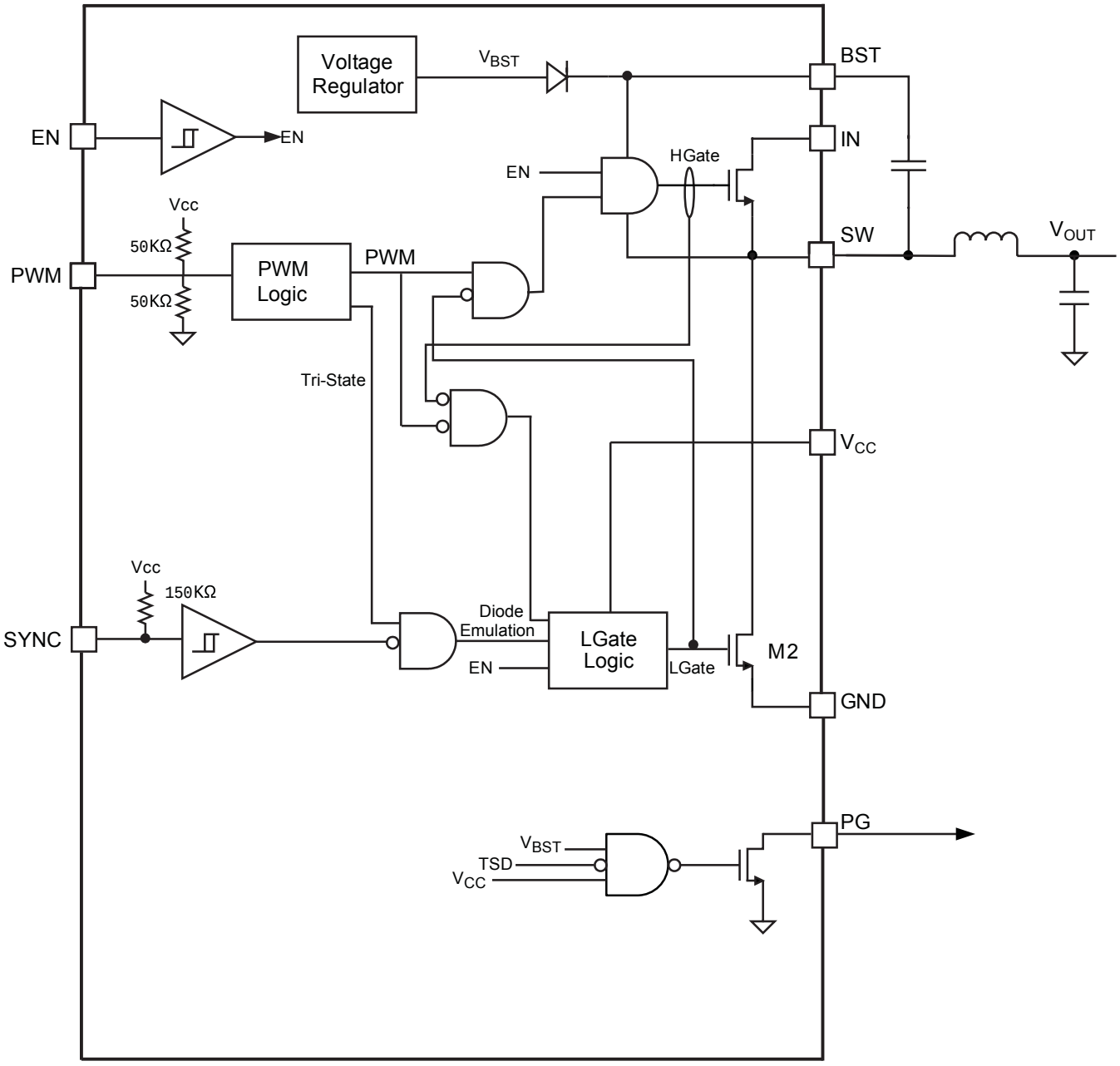
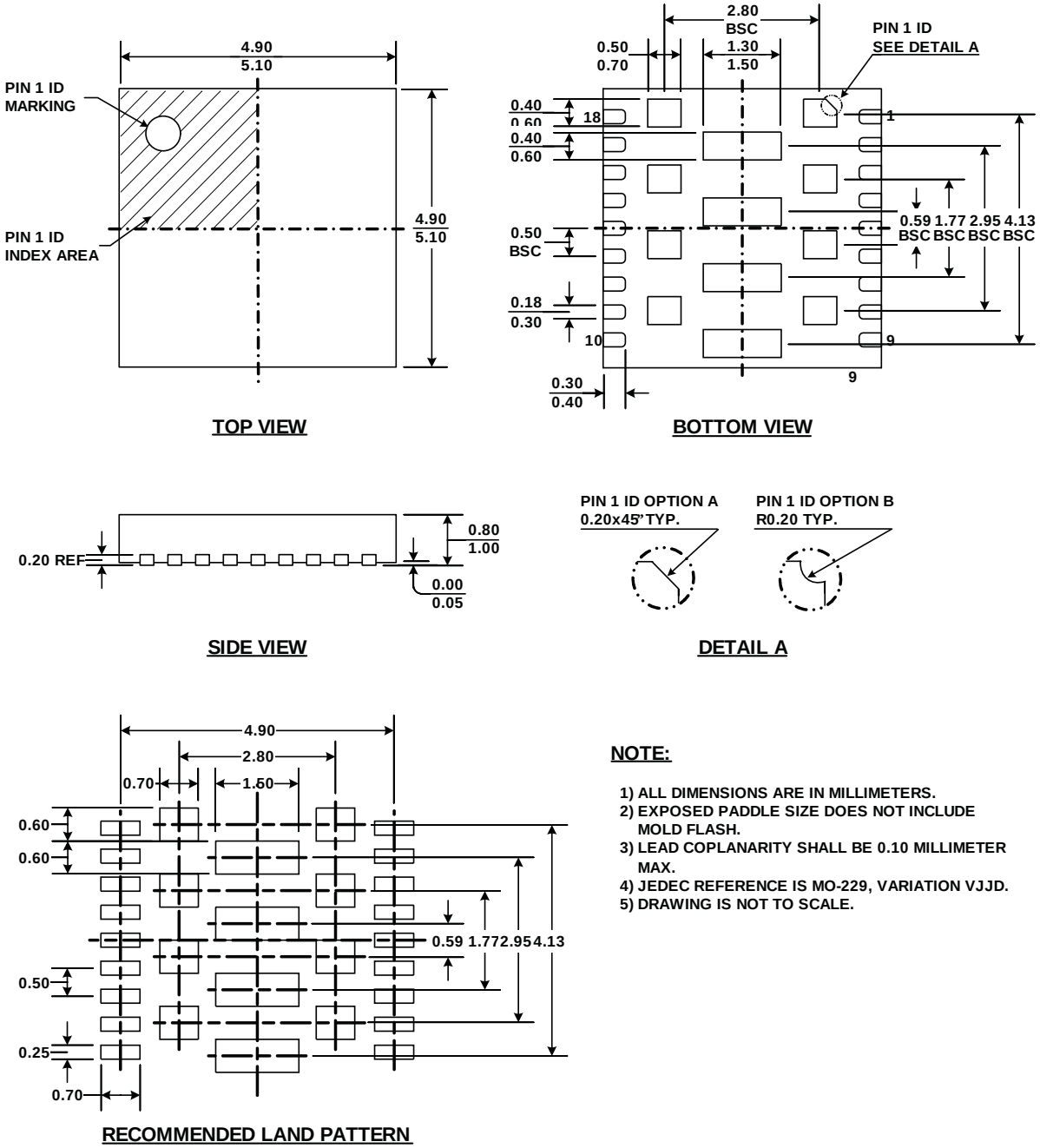


Figure 2—Functional Block Diagram

PACKAGE INFORMATION

FCTQFN18L (EXPOSED PAD)



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-229, VARIATION VJJD.
5) DRAWING IS NOT TO SCALE.