

ISD15D00
Digital ChipCorder
with
Digital Audio Interface

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1 GENERAL DESCRIPTION

The ISD15D00 is a digital ChipCorder[®] featuring digital compression, comprehensive memory management, and integrated analog/digital audio signal paths. The ISD15D00 utilizes serial flash memory to provide non-volatile audio playback for a two-chip solution. The ISD15D00 provides an I²S digital audio interface, faster digital programming, higher sampling frequency, and a signal path with SNR 80dB.

The ISD15D00 can take digital audio data via I²S or SPI interface. When I²S input is selected, it will replace the analog audio inputs and will support sample rates of 32, 44.1 or 48 kHz depending upon clock configuration. When SPI interface is chosen, the sample rate of the audio data sent must be one of the ISD15D00 supported sample rates.

The ISD15D00 has inbuilt analog audio inputs, analog audio line driver, and speaker driver output.

The analog audio input, Aux-in, has a fixed gain configured by SPI command. Aux-in can directly feed-through to the analog outputs; it can also mix with the DAC output and then feed-through to the analog outputs.

Analog outputs are available in two forms: (1) Aux-out is an analog single-ended voltage output; (2) Class-AB BTL (bridge-tied-load) is an analog differential voltage output. Class-AB BTL delivers 0.7-watt output power at $V_{CCSPK} = 4.5V$.

Class-D PWM direct-drive is also available, which delivers 0.9-watt output power at $V_{CCSPK} = 4.5V$.

2 FEATURES

- External Memory:
 - The ISD15D00 supports the following flash:

Manufacturer	Winbond		Numonyx			MXIC
Family	25X	25Q	25P	25PX	25PE	25L / 25V
JEDEC ID	EF 30 1X	EF 40 1X	20 20 1X	20 71 1X	20 80 1X	C2 20 1X

- The addressing ability of ISD15D00 is up to 128Mbit, which is 64-minute playback time based on 8kHz/4bit ADPCM.
- Inbuilt 3V voltage regulator to provide power source to the external flash memory
- Fast Digital Programming
 - Programming rate can go up to 1Mbits/second mainly limited by the flash memory write rate.
- Memory Management
 - Store pre-recorded audio (Voice Prompts) using high quality digital compression
 - Use a simple index-based command for playback
 - Execute pre-programmed macro scripts (Voice Macros) designed to control the configuration of the device and play back Voice Prompts sequences.
- Sample Rate
 - Seven sampling frequencies are available for a given master sample rate. For example, the sampling frequencies of 4, 5.3, 6.4, 8, 12.8, 16 and 32kHz are available when the device is clocked at a 32kHz master sample rate.
 - For I²S operation, 32, 44.1 and 48kHz master sample rates are available with playback sampling frequencies scaling accordingly.
- Compression Algorithms
 - For Pre-Recorded Voice Prompts
 - μ -Law: 6, 7 or 8 bits per sample

- Differential μ -Law: 6, 7 or 8 bits per sample
- PCM: 8, 10 or 12 bits per sample
- Enhanced ADPCM: 2, 3, 4 or 5 bits per sample
- Variable-bit-rate optimized compression. This allows best possible compression given a metric of SNR and background noise levels.
- Oscillator
 - Internal oscillator with internal reference: 2.048 MHz
 - Internal oscillator with external resistor: 2.048 MHz with $R_{osc} = 80k\Omega$
 - I²S bit clock input
- Inputs
 - Aux-in: Analog input with 2-bit gain control configured by SPI command
- Outputs
 - PWM: Class-D speaker driver to directly drive an 8 Ω speaker or buzzer
 - Deliver 0.9-watt output power at $V_{CCSPK} = 4.5V$
 - Aux-out: an analog single-ended voltage output
 - Class-AB BTL: an analog differential voltage output
 - Deliver 0.7-watt output power at $V_{CCSPK} = 4.5V$
 - Class-AB BTL can directly drive an 8 Ω speaker or buzzer
 - Class-AB BTL can drive an 8 Ω speaker or buzzer via an external amplifier
- I/Os
 - SPI interface: MISO, MOSI, SCLK, SS for commands and digital audio data
 - I²S interface: I²S_CLK, I²S_WS, I²S_SDI, I²S_SDO for digital audio data
 - 8 GPIO pins:
 - 4 GPIO pins share with I²S
 - 4 GPIO pins share with SPI Interface
 - GPIO pins can trigger Voice Macro for a pushbutton application
- 8-bit Volume Control set by SPI command for flexible mixing
- Operating Voltage: 2.7 ~ 5.5V
- Standby Current: 1 μ A typical
- Package:
 - Green QFN-32
- Temperature Options:
 - Industrial: -40°C to 85°C

3 BLOCK DIAGRAM

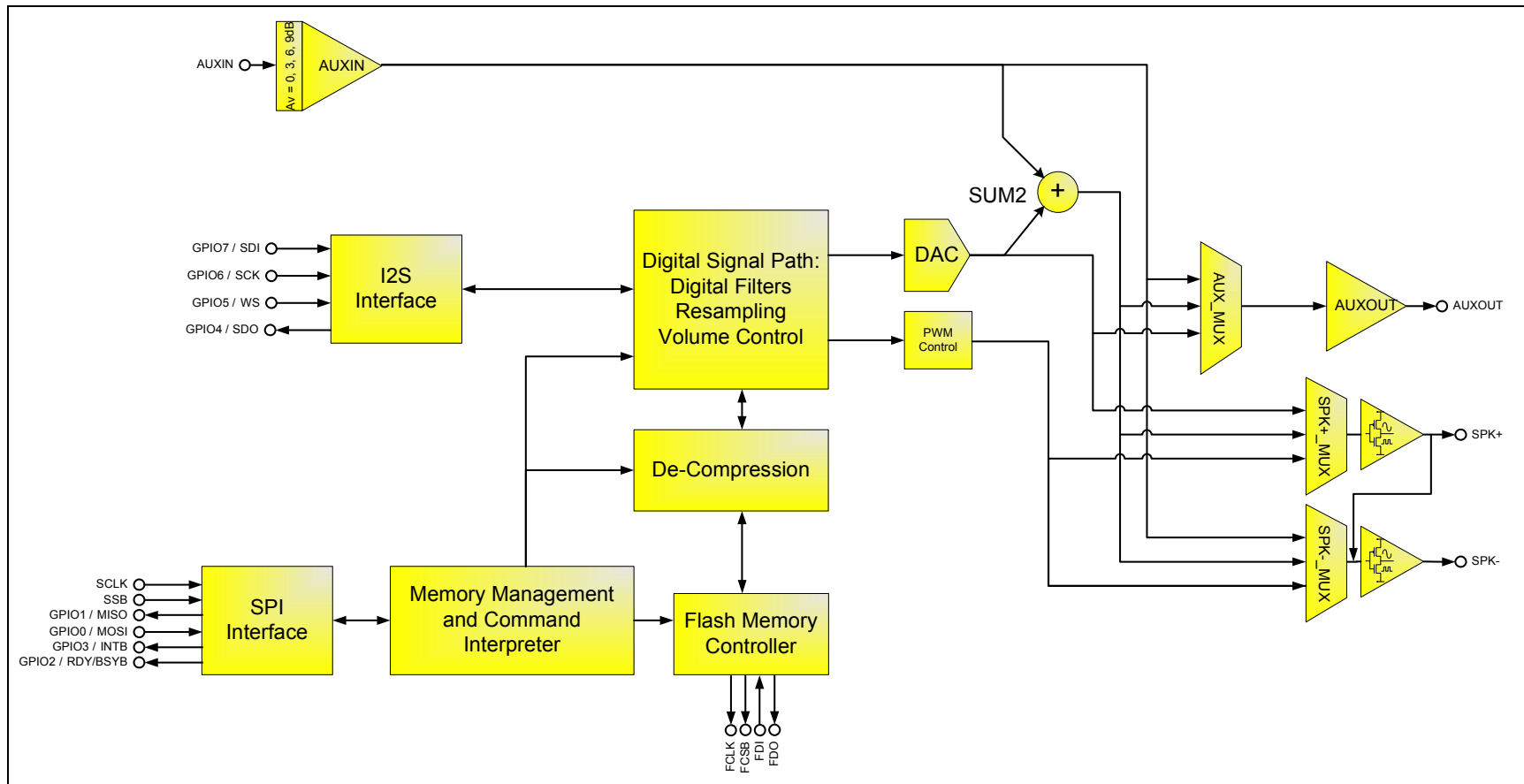


Figure 3-1 ISD15D00 Block Diagram

4 PINOUT CONFIGURATION

4.1 QFN-32

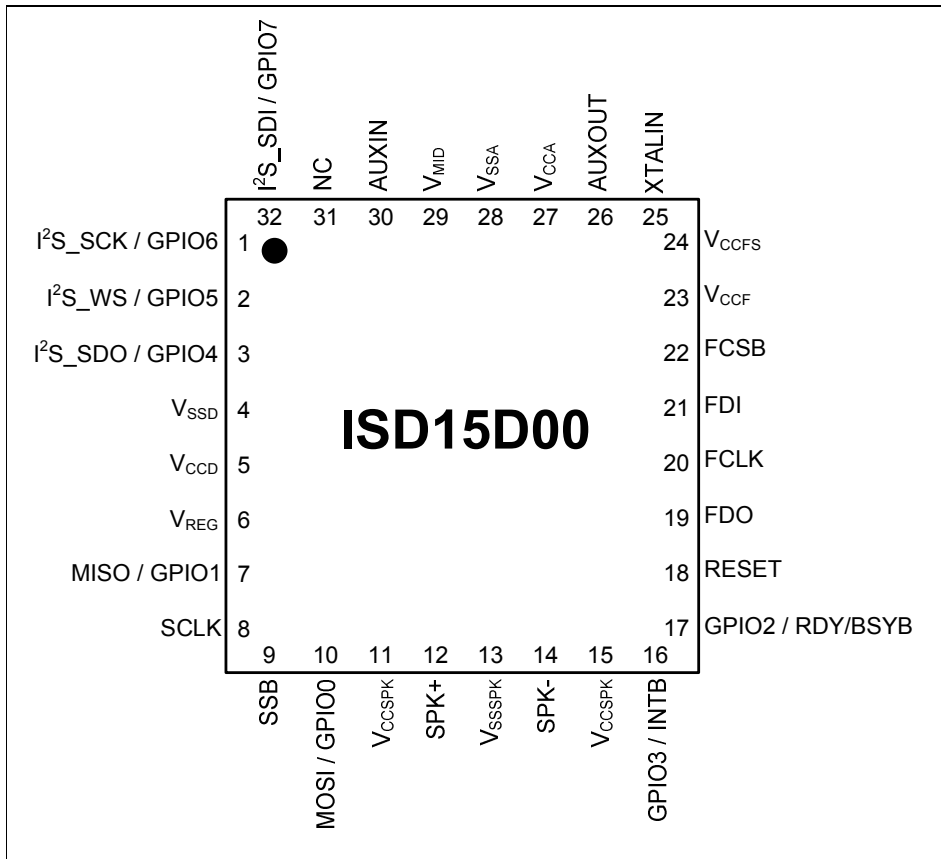


Figure 4-1 ISD15D00 QFN-32 Pin Configuration.

5 PIN DESCRIPTION

Pin Number QFN-32	Pin Name	I/O	Function
32	GPIO7 / I ² S_SDI	I/O	A GPIO pin. By default this pin is a pull-high input. Can be configured as Serial Data Input of the I ² S interface.
1	GPIO6 / I ² S_SCK	I/O	A GPIO pin. By default this pin is a pull-high input. Can be configured as Clock input in slave mode or clock output in master mode. This pin can be configured as an external clock buffer if I ² S is not used.
2	GPIO5 / I ² S_WS	I/O	A GPIO pin. By default this pin is a pull-high input. Can be configured as Word Select (WS) input in slave mode or WS output in master mode.
3	GPIO4 / I ² S_SDO	I/O	A GPIO pin. By default this pin is a pull-high input. Can be configured as Serial Data Output of the I ² S Interface.
4	V _{SSD}	I	Digital Ground.
5	V _{CCD}	I	Digital power supply.
6	V _{REG}	O	A 1.8V regulator to supply the internal logic. A minimum 1uF capacitor with low ESR<0.5OHM should be connected to this pin for supply decoupling and stability.
7	MISO / GPIO1	O	Master-In-Slave-Out. Serial output from the ISD15D00 to the host. This pin is in tri-state when SSB=1. Can be configured as GPIO1.
8	SCLK	I	Serial Clock input to the ISD15D00 from the host.
9	SSB	I	Slave Select input to the ISD15D00 from the host. When SSB is low device is selected and responds to commands on the SPI interface.
10	MOSI / GPIO0	I	Master-Out-Slave-In. Serial input to the ISD15D00 from the host. Can be configured as GPIO0.
11	V _{CCSPK}	I	In PWM mode: Digital Power for the PWM Driver. Deliver 0.9-watt output power at V _{CCSPK} = 4.5V. Or, In Class-AB mode: Analog Power for the Class-AB output. Class-AB BTL delivers 0.7-watt output power at V _{CCSPK} = 4.5V.

Pin Number QFN-32	Pin Name	I/O	Function
12	SPK+	O	PWM driver positive output. This SPK+ output, together with SPK- pin, provide a differential output to drive 8Ω speaker or buzzer. During power down this pin is in tri-state. Or, can be configured as Class-AB BTL which, together with SPK- pin, provides a differential voltage output. Or, can be configured as a Class-AB single-ended output.
13	V _{SSSPK}	I	In PWM mode: Digital Ground for the PWM Driver. Or, In Class-AB mode: Analog Ground for the Class-AB output.
14	SPK-	O	PWM driver negative output. This SPK- output, together with SPK+ pin, provides a differential output to drive 8Ω speaker or buzzer. During power down this pin is tri-state. Or, can be configured as Class-AB BTL which, together with SPK+ pin, provides a differential voltage output. Or, can be configured as a Class-AB single-ended output.
15	V _{CCSPK}	I	In PWM mode: Digital Power for the PWM Driver. Deliver 0.9-watt output power at V _{CCSPK} = 4.5V. Or, In Class-AB mode: Analog Power for the Class-AB output. Class-AB BTL delivers 0.7-watt output power at V _{CCSPK} = 4.5V.
16	INTB / GPIO3	O	Active low interrupt request pin. This pin is an open-drain output. Can be configured as GPIO3.
17	RDY/BSYB / GPIO2	O	An output pin to report the status of data transfer on the SPI interface. "High" indicates that ISD15D00 is ready to accept new SPI commands or data. Can be configured as GPIO2.
18	RESET	I	Applying power to this pin will reset the chip. (A high pulse of 50ms or more will reset the chip.)
19	FDO	O	Serial data output of the external serial flash interface. Connects to data input (DI) of external serial flash.
20	FCLK	O	Serial data CLK of the external serial flash interface.
21	FDI	I	Serial data input to external serial flash interface. Connects to data output (DO) of external flash memory.
22	FCSB	O	Chip Select Bar of the external serial flash interface.
23	V _{CCF}	O	Digital power supply for the external flash memory. A minimum 1uF capacitor with low ESR<0.5OHM should be connected to this pin for supply decoupling and stability. Refer to the application diagram.

Pin Number QFN-32	Pin Name	I/O	Function
24	V _{CCFS}	I	Digital power supply for the inbuilt voltage regulator for the external flash memory. A 0.1uF capacitor should be connected to this pin for supply decoupling and stability. Refer to the application diagram.
25	XTALIN	I	The CLK_CFG register determines one of the following configuration: A resistor connected to GND as a reference current to the internal oscillator.
26	Aux-out	O	Aux Out. This pin is an analog voltage output. If AUXOUT is not used, this pin should be left unconnected.
27	V _{CCA}	I	Analog power supply pin.
28	V _{SSA}	I	Analog ground pin.
29	V _{MID}	O	Middle voltage reference for the swing of analog/digital audio outputs. A 4.7uF capacitor should be connected to this pin for supply decoupling and stability.
30	Aux-in	I	Auxiliary input with the gain set by SPI command If Aux-in is not used, this pin should be left unconnected.
31	NC		This pin should be left unconnected.

6 ELECTRICAL CHARACTERISTICS

6.1 OPERATING CONDITIONS

OPERATING CONDITIONS (INDUSTRIAL PACKAGED PARTS)

CONDITIONS	VALUES
Operating temperature range (Case temperature)	-40°C to +85°C
Digital Supply voltage (V_{CCD}) ^[1]	+2.7V to +5.5V
Digital Ground voltage (V_{SSD}) ^[2]	0V
Analog Supply voltage (V_{CCA}) ^[3]	+2.7V to +5.5V
Analog Ground voltage (V_{SSA}) ^[2]	0V
Speaker Supply voltage (V_{CCSPK}) ^[3]	+2.7V to +5.5V
Speaker Ground voltage (V_{SSSPK}) ^[2]	0V
Flash Source Supply voltage (V_{CCFS}) ^[4] – to regulate V_{CCF}	+2.7V to +5.5V
Flash Source Supply voltage (V_{CCFS}) ^[4] – tied to V_{CCF}	+2.25V to +3.6V
Flash Supply voltage - (V_{CCF}) ^[4] – regulated from V_{CCFS}	+2.4V to +3.0V
Flash Supply voltage - (V_{CCF}) ^[4] – tied to V_{CCFS}	+2.25V to +3.6V

NOTES:

^[1] V_{CCD} 2.7 ~ 5.5V; No restrictions with respect to V_{CCA} and V_{CCSPK} .

^[2] $V_{SSD} = V_{SSA} = V_{SSSPK}$

^[3] In Class-AB mode: V_{CCSPK} must equal V_{CCA} . Otherwise: $V_{CCSPK} \geq V_{CCA}$.

^[4] If V_{CCFS} is guaranteed to be below 3.6V (or upper flash supply limit), then V_{CCF} should be tied to V_{CCFS} .

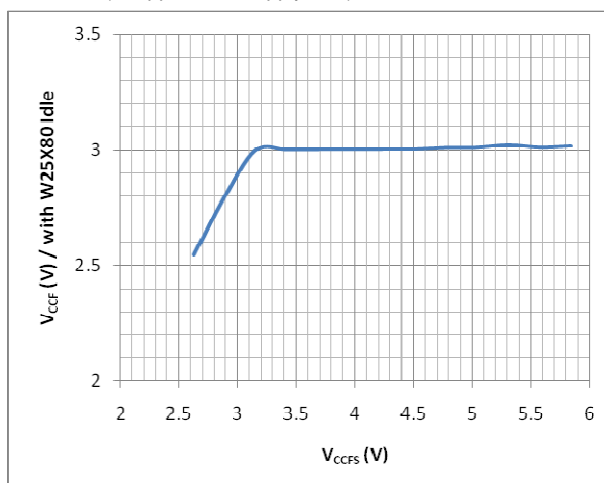


Figure 6-1 V_{CCF} vs. V_{CCFS} – V_{CCF} is regulated internally from V_{CCFS} ^[4]

6.2 DC PARAMETERS

PARAMETER	SYMBOL	MIN	TYP [1]	MAX	UNIT S	CONDITIONS
Digital Supply Voltage	V_{CCD}	2.7		5.5	V	
Analog Supply Voltage	V_{CCA}	2.7		5.5	V	
Speaker Supply Voltage	V_{CCSPK}	2.7		5.5	V	
Flash Source Supply Voltage	V_{CCFS}	2.7		5.5	V	to regulate V_{CCF}
		2.25		3.6		tied to V_{CCF}
Flash Supply Voltage (refer to Figure 6-1)	V_{CCF}		V_{CCFS} -0.3		V	regulated from V_{CCFS} $V_{CCFS} = 2.7 \sim 3.3V$
			3.0			regulated from V_{CCFS} $V_{CCFS} = 3.3 \sim 5.5V$
		2.25		3.6		tied to V_{CCFS}
Input Low Voltage	V_{IL}	$V_{SSD}-0.3$		$0.3 \times V_{CCD}$	V	
Input High Voltage	V_{IH}	$0.7 \times V_{CCD}$		V_{CCD}	V	
Output Low Voltage	V_{OL}	$V_{SSD}-0.3$		$0.3 \times V_{CCD}$	V	$I_{OL} = 1mA$
Output High Voltage	V_{OH}	$0.7 \times V_{CCD}$		V_{CCD}	V	$I_{OH} = -1mA$
INTB Output Low Voltage	V_{OH1}			0.4	V	
Playback Current	$I_{DD_Playback}$			30	mA	
Standby Current	I_{SB}		1	10	μA	
Input Leakage Current	I_{IL}		± 1		μA	Force V_{CCD}

Notes: [1] Conditions $V_{CCD}=V_{CCA}=V_{CCSPK}=V_{CCFS}=3V$, $T_A=25^\circ C$ unless otherwise stated

6.3 AC PARAMETERS

6.3.1 Inputs

AUX-IN:

Conditions: $V_{CCD} = 3.3V$, $V_{CCA} = V_{CCSPK} = 5V$, $MCLK = 16.384MHz$, $T_A = +25^{\circ}C$, 1kHz signal

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Auxiliary Analog Inputs (AUXIN)						
Full scale input signal ¹		Gain = 0dB		1.0 0		Vrms dBV
AUX Programmable gain			0		9	dB
AUX programmable gain step size		Guaranteed Monotonic		3		dB
Input resistance		Aux direct-to-out path, only		21		k Ω
		Input gain = +9.0dB		27		k Ω
		Input gain = +6.0dB		33		k Ω
		Input gain = +3.0dB		40		k Ω
		Input gain = 0dB				
Aux-in Gain Accuracy	$A_{AUX(GA)}$		-0.5dB		+0.5dB	dB

Conditions: $V_{CCD} = 3.3V$, $V_{CCA} = V_{CCSPK} = 3.3V$, $MCLK = 16.384MHz$, $T_A = +25^{\circ}C$, 1kHz signal

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Auxiliary Analog Inputs (AUXIN)						
Full scale input signal ¹		Gain = 0dB		1.0 0		Vrms dBV
AUX Programmable gain			0		9	dB
AUX programmable gain step size		Guaranteed Monotonic		3		dB
Input resistance	R_{aux_in}	Aux direct-to-out path, only		21		k Ω
		Input gain = +9.0dB		27		k Ω
		Input gain = +6.0dB		33		k Ω
		Input gain = +3.0dB		40		k Ω
		Input gain = 0dB				
Aux-in Gain Accuracy	$A_{AUX(GA)}$		-0.5dB		+0.5dB	dB

6.3.2 Outputs

Aux-out

Conditions: $V_{CCD} = 3.3V$, $V_{CCA} = V_{CCSPK} = 5V$, $MCLK = 16.384MHz$, $T_A = +25^{\circ}C$, 1kHz signal

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Digital to Analog Converter (DAC) driving AUXOUT with 5kΩ / 100pF load						
Full-scale output		Gain paths all at 0dB gain		$V_{CCA} / 3.3$		V_{rms}
Signal-to-noise ratio	SNR	A-weighted		85		dB
Total harmonic distortion ²	THD+N	$R_L = 5k\Omega$; full-scale signal A-weighted		-80		dB

Conditions: $V_{CCD} = 3.3V$, $V_{CCA} = V_{CCSPK} = 3.3V$, $MCLK = 16.384MHz$, $T_A = +25^{\circ}C$, 1kHz signal

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Digital to Analog Converter (DAC) driving AUXOUT with 5kΩ / 100pF load						
Full-scale output		Gain paths all at 0dB gain		$V_{CCA} / 3.3$		V_{rms}
Signal-to-noise ratio	SNR	A-weighted		80		dB
Total harmonic distortion ²	THD+N	$R_L = 5k\Omega$; full-scale signal A-weighted		-77		dB

PWM OUTPUT

Conditions: $V_{CCD} = 3.3V$, $V_{CCA} = V_{CCSPK} = 5V$, MCLK = 16.384MHz, $T_A = +25^{\circ}C$, 1kHz signal

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Speaker PWM Output (SPK_PLUS / SPK_MINUS with 8Ω bridge-tied-load)						
Signal-to-noise ratio ³	SNR	A-weighted + Class D Filter		65		dB
Total harmonic distortion ²	THD	A-weighted + Class D Filter		-40		dB
Efficiency	E_{PWM}	8Ω bridge-tied-load Pout > 0.2W		85		%

Conditions: $V_{CCD} = 3.3V$, $V_{CCA} = V_{CCSPK} = 3.3V$, MCLK = 16.384MHz, $T_A = +25^{\circ}C$, 1kHz signal

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Speaker PWM Output (SPK_PLUS / SPK_MINUS with 8Ω bridge-tied-load)						
Signal-to-noise ratio ³	SNR	A-weighted + Class D Filter		65		dB
Total harmonic distortion ²	THD	A-weighted + Class D Filter		-40		dB
Efficiency	E_{PWM}	8Ω bridge-tied-load Pout > 0.2W		80		%

CLASS-AB BTL OUTPUT

Conditions: $V_{CCD} = 3.3V$, $V_{CCA} = V_{CCSPK} = 5V$, $MCLK = 16.384MHz$, $T_A = +25^{\circ}C$, 1kHz signal

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Speaker CLASS-AB BTL Output (SPK_PLUS / SPK_MINUS with 8Ω bridge-tied-load)						
Full scale output		Gain paths all at 0dB gain	$V_{CCA} / 3.3$			V_{rms}
Signal-to-noise ratio	SNR	A-weighted		90		dB
Total harmonic distortion ²	THD	A-weighted		-60		dB
Efficiency	E_{AB}	8Ω bridge-tied-load Pout > 0.7W		50		%

Conditions: $V_{CCD} = 3.3V$, $V_{CCA} = V_{CCSPK} = 3.3V$, $MCLK = 16.384MHz$, $T_A = +25^{\circ}C$, 1kHz signal

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Speaker CLASS-AB BTL Output (SPK_PLUS / SPK_MINUS with 8Ω bridge-tied-load)						
Full scale output		Gain paths all at 0dB gain	$V_{CCA} / 3.3$			V_{rms}
Signal-to-noise ratio	SNR	A-weighted		84		dB
Total harmonic distortion ²	THD	A-weighted		-60		dB
Efficiency	E_{AB}	8Ω bridge-tied-load Pout > 0.4W		50		%

Notes

1. Full Scale is relative to the magnitude of V_{CCA} and can be calculated as $FS = V_{CCA}/3.3$.
2. Distortion is measured in the standard way as the combined quantity of distortion products plus noise. The signal level for distortion measurements is at 3dB below full scale, unless otherwise noted.
3. SNR measured with a -100dbFS signal at input.

6.3.3 SPI Timing

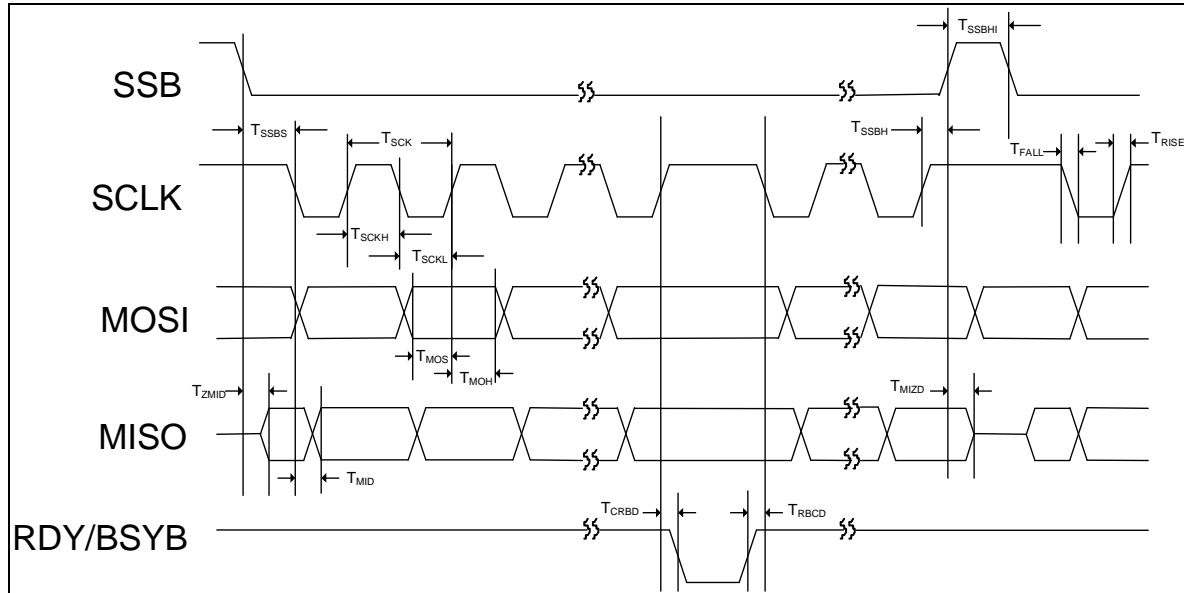


Figure 6-2 SPI Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{SCK}	SCLK Cycle Time	60	---	---	ns
T_{SCKH}	SCLK High Pulse Width	25	---	---	ns
T_{SCKL}	SCLK Low Pulse Width	25	---	---	ns
T_{RISE}	Rise Time	---	---	10	ns
T_{FALL}	Fall Time	---	---	10	ns
T_{SSBS}	SSB Falling Edge to 1 st SCLK Falling Edge Setup Time	30	---	---	ns
T_{SSBH}	Last SCLK Rising Edge to SSB Rising Edge Hold Time	30ns	---	50us	---
T_{SSBHI}	SSB High Time between SSB Lows	20	---	---	ns
T_{MOS}	MOSI to SCLK Rising Edge Setup Time	15	---	---	ns
T_{MOH}	SCLK Rising Edge to MOSI Hold Time	15	---	---	ns
T_{ZMID}	Delay Time from SSB Falling Edge to MISO Active	--	--	12	ns
T_{MIZD}	Delay Time from SSB Rising Edge to MISO Tri-state	--	--	12	ns

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{MID}	Delay Time from SCLK Falling Edge to MISO	---	---	12	ns
T_{CRBD}	Delay Time from SCLK Rising Edge to RDY/BSYB Falling Edge	--	--	12	ns
T_{RBCD}	Delay Time from RDY/BSYB Rising Edge to SCLK Falling Edge	0	--	--	ns

6.3.4 I²S Timing

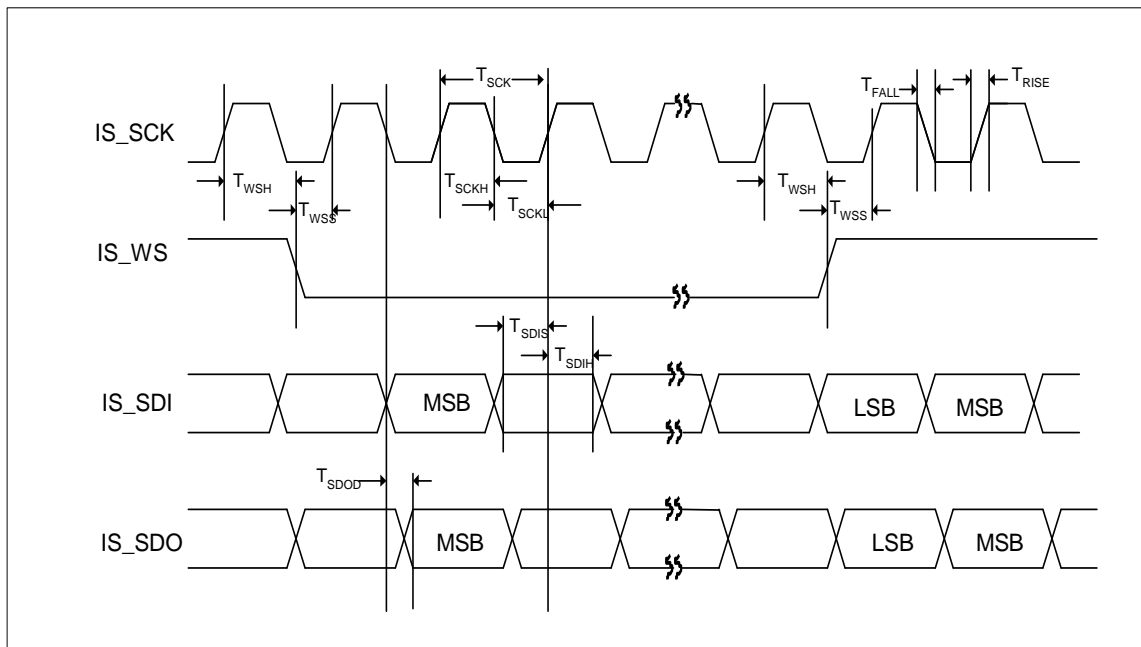


Figure 6-3 I²S Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{SCK}	IS_SCK Cycle Time	60	---	---	ns
T_{SCKH}	IS_SCK High Pulse Width	25	---	---	ns
T_{SCKL}	IS_SCK Low Pulse Width	25	---	---	ns
T_{RISE}	Rise Time	---	---	10	ns
T_{FALL}	Fall Time	---	---	10	ns

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T _{WSS}	WS to IS_SCK Rising Edge Setup Time	20	---	---	ns
T _{WSH}	IS_SCK Rising Edge to IS_WS Hold Time	20	---	---	ns
T _{SDIS}	IS_SDI to IS_SCK Rising Edge Setup Time	15	---	---	ns
T _{SDIH}	IS_SCK Rising Edge to IS_SDI Hold Time	15	---	---	ns
T _{SDOD}	Delay Time from IS_SCLK Falling Edge to IS_SDO	---	---	12	ns

7 APPLICATION DIAGRAM

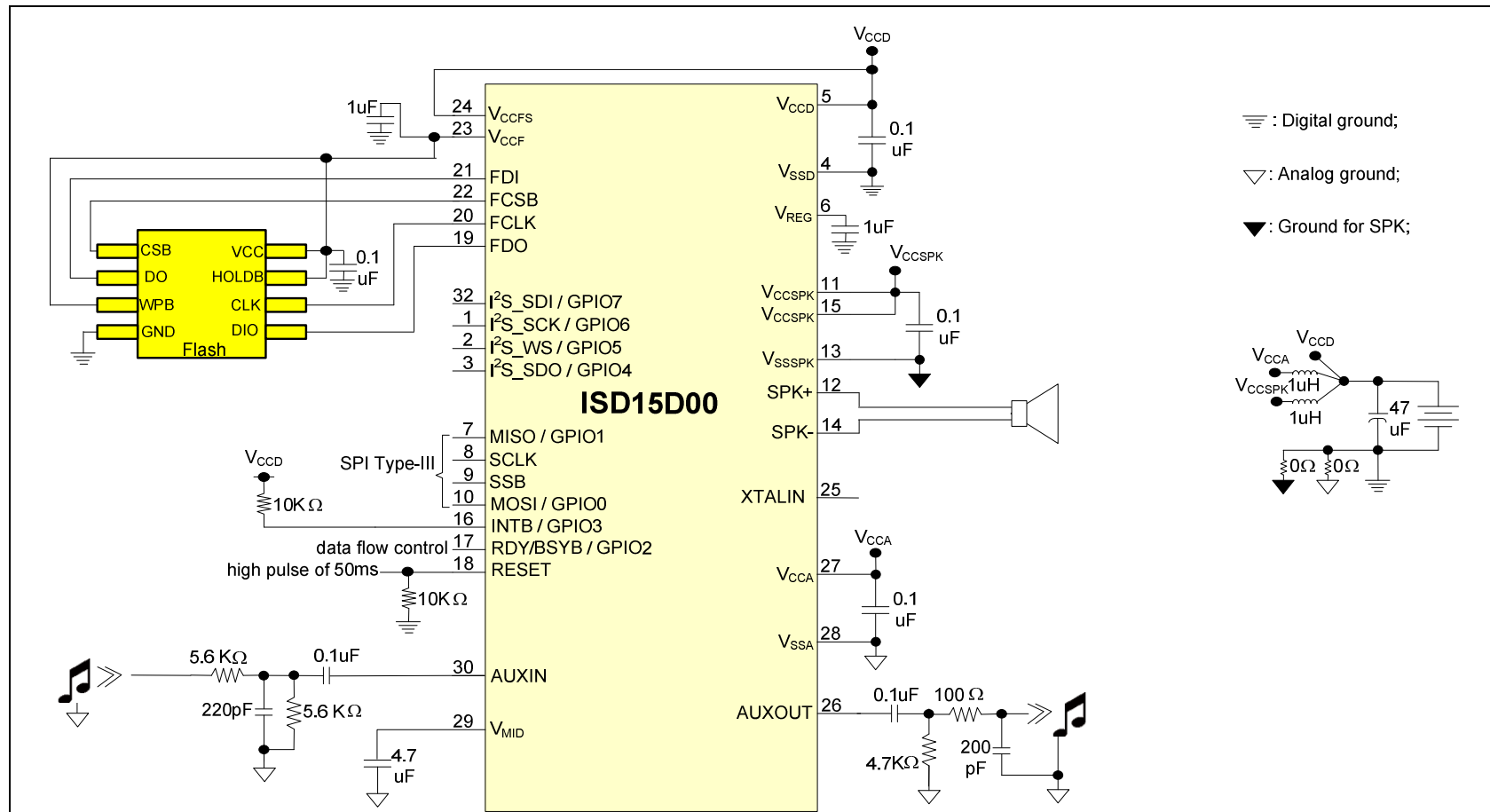


Figure 7-1 ISD15D00 Application Diagram – V_{CCF} is regulated internally from V_{CCFS}

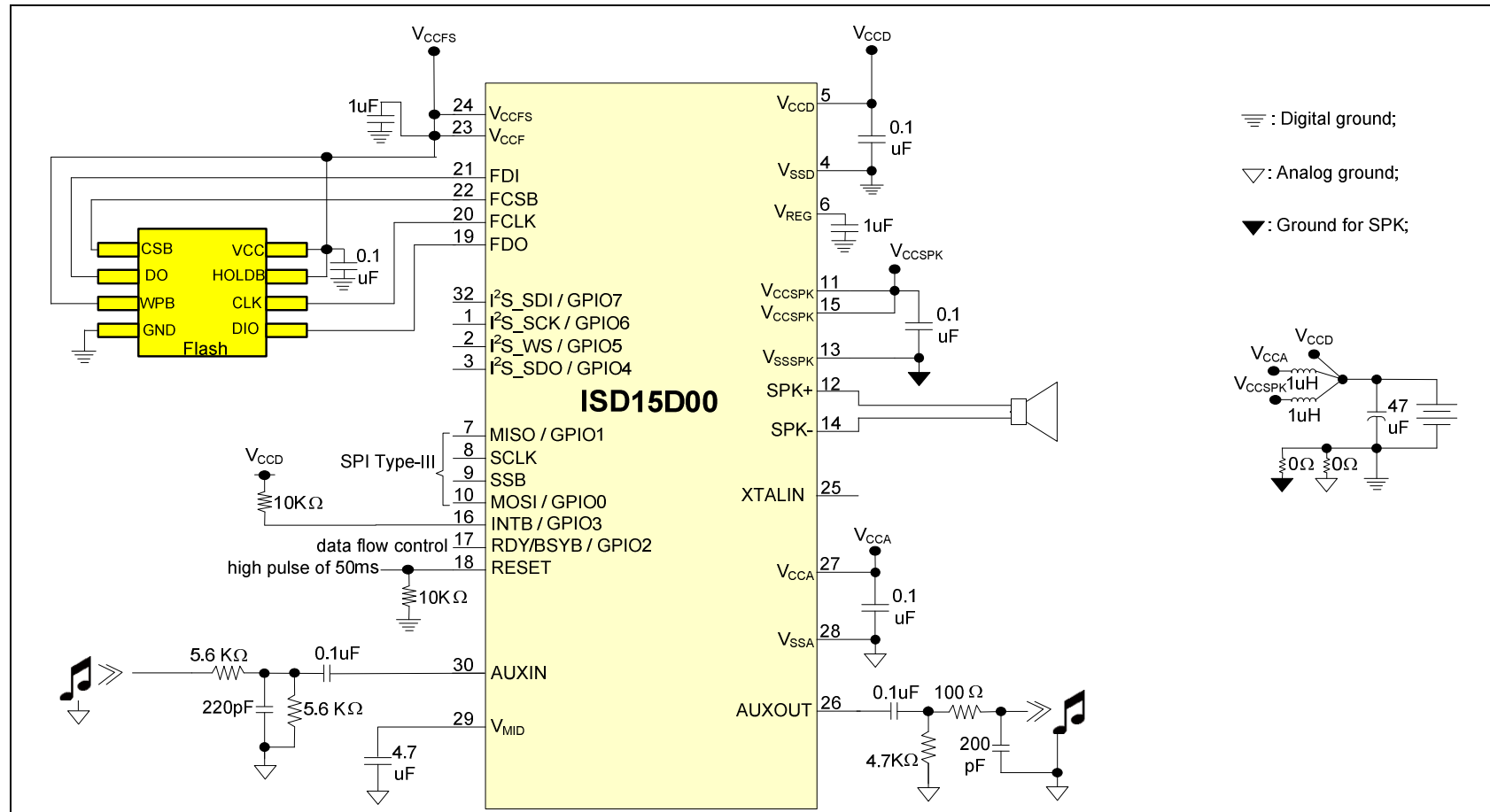
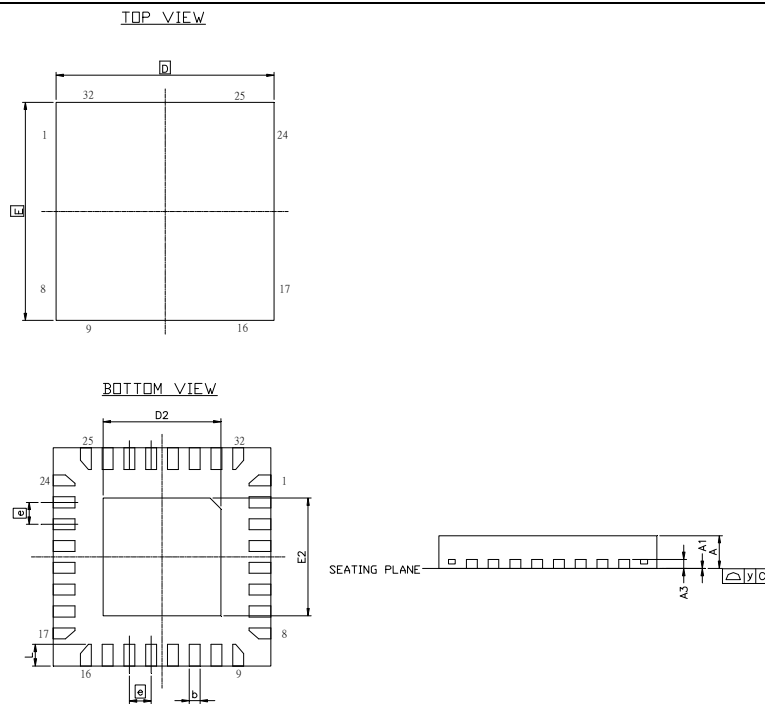


Figure 7-2 ISD15D00 Application Diagram – V_{CCF} is tied to V_{CCFS}

The above application examples are for references only. It makes no representation or warranty that such applications shall be suitable for the use specified. Each design has to be optimized in its own system for the best performance on voice quality, current consumption, functionalities and etc.

8 PACKAGE SPECIFICATION

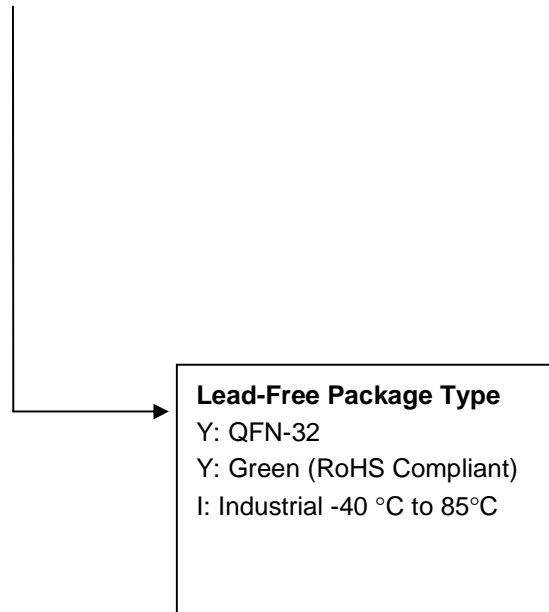
8.1 QFN-32 (5X5 MM², THICKNESS 0.8MM ,PITCH 0.5 MM)



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	0.02	0.05	0	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC			0.197 BSC		
D2	2.60	2.70	2.80	0.1024	0.1063	0.1102
E	5.00 BSC			0.197 BSC		
E2	2.60	2.70	2.80	0.1024	0.1063	0.1102
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
y	0.10			0.0039		

9 ORDERING INFORMATION

I15D00 YYI



10 REVISION HISTORY

Version	Date	Description
0.23	Aug 3, 2009	Initially released as the Preliminary Datasheet.
0.26	Aug 17, 2009	Update application diagram.
0.27	Sep 28, 2009	Update the list of supported Flash Memory.
0.29	Nov 18, 2009	Update: <ul style="list-style-type: none">• Block Diagram.• Electrical Characteristics.
0.34	Dec 7, 2009	Add QFN-32 Package.
0.35	Feb 8, 2010	Update block diagram.
0.40	July 1, 2010	Update crystal configuration.
0.50	Aug 12, 2010	Update PWM spec.
0.60	Mar 31, 2011	Class-AB output delivers 0.7-watt at 4.5V.
0.63	Apr 13, 2011	Update package information.
0.64	June 16, 2011	Update description of Rise and Fall time.

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