ARM Cortex™-M0

32-BIT MICROCONTROLLER

NuMicro™ Family
Mini51 Series Product Brief

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1 GENERAL DESCRIPTION

The NuMicro Mini51™ series 32-bit microcontroller is embedded with an ARM® Cortex™-M0 core for industrial controls and applications which require high performance, high integration, and low cost. The Cortex™-M0 is the newest ARM embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller.

The NuMicro Mini51™ series can run up to 24 MHz, and thus can afford to support a variety of industrial controls and applications requiring high CPU performance. The NuMicro Mini51™ series provides 4K/8K/16K-byte embedded program flash, size configurable data flash (shared with program flash), 2K-byte flash for the ISP, and 2K-byte embedded SRAM.

A number of system-level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, PWM, ADC, Watchdog Timer, and low voltage detector, have been incorporated in the NuMicro Mini51™ series to reduce component count, board space, and system cost. These useful functions make the NuMicro Mini51™ series powerful for a wide range of applications.

Additionally, the NuMicro Mini51™ series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, allowing user to update program memory without removing a chip from an actual end product.

2 FEATURES

- Core
  - ARM® Cortex™-M0 core running up to 24 MHz
  - One 24-bit system timer
  - Supports low power Idle mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for 32 interrupt inputs, each with 4-level priority
  - Supports Serial Wire Debug (SWD) with 2 watchpoints/4 breakpoints
- Built-in LDO for Wide Operating Voltage Range: 2.5V to 5.5V
- Memory
  - 4KB/8KB/16KB flash memory for program memory (APROM)
  - Configurable flash memory for data memory (Data Flash)
  - 2KB flash memory for loader (LDROM)
  - 2KB SRAM for internal scratch-pad RAM (SRAM)
- In-System Programming (ISP) and In-Circuit Programming (ICP)
- Clock Control
  - Programmable system clock source
    - Switch clock sources on-the-fly
  - 4 ~ 24 MHz crystal oscillator (HXT)
  - 32.768K crystal oscillator (LXT) for idle wake-up and system operation clock
  - 22.1184 MHz internal oscillator (HIRC) (1% accuracy at 25^0C, 5V)
    - Dynamically calibrating the HIRC OSC to 22.0 MHz ±1% from -40^0C to 85^0C by external 32.768K crystal oscillator (LXT)
  - 10 KHz internal low-power oscillator (LIRC) for watchdog and idle wake-up
- I/O Port
  - Up to 30 GPIO (General Purpose I/O) pins for LQFP-48 package
  - Software-configured I/O type
    - Quasi-bidirectional input/output
    - Push-pull output
    - Open-drain output
    - Input-only (high impendence)
  - Optional Schmitt trigger input
- Timer
  - Two 24-bit Timers with 8-bit prescaler
    - Supports Event Counter mode
    - Supports Toggle Output mode

- Supports external trigger in Pulse Width Measurement mode
  - Supports external trigger in Pulse Width Capture mode

- Watchdog Timer
  - Programmable clock source and time-out period
  - Supports wake-up function in Power-down mode and Idle mode
  - Interrupt or reset selectable when time-out happens
- PWM
  - Up to three built-in 16-bit PWM generators with six PWM outputs or three complementary paired PWM outputs
  - Supports edge alignment or center alignment
  - Supports fault detection
  - Individual clock source, clock divider, 8-bit prescalar and dead-zone generator for each PWM generator
  - PWM interrupt synchronized to PWM period
- UART (Universal Asynchronous Receiver/Transmitters)
  - One UART device
  - Buffered receiver and transmitter with 16-byte FIFO
  - Optional flow control function (CTSn and RTSn)
  - Supports IrDA (SIR) function
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports RS-485 function
- SPI (Serial Peripheral Interface)
  - One SPI device
  - Masters up to 12 MHz, and Slaves up to 4 MHz
  - Supports SPI Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - Byte Suspend mode in 32-bit transmission
- I^2C
  - Supports Master/Slave mode
  - Bi-directional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus

- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Programmable clocks allowing for versatile rate control
- Supports multiple address recognition (4 slave addresses with mask option)

- ADC (Analog-to-Digital Converter)
  - 10-bit SAR ADC with 150K SPS
  - Up to 8-ch single-end input and one internal input from band-gap
  - Conversion started by software or external pin
- Analog Comparator
  - Two analog comparators with programmable 16-level internal voltage reference
  - Built-in CRV (comparator reference voltage)
- BOD (Brown-Out Detection) Reset
  - Three programmable threshold levels: 3.8V/2.7V/2.0V (default as 2.0V)
  - Optional BOD interrupt or reset
- 96-bit unique ID
- Operating Temperature: -40℃~85℃
- Packages:
  - Green package (RoHS)
  - LQFP 48-pin (7x7), QFN 33-pin (5x5), QFN 33-pin (4x4)

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro Mini51™ Series Product Selection Guide

Part Number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity			Comp.	PWM	ADC	ISP ICP	IRC 22.1184 MHz	Package
							UART	SPI	I^2C						
MINI51LAN	4 KB	2 KB	Configurable	2 KB	up to 30	2x32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI51ZAN	4 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(5x5)
MINI51TAN	4 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(4x4)
MINI52LAN	8 KB	2 KB	Configurable	2 KB	up to 30	2x32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI52ZAN	8 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(5x5)
MINI52TAN	8 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(4x4)
MINI54LAN	16 KB	2 KB	Configurable	2 KB	up to 30	2x32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI54ZAN	16 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(5x5)
MINI54TAN	16 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(4x4)

Figure 3.1-1 NuMicro Mini51™ Series Product Selection Guide

3.2 PIN CONFIGURATION

3.2.1 LQFP 48-pin

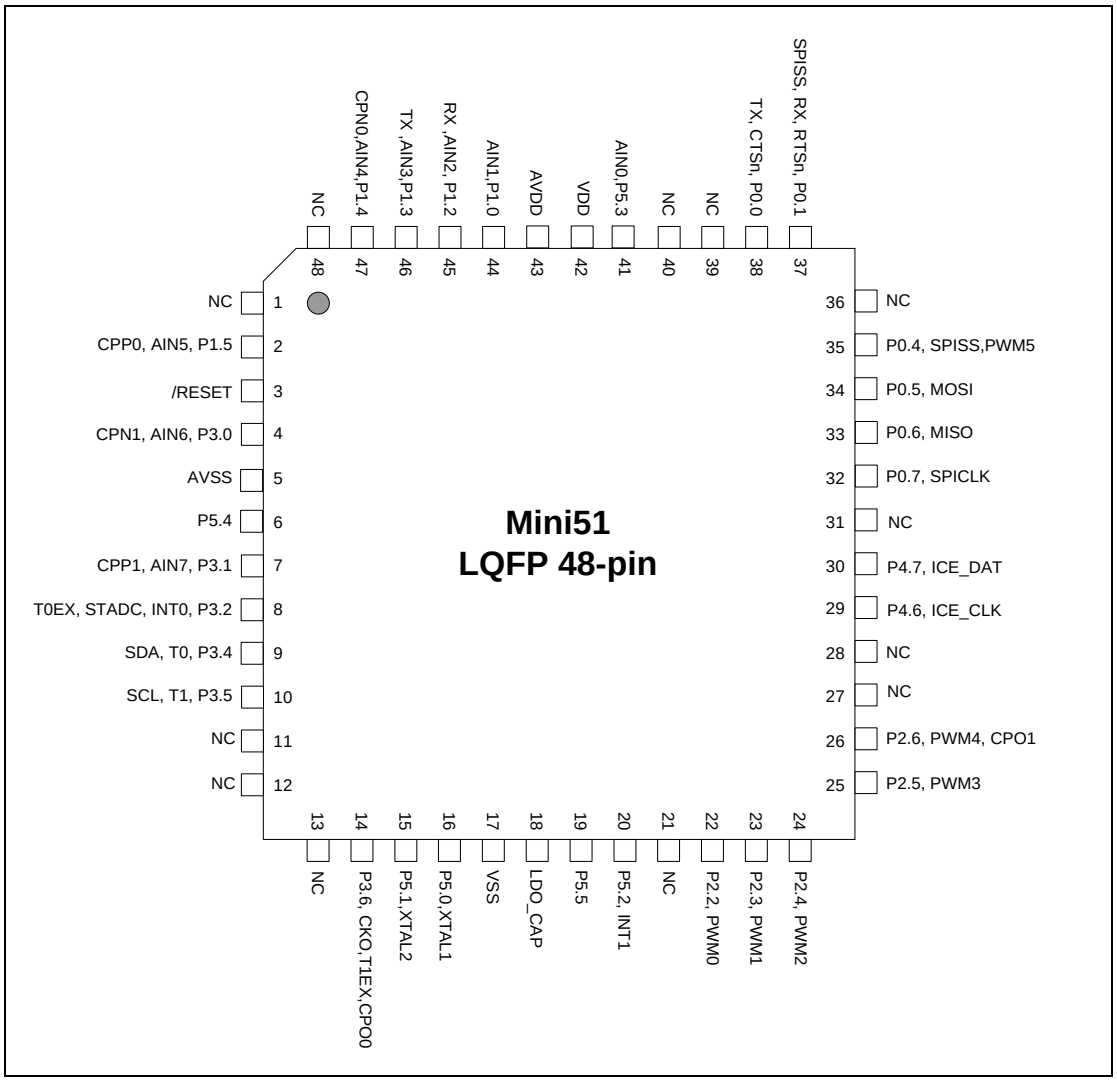


Figure 3.2-1 NuMicro Mini51™ Series LQFP 48-pin Assignment

3.2.2 QFN 33-pin

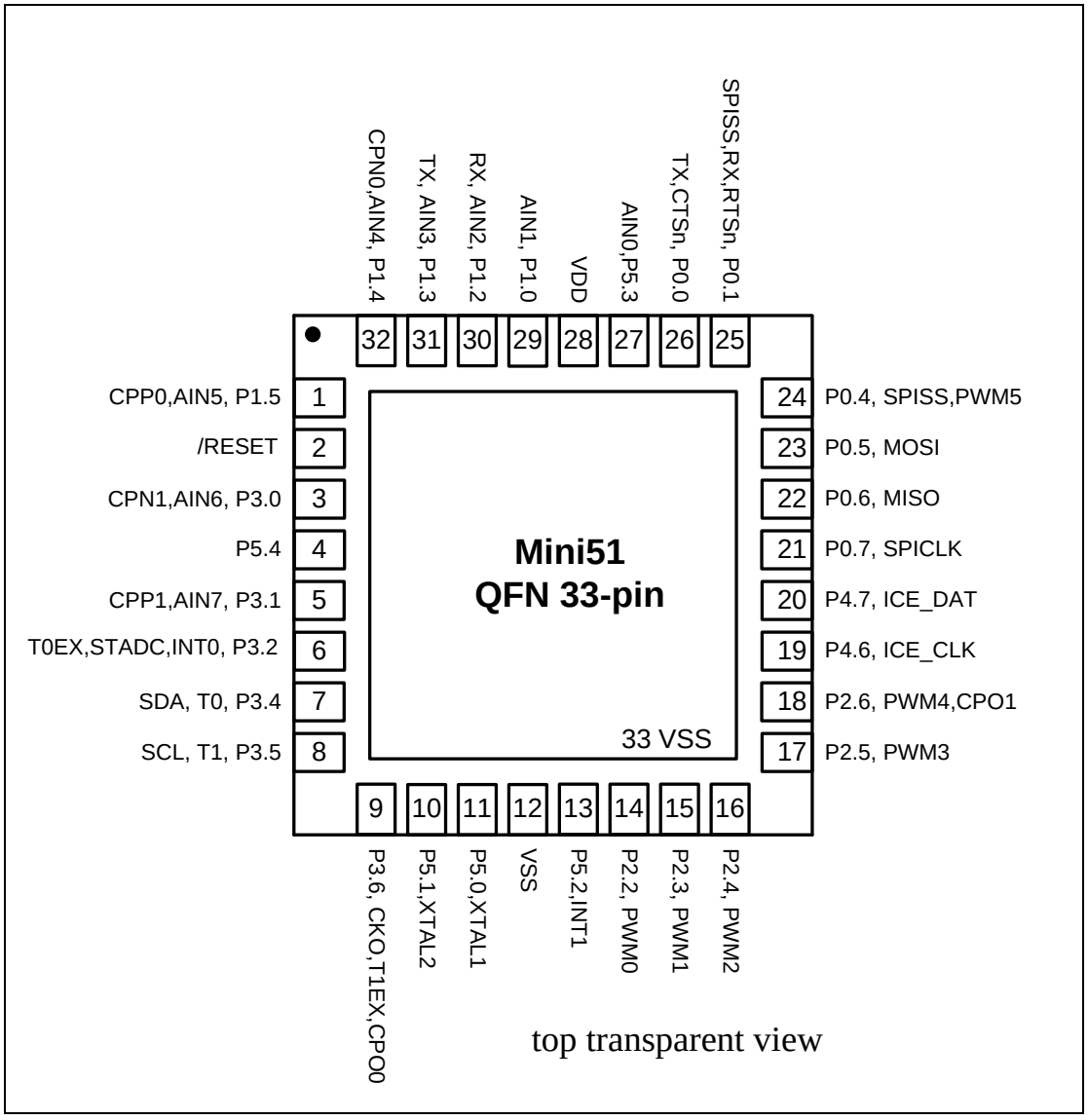


Figure 3.2-2 NuMicro Mini51™ Series QFN 33-pin Assignment

4 BLOCK DIAGRAM

4.1 NuMicro Mini51™ Block Diagram

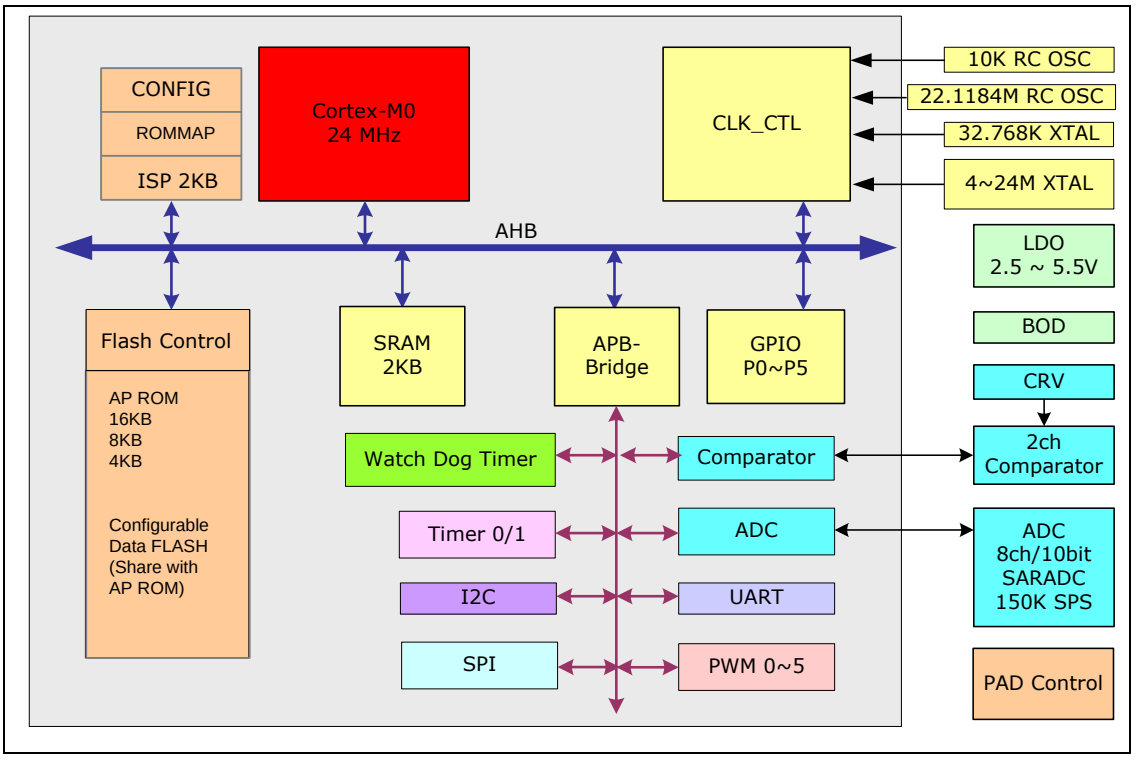
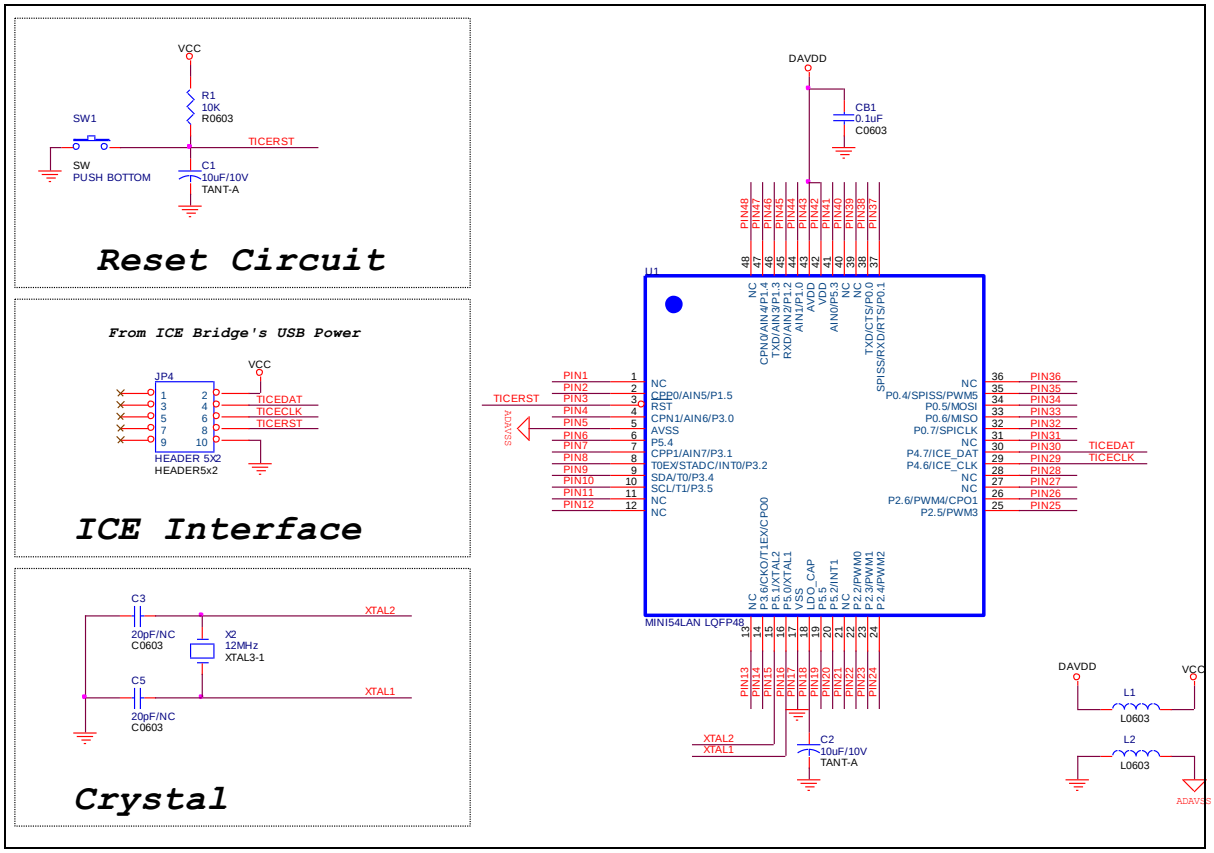


Figure 4.1-1 NuMicro Mini51™ Series Block Diagram

5 APPLICATION CIRCUIT



6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	Min	MAX	UNIT
DC power supply	V_{DD}–V_{SS}	-0.3	+7.0	V
Input voltage	VIN	V_{SS}-0.3	V_{DD}+0.3	V
Oscillator frequency	$1/t_{CLCL}$	4	24	MHz
Operating temperature	TA	-40	+85	°C
Storage temperature	TST	-55	+150	°C
Maximum current into VDD		-	120	mA
Maximum current out of VSS			120	mA
Maximum current sunk by a I/O pin			35	mA
Maximum current sourced by a I/O pin			35	mA
Maximum current sunk by total I/O pins			100	mA
Maximum current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

6.2 DC Electrical Characteristics

(VDD-VSS = 5.0 V, TA = 25°C, FOSC = 24 MHz unless otherwise specified.)

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} = 2.5 V ~ 5.5 V up to 24 MHz
V_{DD} rise rate to ensure internal operation correctly	V_{RISE}	0.05			V/mS	
Power ground	V_{SS} AV_{SS}	-0.3			V	
LDO output voltage	V_{LDO}	-10%	1.8	+10%	V	V_{DD} = 2.5V ~ 5.5V
Analog operating voltage	AV_{DD}	0		V_{DD}	V	
Operating current Normal run mode at 24 MHz	I_{DD1}		9.5		mA	V_{DD} = 5.5V at 24 MHz, all IP Enabled
	I_{DD2}		7.5		mA	V_{DD} = 5.5V at 24 MHz, all IP Disabled
	I_{DD3}		7.5		mA	V_{DD} = 3.3V at 24 MHz, all IP Enabled
	I_{DD4}		6		mA	V_{DD} = 3.3V at 24 MHz, all IP Disabled
Operating current Normal run mode at 12 MHz	I_{DD5}		5.5		mA	V_{DD} = 5.5V at 12 MHz, all IP Enabled
	I_{DD6}		4.5		mA	V_{DD} = 5.5V at 12 MHz, all IP Disabled
	I_{DD7}		4		mA	V_{DD} = 3.3V at 12 MHz, all IP Enabled
	I_{DD8}		3		mA	V_{DD} = 3.3V at 12 MHz, all IP Disabled
Operating current Normal run mode at 4 MHz	I_{DD9}		3.6		mA	V_{DD} = 5.5V at 4 MHz, all IP Enabled
	I_{DD10}		3.3		mA	V_{DD} = 5.5V at 4 MHz, all IP Disabled
	I_{DD11}		1.7		mA	V_{DD} = 3.3V at 4 MHz, all IP Enabled
	I_{DD12}		1.4		mA	V_{DD} = 3.3V at 4 MHz, all IP Disabled
Operating current Normal run mode at 22.1184 MHz IRC	I_{DD13}		6.6		mA	V_{DD} = 5.5V at 22.1184 MHz, all IP Enabled
	I_{DD14}		5		mA	V_{DD} = 5.5V at 22.1184 MHz, all IP Disabled
	I_{DD15}		6.6		mA	V_{DD} = 3.3V at 22.1184 MHz, all IP Enabled
	I_{DD16}		5		mA	V_{DD} = 3.3V at 22.1184 MHz, all IP Disabled

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Operating current Normal run mode at 32.768 KHz crystal oscillator	I_{DD17}		116		μA	V_{DD} = 5.5V at 32.768 KHz, all IP Enabled
	I_{DD18}		113		μA	V_{DD} = 5.5V at 32.768 KHz, all IP Disabled
	I_{DD19}		112		μA	V_{DD} = 3.3V at 32.768 KHz, all IP Enabled
	I_{DD20}		100		μA	V_{DD} = 3.3V at 32.768 KHz, all IP Disabled
Operating current Normal run mode at 10 KHz IRC	I_{DD21}		109		μA	V_{DD} = 5.5V at 10 KHz, all IP Enabled
	I_{DD22}		108		μA	V_{DD} = 5.5V at 10 KHz, all IP Disabled
	I_{DD23}		100		μA	V_{DD} = 3.3V at 10 KHz, all IP Enabled
	I_{DD24}		98		μA	V_{DD} = 3.3V at 10 KHz, all IP Disabled
Operating current Idle mode at 24 MHz	I_{IDLE1}		5.5		mA	V_{DD} = 5.5V at 24 MHz, all IP Enabled
	I_{IDLE2}		3.5		mA	V_{DD} = 5.5V at 24 MHz, all IP Disabled
	I_{IDLE3}		3.8		mA	V_{DD} = 3.3V at 24 MHz, all IP Enabled
	I_{IDLE4}		1.8		mA	V_{DD} = 3.3V at 24 MHz, all IP Disabled
Operating current Idle mode at 12 MHz	I_{IDLE5}		3.3		mA	V_{DD} = 5.5V at 12 MHz, all IP Enabled
	I_{IDLE6}		2.6		mA	V_{DD} = 5.5V at 12 MHz, all IP Disabled
	I_{IDLE7}		2		mA	V_{DD} = 3.3V at 12 MHz, all IP Enabled
	I_{IDLE8}		1		mA	V_{DD} = 3.3V at 12 MHz, all IP Disabled
Operating current Idle mode at 4 MHz	I_{IDLE9}		3		mA	V_{DD} = 5.5V at 4 MHz, all IP Enabled
	I_{IDLE10}		2.3		mA	V_{DD} = 5.5V at 4 MHz, all IP Disabled
	I_{IDLE11}		1		mA	V_{DD} = 3.3V at 4 MHz, all IP Enabled
	I_{IDLE12}		0.7		mA	V_{DD} = 3.3V at 4 MHz, all IP Disabled
Operating current Idle mode at 22.1184 MHz IRC	I_{IDLE13}		3.0		mA	V_{DD} = 5.5V at 22.1184 MHz, all IP Enabled
	I_{IDLE14}		1.2		mA	V_{DD} = 5.5V at 22.1184 MHz, all IP Disabled
	I_{IDLE15}		3.0		mA	V_{DD} = 3.3V at 22.1184 MHz, all IP Enabled

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
	I_{IDLE16}		1.2		mA	V_{DD} = 3.3V at 22.1184 MHz, all IP Disabled
Operating current Idle mode at 32.768 KHz crystal oscillator	I_{IDLE17}		110		µA	V_{DD} = 5.5V at 32.768 KHz, all IP Enabled
	I_{IDLE18}		107		µA	V_{DD} = 5.5V at 32.768 KHz, all IP Disabled
	I_{IDLE19}		105		µA	V_{DD} = 3.3V at 32.768 KHz, all IP Enabled
	I_{IDLE20}		102		µA	V_{DD} = 3.3V at 32.768 KHz, all IP Disabled
Operating current Idle mode at 10 KHz IRC	I_{IDLE21}		103		µA	V_{DD} = 5.5V at 10 KHz, all IP Enabled
	I_{IDLE22}		102		µA	V_{DD} = 5.5V at 10 KHz, all IP Disabled
	I_{IDLE23}		96		µA	V_{DD} = 3.3V at 10 KHz, all IP Enabled
	I_{IDLE24}		95		µA	V_{DD} = 3.3V at 10 KHz, all IP Disabled
Standby current Power-down mode	I_{PWD1}		10		µA	V_{DD} = 5.0V, CPU STOP All IP and Clock OFF
	I_{PWD2}		5		µA	V_{DD} = 3.3V, CPU STOP All IP and Clock OFF
Standby current Power-down mode with 32.768 KHz crystal enabled	I_{PWD3}		12		µA	V_{DD} = 5.0V, CPU STOP All IP and Clock OFF except 32.768KHz crystal oscillator
	I_{PWD4}		7		µA	V_{DD} = 3.3V, CPU STOP All IP and Clock OFF except 32.768KHz crystal oscillator
Input current P0~P5 (Quasi-bidirectional mode)	I_{IN1}		-50	-60	µA	V_{DD} = 5.5 V, V_{IN} = 0 V or V_{IN} = V_{DD}
Input current at /RESET[1]	I_{IN2}	-55	-45	-30	µA	V_{DD} = 3.3 V, V_{IN} = 0.45 V
Input leakage current PA, PB, PC, PD, PE	I_{LK}	-0.1	-	+0.1	µA	V_{DD} = 5.5 V, 0<V_{IN}<V_{DD}
Logic 1 to 0 transition current PA~PE (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	µA	V_{DD} = 5.5 V, V_{IN}<2.0 V
Input low voltage	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5 V

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
P0~P5 (TTL input)		-0.3	-	0.6		V_{DD} = 2.5 V
Input high voltage P0~P5 (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} = 3.0V
Input low voltage P0~P5, (Schmitt input)	V_{IL2}		0.4 V_{DD}		V	
Input high voltage P0~P5, (Schmitt input)	V_{IH2}		0.6 V_{DD}		V	
Hysteresis voltage of P0~P5 (Schmitt input)	V_{HY}		0.2 V_{DD}		V	
Input low voltage XTAL1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input high voltage XTAL1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Internal /RESET pin pull-up resistor	R_{RST}	40	-	100	KΩ	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.5	-	0.3 V_{DD}	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	0.6 V_{DD}	-	V_{DD}+0.5	V	
Source current P0~P5. (Quasi-bidirectional mode)	I_{SR11}	-300	-370	-450	µA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-70	-90	µA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-60	-80	µA	V_{DD} = 2.5V, V_S = 2.0V
Source current P0~P5, (Push-pull mode)	I_{SR21}	-20	-24	-28	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5V, V_S = 2.0V
Sink current P0~P5, (Quasi-bidirectional and Push-pull mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5V, V_S = 0.45V

Notes:

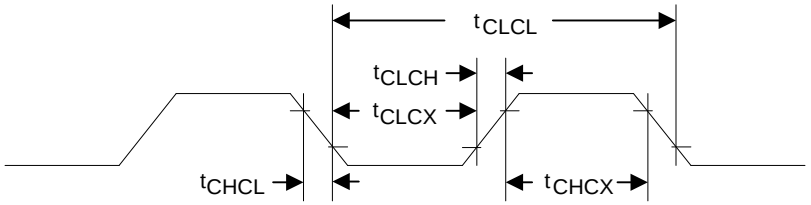
1. /RESET pin is a Schmitt trigger input.

2. Crystal Input is a CMOS input.
3. Pins of P0~P5 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, the transition current reaches its maximum value when V_{IN} approximates to 2V.

6.3 AC Electrical Characteristics

6.3.1 External Input Clock

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Clock high time	t_{CHCX}	20			nS	
Clock low time	t_{CLCX}	20			nS	
Clock rise time	t_{CLCH}			10	nS	
Clock fall time	t_{CHCL}			10	nS	



Note: Duty cycle is 50%.

6.3.2 External 4 ~ 24 MHz XTAL Oscillator

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Oscillator frequency	f_{HXTAL}	4	12	24	MHz	V_{DD} = 2.5V ~ 5.5V
Temperature	T_{HXTAL}	-40		+85	°C	
Operating current	I_{HXTAL}		TBD		mA	V_{DD} = 5.0V

6.3.3 Typical Crystal Application Circuit

CRYSTAL	C1	C2
4 MHz ~ 24 MHz	Optional (depending on crystal specification)	

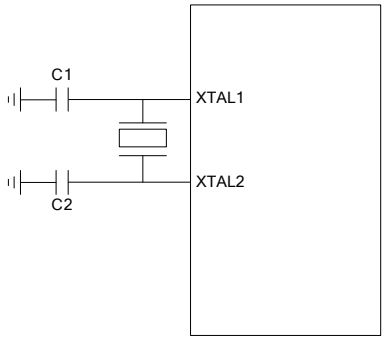


Figure 6.3-1 Typical Crystal Application Circuit

6.3.4 External 32.768 KHz XTAL Oscillator

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Oscillator frequency	fL_{XTAL}		32.768		KHz	V_{DD} = 2.5V ~ 5.5V
Temperature	TL_{XTAL}	-40		+85	°C	
Operating current	I_{HXTAL}		TBD		μA	V_{DD} = 5.0V

6.3.5 Internal 22.1184 MHz RC Oscillator

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Supply voltage[1]	V_{HRC}		1.8		V	
Center frequency	F_{HRC}	21.89	22.1184	22.34	MHz	25°C, V_{DD} = 5V
		20.57	22.1184	23.23	MHz	-40°C~+85 °C, V_{DD} = 2.5V~5.5V
		21.78	22.0	22.22	MHz	-40°C~+85 °C, V_{DD} = 2.5V~5.5V 32.768K crystal oscillator Enabled and TRIM_SEL = 1
Operating current	I_{HRC}		TBD		mA	

Note: Internal operation voltage comes from LDO.

6.3.6 Internal 10 KHz RC Oscillator

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Supply voltage[1]	V_{LRC}		1.8		V	
Center frequency	F_{LRC}	7	10	13	KHz	25°C, V_{DD} = 5V
		5	10	15	KHz	-40°C = ~+85 °C, V_{DD} = 2.5V~5.5V
Operating current	I_{LRC}		TBD		μA	V_{DD} = 5V

Note: Internal operation voltage comes from LDO.

6.4 Analog Characteristics

(V_{DD}-V_{SS} = 5.0V, TA = 25°C, FOSC = 24 MHz unless otherwise specified.)

6.4.1 Brown-Out Reset (BOD)

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Operating voltage	V_{BOD}	2.0		5.5	V	
Operating current	I_{BOD}		5	15	μA	V_{DD} = 5V BOD27 and BOD38 Enabled
BOD38 detection level	V_{B38dt}	3.6	3.8	4.0	V	25°C
BOD27 detection level	V_{B27dt}	2.6	2.7	2.8	V	25°C

6.4.2 Low Voltage Reset (LVR)

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Operating voltage	V_{BOD}	2.0		5.5	V	
Operating current	I_{BOD}		1	2	μA	
Detection level	V_{LVR}		2.0		V	25°C
LVR always enabled		1.6	2.0	2.4	V	-40°C ~ +85°C

6.4.3 Analog Comparator

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Operating voltage	V_{BOD}	2.5	3.3	5.5	V	
Operating current	I_{CMP}		40	80	μA	
Input offset voltage	V_{OFFSET}		10	20	mV	
Output swing voltage	V_{swin}	0.2		V_{DD}-0.2	V	
Input common mode range (V_{CM})	V_{CM}	0.1		V_{DD}-0.1	V	
DC gain	G_{DC}		70		dB	
Propagation delay	T_{PDLY}		200		ns	V_{CM} = 1.2V The difference voltage in CPPx and CPNx is 0.1V
Hysteresis	V_{HYS}		±10		mV	One bit control W/O and W. hysteresis @V_{CM} = 0.2V ~ VDD-0.2V

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Stable time	T_{STBL}			2	µS	CPPx = 1.3V and CPNX = 1.2V

6.4.4 Analog Comparator Reference Voltage (CRV)

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Operating voltage	V_{BOD}	2.5		5.5	V	
CRV step size	V_{STEP}		V_{DD}/24		V	VDD = 5V, BOD27 and BOD38 Enabled
CRV output voltage absolute accuracy	A_{CRV}	-5		+5	%	
Unit resistor value	R_{CRV}		2K		ohm	

6.4.5 10-bit ADC

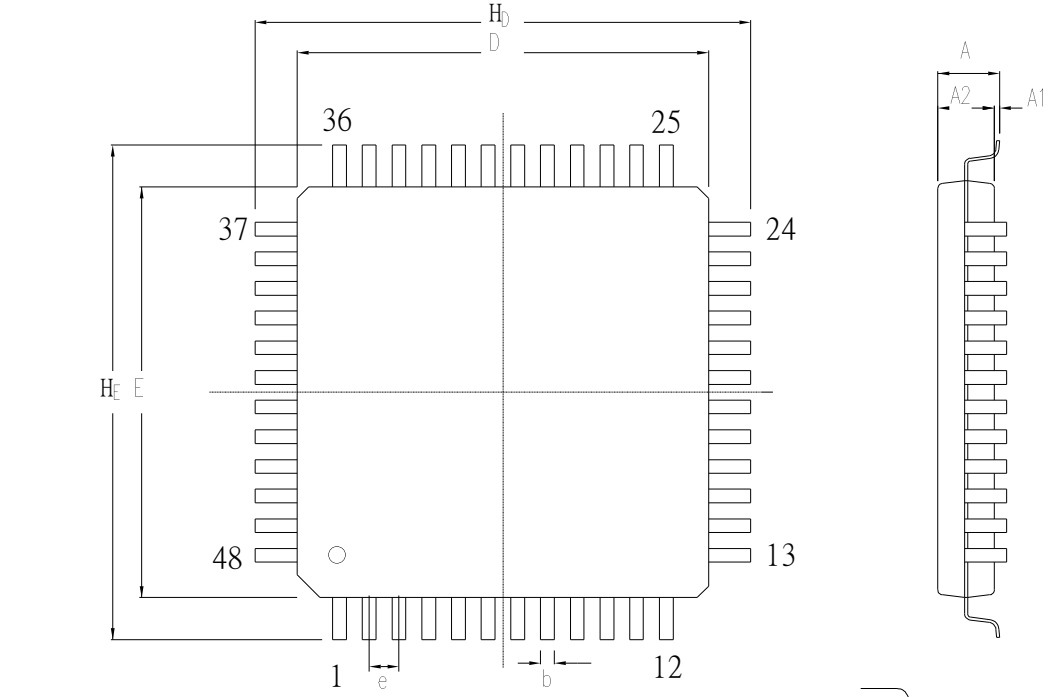
PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Operating voltage	AV_{DD}	2.7		5.5	V	$AV_{DD} = V_{DD}$
Operating current	I_{ADC}			1	mA	$AV_{DD} = V_{DD} = 5V$, F_{SPS} = 150K
Resolution	R_{ADC}			10	bit	
Reference voltage	V_{REF}		A_{VDD}		V	V_{REF} connected to A_{VDD} in chip
ADC input voltage	V_{IN}	0		V_{REF}	V	
Conversion time	T_{CONV}	6.7			µS	
Sampling rate	F_{SPS}	150K			Hz	V_{DD} = 5V, ADC clock = 6MHz Free running conversion
Integral non-linearity error (INL)	INL			±1	LSB	
Differential non-linearity (DNL)	DNL			±1	LSB	
Gain error	E_G			±2	LSB	
Offset error	E_{OFFSET}			3	LSB	
Absolute error	E_{ABS}			4	LSB	
ADC clock frequency	F_{ADC}	5K		6M	Hz	V_{DD} = 5V
Clock cycle	AD_{CYC}	38			Cycle	
Bang-gap voltage	V_{BG}	1.27	1.35	1.44	V	-40°C ~ +85°C

6.4.6 Flash Memory Characteristics

PARAMETER	Sym.	Specification				TEST CONDITIONS
		Min.	TYP.	Max.	Unit	
Cycling (erase/write) Program memory	N_{CYC}	100			K cycle	
Data retention	T_{RET}	10			years	T_A = +85°C
Erase time of ISP mode	T_{ERASE}	2.3	2.5	2.7	mS	Erase time for one page
Program time of ISP mode	T_{PROG}	57	62	67	μS	Programming time for one word
Program current	I_{PROG}		3.3		mA	V_{DD} = 5.5V

7 PACKAGE DIMENSION

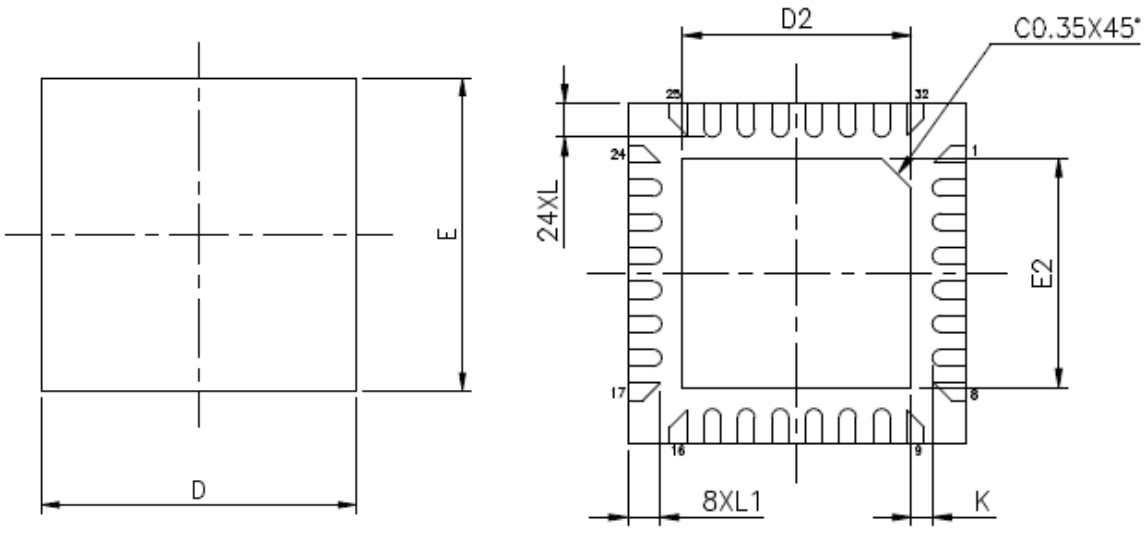
7.1 48-pin LQFP

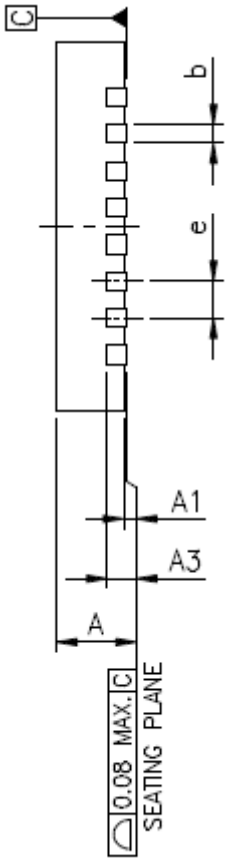


Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0	—	7	0	—	7

7.2 33-pin QFN (4mm x 4mm)

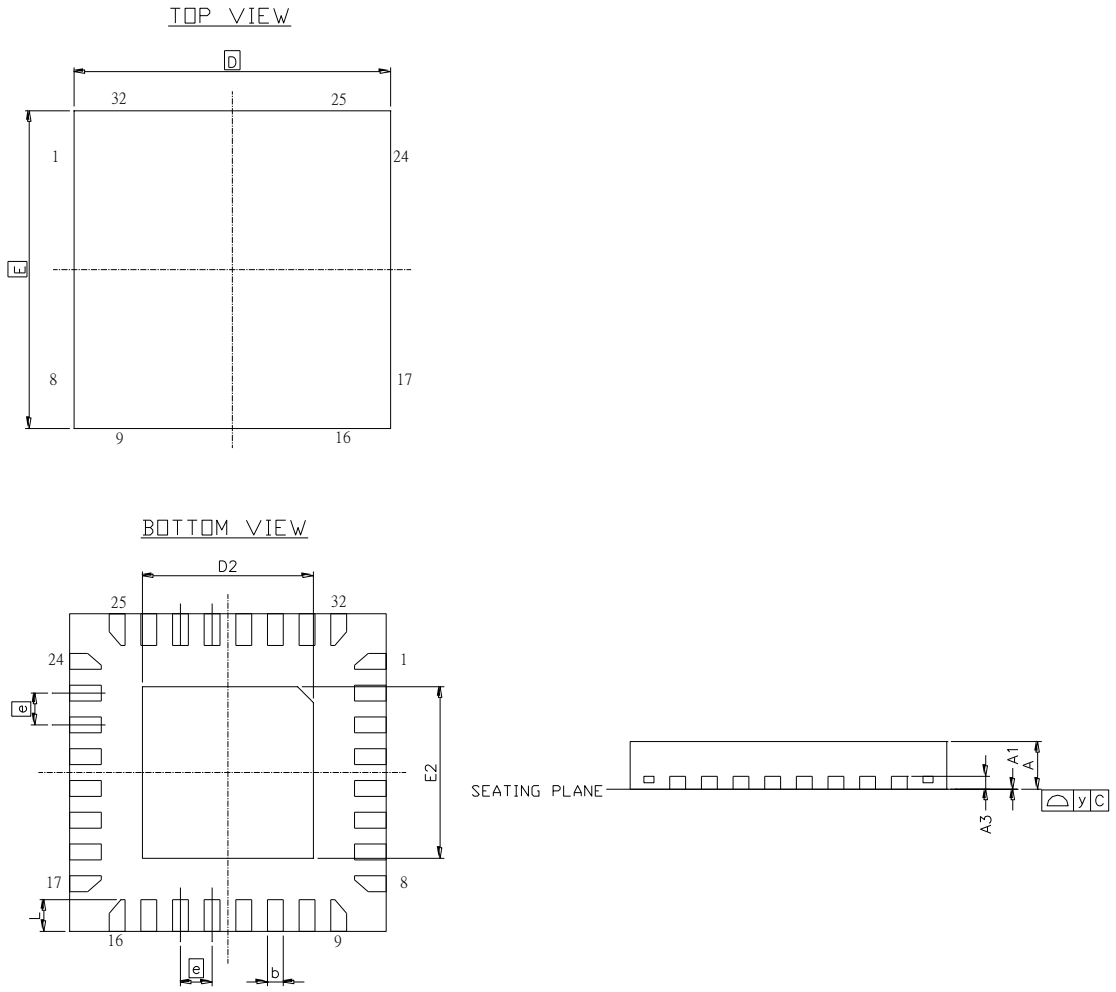




DIMENSION	MILLIMETERS		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.15	0.20	0.25
D	4.00 BSC		
E	4.00 BSC		
e	0.40 BSC		
L	0.35	0.40	0.45
L1	0.332	0.382	0.432
K	0.20	—	—

	E2			D2		
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
114X114 MIL	2.60	2.70	2.75	2.60	2.70	2.75

7.3 33-pin QFN (5mm x 5mm)



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	0.02	0.05	0	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC			0.197 BSC		
E	5.00 BSC			0.197 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
y	0.10			0.0039		

SYMBOL	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
DIMENSION (MM)	3.4	3.5	3.6	3.4	3.5	3.6

8 REVISION HISTORY

Date	Revision	Changes
Sep 6, 2011	1.00	Initial release
Oct 20, 2011	1.01	1. Change electrical characteristics of comparator, 22MHZ RC oscillator, ADC and band-gap. 2. Add electrical characteristics of Flash memory 3. Change maximum SPI frequency as 12MHz 4. Fix some typos.
Dec 1, 2011	1.02	1. Fix electrical characteristics of 22MHZ RC oscillator 2. Modify 33-pin QFN 5mmx5mm package outline specification. 3. Fix some typos.
Feb 9, 2012	1.03	1. Added the VDD rise rate specification. 2. Revised the minimum ADC clock frequency specification. 3. Revised the minimum and maximum specification of band-gap voltage.

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