NUC710ADN
16/32-bit ARM microcontroller
Product Data Sheet

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1. GENERAL DESCRIPTION

The NUC710 is built around an outstanding CPU core, the 16/32 ARM7TDMI RISC processor, designed by Advanced RISC Machines, Ltd. It offers 4K-byte I-cache/SRAM and 4K-byte D-cache/SRAM, is a low power, general-purpose integrated circuit. Its simple, elegant, and fully static design is particularly suitable for cost sensitive and power sensitive applications.

One 10/100 Mb MAC of Ethernet controller is built-in to reduce total system cost. An LCD controller is also built-in to support TFT and low cost STN LCD modules.

With one USB 1.1 host controller, one USB 1.1 device controller, two smart card host controllers, four independent UARTs, one Watchdog timer, up to 71 programmable I/O ports, PS/2 keyboard controller and an advanced interrupt controller, the NUC710 is particularly suitable for point-of-sale (POS) system, access control and as a data collector.

The NUC710 also provides one AC97/I²S controller, one SD host controller, one 2-Channel GDMA, two 24-bit timers with 8-bit pre-scale, The external bus interface (EBI) controller provides for SDRAM, ROM/SRAM, flash memory and I/O devices. The System Manager includes an internal 32-bit system bus arbiter and a PLL clock controller. With a wide range of serial communication and Ethernet interfaces, the NUC710 is also suitable for communication gateways as well as many other general-purpose applications.

2. FEATURES

Architecture

- Fully 16/32-bit RISC architecture
- Little/Big-Endian mode supported
- Efficient and powerful ARM7TDMI core
- Cost-effective JTAG-based debug solution

External Bus Interface

- 8/16/32-bit external bus support for ROM/SRAM, flash memory, SDRAM and external I/Os
- Support for SDRAM
- Programmable access cycle (0-7 wait cycle)
- Four-word depth write buffer for SDRAM write data
- Cost-effective memory-to-peripheral DMA interface

Instruction and Data Cache

- Two-way, Set-associative, 4K-byte I-cache and 4K-byte D-cache
- Support for LRU (Least Recently Used) Protocol
- Cache can be configured as internal SRAM
- Support Cache Lock function

Ethernet MAC Controller

- DMA engine with burst mode
- MAC Tx/Rx buffers (256 bytes Tx, 256 bytes Rx)
- Data alignment logic
- Endian translation
- 100/10-Mbit per second operation
- Full compliance with IEEE standard 802.3
- RMII interface only
- Station Management Signaling
- On-Chip CAM (up to 16 destination addresses)
- Full-duplex mode with PAUSE feature
- Long/short packet modes
- PAD generation

LCD Controller (LCDC)

(1) STN LCD Display

- Supports 4-bit single scan Monochrome STN LCD panel, 8-bit single scan Monochrome STN LCD panel, 8-bit single scan Color STN LCD panel
- Up to 16 gray levels display for Monochrome STN LCD panel
- Up to 4096(12bpp) colors display for Color STN LCD panel
- Virtual coloring method: Frame Rate Control (16-level)
- Anti-flickering method: Time-based Dithering

(2) TFT LCD Display

- Supports Sync-type TFT LCD panel and Sync-type High-color TFT LCD panel
- Supports direct or palletized color display

(3) TV Encoder

- Supports 8-bit YCbCr data output format to connect with external TV Encoder

(4) LCD Preprocessing

- Supports RGB Raw-data or YUV422 packet format
- Programmable parameters for different image sizes
- Two built-in FIFOs, FIFO 1 is for Video images and FIFO 2 is for OSD images. Each FIFO is 16 words deep

(5) LCD Post processing

- Support for one OSD (On-Screen-Display) overlay
- Supports various OSD functions
- Programmable parameters for different display panels

(6) Others

- Color-look up table size 256x32 bit for TFT used when displaying 1bpp, 2bpp, 4bpp, 8bpp image
- Dedicated DMA for block transfer mode

DMA Controller

- 2-channel General DMA for memory-to-memory data transfers without CPU intervention
- Initialed by a software or external DMA request
- Increments or decrements a source or destination address in 8-bit, 16-bit or 32-bit data transfers
- 4-data burst mode

UART

- Four UART (serial I/O) blocks with interrupt-based operation
- Support for 5-bit, 6-bit, 7-bit or 8-bit serial data transmission
- Programmable baud rates
- 1, ½ or 2 stop bits
- Odd or even parity

- Break generation and detection
- Parity, overrun and framing error detection
- X16 clock mode
- UART1 supports Bluetooth, and UART2 supports IrDA1.0 SIR

Timers

- Two programmable 24-bit timers with 8-bit prescaler
- One programmable 20-bit timer with optional 8-bit prescaler Watchdog timer
- One-shot mode, periodical mode or toggle mode operation

Programmable I/Os

- 71 programmable I/O ports
- Pins individually configurable for input, output or I/O mode for dedicated signals
- I/O ports are configurable for Multiple functions

Advanced Interrupt Controller

- 31 interrupt sources, including 6 external interrupt sources
- Programmable normal or fast interrupt mode (IRQ, FIQ)
- Programmable as either edge-triggered or level-sensitive for 6 external interrupt sources
- Programmable as either low-active or high-active for 6 external interrupt sources
- Priority methodology is encoded to allow for interrupt daisy-chaining
- Automatically mask out the lower priority interrupt during interrupt nesting

USB Host Controller

- USB 1.1 compliant
- Compatible with Open HCI 1.0 specification
- Supports low-speed and full speed devices
- Built-in DMA for real time data transfer
- Two on-chip USB transceivers with one optionally shared with USB Device Controller

USB Device Controller

- USB 1.1 compliant
- Supports four USB endpoints including one control endpoint and 3 configurable endpoints for rich USB functions

Two PLLs

- The external clock can be multiplied by on-chip PLL to provide high frequency system clock
- The input frequency range is 3-30MHz; 15MHz is preferred.
- One PLL for both CPU and USB host/device controller
- One PLL for LCD pixel clock and audio IIS 12.288/16.934MHz clock source

- Programmable clock frequency

Real Time Clock (RTC)

- 32.768KHz operation
- Time counter (second, minute, hour) and calendar counter (day, month, year)
- Alarm register (second, minute, hour, day, month, year)
- 12 or 24-hour mode selectable
- Automatically recognizes leap years
- Weekday counter
- Frequency compensate register (FCR)
- Besides the FCR, all clock and alarm data are expressed in BCD
- Supports tick time interrupts

4-Channel PWM

- Four 16-bit timers with PWM
- Two 8-bit prescalers & Two 4-bit dividers
- Programmable duty control of output waveform
- Auto reload mode or one-shot pulse mode
- Dead-zone generator

I2C Master

- Two Channel I2C
- Compatible with Philips I^2C standard, support master mode only
- Supports multi master operation
- Clock stretching and wait state generation
- Provides multi-byte transmission, up to 4 bytes can be transmitted in a single transfer
- Software programmable acknowledge bit
- Arbitration lost interrupt, with automatic transfer cancellation
- Start/Stop/Repeated Start/Acknowledge generation
- Start/Stop/Repeated Start detection
- Bus busy detection
- Supports 7 bit addressing mode
- Software mode I^2C

Universal Serial Interface (USI)

- 1-Channel USI
- Support USI (Microwire/SPI) master mode
- Full duplex synchronous serial data transfer
- Variable length of transfer word up to 32 bits
- Provide burst mode operation, transmit/receive can be executed up to four times in one transfer
- MSB or LSB first data transfer
- Rx and Tx on both positive or negative edge of serial clock independently
- Two slave/device select lines
- Fully static synchronous design with one clock domain

2-Channel AC97/I2S Audio Codec Host Interface

- AHB master port and an AHB slave port are offered in the audio controller.
- 8-beat incrementing burst
- Bus lock during 8-beat incrementing burst
- At the middle or end of a destination address, a DMA_IRQ is automatically requested from the CPU

Smart Card Host Interface (SCHI)

- ISO-7816 compliant
- PC/SC T=0, T=1 compliant
- 16-byte transmitter FIFO and 16-byte receiver FIFO
- FIFO threshold interrupt to optimize system performance
- Programmable transmission clock frequency
- Versatile baud rate configuration
- UART-like register file structure
- General-purpose C4, C8 channels

SD Host Interface

- Directly connect to Secure Digital (SD, MMC) flash memory card.
- Supports DMA functions to accelerate the data transfer between the internal buffer, external SDRAM, and flash memory cards.
- Two 512 byte internal buffers are embedded inside the controller.
- No SPI mode.

KeyPad Scan Interface

- Scan up to 16 rows by 8 columns with an external 4 to 16 decoder and 4 rows by 8 columns array without auxiliary components
- Programmable de-bounce time
- One or two keys scan with interrupt and three keys reset function.

- Wakeup CPU from IDEL/Power Down mode

PS2 Host Interface

- APB slave consisted of PS2 protocol.
- Connect IBM keyboard or bar code reader through PS2 interface.
- Provide hardware scan code to ASCII translation

Power management

- Programmable clock enables individual peripherals
- IDLE mode to halt ARM Core and keep peripheral working
- Power-Down mode to stop all clocks included external crystal oscillator.
- Exit IDLE by all interrupts
- Exit Power-Down by keypad, USB device and external interrupts

Operating Voltage Range

- 3.0 ~ 3.6 V for IO Buffer
- 1.62 ~ 1.98 V for Core Logic

Operating Temperature Range

- -40℃ ~ +85 ℃

Operating Frequency

- Up to 80 MHz

Package Type

- 176-pin LQFP

3. PIN DIAGRAM

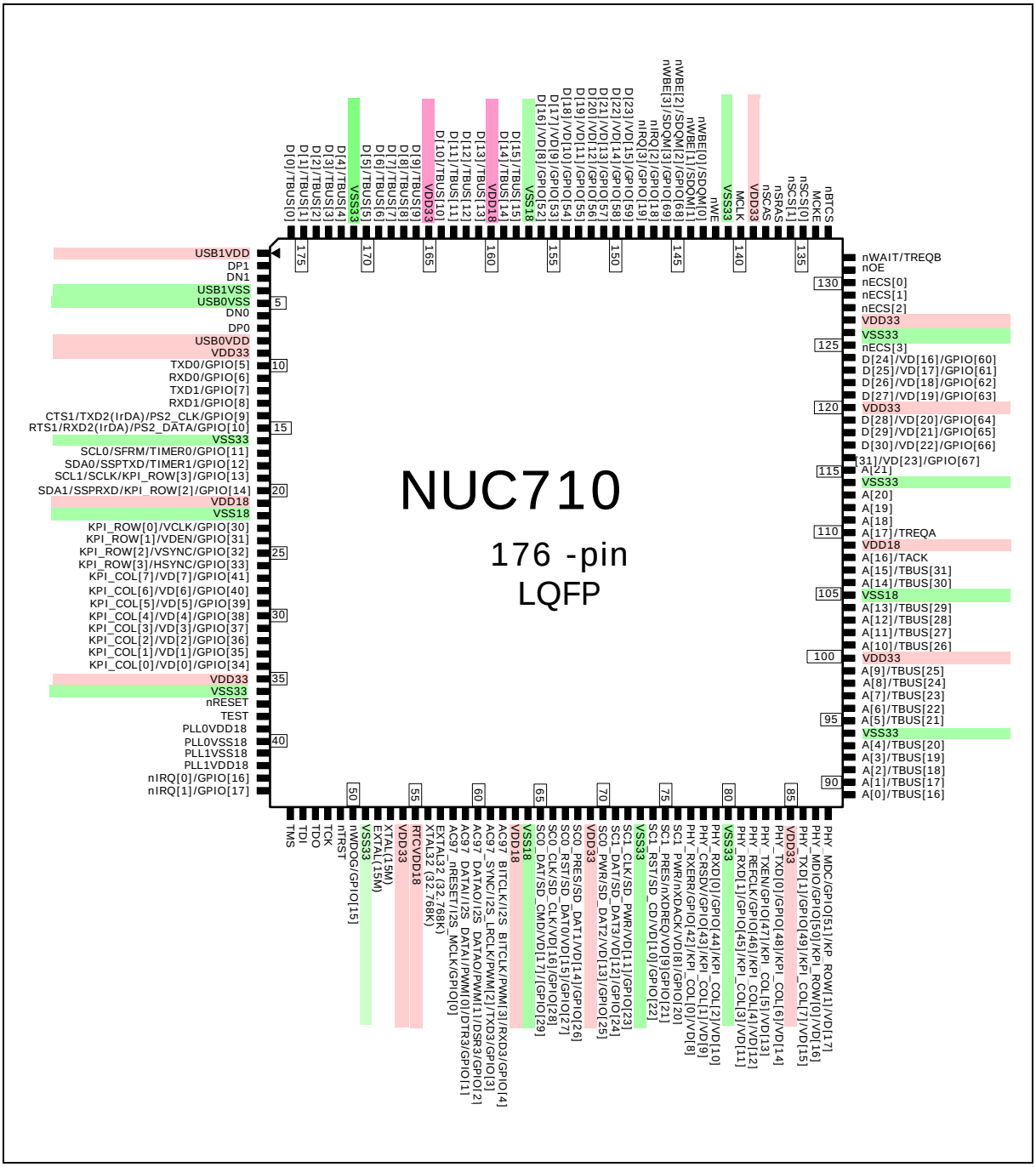


Fig 3.1 Pin Diagram

4. PIN ASSIGNMENTS

Table 4.1 NUC710 Pin Assignments

PIN NAME	176-PIN LQFP
Clock & Reset	**(5 pins)**
EXTAL (15M)	52
XTAL (15M)	53
EXTAL32 (32.768K)	57
XTAL32 (32.768K)	56
nRESET	37
JTAG Interface	**(5 pins)**
TMS	45
TDI	46
TDO	47
TCK	48
nTRST	49
External Bus Interface	**(72 pins)**
A [21]	115
A [20:0]	113-110,108-106, 104-101,99-95, 93-89
D [31:16] / VD [23:8] / GPIO [67:52]	116-119,121-124, 149-156
D [15:0]	158,159,161-164, 166-170,172-176
nWBE [3:2] / SDQM [3:2] / GPIO[69:68]	146,145
nWBE [1;0] / SDQM [1:0]	144,143
nSCS [1:0]	136,135
nSRAS	137
nSCAS	138
MCKE	134
nSWE	142
MCLK	140
nWAIT/ GPIO[70] / nIRQ5	132
nBTCS	133
nECS [3]	125
nECS [2:0]	128-130
nOE	131

Table 4.1 NUC710 Pin Assignments (Continued)

PIN NAME	176-PIN LQFP
Ethernet Interface	**(10 pins)**
PHY_MDC / GPIO [51] / KPROW[1] / VD[17]	88
PHY_MDIO / GPIO [50] / KPROW[0] / LD[16]	87
PHY_TXD [1:0] / GPIO[49:48] / KPCOL[7:6] / VD[15:14]	86,84
PHY_TXEN / GPIO [47] / KPCOL[5] / VD[13]	83
PHY_REFCLK / GPIO [46] / KPCOL[4] / VD[12]	82
PHY_RXD [1:0] / GPIO [45:44] / KPCOL[3:2] / VD[11:10]	81,79
PHY_CRSDV / GPIO [43] / KPCOL[1] / VD[9]	78
PHY_RXERR / GPIO [42] / KPCOL[0] / VD[8]	77
AC97/I2S/PWM/UART3	**(5 pins)**
AC97_nRESET / I2S_MCLK / GPIO [0] / USB_PWREN	58

Table 4.1 NUC710 Pin Assignments (Continued)

PIN NAME	176-PIN LQFP
AC97/I2S/PWM/UART3	**(5 pins)**
AC97_DATAI / I2S_DATAI / PWM [0] / DTR3 / GPIO [1]	59
AC97_DATAO / I2S_DATAO / PWM [1] / DSR3 / GPIO [2]	60
AC97_SYNC / I2S_LRCLK / PWM [2] / TXD3 / GPIO [3]	61
AC97_BITCLK / I2S_BITCLK / PWM [3] / RXD3 GPIO [4]	62
USB Interface	**(4 pins)**
DP0	7
DN 0	6
DP1	2
DN1	3
Miscellaneous	**(7 pins)**
nIRQ [3:2] / GPIO [19:18]	148,147
nIRQ [1] / GPIO [17] / USB_OVRCUR	44
nIRQ [0] / GPIO [16]	43
nWDOG / GPIO [15] / USB_PWREN	50
RTCVDD18	55

Table 4.1 NUC710 Pin Assignments (Continued)

NAME	176-PIN LQFP
I2C/USI(Microwire/SPI)	**(4 pins)**
SCL0 / SFRM / Timer0 / GPIO [11]	17
SDA0 / SSPTXD / Timer1 / GPIO [12]	18
SCL1 / SCLK / GPIO [13] / KPROW[3]	19
SDA1 / SSPRXD / GPIO [14] / KPROW[2]	20
UART0/UART1/UART2/PS2	**(6 pins)**
TXD0 / GPIO [5]	10
RXD0 / GPIO [6]	11
TXD1 / GPIO [7]	12
RXD1 / GPIO [8]	13
CTS1 / TXD2(IrDA) / PS2_CLK / GPIO [9]	14
RTS1 / RXD2(IrDA) / PS2_DATA / GPIO [10]	15

Table 4.1 NUC710 Pin Assignments (Continued)

NAME	176-PIN LQFP
SCHI/SD/XDMA	**(10 pins)**
SC0_DAT / SD_CMD / GPIO [29] / VD[17]	65
SC0_CLK / SD_CLK / GPIO [28] / VD[16]	66
SC0_RST / SD_DAT0 / GPIO [27] / VD[15]	67
SC0_PRES / SD_DAT1 / GPIO [26] / VD[14]	68
SC0_PWR / SD_DAT2 / GPIO [25] / VD[13]	70
SC1_DAT / SD_DAT3 / GPIO [24] / VD[12]	71
SC1_CLK / GPIO [23] / VD[11]	72
SC1_RST / SD_CD / GPIO [22] / VD[10]	74
SC1_PRES / nXDREQ / GPIO [21] / VD[9]	75
SC1_PWR / nXDACK / GPIO [20] / VD[8]	76

Table 4.1 NUC710 Pin Assignments (Continued)

NAME	176-PIN LQFP
LCDC	**(12 pins)**
VD[7:0] / GPIO [41:34]/ KPCOL[7:0]	27-34
HSYNC / GPIO [33]/ KPROW[3]	26
VSYNC / GPIO [32]/ KPROW[2]	25
VDEN / GPIO [31]/ KPROW[1]	24
VCLK / GPIO [30]/ KPROW[0]	23
Power/Ground	**(36 pins)**
VDD18	21,63,109,160
VSS18	22,38,64,105,157
VDD33	9,35,54,69,85,100, 120,127,139,165
VSS33	16,36,51,73,80,94, 114,126,141,171
USBVDD	1,8
USBVSS	4,5
PLLVDD18	39,42
PLLVSS18	40,41

5. PIN DESCRIPTIONS

Table 5.1 NUC710 Pin Descriptions

PIN NAME	IO TYPE	DESCRIPTION
Clock & Reset		
EXTAL (15M)	I	15MHz External Clock / Crystal Input
XTAL (15M)	O	15MHz Crystal Output
EXTAL32(32.768K)	I	32768Hz External Clock / Crystal Input (for RTC)
XTAL32(32.768K)	O	32768Hz Crystal Output (for RTC)
nRESET	IS	System Reset, active-low
JTAG Interface		
TCK	IDS	JTAG Test Clock, internal pull-down with 58K ohm
TMS	IUS	JTAG Test Mode Select, internal pull-up with 70K ohm
TDI	IUS	JTAG Test Data in, internal pull-up with 70K ohm
TDO	O	JTAG Test Data out
nTRST	IUS	JTAG Reset, active-low, internal pull-up with 70K ohm
External Bus Interface		
A [21:18]	O	Address Bus (MSB) of external memory and IO devices.
A [17:0]	IOS	Address Bus of external memory and IO devices.
D [31:16] / VD[23:8] / GPIO [67:52]	IOU	Data Bus (MSB) of external memory and IO device, internal pull-up with 70K ohm. General Programmable In/Out Port GPIO [67:52].
D [15:0] /	IOU	Data Bus (LSB) of external memory and IO device. The internal pull-up resistors are turned on when D[15:0] is in input mode.
nWBE [3:0] / SDQM [3:0] / GPIO[69:68]	IOU	Write Byte Enable for specific device (nECS [3:0]). Data Bus Mask signal for SDRAM (nSCS [1:0]), active-low. General Programmable In/Out Port [69:68]
nSCS [1:0]	O	SDRAM chip select for two external banks, active-low.
nSRAS	O	Row Address Strobe for SDRAM, active-low.
nSCAS	O	Column Address Strobe for SDRAM, active-low.
nSWE	O	SDRAM Write Enable, active-low
MCKE	O	SDRAM Clock Enable, active-high
MCLK	O	System Master Clock Out, SDRAM clock, output with slew-rate control
nWAIT / GPIO[70] / nIRQ5	IOU	External Wait, active-low. This pin indicates that the external devices need more active cycle during access operation. General Programmable In/Out Port GPIO[70]. If memory and IO devices in EBI do not need a wait request, it can be configured as GPIO[7] or nIRQ5
nBTCS	O	ROM/Flash Chip Select, active-low.
nECS [3:0]	O	External I/O Chip Select, active-low.
nOE	O	ROM/Flash, External Memory Output Enable, active-low.

Table 5.1 NUC710 Pin Descriptions (Continued)

PIN NAME	IO TYPE	DESCRIPTION
Ethernet Interface		
PHY_MDC / GPIO [51] / KPROW[1] / VD[17]	IOU	RMII Management Data Clock for Ethernet. It is the reference clock of MDIO. Each MDIO data will be latched at the positive edge of MDC clock. General Programmable In/Out Port [51] Keypad ROW[1] scan output. LCD Pixel Data Output[17].
PHY_MDIO / GPIO [50] / KPROW[0] / VD[16]	IO	RMII Management Data I/O for Ethernet. It is used to transfer RMII control and status information between PHY and MAC. General Programmable In/Out Port [51] Keypad ROW[0] scan output. LCD Pixel Data Output[16].
PHY_TXD [1:0] / GPIO [49:48] / KPCOL[7:6] / VD[15]	IOU	2-bit Transmit Data bus for Ethernet. General programmable In/Out Port [49:48] Keypad Column input [7:6], active low LCD Pixel Data Output[15].
PHY_TXEN / GPIO [47] / KPCOL[5] / VD[14:13]	IOU	PHY_TXEN shall be asserted synchronously with the first 2-bits of the preamble and shall remain asserted while all di-bits to be transmitted present. Of course, it is synchronized with PHY_REFCLK. General Programmable In/Out Port [47] Keypad column input [5], active low LCD Pixel Data Output[14:13].
PHY_REFCLK / GPIO [46] / KPCOL[4] / VD[12]	IOS	Reference Clock. The clock shall be 50MHz +/- 50 ppm with minimum 35% duty cycle at high or low state. General Programmable In/Out port [46] Keypad column input [4], active low LCD Pixel Data Output[12].
PHY_RXD [1:0] / GPIO [45:44] / KPCOL[3:2] / VD[11:10]	IOS	2-bit Receive Data bus for Ethernet. General Programmable In/Out Port [45:44] Keypad column input [3:2], active low LCD Pixel Data Output[11:10].
PHY_CRSDV / GPIO [43] / KPCOL[1] / VD[9]	IOS	Carrier Sense / Receive Data Valid for Ethernet. The PHY_CRSDV shall be asserted by PHY when the receive medium is non-idle. Loss of carrier shall result in the de-assertion of PHY_CRSDV synchronous to the cycle of PHY_REFCLK, and only on 2-bit receive data boundaries. General Programmable In/Out port [43] Keypad column input [1], active low LCD Pixel Data Output[9].
PHY_RXERR / GPIO [42] / KPCOL[0] / VD[8]	IOS	Receive Data Error for Ethernet indicates a data error detected by PHY. The assertion should last longer than the period of PHY_REFCLK. When PHY_RXERR is asserted, the MAC will report a CRC error. General programmable In/Out port [42] Keypad column input [0], active low LCD Pixel Data Output[8].

Table 5.1 NUC710 Pin Descriptions (Continued)

PIN NAME	IO TYPE	DESCRIPTION
AC97/I2S/PWM/UART3		
AC97_nRESET / I2S_MCLK / GPIO [0] / nIRQ4 / USB_PWREN	IOU	AC97 CODEC Host Interface RESET Output. I2S CODEC Host Interface System Clock Output. General Purpose In/Out port [0] External interrupt request. USB host power enable output
AC97_DATAI / I2S_DATAI / PWM [0] / DTR4 / GPIO [1]	IOU	AC97 CODEC Host Interface Data Input. I2S CODEC Host Interface Data Input. PWM Channel 0 Output. Data Terminal Ready for UART4. General Purpose In /Out port [1]
AC97_DATAO / I2S_DATAO / PWM [1] / DSR4 / GPIO [2]	IOU	AC97 CODEC Host Interface Data Output. I2S CODEC Host Interface Data Output. PWM Channel 1 Output. Data Set Ready for UART4. General Purpose In/Out port [2]
AC97_SYNC / I2S_LRCLK / PWM [2] / TXD4 / GPIO [3]	IOU	AC97 CODEC Host Interface Synchronous Pulse Output. I2S CODEC Host Interface Left/Right Channel Select Clock. PWM Channel 2 Output. Transmit Data for UART4. General Purpose In/Out port [3]
AC97_BITCLK / I2S_BITCLK / PWM [3] / RXD4 / GPIO [4]	IOS	AC97 CODEC Host Interface Bit Clock Input. I2S CODEC Host Interface Bit Clock. PWM Channel 3 Output. Receive Data for UART4. General Purpose In/Out port [4].
USB Interface		
DP0	IO	Differential Positive USB IO signal
DN0	IO	Differential Negative USB IO signal
DP1	IO	Differential Positive USB IO signal
DN1	IO	Differential Negative USB IO signal
Miscellaneous		
nIRQ [3:2] / GPIO [19:18]	IOU	External Interrupt Request General Purpose I/O.
nIRQ [1:0] / GPIO [17:16] USB_OVRCUR	IOU	External Interrupt Request General Purpose I/O nIRQ1 is used as USB host over-current detection input
nWDOG / GPIO [15] / USB_PWREN	IOU	Watchdog Timer Timeout Flag and Keypad 3-keys reset output, active low General Purpose In/output USB host power switch enable output
RTCVDD	P	RTC independent battery power (1.8V)

Table 5.1 NUC710 Pin Descriptions (Continued)

PIN NAME	IO TYPE	DESCRIPTION
I2C/USI(Microwire/SPI)		
SCL0 / SFRM / Timer0 / GPIO [11]	IOU	I2C Serial Clock Line 0. USI Serial Frame. Timer0 time out output. General Purpose In/Out port [11].
SDA0 / SSPTXD / Timer1 / GPIO [12]	IOU	I2C Serial Data Line 0 USI Serial Transmit Data Timer1 time out output General Purpose In/Out port [12]
SCL1 / SCLK / GPIO [13] KPROW[3]	IOU	I2C Serial Clock Line 1 USI Serial Clock General Purpose In/Out port [13] Keypad row scan output [3]
SDA1 / SSPRXD / GPIO [14] / KPROW[2]	IDU	I2C Serial Data Line 1 USI Serial Receive Data General Purpose In/Out port [14] Keypad scan output [2]
UART0/UART1/UART2		
TXD0 / GPIO [5]	IOU	UART0 Transmit Data. General Purpose In/Out [5]
RXD0 / GPIO [6]	IOU	UART0 Receive Data. General Purpose In/Out [6]
TXD1 / GPIO [7]	IOU	UART1 Transmit Data. General Purpose In/Out [7]
RXD1 / GPIO [8]	IOU	UART1 Receive Data. General Purpose In/Out [8]
CTS1/ TXD2(IrDA) / PS2_CLK / GPIO [9]	IOU	UART1 Clear To Send for Bluetooth application UART2 Transmit Data supporting SIR IrDA. PS2 Interface Clock Input/Output General Purpose In/Out [9]
RTS1/ RXD2(IrDA) / PS2_DATA / GPIO [10]	IOU	UART1 Request To Send for Bluetooth application UART2 Receive Data supporting SIR IrDA. PS2 Interface Bi-Directional Data Line. General Purpose In/Out [10]
SCHI/SD/XDMA		
SC0_DAT/ SD_CMD / GPIO [29] / VD[17]	IOU	Smart Card I/O Contact to Card 0. SD Mode – Command/Response; General Purpose In/Out [29] LCD Pixel Data Output[17].
SC0_CLK / SD_CLK / GPIO [28] / VD[16]	IO	Smart Card Clock Output to Card 0. SD Mode – Clock; General Purpose In/Out [28] LCD Pixel Data Output[16].

Table 5.1 NUC710 Pin Descriptions (Continued)

PIN NAME	IO TYPE	DESCRIPTION
SCHI/SD/XDMA		
SC0_RST / SD_DAT0 / GPIO [27] / VD[15]	IO	Smart Card Reset Output to Card 0. SD Mode – Data Line Bit 0; General Purpose In/Out [27] LCD Pixel Data Output[15].
SC0_PRES / SD_DAT1 / GPIO [26] VD[14]	IO	Smart Card 0 Presence Contact Input. SD Mode – Data Line Bit 1. General Purpose In/Out [26] LCD Pixel Data Output[14].]
SC0_nPWR / SD_DAT2 / GPIO [25] / VD[13]	IO	Smart Card 0 Power FET Control Signal Output. SD Mode – Data Line Bit 2. General Purpose In/Out [25] LCD Pixel Data Output[13].
SC1_DAT / SD_DAT3 / GPIO [24] / VD[12]	IO	Smart Card I/O Contact to Card 1. SD Mode – Data Line Bit 3; General Purpose In/Out [24] LCD Pixel Data Output[12].
SC1_CLK / GPIO [23] / VD[11]	IO	Smart Card Clock Output to Card 1. General Purpose In/Out [23] LCD Pixel Data Output[11].
SC1_RST / SD_CD / GPIO [22] / VD[10]	IO	Smart Card Reset Output to Card 1. SD Mode – Card Detect. General Purpose In/Out [22] LCD Pixel Data Output[10].
SC1_PRES / nXDREQ / GPIO [21] / VD[9]	IO	Smart Card 1 Presence Contact Input. External DMA Request. General Purpose In/Out [21] LCD Pixel Data Output[9].
SC1_nPWR / nXDACK / GPIO [20] / VD[8]	IO	Smart Card 1 Power FET Control Signal Output. External DMA Acknowledgement. General Purpose In/Out [20] LCD Pixel Data Output[8].
LCD Interface		
VD [7:0] / GPIO [41:34]/ KPCOL[7:0]	IOU	LCD Pixel Data Output [7:0]. General Purpose In/Out [41:34] Keypad Column input [7:0], active low
HSYNC / GPIO [33]/ KPROW[3]	IOU	Horizontal Sync General Purpose In/Out [33] Keypad ROW[3] scan output.
VSYNC / GPIO [32]/ KPROW[2]	IOU	Vertical Sync General Purpose In/Out [32] Keypad ROW[2] scan output.
VDEN / GPIO [31]/ KPROW[1]	IOU	Data Enable or Display Control Signal. General Purpose In/Out [31] Keypad ROW[1] scan output.

Table 5.1 NUC710 Pins Description (Continued)

PIN NAME	IO TYPE	DESCRIPTION
Power/Ground		
VDD18	P	Core Logic power (1.8V)
VSS18	G	Core Logic ground (0V)
VDD33	P	IO Buffer power (3.3V)
VSS33	G	IO Buffer ground (0V)
USBVDD	P	USB power (3.3V)
USBVSS	G	USB ground (0V)
PLL0_VDD18	P	PLL 0 power (1.8V)
PLL0_VSS18	G	PLL 0 ground (0V)
PLL1_VDD18	P	PLL 1 power (1.8V)
PLL1_VSS18	G	PLL 1 ground (0V)

Table 5.2 NUC710 176-pin LQFP Multi-function List

PIN NO.	DEFAULT	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
USB1.1 Host/Device Interface					
1	**USB1VDD**	USB1VDD	-	-	-
2	**DP1**	DP1	-	-	-
3	**DN1**	DN1	-	-	-
4	**USB1VSS**	USB1VSS	-	-	-
5	**USB0VSS**	USB0VSS	-	-	-
6	**DN0**	DN0	-	-	-
7	**DP0**	DP0	-	-	-
8	**USB0VDD**	USB0VDD	-	-	-
9	**VDD33**	VDD33	-	-	-
UART[2:0]/PS2 Interface					
10	**GPIO[5]**	GPIO[5]	UART_TXD0	-	-
11	**GPIO[6]**	GPIO[6]	UART_RXD0	-	-
12	**GPIO[7]**	GPIO[7]	UART_TXD1	-	-
13	**GPIO[8]**	GPIO[8]	UART_RXD1	-	-
14	**GPIO[9]**	GPIO[9]	UART_TXD2	UART_CTS1	PS2_CLK
15	**GPIO[10]**	GPIO[10]	UART_RXD2	UART_RTS1	PS2_DATA
16	**VSS33**	VSS33	-	-	-
I2C/USI Interface					
17	**GPIO[11]**	GPIO[11]	I2C_SCL0	SSP_FRAM	TIMER0
18	**GPIO[12]**	GPIO[12]	I2C_SDA0	SSP_TXD	TIMER1
19	**GPIO[13]**	GPIO[13]	I2C_SCL1	SSP_RXD	KPROW[2]
20	**GPIO[14]**	GPIO[14]	I2C_SDA1	SSP_SCLK	KPROW[3]
21	**VDD18**	VDD18	-	-	-
22	**VSS18**	VSS18	-	-	-
LCD /KeyPad Interface					
23	**GPIO[30]**	GPIO[30]	LCD_VCLK	KPROW[0]	-
24	**GPIO[31]**	GPIO[31]	LCD_VDEN	KPROW[1]	-
25	**GPIO[32]**	GPIO[32]	LCD_VSYNC	KPROW[2]	-
26	**GPIO[33]**	GPIO[33]	LCD_HSYNC	KPROW[3]	-
27	**GPIO[41]**	GPIO[41]	LCD_VD[7]	KPCOL[7]	-

Table 5.2 NUC710 176-pin LQFP Multi-function List (Continued)

PIN NO.	DEFAULT	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
LCD /Keypad Interface					
28	**GPIO[40]**	GPIO[40]	LCD_VD[6]	KPCOL[6]	-
29	**GPIO[39]**	GPIO[39]	LCD_VD[5]	KPCOL[5]	-
30	**GPIO[38]**	GPIO[38]	LCD_VD[4]	KPCOL[4]	-
31	**GPIO[37]**	GPIO[37]	LCD_VD[3]	KPCOL[3]	-
32	**GPIO[36]**	GPIO[36]	LCD_VD[2]	KPCOL[2]	-
33	**GPIO[35]**	GPIO[35]	LCD_VD[1]	KPCOL[1]	-
34	**GPIO[34]**	GPIO[34]	LCD_VD[0]	KPCOL[0]	-
35	**VDD33**	VDD33	-	-	-
36	**VSS33**	VSS33	-	-	-
System Reset					
37	**nRESET**	nRESET	-	-	-
38	**VSS33**	VSS33	-	-	-
PLL Power/Ground					
39	**PLL0_VDD18**	PLL0_VDD18	-	-	-
40	**PLL0_VSS18**	PLL0_VSS18	-	-	-
41	**PLL1_VSS18**	PLL1_VSS18	-	-	-
42	**PLL1_VDD18**	PLL1_VDD18	-	-	-
External IRQ[1:0]/USB Over Current					
43	**GPIO[16]**	GPIO[16]	nIRQ[0]	-	-
44	**GPIO[17]**	GPIO[17]	nIRQ[1]	USB_OVRCUR	-
JTAG Interface					
45	**TMS**	TMS	-	-	-
46	**TDI**	TDI	-	-	-
47	**TDO**	TDO	-	-	-
48	**TCK**	TCK	-	-	-
49	**nTRST**	nTRST	-	-	-
Watchdog/USB Power Enable					
50	**GPIO[15]**	GPIO[15]	nWDOG	USB_PWREN	-
51	**VSS33**	VSS33	-	-	-

Table 5.2 NUC710 176-pin LQFP Multi-function List (Continued)

PIN NO.	DEFAULT	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
System/RTC Clock					
52	**EXTAL(15M)**	EXTAL(15M)	-	-	-
53	**XTAL(15M)**	XTAL(15M)	-	-	-
54	**VDD33**	VDD33	-	-	-
55	**RTCVDD18**	RTCVDD18	-	-	-
56	**XTAL32 (32K)**	XTAL32 (32K)	-	-	-
57	**EXTAL32 (32K)**	EXTAL32 (32K)	-	-	-
AC97/I2S/PWM/UART3 Interface					
58	**GPIO[0]**	GPIO[0]	AC97_nRESET	IRQ4	USB_PWREN
59	**GPIO[1]**	GPIO[1]	AC97_DATAI	PWM0	UART_DTR3
60	**GPIO[2]**	GPIO[2]	AC97_DATAO	PWM1	UART_DSR3
61	**GPIO[3]**	GPIO[3]	AC97_SYNC	PWM2	UART_TXD3
62	**GPIO[4]**	GPIO[4]	AC97_BITCLK	PWM3	UART_RXD3
63	**VDD18**	VDD18	-	-	-
64	**VSS18**	VSS18	-	-	-
Smartcard/SD/USB Power/XDMAREQ/LCD Interface					
65	**GPIO[29]**	GPIO[29]	SD_CMD	SC0_IO	LCD_VD[17]
66	**GPIO[28]**	GPIO[28]	SD_CLK	SC0_CLK	LCD_VD[16]
67	**GPIO[27]**	GPIO[27]	SD_DAT[0]	SC0_RST	LCD_VD[15]
68	**GPIO[26]**	GPIO[26]	SD_DAT[1]	SC0_PRES	LCD_VD[14]
69	**VDD33**	VDD33			
70	**GPIO[25]**	GPIO[25]	SD_DAT[2]	SC0_PWR	LCD_VD[13]
71	**GPIO[24]**	GPIO[24]	SD_DAT[3]	SC1_IO	LCD_VD[12]
72	**GPIO[23]**	GPIO[23]	USBPWREN	SC1_CLK	LCD_VD[11]
73	**VSS33**	VSS33			
74	**GPIO[22]**	GPIO[22]	SD_CD	SC1_RST	LCD_VD[10]
75	**GPIO[21]**	GPIO[21]	nXQREQ	SC1_PRES	LCD_VD[9]
76	**GPIO[20]**	GPIO[20]	nXDACK	SC1_PWR	LCD_VD[8]

Table 5.2 NUC710 176-pin LQFP Multi-function List (Continued)

PIN NO.	DEFAULT	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
Ethernet RMII/Keypad Interface					
77	**GPIO[42]**	GPIO[42]	PHY_RXERR	KPCOL[0]	LCD_VD[8]
78	**GPIO[43]**	GPIO[43]	PHY_CRSDV	KPCOL[1]	LCD_VD[9]
79	**GPIO[44]**	GPIO[44]	PHY_RXD[0]	KPCOL[2]	LCD_VD[10]
80	**VSS33**	VSS33	-	-	-
81	**GPIO[45]**	GPIO[45]	PHY_RXD[1]	KPCOL[3]	LCD_VD[11]
82	**GPIO[46]**	GPIO[46]	PHY_REFCLK	KPCOL[4]	LCD_VD[12]
83	**GPIO[47]**	GPIO[47]	PHY_TXEN	KPCOL[5]	LCD_VD[13]
84	**GPIO[48]**	GPIO[48]	PHY_TXD[0]	KPCOL[6]	LCD_VD[14]
85	**VDD33**	VDD33	-	-	
86	**GPIO[49]**	GPIO[49]	PHY_TXD[1]	KPCOL[7]	LCD_VD[15]
87	**GPIO[50]**	GPIO[50]	PHY_MDIO	KPROW[0]	LCD_VD[16]
88	**GPIO[51]**	GPIO[51]	PHY_MDC	KPROW[1]	LCD_VD[17]
Memory Address/Data/Control					
89	**A[0]**	A[0]	-	-	-
90	**A[1]**	A[1]	-	-	-
91	**A[2]**	A[2]	-	-	-
92	**A[3]**	A[3]	-	-	-
93	**A[4]**	A[4]	-	-	-
94	**VSS33**	VSS33	-	-	-
95	**A[5]**	A[5]	-	-	-
96	**A[6]**	A[6]	-	-	-
97	**A[7]**	A[7]	-	-	-
98	**A[8]**	A[8]	-	-	-
99	**A[9]**	A[9]	-	-	-
100	**VDD33**	VDD33	-	-	-
101	**A[10]**	A[10]	-	-	-
102	**A[11]**	A[11]	-	-	-
103	**A[12]**	A[12]	-	-	-
104	**A[13]**	A[13]	-	-	-

Table 5.2 NUC710 176-pin LQFP Multi-function List (Continued)

PIN NO.	DEFAULT	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
Memory Address/Data/Control					
105	**VSS18**	VSS18	-	-	-
106	**A[14]**	A[14]	-	-	-
107	**A[15]**	A[15]	-	-	-
108	**A[16]**	A[16]	-	-	-
109	**VDD18**	VDD18	-	-	-
110	**A[17]**	A[17]	-	-	-
111	**A[18]**	A[18]	-	-	-
112	**A[19]**	A[19]	-	-	-
113	**A[20]**	A[20]	-	-	-
114	**VSS33**	VSS33	-	-	-
115	**A[21]**	A[21]	-	-	-
116	**D[31]**	GPIO[67]	D[31]	LCD_VD[23]	-
117	**D[30]**	GPIO[66]	D[30]	LCD_VD[22]	-
118	**D[29]**	GPIO[65]	D[29]	LCD_VD[21]	-
119	**D[28]**	GPIO[64]	D[28]	LCD_VD[20]	-
120	**VDD33**	VDD33	-	-	-
121	**D[27]**	GPIO[63]	D[27]	LCD_VD[19]	-
122	**D[26]**	GPIO[62]	D[26]	LCD_VD[18]	-
123	**D[25]**	GPIO[61]	D[25]	LCD_VD[17]	-
124	**D[24]**	GPIO[60]	D[24]	LCD_VD[16]	-
125	**nECS[3]**	nECS[3]	-	-	-
126	**VSS33**	VSS33	-	-	-
127	**VDD33**	VDD33	-	-	-
128	**nECS[2]**	nECS[2]	-	-	-
129	**nECS[1]**	nECS[1]	-	-	-
130	**nECS[0]**	nECS[0]	-	-	-
131	**nOE**	nOE	-	-	-
132	**nWAIT**	GPIO[71]	nWAIT	IRQ5	-
133	**nBTCS**	nBTCS	-	-	-
134	**MCKE**	MCKE	-	-	-

Table 5.2 NUC710 176-pin LQFP Multi-function List (Continued)

PIN NO.	DEFAULT	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
Memory Address/Data/Control					
135	**nSCS[0]**	nSCS[0]	-	-	-
136	**nSCS[1]**	nSCS[1]	-	-	-
137	**nSRAS**	nSRAS	-	-	-
138	**nSCAS**	nSCAS	-	-	-
139	**VDD33**	VDD33	-	-	-
140	**MCLK**	MCLK	-	-	-
141	**VSS33**	VSS33	-	-	-
142	**nWE**	nWE	-	-	-
143	**nWBE_SDQM[0]**	nWBE_SDQM[0]	-	-	-
144	**nWBE_SDQM[1]**	nWBE_SDQM[1]	-	-	-
145	**nWBE_SDQM[2]**	GPIO[68]	nWBE_SDQM[2]	-	-
146	**nWBE_SDQM[3]**	GPIO[69]	nWBE_SDQM[3]	-	-
147	**GPIO[18]**	GPIO[18]	nIRQ[2]	-	-
148	**GPIO[19]**	GPIO[19]	nIRQ[3]	-	-
149	**GPIO[59]**	GPIO[59]	D[23]	LCD_VD[15]	-
150	**D[22]**	GPIO[58]	D[22]	LCD_VD[14]	-
151	**D[21]**	GPIO[57]	D[21]	LCD_VD[13]	-
152	**D[20]**	GPIO[56]	D[20]	LCD_VD[12]	-
152	**D[20]**	GPIO[56]	D[20]	LCD_VD[12]	-
153	**D[19]**	GPIO[55]	D[19]	LCD_VD[11]	-
154	**D[18]**	GPIO[54]	D[18]	LCD_VD[10]	-
155	**D[17]**	GPIO[53]	D[17]	LCD_VD[9]	-
156	**D[16]**	GPIO[52]	D[16]	LCD_VD[8]	-
157	**VSS18**	VSS18	-	-	-
158	**D[15]**	D[15]	-	-	-
159	**D[14]**	D[14]	-	-	-
160	**VDD18**	VDD18	-	-	-
161	**D[13]**	D[13]	-	-	-
162	**D[12]**	D[12]	-	-	-

Table 5.2 NUC710 176-pin LQFP Multi-function List (Continued)

PIN NO.	DEFAULT	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
Memory Address/Data/Control					
163	**D[11]**	D[11]	-	-	-
164	**D[10]**	D[10]	-	-	-
165	**VDD33**	VDD33	-	-	-
166	**D[9]**	D[9]	-	-	-
167	**D[8]**	D[8]	-	-	-
168	**D[7]**	D[7]	-	-	-
169	**D[6]**	D[6]	-	-	-
170	**D[5]**	D[5]	-	-	-
171	**VSS33**	VSS33	-	-	-
172	**D[4]**	D[4]	-	-	-
173	**D[3]**	D[3]	-	-	-
174	**D[2]**	D[2]	-	-	-
175	**D[1]**	D[1]	-	-	-
176	**D[0]**	D[0]	-	-	-

6. ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings

Ambient temperature	-40 °C ~ +85°C
Storage temperature	-50 °C ~ +125°C
Voltage on any pin	-0.5V ~ 6V
Power supply voltage (Core logic)	-0.5V ~ 1.92V
Power supply voltage (IO Buffer)	-0.5V ~ 3.6V
Injection current (latch-up testing)	100mA
Crystal Frequency	4MHz ~ 30MHz

6.2 DC Specifications

6.2.1 Digital DC Characteristics

(Normal test conditions: VDD33/USBVDD = 3.3V+/- 0.3V, VDD18/DVDD18/AVDD18 = 1.8V+/- 0.18V TA = -40 °C ~ +85 °C unless otherwise specified)

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
VDD33/ USB1VDD USB2VDD	Power Supply		3.00	3.60	V
VDD18/ DVDD18/ AVDD18/ RTCVDD18	Power Supply		1.62	1.98	V
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{IH}	Input High Voltage		2.0	5.5	V
VT+	Schmitt Trigger positive-going threshold		1.47	1.5	V
VT-	Schmitt trigger negative-going threshold		0.89	0.95	V
V_{OL}	Output Low Voltage	Depend on driving	-	0.4	V
V_{OH}	Output High Voltage	Depend on driving	2.4	-	V
I_{CC1}	1.8V Supply Current	F_{CPU} = 80MHz	120(1)		mA
ICC2	3.3V Supply Current	F_{CPU} = 80MHz	40(1)		mA
I_{CCRTC}	RTC 1.8V Supply Current	F_{RTC} = 32.768KHZ	-	7	uA

Digital DC Characteristics, continued

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
IPD1	1.8V Supply Current, Power down mode		11(2)	-	uA
IPD2	3.3V Supply Current, Power down mode	All IOs are connected to 3.3V or 0V	1(3)	-	uA
I_{IH}	Input High Current	V_{IN} = 2.4 V	-1	1	μA
I_{IL}	Input Low Current	V_{IN} = 0.4 V	-1	1	μA
I_{IHP}	Input High Current (pull-up)	V_{IN} = 2.4 V	-15	-10	μA
I_{ILP}	Input Low Current (pull-up)	V_{IN} = 0.4 V	-55	-25	μA
I_{IHD}	Input High Current (pull-down)	V_{IN} = 2.4 V	25	60	μA
I_{ILD}	Input Low Current (pull-down)	V_{IN} = 0.4 V	5	10	μA

NOTE:
1. The operation current is measured in room temperature and run SDRAM read/write test program only.
   All IPs' clocks are enabled.
2. Both USB transceivers are disabled and D15-D8 for power-on setting are connected to 3.3V

Table 7.2.1TSMC IO DC Characteristics

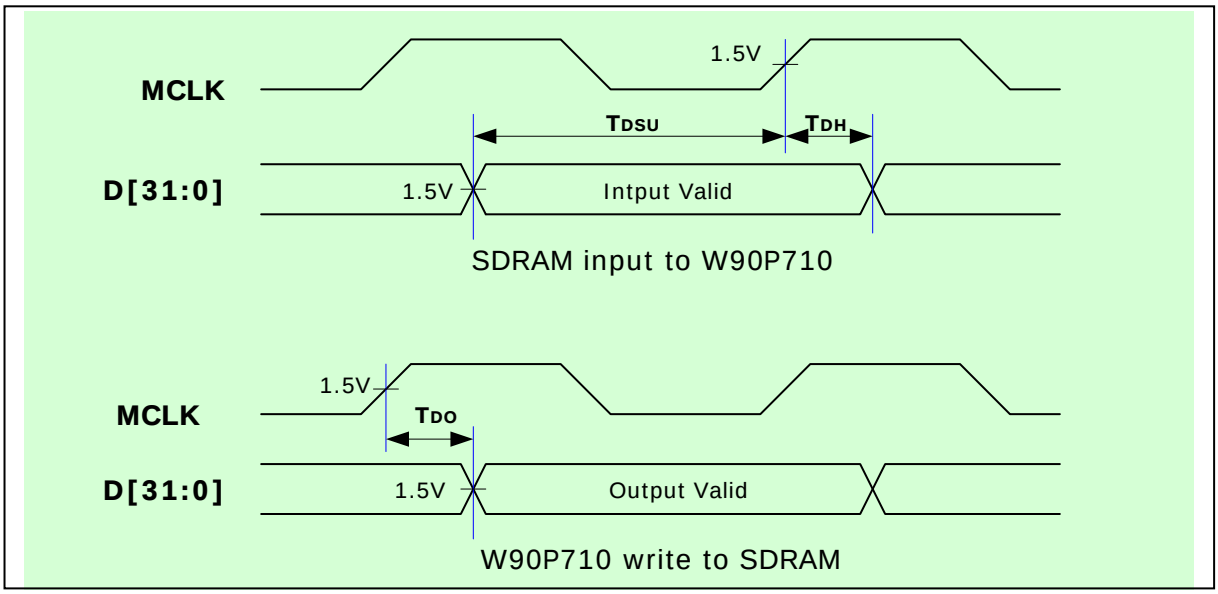
PARAMETER		MIN.	TYP.	MAX.
V_{IL}	Input Low Voltage	-0.3V		0.8V
V_{IH}	Input High Voltage	2V		5.5V
V_T	Threshold point	1.46V	1.59V	1.75V
V_{T+}	Schmitt trig low to high threshold point	1.47V	1.50V	1.50V
V_{T-}	Schmitt trig, high to low threshold point	0.90V	0.94V	0.96V
I_I	Input leakage current @V_I= 3.3V or 0V			+/- 10uA
I_{oz}	Tri-state output leakage current @Vo =3.3V or 0V			+/- 10UA
R_{PU}	Pull-up resistor	44KΩ	66KΩ	110KΩ
R_{PD}	Pull-down resistor	25KΩ	50KΩ	110KΩ
V_{OL}	Output low voltage @$_{IOL}$(min)			0.4V
V_{OH}	Output high voltage @I_{OH} (min)	2.4V		
I_{OL}	Low level output current @V_{OL} = 0.4V 4mA	4.9mA	7.4mA	9.8mA
	Low level output current @V_{OL} = 0.4V 8mA	9.7mA	14.9mA	19.5mA
	Low level output current @V_{OL} = 0.4V 12mA	14.6mA	22.3mA	29.3mA
I_{OH}	High level output current @V_{OH} = 2.4V 4mA	6.3mA	12.8mA	21.2mA
	High level output current @V_{OH} = 2.4V 8mA	12.7mA	25.6mA	42.4mA
	High level output current @V_{OH} = 2.4V 12mA	19.0mA	38.4mA	63.6mA
NOTE: The values in this table are copied from TSMC 1P5M IO library tpz937g_240b silicon report. This table is just for reference. For a more precise DC value, refer to the Alpha-Test result.				

6.2.2 USB Transceiver DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DI}	Differential Input Sensitivity	|DP – DM|	0.2		V
V_{CM}	Differential Common Mode Range	Includes V_{DI} range	0.8	2.5	V
V_{SE}	Single Ended Receiver Threshold		0.8	2.0	V
V_{OL}	Static Output Low Voltage	RL of 1.5 KΩ to 3.6 V		0.3	V
V_{OH}	Static Output High Voltage	RL of 15 KΩ to VSS	2.8	3.6	V
V_{CRS}	Output Signal Crossover Voltage		1.3	2.0	V
Z_{DRV}	Driver Output Resistance	Steady state drive	28	43	Ω
C_{IN}	Pin Capacitance			20	pF

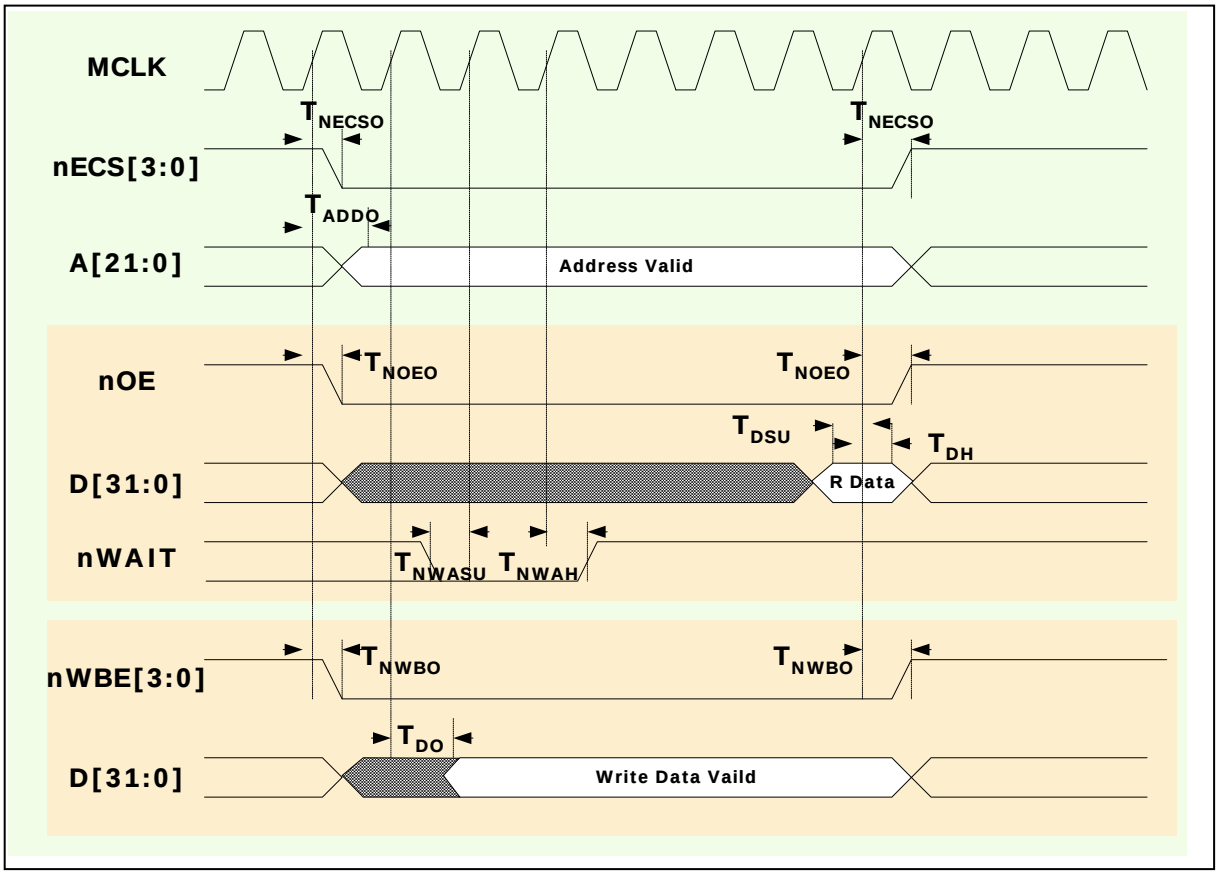
6.3 AC Specifications

6.3.1 EBI/SDRAM Interface AC Characteristics



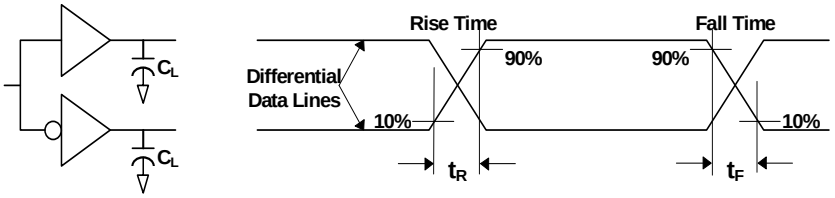
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_{DSU}	D [31:0] Setup Time	2		ns
T_{DH}	D [31:0] Hold Time	2		ns
T_{DO}	D [31:0], A [24:0], nSCS [1:0], SDQM [3:0], CKE, nSWE, nSRAS, nSCAS	2	7	ns

6.3.2 EBI/(ROM/SRAM/External I/O) AC Characteristics



SYMBOL	DESCRIPTION	MIN	MAX	UNIT
T_{ADDO}	Address Output Delay Time	2	7	ns
T_{NCSO}	ROM/SRAM/Flash or External I/O Chip Select Delay Time	2	7	ns
T_{NOEO}	ROM/SRAM or External I/O Bank Output Enable Delay	2	7	ns
T_{NWBO}	ROM/SRAM or External I/O Bank Write Byte Enable Delay	2	7	ns
T_{DH}	Read Data Hold Time	0		ns
T_{DSU}	Read Data Setup Time	7		ns
T_{DO}	Write Data Output Delay Time (SRAM or External I/O)	2	7	ns
T_{NWASU}	External Wait Setup Time	3		ns
T_{NWAH}	External Wait Hold Time	1		ns

6.3.3 USB Transceiver AC Characteristics



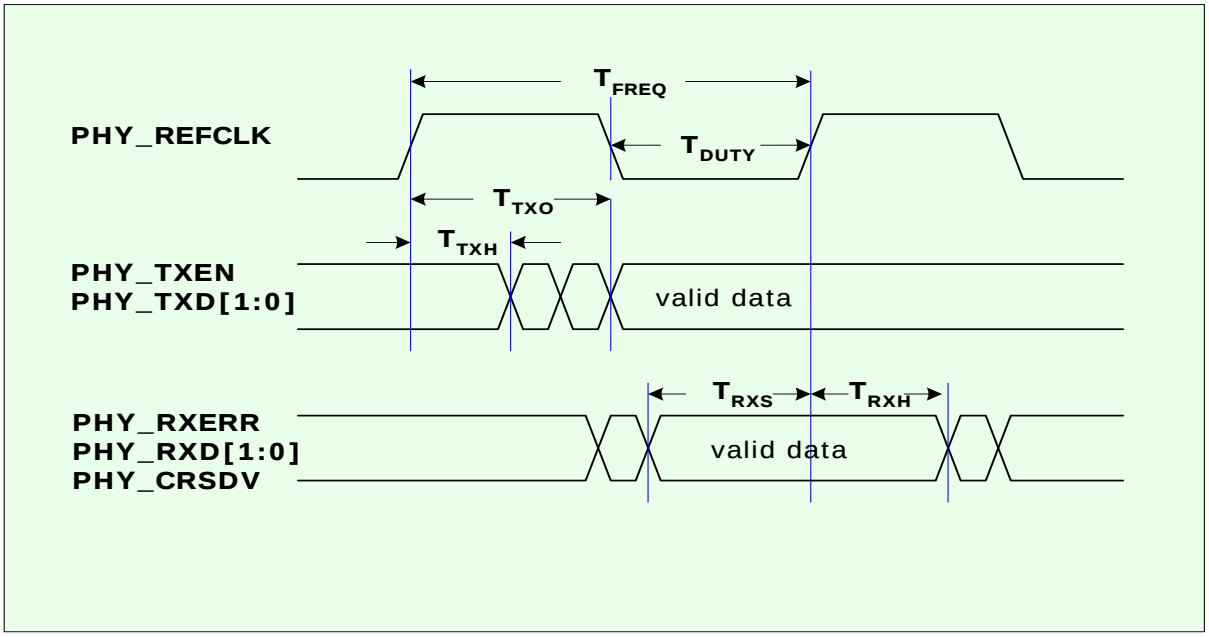
Data Signal Rise and Fall Time

USB Transceiver AC Characteristics

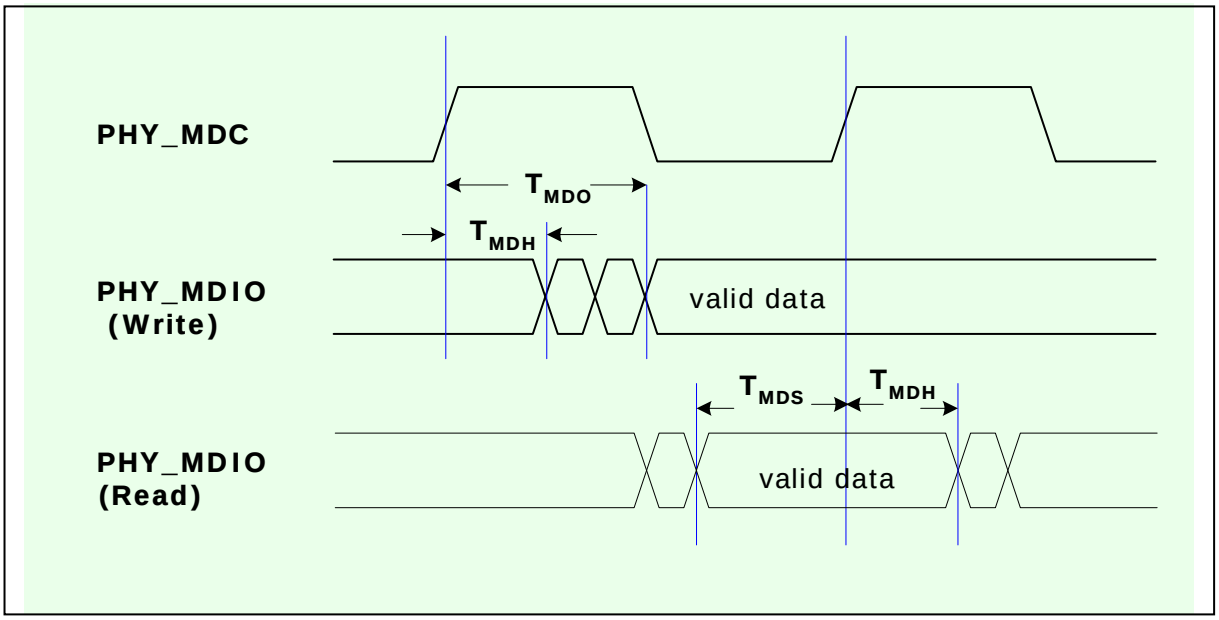
SYMBOL	DESCRIPTION	CONDITIONS	MIN	MAX	UNIT
T_R	Rise Time	CL = 50 pF	4	20	ns
T_F	Fall Time	CL = 50 pF	4	20	ns
T_{RFM}	Rise/Fall Time Matching		90	110	%
T_{DRATE}	Full Speed Data Rate	Average bit rate (12 Mb/s ± 0.25%)	11.97	12.03	Mbps

6.3.4 EMC RMII AC Characteristics

Signal timing characteristics conforms to guidelines specified in IEEE Std. 802.3.

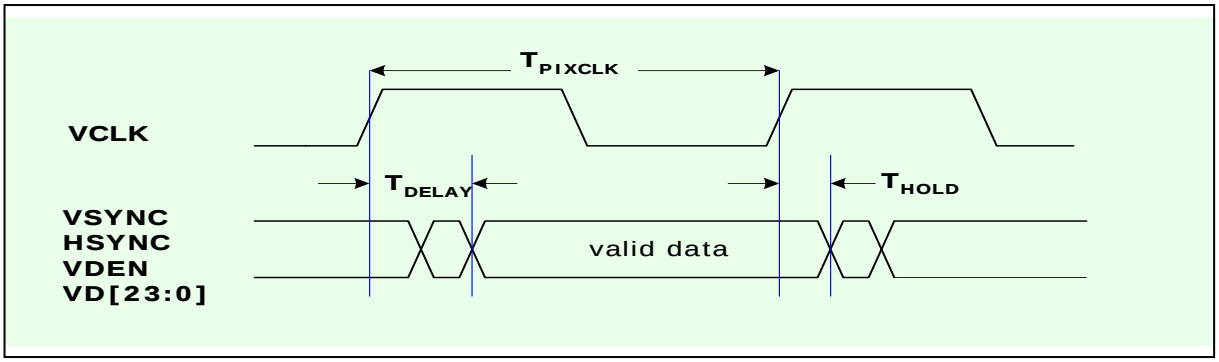


SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{FREQ}	RMII reference clock frequency		50		MHz
T_{DUTY}	RMII clock duty	35%	50%	65%	ns
T_{TXO}	Transmit data output delay	5	-	15	ns
T_{TXH}	Transmit data hold time	2	-	-	ns
T_{RXS}	Receive data setup time	4	-	-	ns
T_{RXH}	Receive data hold time	2	-	-	ns



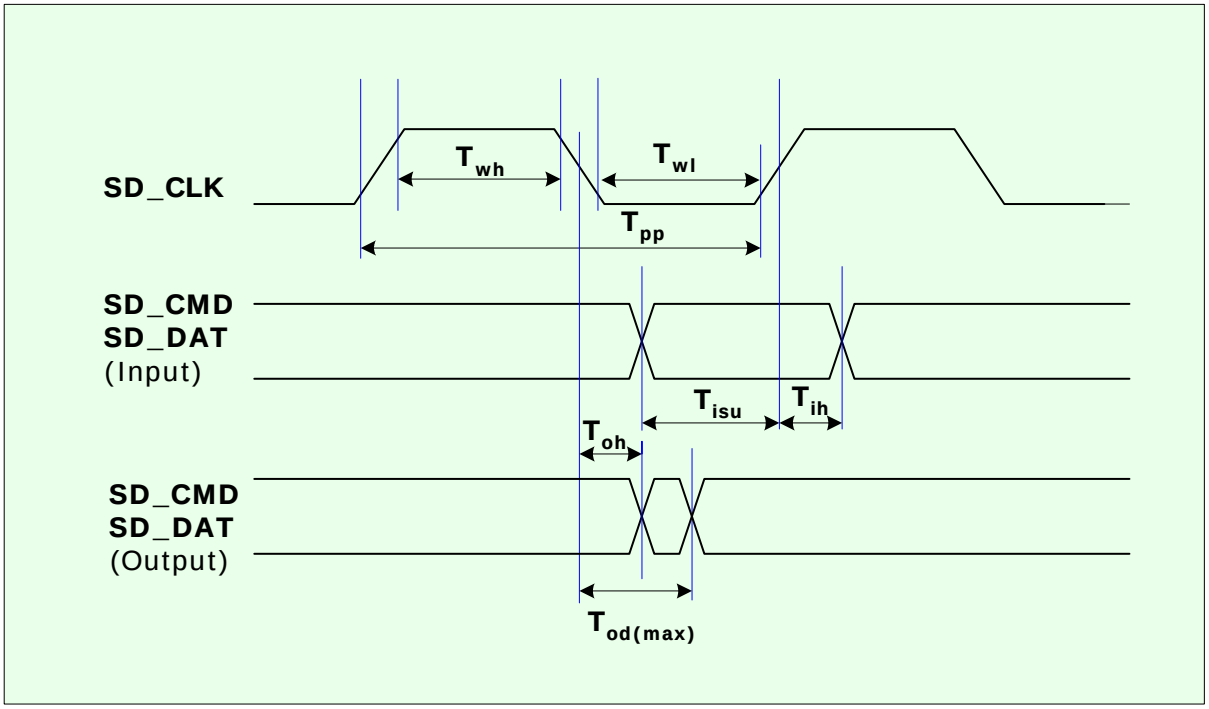
SYMBOL	DESCRIPTION	MIN	MAX	UNIT
T_{MDO}	MDIO Output Delay Time	0	15	ns
T_{MDSU}	MDIO Setup Time	5		ns
T_{MDH}	MDIO Hold Time	5		ns

6.3.5 LCD Interface AC Characteristics



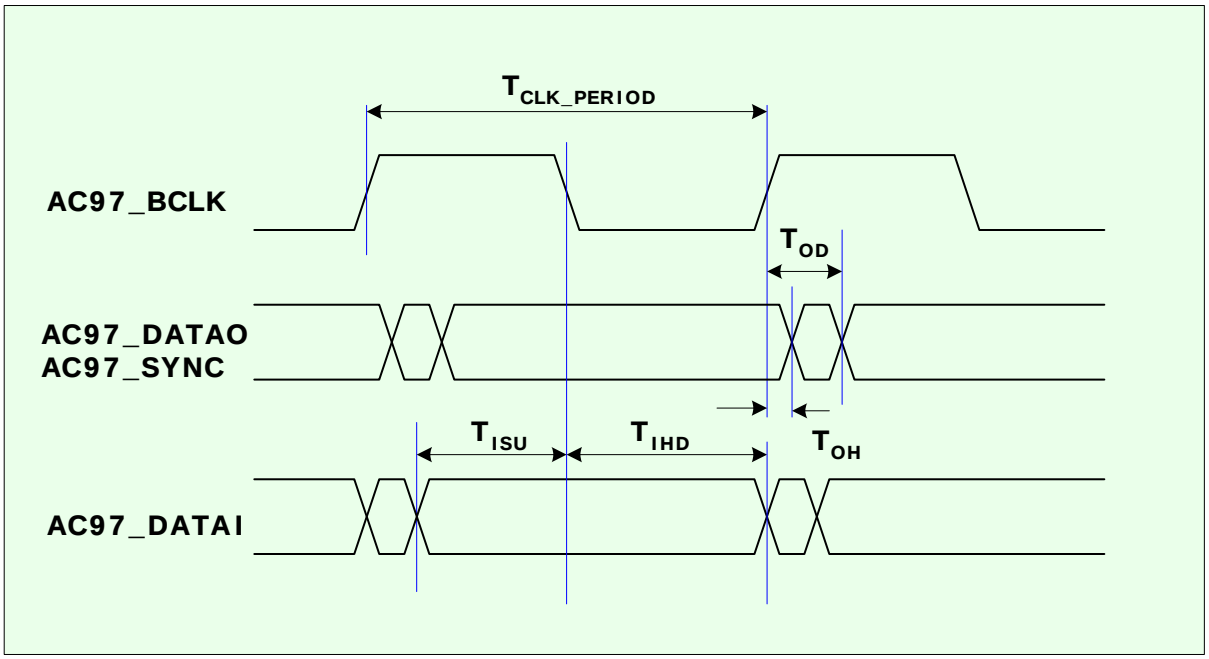
SYMBOLS	DESCRIPTION	MIN	MAX	UNIT
T_{PIXCLK}	Pixel clock frequency	-	40	MHz
T_{DELAY}	VSYNC, HSYNC, VDEN and VD [23:0] output delay from VCLK rising edge	5	15	ns
T_{HOLD}	VSYNC, HSYNC, VDEN and VD [23:0] output data hold time from VCLK rising edge	0	5	ns

6.3.6 SD Interface AC Characteristics

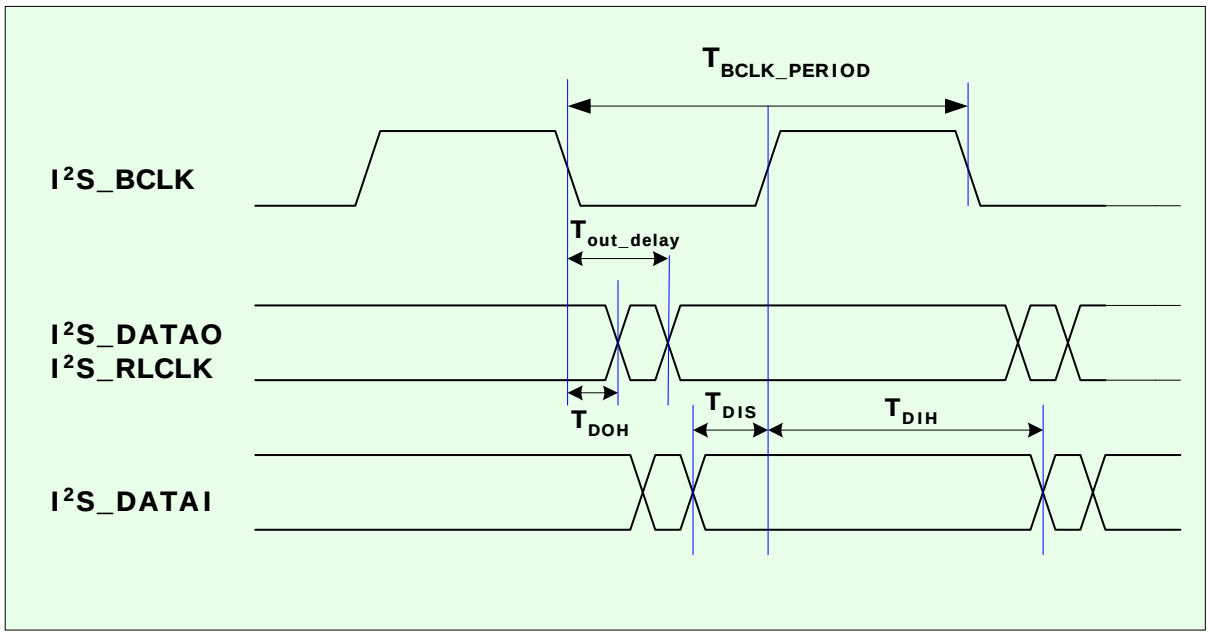


SYMBOLS	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
T_{pp}	SD Clock Frequency	--	--	20	MHz
T_{wh}	SD Clock High Time	10	--	--	ns
T_{wl}	SD Clock Low Time	10	--	--	ns
Input CMD, DAT (reference to SD_CLK rising edge)					
T_{isu}	Input Setup Time	5	--	--	ns
T_{ih}	Input Hold Time	5	--	--	ns
Output CMD, DAT (reference to SD_CLK falling edge)					
T_{od}	Output Delay Time	0	--	14	ns

6.3.7 AC97/I2S Interface AC Characteristics

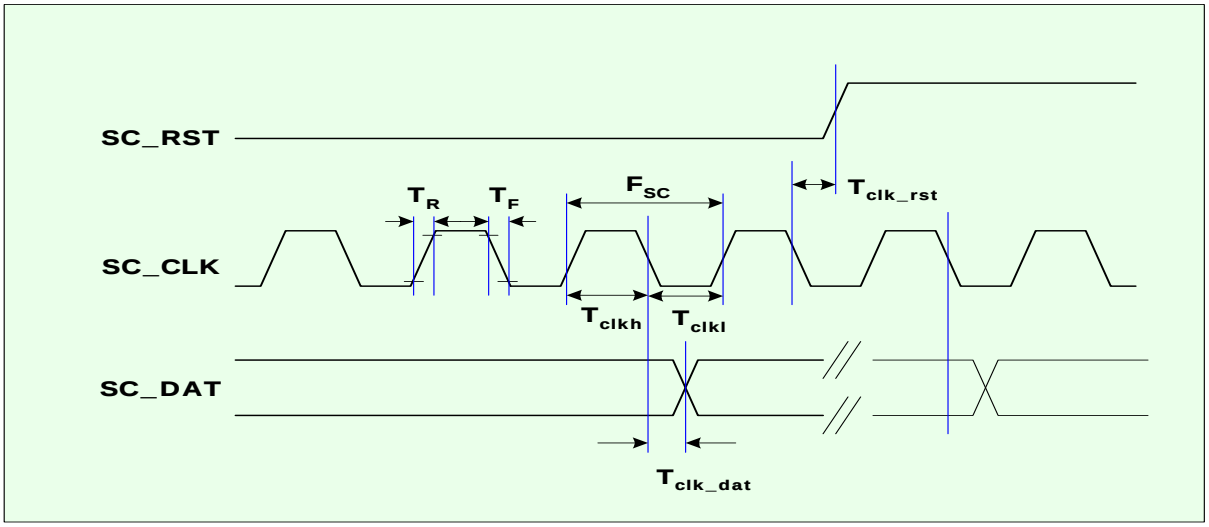


SYMBOLS	DESCRIPTION	MIN	TYP.	MAX	UNIT
T_{CLK_PERIOD}	AC97 Bit Clock Frequency	--	12.288	--	MHz
T_{OD}	AC97_DATAO and AC97_SYNC output delay from AC97_BCLK rising edge	--	--	30	ns
T_{OH}	AC97_DATAO and AC97_SYNC output hold time from AC97_BCLK rising edge	5	--	--	ns
T_{ISU}	AC97_DATAI input setup time to AC97_BCLK falling edge	10	--	--	ns
T_{IHD}	AC97_DATAI input hold time from AC97_BCLK falling edge	5	--	--	ns



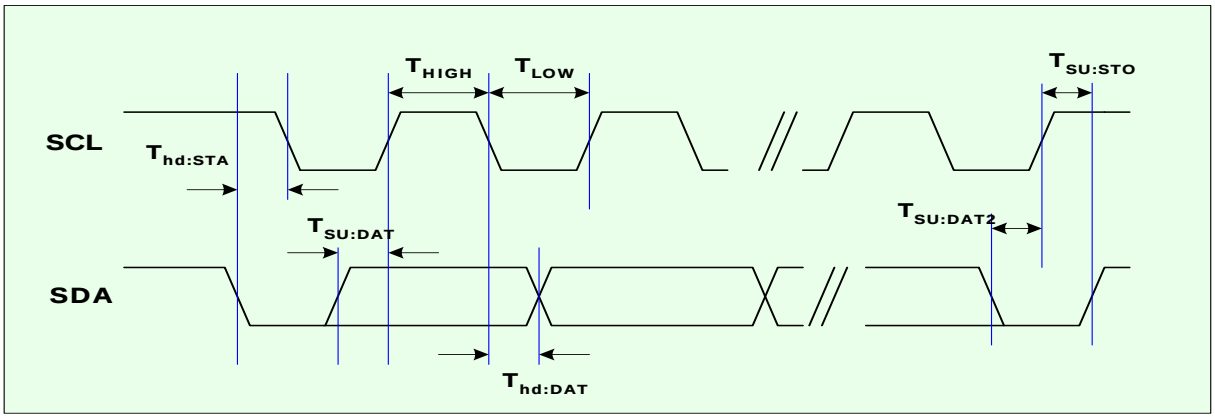
SYMBOLS	DESCRIPTION	MIN	MAX	UNIT
T_{BCLK_PERIOD}	IIS Bit Clock Frequency	Note: depending on codec specifications. and register settings		MHz
T_{out_delay}	IIS_DATAO and IIS_RLCLK output delay from IIS_BCLK falling edge	--	30	ns
T_{DOH}	IIS_DATAO and IIS_RLCLK data output hold time from IIS_BCLK falling edge	0	--	ns
T_{DIS}	IIS_DATAI input setup time to IIS_BCLK rising edge	10	--	ns
T_{DIH}	IIS_DATAI input hold time from IIS_BCLK rising edge	100	--	ns

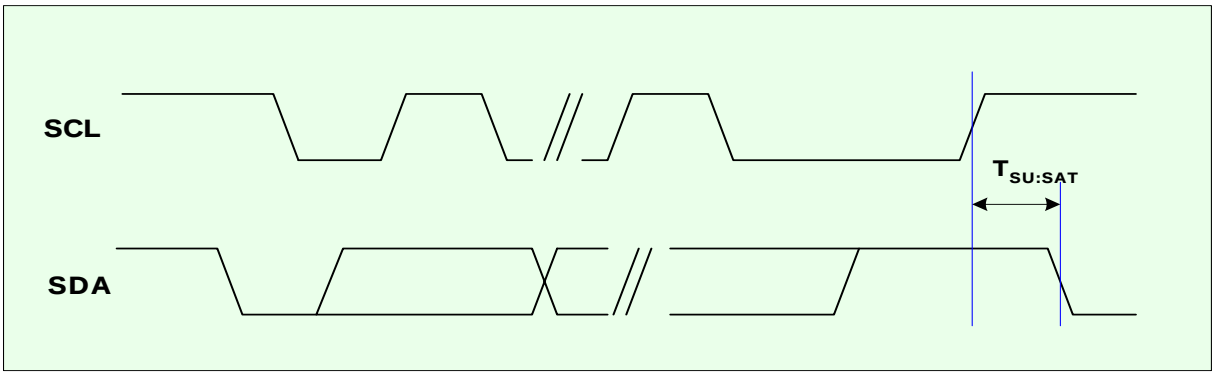
6.3.8 Smart Card Interface AC Characteristics



SYMBOL	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
T_R and T_F for RST	Rising and falling time of RST signal	CL = 30pF (Max)			0.8	us
T_R and T_F for CLK	Rising and falling time of CLK signal	CL = 30pF (Max)	4		8% of clock period	
T_R and T_F for DAT (Transmit)	Rising and falling time of DAT signal in transmission mode	CL = 30pF (Max)			0.8	us
T_R and T_F for DAT (Receive)	Rising and falling time of DAT signal in receive mode				1.2	us
F_{SC}	Smart card clock frequency		1	2.5	20	MHz
T_{clkh}	Smart card clock high time		40%	50%	60%	clock
T_{clkl}	Smart card clock low time		40%	50%	60%	clock
T_{clk_dat}	DAT output delay from SC_CLK falling edge		5	-	20	ns
T_{clk_rst}	RST output delay from SC_CLK falling edge		5	-	10	ns

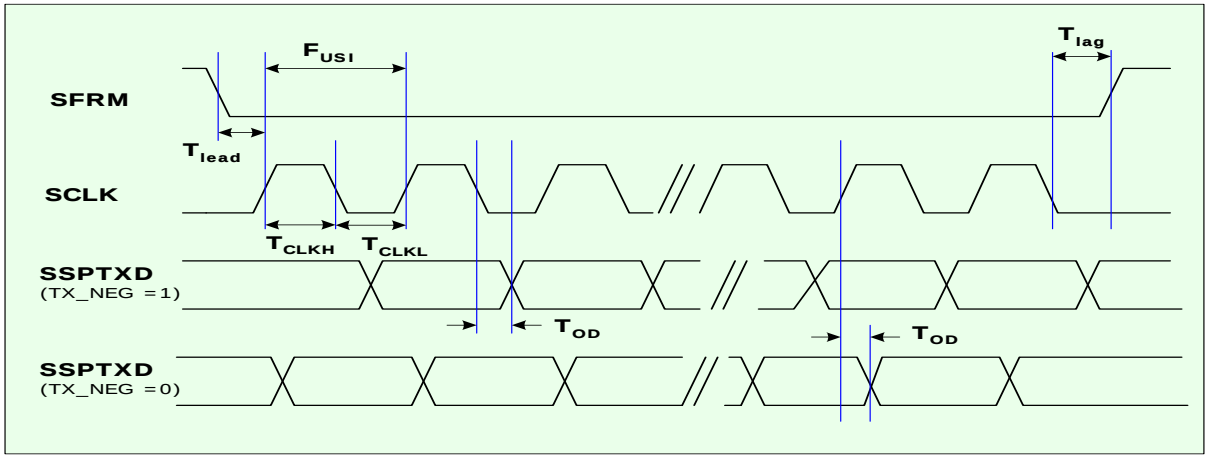
6.3.9 I2C Interface AC Characteristics

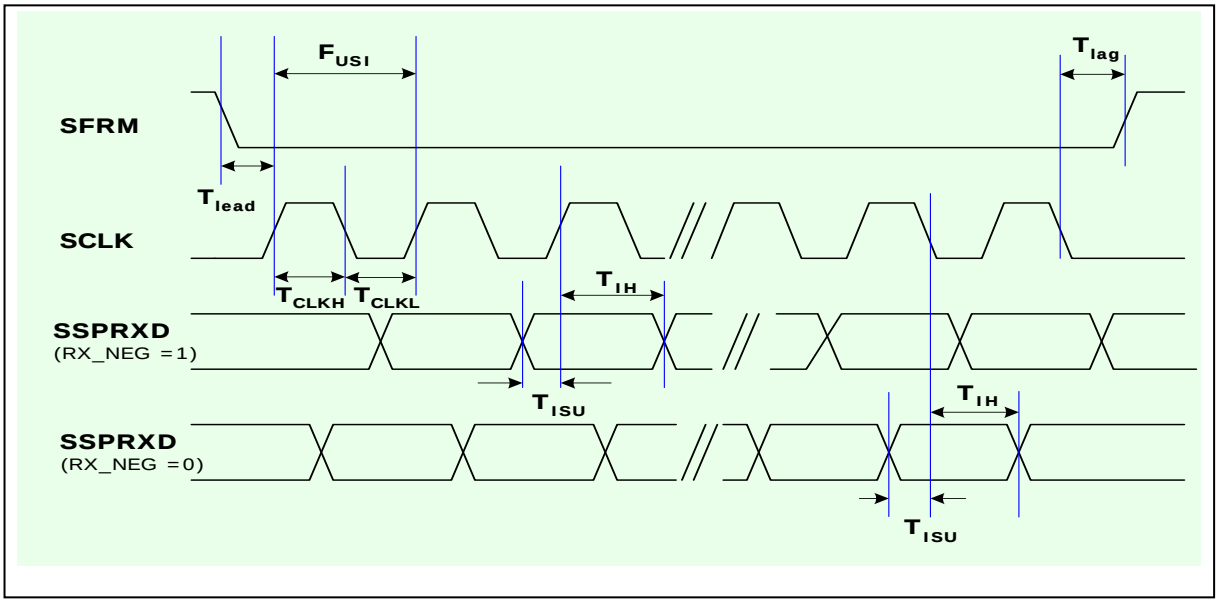




SYMBOL	DESCRIPTION	MIN	MAX	UNIT
T_{HIGH}	I^2C Clock high time	1	-	us
T_{LOW}	I^2C clock low time	1	-	us
$T_{hd:STA}$	Start condition hold time	1	-	us
$T_{SU:DAT}$	Receive data setup time	0.1	-	us
	Transmit data output delay	-	0.5	us
$T_{HD:DAT}$	Receive data hold time	1	-	us
	Transmit data hold time	0	0.9	us
$T_{SU:DAT2}$	SDA setup time (before STOP condition)	0.5	-	us
$T_{SU:STO}$	Stop condition setup time	1	-	us
$T_{SU:STA}$	Restart condition setup time	1.5	-	us

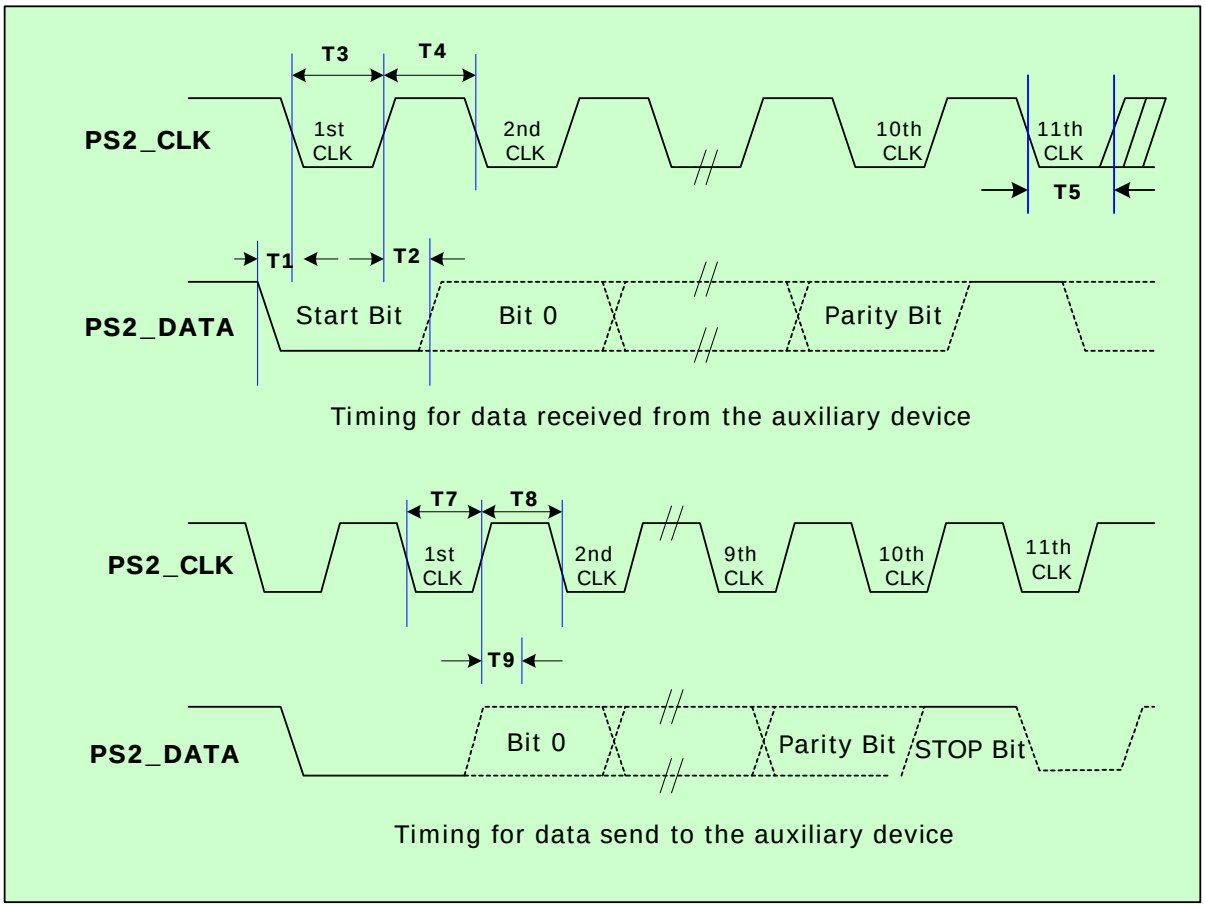
6.3.10 USI Interface AC Characteristics





SYMBOL	DESCRIPTION	MIN	MAX	UNIT
F_{USI}	USI clock frequency	-	20	MHz
T_{CLKH}	USI clock high time	12.5	-	ns
T_{CLKL}	USI clock low time	-	-	ns
T_{ISU}	Data input setup time	-	14	ns
T_{IH}	Data input hold time	0	-	ns
T_{lead}	USI enable lead time	12.5	-	ns
T_{lag}	USI enable lag time	12.5	-	ns
T_{OD}	USI output data valid time	-	30	ns

6.3.11 PS2 Interface AC Characteristics



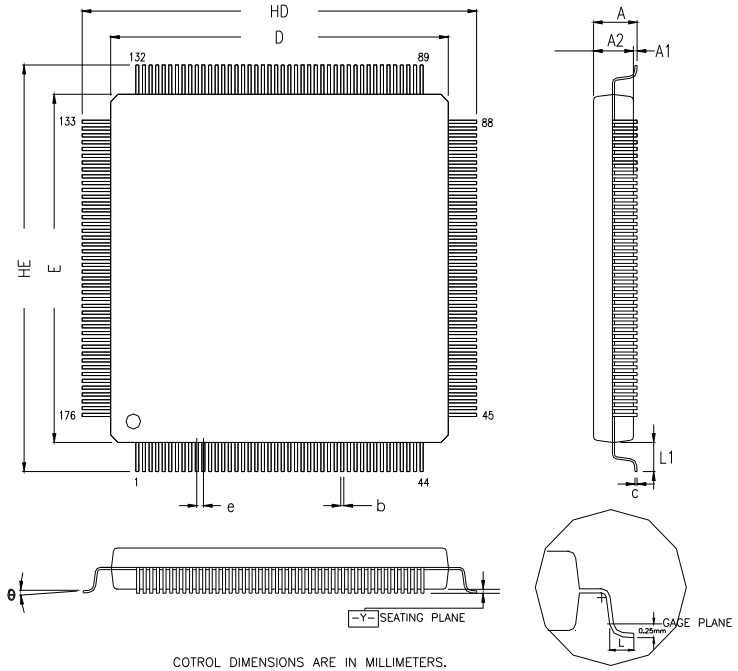
SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T1	Time from DATA transition to falling edge of CLK	5	25	us
T2	Time form rising edge of CLK to DATA transition	5	T4-5	us
T3	Duration of CLK inactive	30	50	us
T4	Duration of clock active	30	50	us
T5	Time to auxiliary device inhibit after clock 11 to ensure the auxiliary device does not start another transmission	0	50	us
T7	Duration of CLK inactive	30	50	us
T8	Duration of CLK active	30	50	us
T9	Time from inactive to active CLK transition, used to time when the auxiliary device samples DATA	30	50	us

7. ORDERING INFORMATION

PART NUMBER	NAME	PACKAGE DESCRIPTION
NUC710ADN	LQFP176	176 Leads, body 22 x 22 x 1.4 mm, Lead free package

8. PACKAGE SPECIFICATIONS

176L LQFP (20X20X1.4 mm footprint 2.0mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	22.00 BSC.			0.866 BSC.		
D	20.00 BSC.			0.787 BSC.		
HE	22.00 BSC.			0.866 BSC.		
E	20.00 BSC.			0.787 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
c	0.09	—	0.20	0.004	—	0.008
Y	—	—	0.10	—	—	0.004

9. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	March 02, 2009	-	Initial Issued

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