32-BIT ARM7TDMI-BASED MCU

NUC745ADN
16/32-bit ARM microcontroller
Product Data Sheet

Table of Contents-

1. GENERAL DESCRIPTION

The NUC745 is built around an outstanding CPU core, the 16/32 ARM7TDMI RISC processor which designed by Advanced RISC Machines, Ltd. It offers 4K-byte I-cache/SRAM and 4K-byte D-cache/SRAM, is a low power, general purpose integrated circuits. Its simple, elegant, and fully static design is particularly suitable for cost sensitive and power sensitive applications.

One 100/10 Mbit MAC of Ethernet controller is built-in to reduce total system cost.

The NUC745 also provides one USB 1.1 host controller, one USB 1.1 device controller, one AC97/I²S controller, one 2-channel GDMA, four independent UARTs, one watchdog timer, two 24-bit timers with 8-bit pre-scale, up to 31 programmable I/O ports, PS2 keyboard controller and an advanced interrupt controller. The external bus interface (EBI) controller provides for SDRAM, ROM/SRAM, flash memory and I/O devices. The system manager includes an internal 32-bit system bus arbiter and a PLL clock controller.

With a wide range of serial communication and Ethernet interfaces, the NUC745 is suitable for communication gateways as well as many other general purpose applications.

Publication Release Date: March 03, 2009

2. FEATURES

Architecture

- Fully 16/32-bit RISC architecture
- Little/Big-Endian mode supported
- Efficient and powerful ARM7TDMI core
- Cost-effective JTAG-based debug solution

External Bus Interface

- 8/16-bit external bus support for ROM/SRAM, flash memory, SDRAM and external I/Os
- Support for SDRAM
- Programmable access cycle (0-7 wait cycle)
- Four-word depth write buffer for SDRAM write data
- Cost-effective memory-to-peripheral DMA interface

Instruction and Data Cache

- Two-way, set-associative, 4K-byte I-cache and 4K-byte D-cache
- Support for LRU (Least Recently Used) protocol
- Cache can be configured as internal SRAM
- Support cache lock function

Ethernet MAC Controller

- DMA engine with burst mode
- MAC Tx/Rx buffers (256 bytes Tx, 256 bytes Rx)
- Data alignment logic
- Endian translation
- 100/10 Mbit per second operation
- Full compliance with IEEE standard 802.3
- RMII interface only
- Station Management Signaling
- On-chip CAM (up to 16 destination addresses)
- Full-duplex mode with PAUSE feature
- Long/short packet modes
- PAD generation

DMA Controller

- 2-channel general DMA for memory-to-memory data transfers without CPU intervention
- Initialed by a software or external DMA request
- Increments or decrements a source or destination address in 8-bit, 16-bit or 32-bit data transfers
- 4-data burst mode

UART

- Four UART (serial I/O) blocks with interrupt-based operation
- Support for 5-bit, 6-bit, 7-bit or 8-bit serial data transmit and receive
- Programmable baud rates
- 1, ½ or 2 stop bits
- Odd or even parity
- Break generation and detection
- Parity, overrun and framing error detection
- X16 clock mode
- UART1 supports Bluetooth, and UART2 supports IrDA1.0 SIR

Timers

- Two programmable 24-bit timers with 8-bit pre-scaler
- One programmable 20 bit with selectable additional 8-bit prescaler watchdog timer
- One-shot mode, periodical mode or toggle mode operation

Programmable I/Os

- 31 programmable I/O ports
- Pins individually configurable to input, output or I/O mode for dedicated signals
- I/O ports are configurable for multiple functions

Advanced Interrupt Controller

- 24 interrupt sources, including 4 external interrupt sources
- Programmable normal or fast interrupt mode (IRQ, FIQ)
- Programmable as either edge-triggered or level-sensitive for 4 external interrupt sources
- Programmable as either low-active or high-active for 4 external interrupt sources
- Priority methodology is encoded to allow for interrupt daisy-chaining
- Automatically mask out the lower priority interrupt during interrupt nesting

USB Host Controller

- USB 1.1 compliant
- Compatible with Open HCI 1.0 specification
- Supports low-speed and full speed devices
- Build-in DMA for real time data transfer
- Two on-chip USB transceivers with one optionally shared with USB device controller

USB Device Controller

- USB 1.1 compliant
- Support four USB endpoints including one control endpoint and 3 configurable endpoints for rich USB functions

Two PLLs

- The external clock can be multiplied by on-chip PLL to provide high frequency system clock
- The input frequency range is 3-30MHz; 15MHz is preferred.
- One PLL for both CPU and USB host/device controller
- One PLL for audio I²S 12.288/16.934MHz clock source
- Programmable clock frequency

4-Channel PWM

- Four 16-bit timers with PWM
- Two 8-bit pre-scalers & Two 4-bit dividers
- Programmable duty control of output waveform (PWM)
- Auto reload mode or one-shot pulse mode
- Dead-zone generator

I^2C Master

- 2-channel I^2C
- Compatible with Philips I^2C standard, support master mode only
- Support multi master operation
- Clock stretching and wait state generation
- Provide multi-byte transmit operation, up to 4 bytes can be transmitted in a single transfer
- Software programmable acknowledge bit
- Arbitration lost interrupt, with automatic transfer cancellation
- Start/Stop/Repeated Start/Acknowledge generation
- Start/Stop/Repeated Start detection

- Bus busy detection
- Supports 7 bit addressing mode
- Software mode I^2C

Universal Serial Interface (USI)

- 1-channel USI
- Support USI (Microwire/SPI) master mode
- Full duplex synchronous serial data transfer
- Variable length of transfer word up to 32 bits
- Provide burst mode operation, transmit/receive can be executed up to four times in one transfer
- MSB or LSB first data transfer
- Rx and Tx on both rising or falling edge of serial clock independently
- Two slave/device select lines
- Fully static synchronous design with one clock domain

2-Channel AC97/I²S Audio Codec Host Interface

- AHB master port and an AHB slave port are offered in audio controller.
- Always 8-beat incrementing burst
- Always bus lock when 8-beat incrementing burst
- When reach middle and end address of destination address, a DMA_IRQ is requested to CPU automatically

KeyPad Scan Interface

- Scan up to 16 rows by 8 columns with an external 4 to 16 decoder and 4x8 array without auxiliary component
- Programmable debounce time
- One or two keys scan with interrupt and three keys reset function.
- Wakeup CPU from IDEL/Power Down mode

PS2 Host Interface

- APB slave consisted of PS2 protocol.
- Connect IBM keyboard or bar-code reader through PS2 interface.
- Provide hardware scan code to ASCII translation

Power management

- Programmable clock enables for individual peripheral
- IDLE mode to halt ARM core and keep peripheral working
- Power-Down mode to stop all clocks included external crystal oscillator.
- Exit IDLE by all interrupts
    - Exit Power-Down by keypad,USB device and external interrupts

Operation Voltage Range

- 3.0 ~ 3.6 V for IO buffer
- 1.62 ~ 1.98 V for core logic

Operation Temperature Range

- TBD

Operating Frequency

- Up to 80 MHz

Package Type

- 128-pin LQFP

3. PIN DIAGRAM

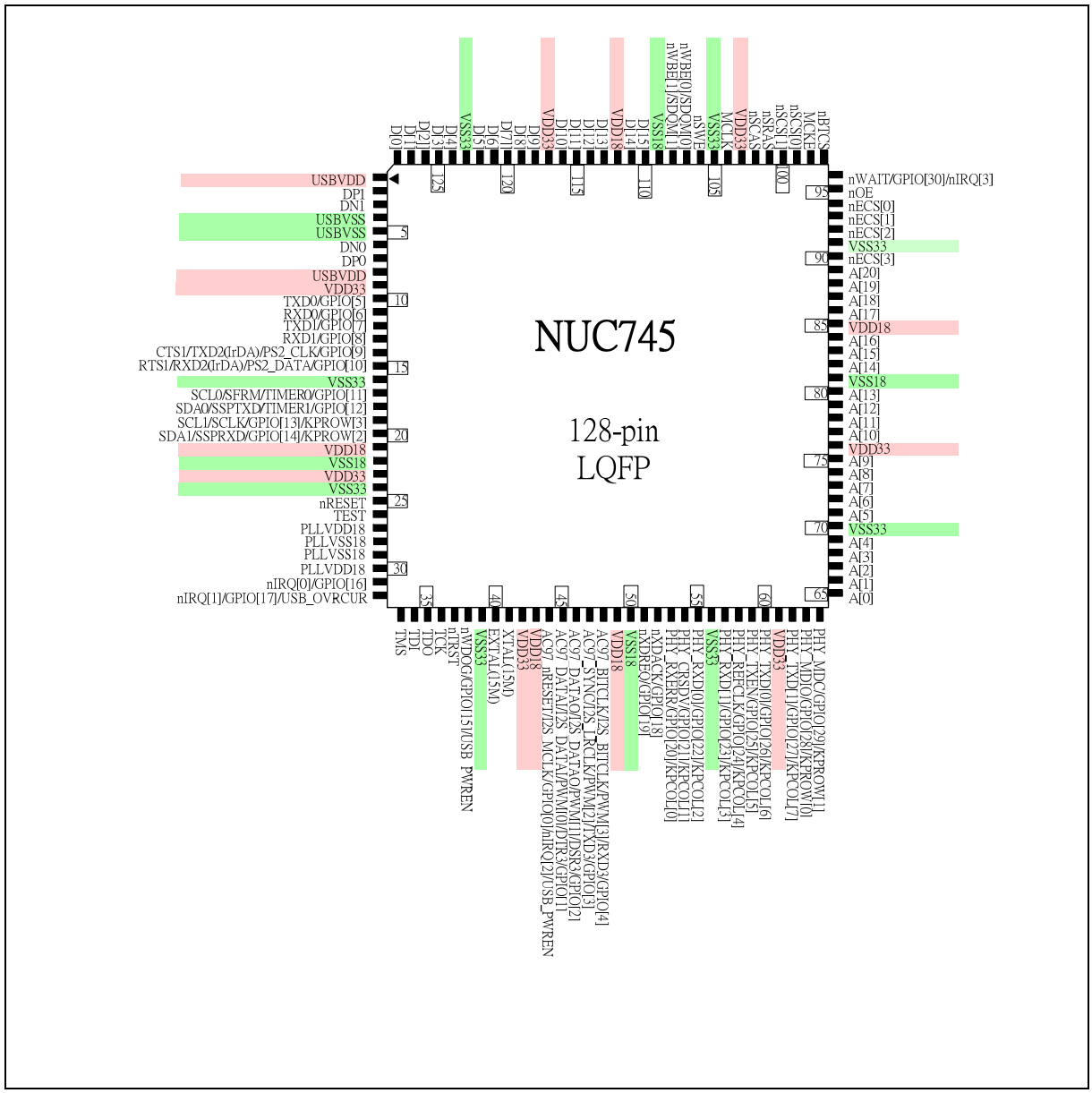


Figure 3.1 Pin Diagram

4. PIN ASSIGNMENT

Table 4.1 NUC745 Pins Assignment

PIN NAME	128-PIN LQFP
Clock & Reset	**(3 pins)**
EXTAL (15M)	40
XTAL (15M)	41
nRESET	25
JTAG Interface	**(5 pins)**
TMS	33
TDI	34
TDO	35
TCK	36
nTRST	37
External Bus Interface	**(53 pins)**
A [20:0]	89-86,84-82,80-77,75-71,69-65
D [15:0]	110-111,113-116,118-122,124-128
nWBE [1;0] / SDQM [1:0]	108,107
nSCS [1:0]	100,99
nSRAS	101
nSCAS	102
MCKE	98
nSWE	106
MCLK	104
nWAIT / GPIO [30] / nIRQ [3]	96
nBTCS	97
nECS [3:0]	90,92-94
nOE	95

Table 4.1 NUC745 Pins Assignment, continued

PIN NAME	128-PIN LQFP
Ethernet Interface	**(10 pins)**
PHY_MDC / GPIO [29] / KPROW [1]	64
PHY_MDIO / GPIO [28] / KPROW [0]	63
PHY_TXD [1:0] / GPIO [27:26] / KPCOL [7:6]	62,60
PHY_TXEN / GPIO [25] / KPCOL [5]	59
PHY_REFCLK / GPIO [24] / KPCOL [4]	58
PHY_RXD [1:0] / GPIO [23:22] / KPCOL [3:2]	57,55
PHY_CRSDV / GPIO [21] / KPCOL [1]	54
PHY_RXERR / GPIO [20] / KPCOL [0]	53
AC97/I²S/PWM/UART3	**(5 pins)**
AC97_nRESET / I²S_MCLK / GPIO [0] / nIRQ [2] / USB_PWREN	44

Table 4.1 NUC745 Pins Assignment, continued

PIN NAME	128-PIN LQFP
AC97/I²S/PWM/UART3	**(5 pins)**
AC97_DATAI / I²S_DATAI / PWM [0] / DTR3 / GPIO [1]	45
AC97_DATAO / I²S_DATAO / PWM [1] / DSR3 / GPIO [2]	46
AC97_SYNC / I²S_LRCLK / PWM [2] / TXD3 / GPIO [3]	47
AC97_BITCLK / I²S_BITCLK / PWM [3] / RXD3 GPIO [4]	48
USB Interface	**(4 pins)**
DP0	7
DN 0	6
DP1	2
DN1	3
Miscellaneous	**(7 pins)**
nIRQ [1] / GPIO [17] / USB_OVRCUR	32
nIRQ [0] / GPIO [16]	31
nWDOG / GPIO [15] / USB_PWREN	38
TEST	26

Table 4.1 NUC745 Pins Assignment, continued

PIN NAME	128-PIN LQFP
I²C/USI(SPI/MW)	**(4 pins)**
SCL0 / SFRM / TIMER0 / GPIO [11]	17
SDA0 / SSPTXD / TIMER1 / GPIO [12]	18
SCL1 / SCLK / GPIO [13] / KPROW [3]	19
SDA1 / SSPRXD / GPIO [14] / KPROW [2]	20
UART0/UART1/UART2/PS2	**(6 pins)**
TXD0 / GPIO [5]	10
RXD0 / GPIO [6]	11
TXD1 / GPIO [7]	12
RXD1 / GPIO [8]	13
CTS1 / TXD2(IrDA) / PS2_CLK / GPIO [9]	14
RTS1 / RXD2(IrDA) / PS2_DATA / GPIO [10]	15

Table 4.1 NUC745 Pins Assignment, continued

PIN NAME	128-PIN LQFP
XDMA	**(2 pins)**
nXDREQ / GPIO [19] /	51
nXDACK / GPIO [18] /	52
Power/Ground	**(36 pins)**
VDD18	21,43,49,85,112
VSS18	22,50,81,109
VDD33	9,23,42,61,76,103,117
VSS33	16,24,39,56,70,91,105,123
USBVDD	1,8
USBVSS	4,5
PLLVDD18	27,30
PLLVSS18	28,29

5. PIN DESCRIPTION

Table 5.1 NUC745 Pins Description

PIN NAME	IO TYPE	DESCRIPTION
Clock & Reset		
EXTAL (15M)	I	15MHz External Clock / Crystal Input
XTAL (15M)	O	15MHz Crystal Output
nRESET	IS	System Reset, active-low
JTAG Interface		
TMS	IUS	JTAG Test Mode Select, internal pull-up with 70K ohm
TDI	IUS	JTAG Test Data in, internal pull-up with 70K ohm
TDO	O	JTAG Test Data out
TCK	IDS	JTAG Test Clock, internal pull-down with 58K ohm
nTRST	IUS	JTAG Reset, active-low, internal pull-up with 70K ohm
External Bus Interface		
A [20:18]	O	Address Bus (MSB) of external memory and IO devices.
A [17:0]	IOS	Address Bus of external memory and IO devices.
D [15:0]	IOS	Data Bus (LSB) of external memory and IO device.
nWBE [1:0] / SDQM [1:0]	IOS	Write Byte Enable for specific device (nECS [1:0]). Data Bus Mask signal for SDRAM (nSCS [1:0]), active-low.
nSCS [1:0]	O	SDRAM chip select for two external banks, active-low.
nSRAS	O	Row Address Strobe for SDRAM, active-low.
nSCAS	O	Column Address Strobe for SDRAM, active-low.
MCKE	O	SDRAM Clock Enable, active-high
nSWE	O	SDRAM Write Enable, active-low
MCLK	O	System Master Clock Out, SDRAM clock, output with slew-rate control
nWAIT / GPIO[30] / nIRQ3	IUS	External Wait, active-low. This pin indicates that the external devices need more active cycle during access operation. General Programmable In/Out Port GPIO[30]. If memory and IO devices in EBI do not need wait request, it can be configured as GPIO[30] or nIRQ3.
nBTCS	O	ROM/Flash Chip Select, active-low.
nECS [3:0]	IO	External I/O Chip Select, active-low.
nOE	O	ROM/Flash, External Memory Output Enable, active-low.

Table 5.1 NUC745 Pins Description, continued

PIN NAME	IO TYPE	DESCRIPTION
Ethernet Interface		
PHY_MDC / GPIO [29] / KPROW [1]	IOU	RMII Management Data Clock for Ethernet. It is the reference clock of MDIO. Each MDIO data will be latched at the rising edge of MDC clock. General Programmable In/Out Port [29] Keypad ROW[1] scan output.
PHY_MDIO / GPIO [28] / KPROW [0]	IO	RMII Management Data I/O for Ethernet. It is used to transfer RMII control and status information between PHY and MAC. General Programmable In/Out Port [28] Keypad ROW[0] scan output.
PHY_TXD [1:0] / GPIO [27:26] / KPCOL [7:6]	IOU	2-bit Transmit Data bus for Ethernet. General programmable In/Out Port [27:26] Keypad column input [7:6], active low
PHY_TXEN / GPIO [25] / KPCOL [5]	IOU	PHY_TXEN shall be asserted synchronously with the first 2-bit of the preamble and shall remain asserted while all di-bits to be transmitted are presented. Of course, it is synchronized with PHY_REFCLK. General Programmable In/Out Port [25] Keypad column input [5], active low
PHY_REFCLK / GPIO [24] / KPCOL [4]	IOS	Reference Clock. The clock shall be 50MHz +/- 50 ppm with minimum 35% duty cycle at high or low state. General Programmable In/Out port [24] Keypad column input [4], active low
PHY_RXD [1:0] / GPIO [23:22] / KPCOL [3:2]	IOS	2-bit Receive Data bus for Ethernet. General Programmable In/Out Port [23:22] Keypad column input [3:2], active low
PHY_CRSDV / GPIO [21] / KPCOL [1]	IOS	Carrier Sense / Receive Data Valid for Ethernet. The PHY_CRSDV shall be asserted by PHY when the receive medium is non-idle. Loss of carrier shall result in the de-assertion of PHY_CRSDV synchronous to the cycle of PHY_REFCLK, and only on 2-bit receive data boundaries. General Programmable In/Out port [21] Keypad column input [1], active low
PHY_RXERR / GPIO [20] / KPCOL [0]	IOS	Receive Data Error for Ethernet. It indicates a data error detected by PHY.The assertion should be lasted for longer than a period of PHY_REFCLK. When PHY_RXERR is asserted, the MAC will report a CRC error. General programmable In/Out port [20] Keypad column input [0], active low

Table 5.1 NUC745 Pins Description, continued

PIN NAME	IO TYPE	DESCRIPTION
AC97/I²S/PWM/UART3		
AC97_nRESET / I²S_MCLK / GPIO [0] / nIRQ [2] / USB_PWREN	IOU	AC97 CODEC Host Interface RESET Output. I²S CODEC Host Interface System Clock Output. General Purpose In/Out port [0] External interrupt request. USB host power enable output
AC97_DATAI / I²S_DATAI / PWM [0] / DTR3 / GPIO [1]	IOU	AC97 CODEC Host Interface Data Input. I²S CODEC Host Interface Data Input. PWM Channel 0 output. Data Terminal Ready for UART3. General Purpose In /Out port [1]
AC97_DATAO / I²S_DATAO / PWM [1] / DSR3 / GPIO [2]	IOU	AC97 CODEC Host Interface Data Output. I²S CODEC Host Interface Data Output. PWM Channel 1 output. Data Set Ready for UART3. General Purpose In/Out port [2]
AC97_SYNC / I²S_LRCLK / PWM [2] / TXD3 / GPIO [3]	IOU	AC97 CODEC Host Interface Synchronous Pulse Output. I²S CODEC Host Interface Left/Right Channel Select Clock. PWM Channel 2 output. Transmit Data for UART3. General Purpose In/Out port [3]
AC97_BITCLK / I²S_BITCLK / PWM [3] / RXD3 / GPIO [4]	IOS	AC97 CODEC Host Interface Bit Clock Input. I²S CODEC Host Interface Bit Clock. PWM Channel 3 output. Receive Data for UART3. General Purpose In/Out port [4].
USB Interface		
DP0	IO	Differential Positive USB IO signal
DN0	IO	Differential Negative USB IO signal
DP1	IO	Differential Positive USB IO signal
DN1	IO	Differential Negative USB IO signal
Miscellaneous		
nIRQ [1:0] / GPIO [17:16] / USB_OVRCUR	IOU	External Interrupt Request General Purpose I/O nIRQ1 is used as USB host over-current detection input
nWDOG / GPIO [15] / USB_PWREN	IOU	Watchdog Timer Timeout Flag and Keypad 3-keys reset output, active low General Purpose In/output USB host power switch enable output
TEST	IDS	This test pin must be short to ground or left unconnected

Table 5.1 NUC745 Pins Description, continued

PIN NAME	IO TYPE	DESCRIPTION
I²C/USI		
SCL0 / SFRM / TIMER0 / GPIO [11]	IOU	I²C Serial Clock Line 0. USI Serial Frame. Timer0 time out output. General Purpose In/Out port [11].
SDA0 / SSPTXD / TIMER1 / GPIO [12]	IOU	I²C Serial Data Line 0 USI Serial Transmit Data Timer1 time out output General Purpose In/Out port [12]
SCL1 / SCLK / GPIO [13] / KPROW [3]	IOU	I²C Serial Clock Line 1 USI Serial Clock General Purpose In/Out port [13] Keypad row scan output [3]
SDA1 / SSPRXD / GPIO [14] / KPROW [2]	IDU	I²C Serial Data Line 1 USI Serial Receive Data General Purpose In/Out port [14] Keypad scan output [2]
UART0/UART1/UART2		
TXD0 / GPIO [5]	IOU	UART0 Transmit Data. General Purpose In/Out [5]
RXD0 / GPIO [6]	IOU	UART0 Receive Data. General Purpose In/Out [6]
TXD1 / GPIO [7]	IOU	UART1 Transmit Data. General Purpose In/Out [7]
RXD1 / GPIO [8]	IOU	UART1 Receive Data. General Purpose In/Out [8]
CTS1/ TXD2(IrDA) / PS2_CLK / GPIO [9]	IOU	UART1 Clear To Send for Bluetooth application UART2 Transmit Data supporting SIR IrDA. PS2 Interface Clock Input/Output General Purpose In/Out [9]
RTS1/ RXD2(IrDA) / PS2_DATA / GPIO [10]	IOU	UART1 Request To Send for Bluetooth application UART2 Receive Data supporting SIR IrDA. PS2 Interface Bi-Directional Data Line. General Purpose In/Out [10]
XDMA		
nXDREQ / GPIO [19] /	IO	External DMA Request. General Purpose In/Out [19]
nXDACK / GPIO [18] /	IO	External DMA Acknowledgement. General Purpose In/Out [18]

Table 5.1 NUC745 Pins Description, continued

PIN NAME	IO TYPE	DESCRIPTION
Power/Ground		
VDD18	P	Core Logic power (1.8V)
VSS18	G	Core Logic ground (0V)
VDD33	P	IO Buffer power (3.3V)
VSS33	G	IO Buffer ground (0V)
USBVDD	P	USB power (3.3V)
USBVSS	G	USB ground (0V)
DVDD18	P	PLL Digital power (1.8V)
DVSS18	G	PLL Digital ground (0V)
AVDD18	P	PLL Analog power (1.8V)
AVSS18	G	PLL Analog ground (0V)

Table 5.2 NUC745 128-pin LQFP Multi-function List

PIN NO.	DEFAULT	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
USB1.1 Host/Device Interface					
1	**USBVDD**	USBVDD	-	-	-
2	**DP1**	DP1	-	-	-
3	**DN1**	DN1	-	-	-
4	**USBVSS**	USBVSS	-	-	-
5	**USBVSS**	USBVSS	-	-	-
6	**DN0**	DN0	-	-	-
7	**DP0**	DP0	-	-	-
8	**USBVDD**	USBVDD	-	-	-
9	**VDD33**	VDD33	-	-	-
UART[2:0]/PS2 Interface					
10	**GPIO[5]**	GPIO[5]	UART_TXD0	-	-
11	**GPIO[6]**	GPIO[6]	UART_RXD0	-	-
12	**GPIO[7]**	GPIO[7]	UART_TXD1	-	-
13	**GPIO[8]**	GPIO[8]	UART_RXD1	-	-
14	**GPIO[9]**	GPIO[9]	UART_TXD2	UART_CTS1	PS2_CLK
15	**GPIO[10]**	GPIO[10]	UART_RXD2	UART_RTS1	PS2_DATA
16	**VSS33**	VSS33	-	-	-
I^2C/USI Interface					
17	**GPIO[11]**	GPIO[11]	I^2C_SCL0	SSP_FRAM	TIMER0
18	**GPIO[12]**	GPIO[12]	I^2C_SDA0	SSP_TXD	TIMER1
19	**GPIO[13]**	GPIO[13]	I^2C_SCL1	SSP_SCLK	KPI_ROW[3]
20	**GPIO[14]**	GPIO[14]	I^2C_SDA1	SSP_RXD	KPI_ROW[2]
21	**VDD18**	VDD18	-	-	-
22	**VSS18**	VSS18	-	-	-
23	**VDD33**	VDD33	-	-	-
24	**VSS33**	VSS33	-	-	-
System Reset & TEST					
25	**nRESET**	nRESET	-	-	-
26	**TEST**	TEST	-	-	-

Table 5.2 NUC745 128-pin LQFP Multi-function List, continued

PLL Power/Ground					
27	**PLL_VDD18**	PLL_VDD18	-	-	-
28	**PLL_VSS18**	PLL_VSS18	-	-	-
29	**PLL_VSS18**	PLL_VSS18	-	-	-
30	**PLL_VDD18**	PLL_VDD18	-	-	-
External IRQ[1:0]/USB Over Current					
31	**GPIO[16]**	GPIO[16]	nIRQ [0]	-	-
32	**GPIO[17]**	GPIO[17]	nIRQ [1]	USB_OVRCUR	-
JTAG Interface					
33	**TMS**	TMS	-	-	-
34	**TDI**	TDI	-	-	-
35	**TDO**	TDO	-	-	-
36	**TCK**	TCK	-	-	-
37	**nTRST**	nTRST	-	-	-
WatchDog/USB Power Enable					
38	**GPIO[15]**	GPIO[15]	nWDOG	USB_PWREN	-
39	**VSS33**	VSS33	-	-	-
System Clock					
40	**EXTAL(15M)**	EXTAL(15M)	-	-	-
41	**XTAL(15M)**	XTAL(15M)	-	-	-
42	**VDD33**	VDD33	-	-	-
43	**VDD18**	VDD18	-	-	-

Table 5.2 NUC745 128-pin LQFP Multi-function List, continued

PIN NO.	DEFAULT	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
AC97/I²S/PWM/UART3 Interface					
44	**GPIO[0]**	GPIO[0]	AC97_nRESET or I²SMCLK	nIRQ [2]	USB_PWREN
45	**GPIO[1]**	GPIO[1]	AC97_DATAI or I²SDATAI	PWM0	UART_DTR3
46	**GPIO[2]**	GPIO[2]	AC97_DATAO or I²SDATAO	PWM1	UART_DSR3
47	**GPIO[3]**	GPIO[3]	AC97_SYNC or I²SLRCLK	PWM2	UART_TXD3
48	**GPIO[4]**	GPIO[4]	AC97_BITCLK or I²SBITCLK	PWM3	UART_RXD3
49	**VDD18**	VDD18	-	-	-
50	**VSS18**	VSS18	-	-	-
XDMAREQ					
51	**GPIO[19]**	GPIO[19]	nXDREQ	-	-
52	**GPIO[18]**	GPIO[18]	nXDACK	-	-
Ethernet RMII/KeyPad Interface					
53	**GPIO[20]**	GPIO[20]	PHY_RXERR	KPI_COL[0]	-
54	**GPIO[21]**	GPIO[21]	PHY_CRSDV	KPI_COL[1]	-
55	**GPIO[22]**	GPIO[22]	PHY_RXD[0]	KPI_COL[2]	-
56	**VSS33**	VSS33	-	-	-
57	**GPIO[23]**	GPIO[23]	PHY_RXD[1]	KPI_COL[3]	-
58	**GPIO[24]**	GPIO[24]	PHY_REFCLK	KPI_COL[4]	-
59	**GPIO[25]**	GPIO[25]	PHY_TXEN	KPI_COL[5]	-
60	**GPIO[26]**	GPIO[26]	PHY_TXD[0]	KPI_COL[6]	-
61	**VDD33**	VDD33	-	-	-
62	**GPIO[27]**	GPIO[27]	PHY_TXD[1]	KPI_COL[7]	-
63	**GPIO[28]**	GPIO[28]	PHY_MDIO	KPI_ROW[0]	
64	**GPIO[29]**	GPIO[29]	PHY_MDC	KPI_ROW[1]	

Table 5.2 NUC745 128-pin LQFP Multi-function List, continued

PIN NO.	DEFAULT	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
Memory Address/Data/Control					
65	**A[0]**	A[0]	-	-	-
66	**A[1]**	A[1]	-	-	-
67	**A[2]**	A[2]	-	-	-
68	**A[3]**	A[3]	-	-	-
69	**A[4]**	A[4]	-	-	-
70	**VSS33**	VSS33	-	-	-
71	**A[5]**	A[5]	-	-	-
72	**A[6]**	A[6]	-	-	-
73	**A[7]**	A[7]	-	-	-
74	**A[8]**	A[8]	-	-	-
75	**A[9]**	A[9]	-	-	-
76	**VDD33**	VDD33	-	-	-
77	**A[10]**	A[10]	-	-	-
78	**A[11]**	A[11]	-	-	-
79	**A[12]**	A[12]	-	-	-
80	**A[13]**	A[13]	-	-	-
81	**VSS18**	VSS18	-	-	-
82	**A[14]**	A[14]	-	-	-
83	**A[15]**	A[15]	-	-	-
84	**A[16]**	A[16]	-	-	-
85	**VDD18**	VDD18	-	-	-
86	**A[17]**	A[17]	-	-	-
87	**A[18]**	A[18]	-	-	-
88	**A[19]**	A[19]	-	-	-
89	**A[20]**	A[20]	-	-	-
90	**nECS[3]**	nECS[3]	-	-	-
91	**VSS33**	VSS33	-	-	-

Table 5.2 NUC745 128-pin LQFP Multi-function List, continued

PIN NO.	DEFAULT	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
Memory Address/Data/Control					
92	**nECS[2]**	nECS[2]	-	-	-
93	**nECS[1]**	nECS[1]	-	-	-
94	**nECS[0]**	nECS[0]	-	-	-
95	**nOE**	nOE	-	-	-
96	**nWAIT**	GPIO[30]	nWAIT	nIRQ [3]	-
97	**nBTCS**	nBTCS	-	-	-
98	**MCKE**	MCKE	-	-	-
99	**nSCS[0]**	nSCS[0]	-	-	-
100	**nSCS[1]**	nSCS[1]	-	-	-
101	**nSRAS**	nSRAS	-	-	-
102	**nSCAS**	nSCAS	-	-	-
103	**VDD33**	VDD33	-	-	-
104	**MCLK**	MCLK	-	-	-
105	**VSS33**	VSS33	-	-	-
106	**nSWE**	nSWE	-	-	-
107	**nWBE/SDQM[0]**	nWBE or SDQM[0]			
108	**nWBE/SDQM[1]**	nWBE or SDQM[1]			
109	**VSS18**	VSS18	-	-	-
110	**D[15]**	D[15]	-	-	-
111	**D[14]**	D[14]	-	-	-
112	**VDD18**	VDD18	-	-	-
113	**D[13]**	D[13]	-	-	-
114	**D[12]**	D[12]	-	-	-
115	**D[11]**	D[11]	-	-	-
116	**D[10]**	D[10]	-	-	-
117	**VDD33**	VDD33	-	-	-
118	**D[9]**	D[9]	-	-	-
119	**D[8]**	D[8]	-	-	-
120	**D[7]**	D[7]	-	-	-

Table 5.2 NUC745 128-pin LQFP Multi-function List, continued

PIN NO.	DEFAULT	FUNCTION0	FUNCTION1	FUNCTION2	FUNCTION3
Memory Address/Data/Control					
121	**D[6]**	D[6]	-	-	-
122	**D[5]**	D[5]	-	-	-
123	**VSS33**	VSS33	-	-	-
124	**D[4]**	D[4]	-	-	-
125	**D[3]**	D[3]	-	-	-
126	**D[2]**	D[2]	-	-	-
127	**D[1]**	D[1]	-	-	-
128	**D[0]**	D[0]	-	-	-

6. ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings

Ambient temperature	-40 °C ~ +85°C
Storage temperature	-40 °C ~ +125°C
Voltage on any pin	-0.5V ~ 6V
Power supply voltage (Core logic)	-0.5V ~ 1.92V
Power supply voltage (IO Buffer)	-0.5V ~ 3.6V
Injection current (latch-up testing)	100mA
Crystal Frequency	4MHz ~ 30MHz

6.2 DC Specifications

6.2.1 Digital DC Characteristics

(Normal test conditions: VDD33/USBVDD = 3.3V+/- 0.3V, VDD18/DVDD18/AVDD18 = 1.8V+/- 0.18V

TA = -40 °C ~ +85 °C unless otherwise specified)

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
VDD33/ USBVDD	Power Supply		3.00	3.60	V
VDD18/ DVDD18/ AVDD18	Power Supply		1.62	1.98	V
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{IH}	Input High Voltage		2.0	5.5	V
VT+	Schmitt Trigger positive-going threshold		1.47	1.5	V
VT-	Schmitt trigger negative-going threshold		0.89	0.95	V
V_{OL}	Output Low Voltage	Depend on driving	-	0.4	V
V_{OH}	Output High Voltage	Depend on driving	2.4	-	V

Continued.

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
I_{CC1}	1.8V Supply Current	F_{CPU} = 80MHz	-	150	mA
ICC2	3.3V Supply Current	FCPU = 80MHz	-	60	mA
ICCRTC	RTC 1.8V Supply Current	FRTC = 32.768KHZ	-	7	uA
I_{IH}	Input High Current	V_{IN} = 2.4 V	-1	1	μA
I_{IL}	Input Low Current	V_{IN} = 0.4 V	-1	1	μA
I_{IHP}	Input High Current (pull-up)	V_{IN} = 2.4 V	-15	-10	μA
I_{ILP}	Input Low Current (pull-up)	V_{IN} = 0.4 V	-55	-25	μA
I_{IHD}	Input High Current (pull-down)	V_{IN} = 2.4 V	25	60	μA
I_{ILD}	Input Low Current (pull-down)	V_{IN} = 0.4 V	5	10	μA

Table 7.2.1 TSMC IO DC Characteristics

PARAMETER		MIN.	TYP.	MAX.
V_{IL}	Input Low Voltage	-0.3V		0.8V
V_{IH}	Input High Voltage	2V		5.5V
V_T	Threshold point	1.46V	1.59V	1.75V
V_{T+}	Schmitt trig low to high threshold point	1.47V	1.50V	1.50V
V_{T-}	Schmitt trig, high to low threshold point	0.90V	0.94V	0.96V
I_I	Input leakage current @V_I= 3.3V or 0V			+/- 10uA
I_{oz}	Tri-state output leakage current @Vo =3.3V or 0V			+/- 10UA
R_{PU}	Pull-up resister	44KΩ	66KΩ	110KΩ
R_{PD}	Pull-down resister	25KΩ	50KΩ	110KΩ
V_{OL}	Output low voltage @$_{IOL}$(min)			0.4V
V_{OH}	Output high voltage @I_{OH} (min)	2.4V		

Continued.

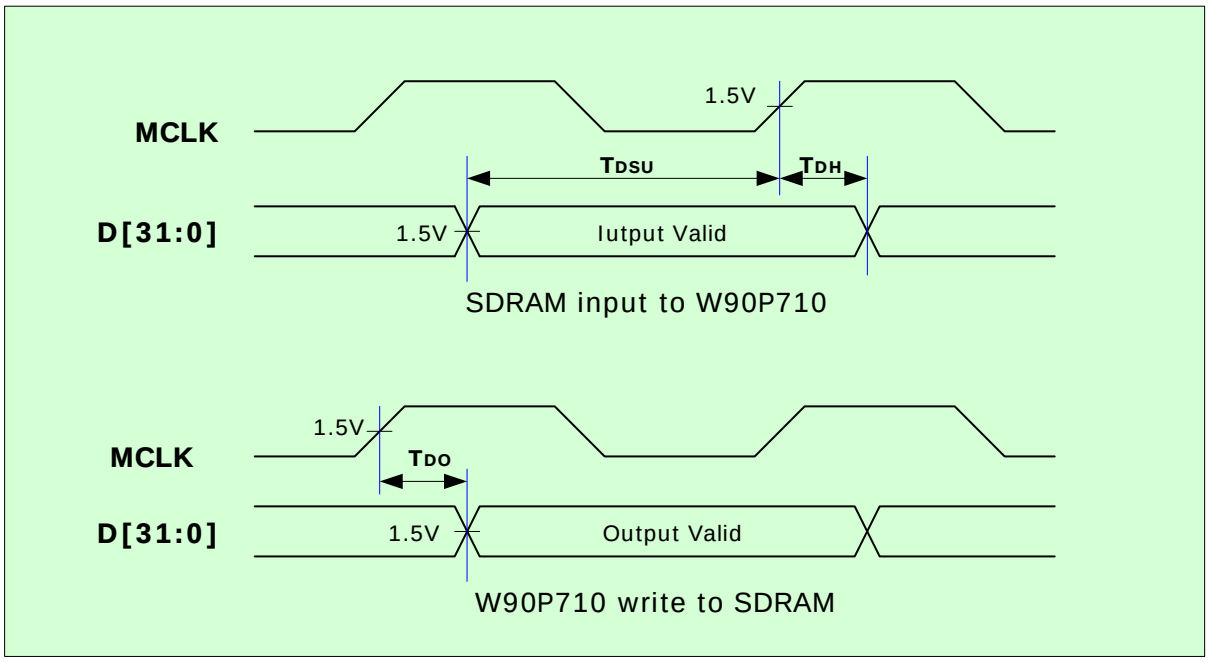
PARAMETER		MIN.	TYP.	MAX.
I_{OL}	Low level output current @V_{OL} = 0.4V 4mA	4.9mA	7.4mA	9.8mA
	Low level output current @V_{OL} = 0.4V 8mA	9.7mA	14.9mA	19.5mA
	Low level output current @V_{OL} = 0.4V 12mA	14.6mA	22.3mA	29.3mA
I_{OH}	High level output current @V_{OH} = 2.4V 4mA	6.3mA	12.8mA	21.2mA
	High level output current @V_{OH} = 2.4V 8mA	12.7mA	25.6mA	42.4mA
	High level output current @V_{OH} = 2.4V 12mA	19.0mA	38.4mA	63.6mA
NOTE: The values in this table are copied from TSMC 1P5M IO library tpz937g_240b silicon report. This table is just for reference. More precision DC vaule should refer to Alpha-Test result.				

6.2.2 USB Transceiver DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DI}	Differential Input Sensitivity	|DP – DM|	0.2		V
V_{CM}	Differential Common Mode Range	Includes V_{DI} range	0.8	2.5	V
V_{SE}	Single Ended Receiver Threshold		0.8	2.0	V
V_{OL}	Static Output Low Voltage	RL of 1.5 KΩ to 3.6 V		0.3	V
V_{OH}	Static Output High Voltage	RL of 15 KΩ to VSS	2.8	3.6	V
V_{CRS}	Output Signal Crossover Voltage		1.3	2.0	V
Z_{DRV}	Driver Output Resistance	Steady state drive	28	43	Ω
C_{IN}	Pin Capacitance			20	pF

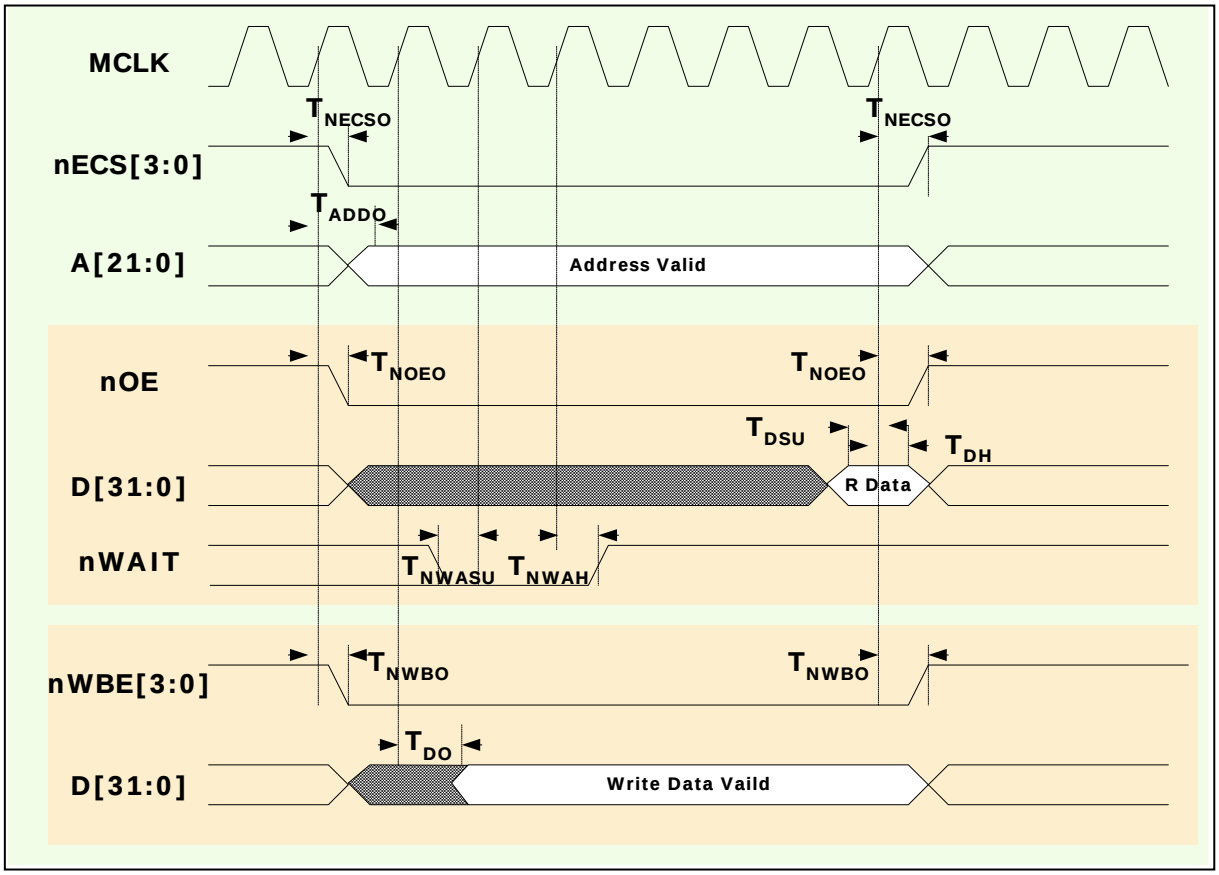
6.3 AC Specifications

6.3.1 EBI/SDRAM Interface AC Characteristics



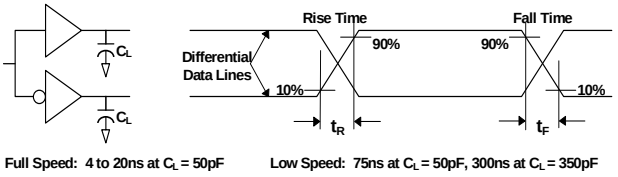
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_{DSU}	D [31:0] Setup Time	2		ns
T_{DH}	D [31:0] Hold Time	2		ns
T_{DO}	D [31:0], A [24:0], nSCS [1:0], SDQM [3:0], CKE, nSWE, nSRAS, nSCAS	2	7	ns

6.3.2 EBI/(ROM/SRAM/External I/O) AC Characteristics



SYMBOL	DESCRIPTION	MIN	MAX	UNIT
T_{ADDO}	Address Output Delay Time	2	7	ns
T_{NCSO}	ROM/SRAM/Flash or External I/O Chip Select Delay Time	2	7	ns
T_{NOEO}	ROM/SRAM or External I/O Bank Output Enable Delay	2	7	ns
T_{NWBO}	ROM/SRAM or External I/O Bank Write Byte Enable Delay	2	7	ns
T_{DH}	Read Data Hold Time	7		ns
T_{DSU}	Read Data Setup Time	0		ns
T_{DO}	Write Data Output Delay Time (SRAM or External I/O)	2	7	ns
T_{NWASU}	External Wait Setup Time	3		ns
T_{NWAH}	External Wait Hold Time	1		ns

6.3.3 USB Transceiver AC Characteristics



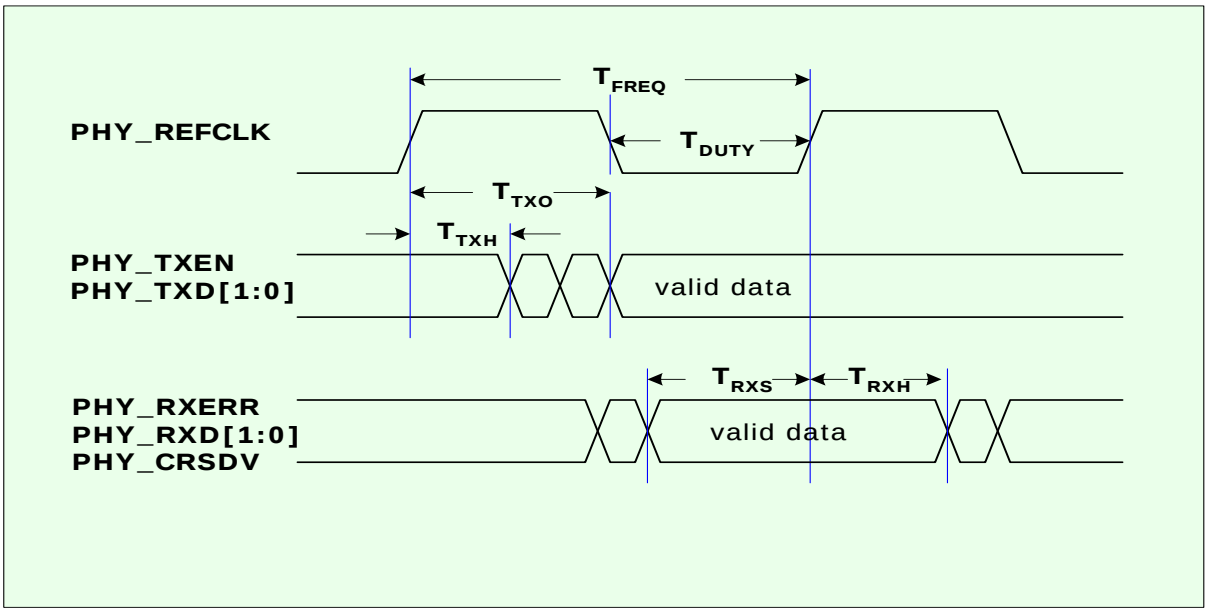
Data Signal Rise and Fall Time

USB Transceiver AC Characteristics

SYMBOL	DESCRIPTION	CONDITIONS	MIN	MAX	UNIT
T_R	Rise Time	CL = 50 pF	4	20	ns
T_F	Fall Time	CL = 50 pF	4	20	ns
T_{RFM}	Rise/Fall Time Matching		90	110	%
T_{DRATE}	Full Speed Data Rate	Average bit rate (12 Mb/s ± 0.25%)	11.97	12.03	Mbps

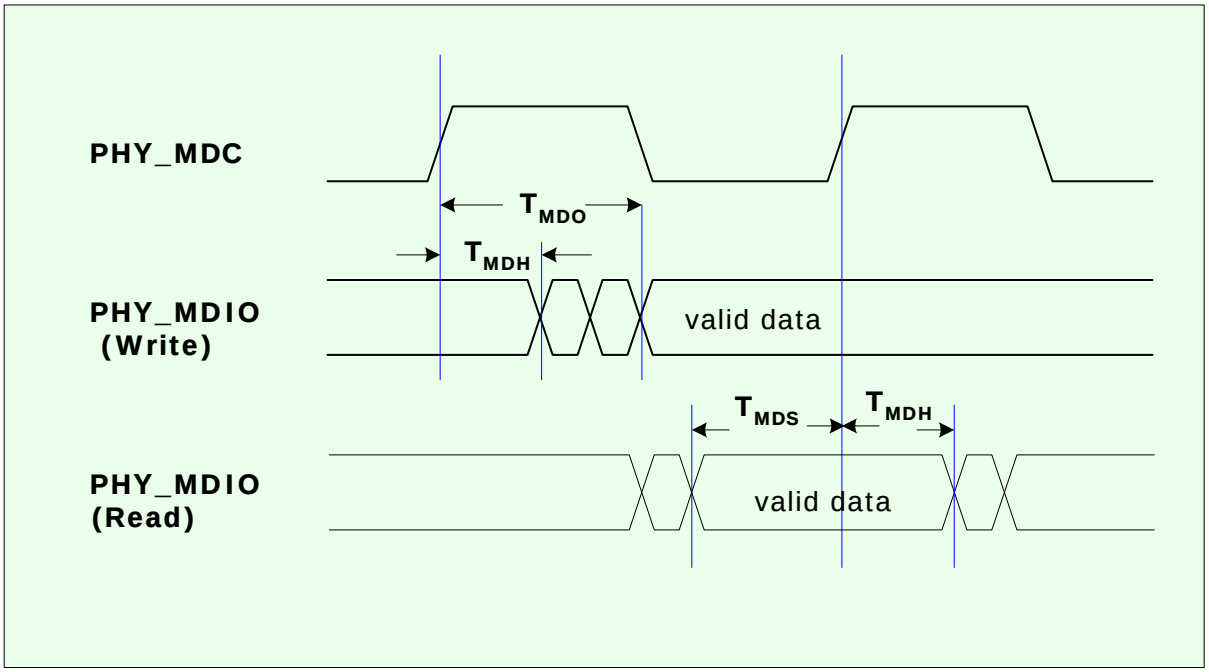
6.3.4 EMC RMII AC Characteristics

The signal timing characteristics conforms to the guidelines specified in IEEE Std. 802.3.



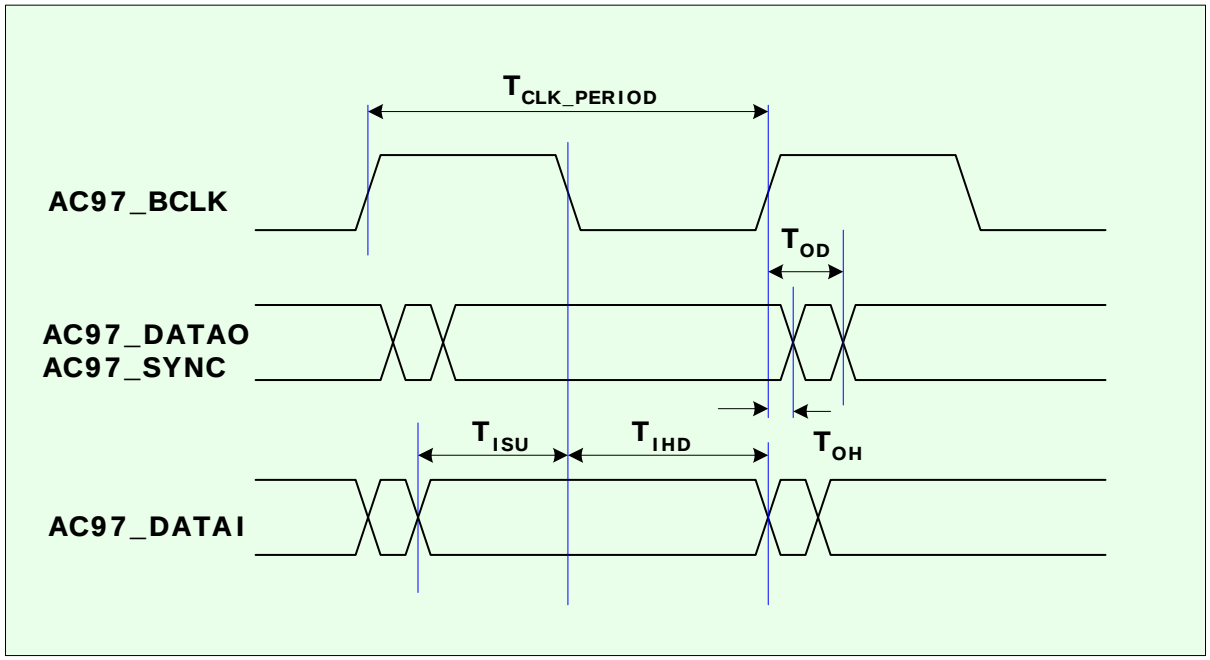
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT

T_{FREQ}	RMII reference clock frequency		50		MHz
T_{DUTY}	RMII clock duty	35%	50%	65%	ns
T_{TXO}	Transmit data output delay	5	-	15	ns
T_{TXH}	Transmit data hold time	2	-	-	ns
T_{RXS}	Receive data setup time	4	-	-	ns
T_{RXH}	Receive data hold time	2	-	-	ns

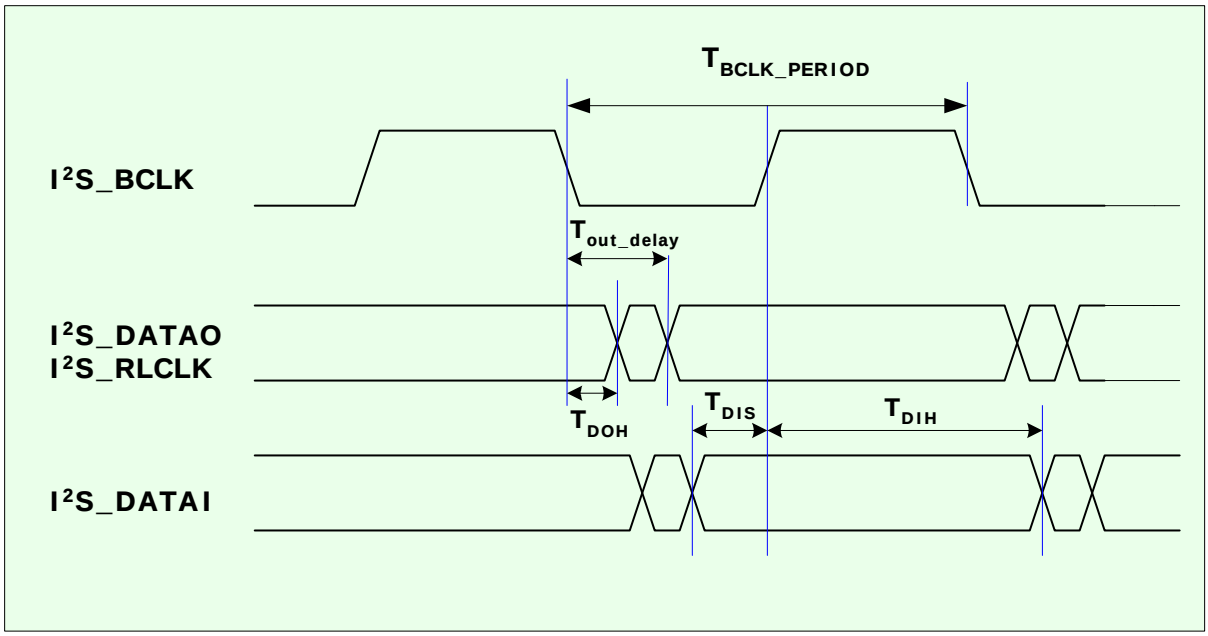


SYMBOL	DESCRIPTION	MIN	MAX	UNIT
T_{MDO}	MDIO Output Delay Time	0	15	ns
T_{MDSU}	MDIO Setup Time	5		ns
T_{MDH}	MDIO Hold Time	5		ns

6.3.5 AC97/I2S Interface AC Characteristics

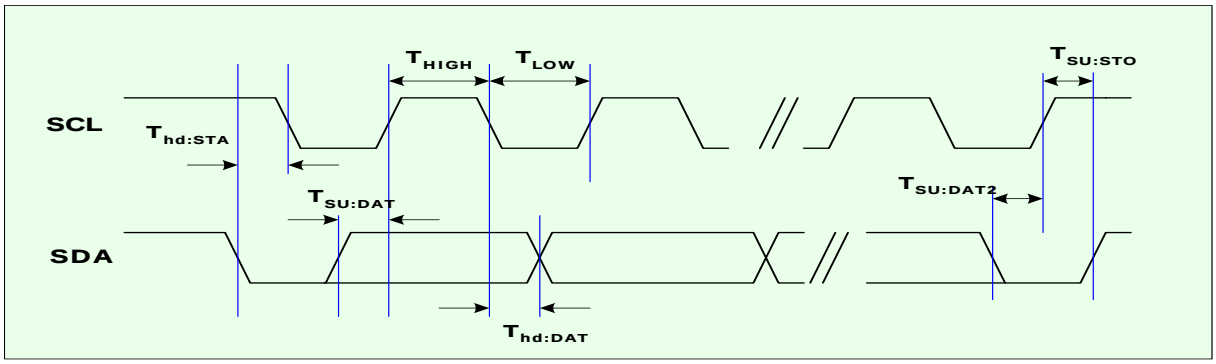


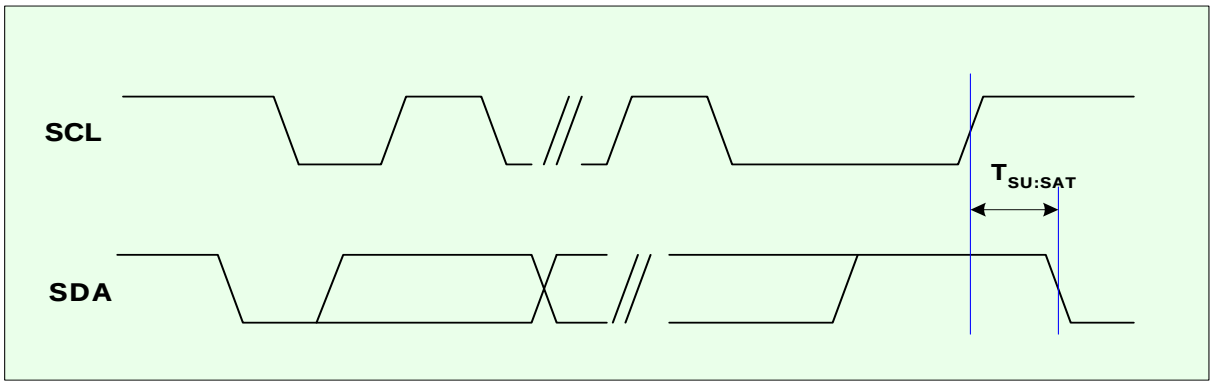
SYMBOLS	DESCRIPTION	MIN	TYP.	MAX	UNIT
T_{CLK_PERIOD}	AC97 Bit Clock Frequency	--	12.288	--	MHz
T_{OD}	AC97_DATAO and AC97_SYNC output delay from AC97_BCLK rising edge	--	--	30	ns
T_{OH}	AC97_DATAO and AC97_SYNC output hold time from AC97_BCLK rising edge	5	--	--	ns
T_{ISU}	AC97_DATAI input setup time to AC97_BCLK falling edge	10	--	--	ns
T_{IHD}	AC97_DATAI input hold time from AC97_BCLK falling edge	5	--	--	ns



SYMBOLS	DESCRIPTION	MIN	MAX	UNIT
T_{BCLK_PERIOD}	IIS Bit Clock Frequency	Note:depend on codec spec. and register setting		MHz
T_{out_delay}	IIS_DATAO and IIS_RLCLK output delay from IIS_BCLK falling edge	--	30	ns
T_{DOH}	IIS_DATAO and IIS_RLCLK data output hold time from IIS_BCLK falling edge	0	--	ns
T_{DIS}	IIS_DATAI input setup time to IIS_BCLK rising edge	10	--	ns
T_{DIH}	IIS_DATAI input hold time from IIS_BCLK rising edge	100	--	ns

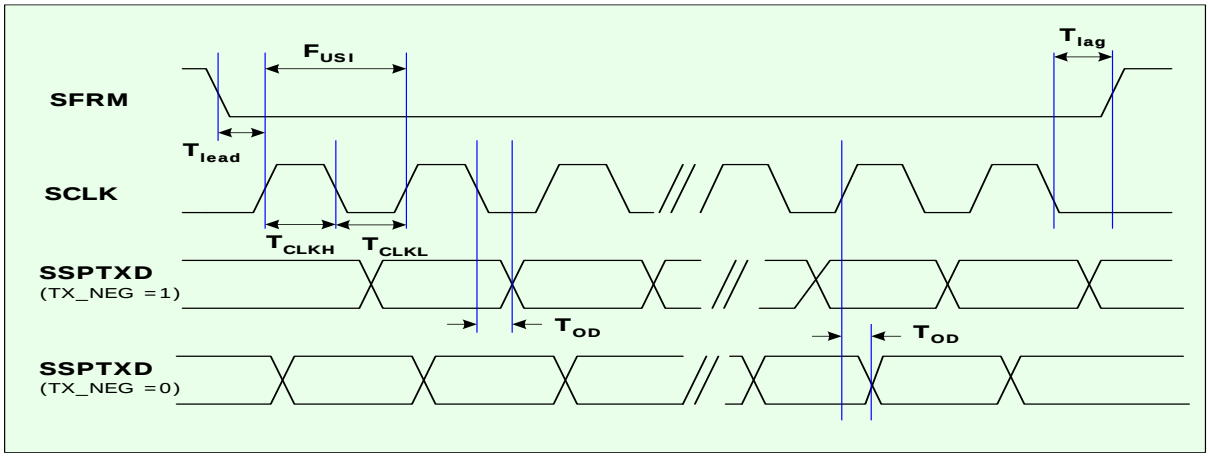
6.3.6 I²C Interface AC Characteristics

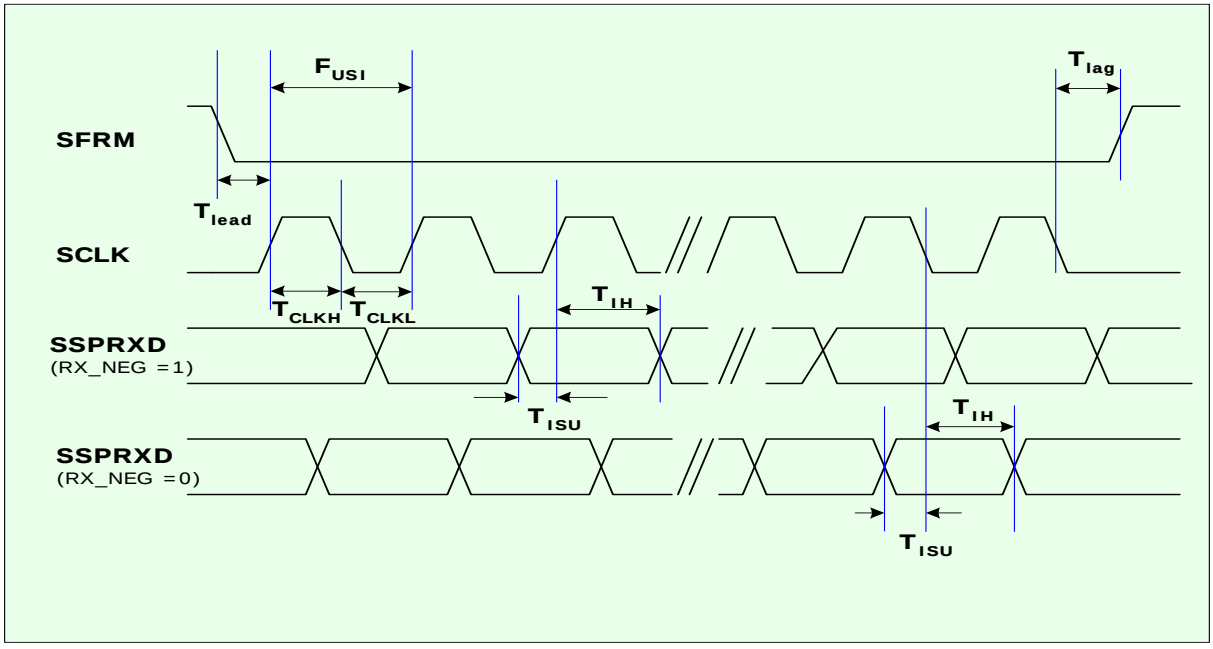




SYMBOL	DESCRIPTION	MIN	MAX	UNIT
T_{HIGH}	I²C Clock high time	1	-	us
T_{LOW}	I²C clock low time	1	-	us
$T_{hd:STA}$	Start condition hold time	1	-	us
$T_{SU:DAT}$	Receive data setup time	0.1	-	us
	Transmit data output delay	-	0.5	us
$T_{HD:DAT}$	Receive data hold time	1	-	us
	Transmit data hold time	0	0.9	us
$T_{SU:DAT2}$	SDA setup time (before STOP condition)	0.5	-	us
$T_{SU:STO}$	Stop condition setup time	1	-	us
$T_{SU:STA}$	Restart condition setup time	1.5	-	us

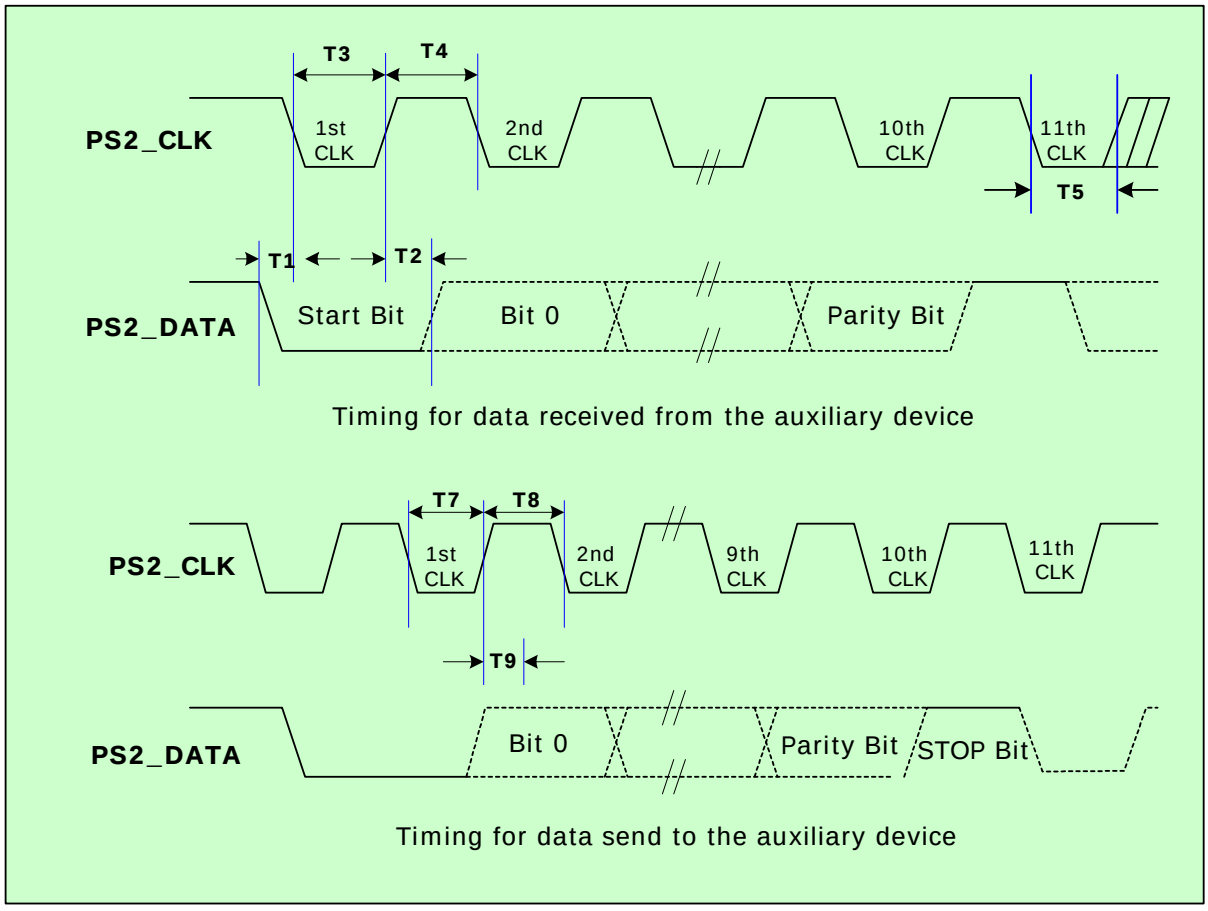
6.3.7 USI Interface AC Characteristics





SYMBOL	DESCRIPTION	MIN	MAX	UNIT
F_{USI}	USI clock frequency	-	20	MHz
T_{CLKH}	USI clock high time	12.5	-	ns
T_{CLKL}	USI clock low time	-	-	ns
T_{ISU}	Data input setup time	-	14	ns
T_{IH}	Data input hold time	0	-	ns
T_{lead}	USI enable lead time	12.5	-	ns
T_{lag}	USI enable lag time	12.5	-	ns
T_{OD}	USI output data valid time	-	30	ns

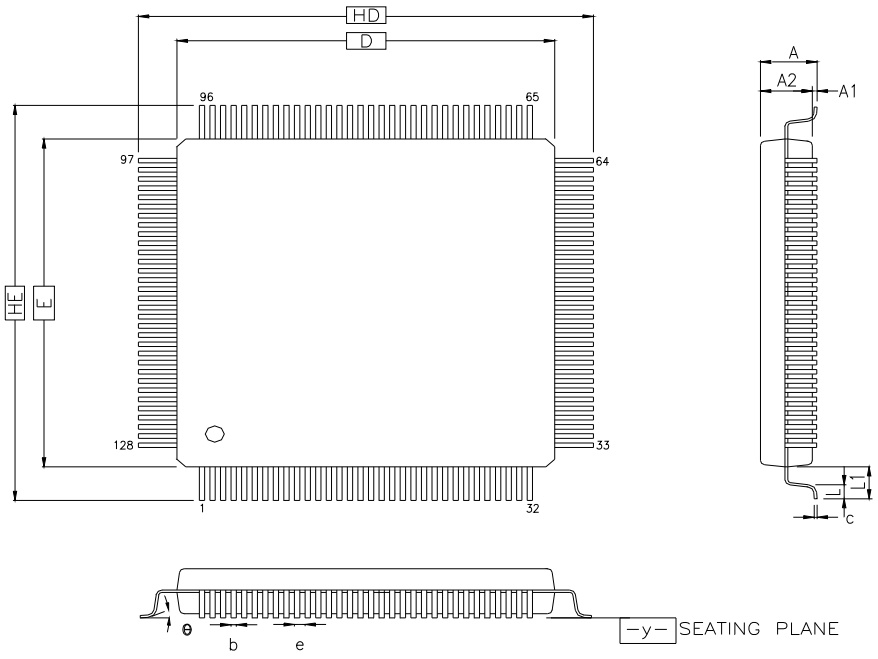
6.3.8 PS2 Interface AC Characteristics



SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T1	Time from DATA transition to falling edge of CLK	5	25	us
T2	Time form rising edge of CLK to DATA transition	5	T4-5	us
T3	Duration of CLK inactive	30	50	us
T4	Duration of clock active	30	50	us
T5	Time to auxiliary device inhibit after clock 11 to ensure the auxiliary device does not start another transmission	0	50	us
T7	Duration of CLK inactive	30	50	us
T8	Duration of CLK active	30	50	us
T9	Time to fom inactive to active CLK transition, used to time when the auxiliary device samples DATA	30	50	us

7. PACKAGE SPECIFICATIONS

128L LQFP (14X14X1.4 mm footprint 2.0mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

8. ORDERING INFORMATION

PART NUMBER	NAME	PACKAGE DESCRIPTION
NUC745ADN	LQFP128	128 Leads, body 14 x 14 x 1.4 mm, Green package

9. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	March 03, 2009	-	Initial Issued

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.