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32-BIT ARM926EJS-BASED MCU

NUC910ABN
32-bit ARM926EJ-S Microcontroller
Product Data Sheet

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1. GENERAL DESCRIPTION

This chip is built around an outstanding CPU core: the 16/32 ARM926EJ-S RISC processor designed by Advanced RISC Machines, Ltd. The ARM926EJ-S core, offers 8K-byte I-cache and 8K-byte D-cache with MMU, is a low power, general-purpose integrated circuits. One 10/100 Mb MAC of Ethernet controller is built-in to reduce total system cost. A TFT type LCD controller, ADC touch screen controller and 2D graphics engine with various integrated on chip functions, this micro-controller is suitable for a high end, high performance and low cost related products as well as general purpose applications.

The following integrated on-chip functions are described in detail in this document.

	Main Function
CPU	• ARM926EJ-S
Platform	• Programmable PLL System Clock Synthesizer
	• AMBA Peripherals
	• Timer, Watchdog Timer
	• Advanced Interrupt Controller
	• General DMA Controller
	• External Bus Interface Controller
Networking	• Ethernet MAC Controller
Analog	• 10-bit ADC (Touch Screen)
Display Interface	• LCD Controller
Graphics	• 2D Graphic Engine
Audio Interface	• 2-Channel I2S Controller
	• 2-Channel AC97 Controller
USB Interface	• USB 1.1/2.0 High/Full/Low Speed Host Controller
	• USB 2.0 High/Full Speed Device Controller
Storage Interface	• NAND Flash Controller with ECC1/ECC4
	• SD/SDIO/MMC Controller
	• Memory Stick (MS) Controller
	• ATAPI Controller
	• Smart Card Controller
Peripheral & Misc.	• GPIO

	Main Function
	• 4-Channel PWM
	• UART/HS-UART
	• USI (SPI/uWire)
	• I2C (Master) Controller
	• Keypad Scan Controller
	• RTC (Real Time Clock)
	• PS2 Controller

2. FEATURES

Architecture

- Efficient and powerful ARM926EJ-S core with fully 16/32-bit RISC architecture
- Little Endian mode supported
- 8K-byte I-cache and 8K-byte D-cache with MMU
- Cost-effective JTAG-based debug solution

Power management

- Programmable clock enable for individual peripherals
- IDLE mode to halt ARM Core and keep peripheral working
- Power-Down mode to stop all clocks included external crystal oscillator.
- Exit IDLE/Power-Down by interrupts
- Wakeup by interrupt, USB device, and RTC

Two PLLs

- The external clock can be multiplied by on-chip PLL to provide high frequency system clock
- The input frequency range is 4-30MHz; 15MHz is preferred.
- Programmable clock frequency

Advanced Interrupt Controller

- 31 interrupt sources, including 8 external interrupt sources
- Programmable normal or fast interrupt mode (IRQ, FIQ)
- Programmable as either edge-triggered or level-sensitive for 8 external interrupt sources
- Programmable as either low-active or high-active for 8 external interrupt sources
- Priority methodology is encoded to allow for interrupt daisy-chaining
- Automatically mask out the lower priority interrupt during interrupt nesting
- Automatically clear the interrupt flag when the interrupt source is programmed to be edge-triggered

General DMA Controller

- 2-channel General DMA for memory-to-memory data transfers without CPU intervention
- Support two external DMA request
- Increments or decrements a source or destination address in 8-bit, 16-bit or 32-bit data transfers

- 8-data burst mode

External Bus Interface

- 8/16/32-bit external bus support for ROM/SRAM, flash memory, SDRAM and external I/Os
- Programmable access cycle (0-7 wait cycle)
- Four-word depth write buffer

Ethernet MAC Controller

- 100/10-Mbps operation
- DMA engine with burst mode
- MAC Tx/Rx buffers (256 bytes Tx, 256 bytes Rx)
- Full compliance with IEEE standard 802.3
- RMII interface only
- Station Management Signaling
- On-Chip CAM (up to 16 destination addresses)
- Full-duplex mode with PAUSE feature
- Long/short packet modes

ADC Interface

- Power supply voltage: 3.3V
- 8 analog input with voltage range: 0 – 3.3 volts
- Touch screen semi-auto/auto conversion modes supported
- Waiting for trigger mode supports
- standby mode supports
- 4-level voltage detector

LCD Controller

- Support the 8/12/16/18/24-bit data interface to connect with 80/68 series MPU type LCM module
- Convert RGB-565, RGB-888X, YUV-422 display data to RGB-444, RGB-565, RGB-666, RGB-888, YUV-422 color format for display output
- Support CCIR-656(with vsync / hsync / data enable sync signal) 8/16-bit YUV data output format to connect with external TV encoder
- Support 8/16 bpp OSD data with Image overlay function to facilitate the diverse graphic UI.
- Support linear 1X – 8X image scaling up function.
- Support Picture-In-Picture display function

- Support hardware cursor.

2-D Graphics Engine

- Color depth 8-bit/16-bit/32-bit in RGB domain or RGB332/RGB565/RGB888 are supported
- Contains 2D Bit Block Transfer (BitBLT) functions as defined in Microsoft GDI. It includes HostBLT, Pattern BLT, Color/Font Expanding BLT, Transparent BLT, Tile BLT, Block Move BLT, Copy File BLT, Color/Font Expansion, and Rectangle Fill, etc.
- Supports fore/background colors and all Microsoft 256 ternary raster-operation codes (ROP)
- Clipping window can be defined as inside or outside clipping
- Implements the alpha-blending function for source/destination picture overlaying
- Fast Bresenham line drawing algorithm is used to draw solid/textured lines
- Supports rectangular border or frame drawing
- Supports picture re-sizing by 1/255 ~ 254/255 down-scaling and 1 ~ 1.996 up-scaling (1+254/255).
- Supports object rotations in different degrees, that is L45/L90/R45/R90/M180/F180/X180, where
  - L45/L90 means rotate left 45/90 degrees,
  - R45/R90 means rotate right 45/90 degrees,
  - M180 means mirror (flop),
  - F180 means up-side-down (flip) and X180 for rotations by 180 degrees

2-Channel AC97 / I2S Controller

- Support I2S interface.
- Support AC97 interface.
- Built-in an 8x32 bits internal buffer.
- Support DMA function for data transfer between internal buffer and system memory.
- Support 16-bit I2S and MSB-justified format.

USB Host Controller with transceiver

- Fully compliant with USB Revision 2.0 specification.
- Enhanced Host Controller Interface (EHCI) Revision 1.0 compatible.
- Open Host Controller Interface (OHCI) Revision 1.0 compatible.
- Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt, Isochronous and Split transfers.
- Built-in DMA for real-time data transfer.
- Support two ports (one port transceiver is shared with USB Device Controller)

USB Device Controller with transceiver

- Compliant with USB version 2.0 specification.
- Software control for device remote-wakeup.
- Supports 6 configurable IN/OUT endpoints in addition to Control Endpoint. Each of these endpoints can be configures as IN or OUT with Isochronous, Bulk or Interrupt transfer.
- Three different modes of operation of an in-endpoint (Auto validation mode, manual validation mode, Fly mode.
- Supports Endpoint Maximum Packet Size up to 1024 bytes.

ATAPI Interface Controller

- ATAPI I/O Interface, ATA/ATAPI-6 compatible
- Provide register transfer mode for read/write device command block registers
- Provide PIO data transfer mode
- Provide Multiword DMA data transfer mode
- Provide Ultra-DMA data transfer mode

Flash Memory Interface (FMI)

- Directly connect to Secure Digital (SD, MMC and SDIO) flash memory card, Memory Stick (Memory stick PRO) and NAND type flash memory.
- Supports DMA function to accelerate the data transfer between the internal buffer, external SDRAM, and flash memory card.
- Two 512 bytes internal buffers are embedded inside

Smart Card Host Interface (SCHI)

- ISO-7816 compliant
- PC/SC T=0, T=1 compliant
- 16-byte transmitter FIFO and 16-byte receiver FIFO
- FIFO threshold interrupt to optimize system performance
- Programmable transmission clock frequency
- Versatile baud rate configuration
- UART-like register file structure
- General-purpose C4, C8 channels

PS2 Host Interface

- PS2 compatible keyboard or mouse interface
- Half-Duplex Bi-directional synchronous serial interface using op-drain outputs for clock and data
- Odd parity generation and checking

I2C Master

- Compatible with I^2C standard, support master mode only
- Multi Master Operation
- Clock stretching and wait state generation
- Provide multi-byte transmit operation, up to 4 bytes can be transmitted in a single transfer
- Software programmable acknowledge bit
- Arbitration lost interrupt, with automatic transfer cancellation
- Start/Stop/Repeated Start/Acknowledge generation
- Start/Stop/Repeated Start detection
- Bus busy detection
- Supports 7 bit addressing mode
- Software mode I^2C

Universal Serial Interface (USI)

- Support MICROWIRE/SPI master mode
- Support full/half duplex synchronous serial data transfer
- Variable length of transfer word up to 32 bits
- Provide burst mode operation, transmit/receive can be executed up to four times in one transfer
- MSB or LSB first data transfer
- Receive and Transmit on both rising or falling edge of serial clock independently

UART

- Five UART (serial I/O) blocks with interrupt-based operation
- Support for 5-bit, 6-bit, 7-bit or 8-bit serial data transmit and receive
- Programmable baud rates
- 1,1½ or 2 stop bits
- Odd or even parity
- Break generation and detection
- Parity, overrun and framing error detection
- X16 clock mode
- Support for Bluetooth, IrDA, Micro-printer control and two debug ports

Timers

- Five programmable 24-bit timers with 8-bit pre-scalar
- One programmable 20-bit Watchdog timer
- One-short mode, period mode or toggle mode operation

4-Channel PWM

- Four 16-bit timers
- Two 8-bit pre-scalars & Two 4-bit divider
- Programmable duty control of output waveform (PWM)
- Auto reload mode or one-shot pulse mode
- Dead-zone generator

Real Time Clock (RTC)

- Time counter (second, minute, hour) and calendar counter (day, month, year)
- Alarm register (second, minute, hour, day, month, year)
- 12 or 24-hour mode selectable
- Recognize leap year automatically
- Day of the week counter
- Frequency compensate register (FCR)
- Beside FCR, all clock and alarm data expressed in BCD code
- Support tick time interrupt

Keypad Scan Interface

- Scan up to 16x8 with an external 4 to 16 decoder; or 4x8 array without auxiliary component

- Programmable de-bounce time
- One or two keys scan with interrupt and three keys reset function.
- Support low power wakeup function

Programmable I/Os

- Pins individually configurable to input, output or I/O mode for dedicated signals
- I/O ports are Programmable and Configurable for Multiple functions

Operation Voltage Range

- VDD18 for IO Buffer: 1.8V+/-10%
- VDD33 for Core Logic: 3.3V+/-10%
- USBVDDC0/USBVDDC1/USBVDDT0/USBVDDT1 for USB: 3.3V+/-5%
- AVDD33 for ADC: 3.3V+/-10%
- RTCVDD18 for RTC: 1.8V+/-10%
- PLLVDD18 for PLL: 1.8V+/-10%

Operation Temperature Range

- -40 ~ 85 °C

Operating Frequency

- Up to 200 MHz for ARM926EJ-S CPU

Package Type

- 324-ball PBGA, Pb free, Halogen free

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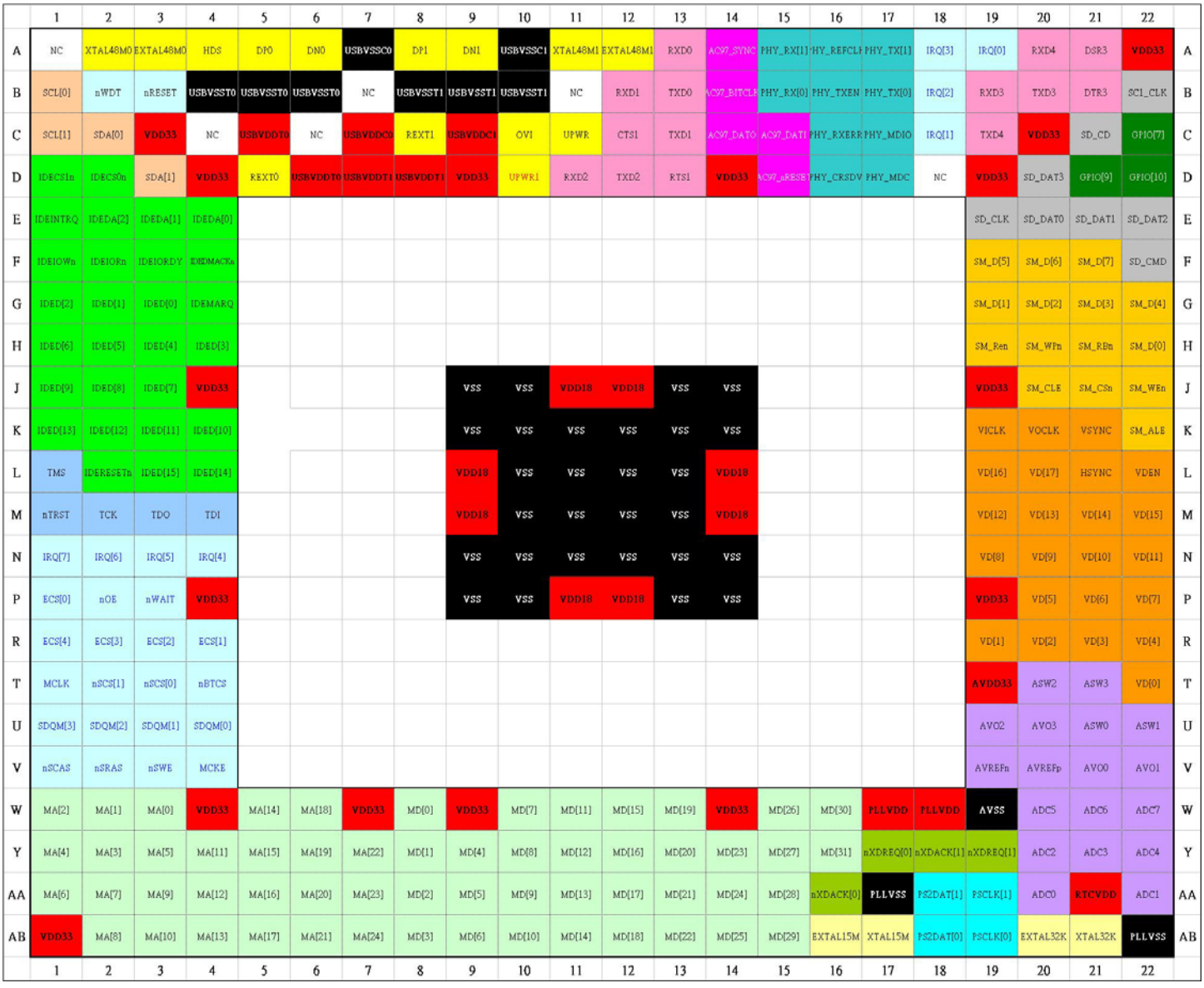
3. PIN DIAGRAM

NUC910 Pin Diagram



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	NC	XTAL48M0	EXTAL48M0	HDS	DP0	DN0	USBVSSC0	DP1	DN1	USBVSSC1	XTAL48M1	EXTAL48M1	RXD0	AC97_SYNC	PHY_RX[1]	HY_REFCLK	PHY_TX[1]	IRQ[3]	IRQ[0]	RXD4	DSR3	VDD33	A
B	SCL[0]	nWDT	nRESET	USBVSST0	USBVSST0	USBVSST0	NC	USBVSST1	USBVSST1	USBVSST1	NC	RXD1	TXD0	AC97_BITCLK	PHY_RX[0]	PHY_TXEN	PHY_TX[0]	IRQ[2]	RXD3	TXD3	DTR3	SCI_CLK	B
C	SCL[1]	SDA[0]	VDD33	NC	USBVDDT0	NC	USBVDDC0	REXT1	USBVDDC1	OVI	UPWR	CTS1	TXD1	AC97_DAT0	AC97_DAT1	PHY_RXERR	PHY_MDIO	IRQ[1]	TXD4	VDD33	SD_CD	GPIO[7]	C
D	IDECS1n	IDECS0n	SDA[1]	VDD33	REXT0	USBVDDT0	USBVDDT1	USBVDDT1	VDD33	UPWR1	RXD2	TXD2	RTS1	VDD33	AC97_nRESET	PHY_CRSDV	PHY_MDC	NC	VDD33	SD_DAT3	GPIO[9]	GPIO[10]	D
E	IDEINTRQ	IDEDA[2]	IDEDA[1]	IDEDA[0]															SD_CLK	SD_DAT0	SD_DAT1	SD_DAT2	E
F	IDEIOWn	IDEIORn	IDEIORDY	IDEDMACKn															SM_D[5]	SM_D[6]	SM_D[7]	SD_CMD	F
G	IDED[2]	IDED[1]	IDED[0]	IDEDMARQ															SM_D[1]	SM_D[2]	SM_D[3]	SM_D[4]	G
H	IDED[6]	IDED[5]	IDED[4]	IDED[3]															SM_Ren	SM_WPn	SM_RBn	SM_D[0]	H
J	IDED[9]	IDED[8]	IDED[7]	VDD33					VSS	VSS	VDD18	VDD18	VSS	VSS					VDD33	SM_CLE	SM_CSn	SM_WEn	J
K	IDED[13]	IDED[12]	IDED[11]	IDED[10]					VSS	VSS	VSS	VSS	VSS	VSS					VICLK	VOCLK	VSYNC	SM_ALE	K
L	TMS	IDERESETn	IDED[15]	IDED[14]					VDD18	VSS	VSS	VSS	VSS	VDD18					VD[16]	VD[17]	HSYNC	VDEN	L
M	nTRST	TCK	TDO	TDI					VDD18	VSS	VSS	VSS	VSS	VDD18					VD[12]	VD[13]	VD[14]	VD[15]	M
N	IRQ[7]	IRQ[6]	IRQ[5]	IRQ[4]					VSS	VSS	VSS	VSS	VSS	VSS					VD[8]	VD[9]	VD[10]	VD[11]	N
P	ECS[0]	nOE	nWAIT	VDD33					VSS	VSS	VDD18	VDD18	VSS	VSS					VDD33	VD[5]	VD[6]	VD[7]	P
R	ECS[4]	ECS[3]	ECS[2]	ECS[1]															VD[1]	VD[2]	VD[3]	VD[4]	R
T	MCLK	nSCS[1]	nSCS[0]	nBTCS															AVDD33	ASW2	ASW3	VD[0]	T
U	SDQM[3]	SDQM[2]	SDQM[1]	SDQM[0]															AVO2	AVO3	ASW0	ASW1	U
V	nSCAS	nSRAS	nSWE	MCKE															AVREFn	AVREFp	AVO0	AVO1	V
W	MA[2]	MA[1]	MA[0]	VDD33	MA[14]	MA[18]	VDD33	MD[0]	VDD33	MD[7]	MD[11]	MD[15]	MD[19]	VDD33	MD[26]	MD[30]	PLLVDD	PLLVDD	AVSS	ADC5	ADC6	ADC7	W
Y	MA[4]	MA[3]	MA[5]	MA[11]	MA[15]	MA[19]	MA[22]	MD[1]	MD[4]	MD[8]	MD[12]	MD[16]	MD[20]	MD[23]	MD[27]	MD[31]	nXDREQ[0]	nXDACK[1]	nXDREQ[1]	ADC2	ADC3	ADC4	Y
AA	MA[6]	MA[7]	MA[9]	MA[12]	MA[16]	MA[20]	MA[23]	MD[2]	MD[5]	MD[9]	MD[13]	MD[17]	MD[21]	MD[24]	MD[28]	nXDACK[0]	PLLVSS	PS2DAT[1]	PSCLK[1]	ADC0	RTCVDD	ADC1	AA
AB	VDD33	MA[8]	MA[10]	MA[13]	MA[17]	MA[21]	MA[24]	MD[3]	MD[6]	MD[10]	MD[14]	MD[18]	MD[22]	MD[25]	MD[29]	EXTAL15M	XTAL15M	PS2DAT[0]	PSCLK[0]	EXTAL32K	XTAL32K	PLLVSS	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

4. PIN ASSIGNMENT

Table 4.1 NUC910 Pins Assignment

Pad Name	NUC910
Clock & Reset	**(9 pins)**
EXTAL15M	AB16
XTAL15M	AB17
EXTAL48M0	A3
XTAL48M0	A2
EXTAL48M1	A12
XTAL48M1	A11
EXTAL32K	AB20
XTAL32K	AB21
nRESET	B3
TAP Interface	**(5 pins)**
TMS	L1
TDI	M4
TDO	M3
TCK	M2
nTRST	M1
External Bus Interface	**(76 pins)**
MA [24:0]	AB7,AA7,Y7,AB6,AA6,Y6,W6,AB5,AA5,Y5,W5,AB4,AA4,Y4, AB3,AA3,AB2,AA2,AA1,Y3,Y1,Y2,W1,W2,W3
MD [31:0]	Y16,W16,AB15,AA15,Y15,W15,AB14,AA14,Y14,AB13, AA13, Y13, W13, AB12, AA12, Y12, W12, AB11, AA11, Y11, W11,AB10,AA10,Y10,W10,AB9, AA9,Y9,AB8,AA8,Y8,W8
nWBE [3:0] / SDQM [3:0]	U1,U2,U3,U4
nSCS [1:0]	T2,T3
nSRAS	V2
nSCAS	V1
MCKE	V4
nSWE	V3
MCLK	T1
nWAIT	P3
nBTCS	T4
nECS [4:0]	R1,R2,R3,R4,P1
nOE	P2

Pad Name	NUC910
Ethernet Interface	**(10 pins)**
PHY_MDC / **GPIOF[0]**	D17
PHY_MDIO / **GPIOF[1]**	C17
PHY_TXD [1:0] / **GPIOF[3:2]**	A17–B17
PHY_TXEN / **GPIOF[4]**	B16
PHY_REFCLK / **GPIOF[5]**	A16
PHY_RXD [1:0] / **GPIOF[7:6]**	A15–B15
PHY_CRSDV / **GPIOF[8]**	D16
PHY_RXERR / **GPIOF[9]**	C16
AC97/I2S/PWM	**(5 pins)**
AC97_nRESET / **I2S_SYSCLK /** **- /** **GPIOG[12]**	D15
AC97_DATAI / **I2S_DATAI /** **PWM [0] /** **GPIOG[13]**	C15
AC97_DATAO / **I2S_DATAO /** **PWM [1] /** **GPIOG[14]**	C14
AC97_SYNC / **I2S_WS /** **PWM [2] /** **GPIOG[15]**	A14
AC97_BITCLK / **I2S_BITCLK /** **PWM [3] /** **GPIOG[16]**	B14

Pad Name	NUC910
USB Interface	**(11 pins)**
DP0	A5
DN0	A6
REXT0	D5
UATEST0	C6
UPWR0	C11
OVI	C10
HDS	A4
DP1	A8
DN1	A9
REXT1	C8
UPWR1	D10
I2C/USI(SPI/MW)	**(4 pins)**
SCL0 / SFRM / GPIOG[0]	B1
SDA0 / SSPTXD / GPIOG[1]	C2
SCL1 / SCLK / GPIOG[2]	C1
SDA1 / SSPRXD / GPIOG[3]	D3

Pad Name	NUC910
External DMA / SD1 Interface / Memory Stick 1	**(4 pins)**
nXDREQ[0] / GPIOG[4] / SD1_CDn / MS1_CDn	Y17
nXDACK[0] / GPIOG[5] / SD1_nPWR / MS1_nPWR	AA16
nXDREQ[1] / GPIOG[6] / SD1_CMD / MS1_BS	Y19
nXDACK[1] / GPIOG[7] / SD1_CLK / MS1_CLK	Y18
PS2 / SD1 Interface / Memory Stick 1	**(4 pins)**
PS2CLK[0] / GPIOG[8] / SD1_DAT0 / MS1_DAT0	AB19
PS2DATA[0] / GPIOG[9] / SD1_DAT1 / MS1_DAT0	AB18
PS2CLK[1] / GPIOG[10] / SD1_DAT2 / MS1_DAT2	AA19
PS2DATA[1] / GPIOG[11] / SD1_DAT3 / MS1_DAT3	AA18

Pad Name	NUC910
UART	**(14 pins)**
TXD0 / GPIOE[0]	B13
RXD0 / GPIOE[1]	A13
TXD1(B) / GPIOE[2]	C13
RXD1(B) / GPIOE[3]	B12
RTS1 (B) / GPIOE[4]	D13
CTS1 (B) / GPIOE[5]	C12
TXD2(IrDA) / DTR1 / GPIOE[6]	D12
RXD2(IrDA) / DSR1 / GPIOE[7]	D11
TXD3(M) / GPIOE[8]	B20
RXD3(M) / GPIOE[9]	B19
DTR3(M) / GPIOE[10]	B21
DSR3(M) / GPIOE[11]	A21
TXD4 / RIn1 / GPIOE[12]	C19
RXD4 / CDn1 / GPIOE[13]	A20

Pad Name	NUC910
Smart Card/ SCHI/SDIO/ Memory Stick 0 /	(11pins)
SC0_DAT / SD0_CMD / MS0_BS / GPIOD[0]	F22
SC0_CLK / SD0_CLK / MS0_CLK / GPIOD[1]	E19
SC0_RST / SD0_DAT0 / MS0_DAT0 / GPIOD[2]	E20
SC0_PRES / SD0_DAT1 / MS0_DAT1 / GPIOD[3]	E21
SC0_nPWR / SD0_DAT2 / MS0_DAT2 / GPIOD[4]	E22
SC1_DAT / SD0_DAT3 / MS0_DAT3 / GPIOD[5]	D20
SC1_RST / SD0_CDn / MS0_CDn / GPIOD[6]	C21
SC1_nPWR / GPIOD[7]	C22
SC1_CLK / SD0_nPWR / MS0_nPWR / GPIOD[8]	B22

SC1_PRES / GPIOD[9]	D21
Pad Name	**NUC910**
NAND Flash(SM) / KPI / LCD	**(15pins)**
SM_CSn / KPI_ROW[0] / VD[18] / GPIOC[0]	J21
SM_ALE / KPI_ROW[1] / VD[19] / GPIOC[1]	K22
SM_CLE / KPI_ROW[2] / VD[20] / GPIOC[2]	J20
SM_WEn / KPI_ROW[3] / VD[21] / GPIOC[3]	J22
SM_REn / VD[22] / GPIOC[4]	H19
SM_WPn / VD[23] / GPIOC[5]	H20
SM_RBn / GPIOC[6] /	H21
SM_D[7:0] / KPI_COL[7:0] / GPIOC[14:7]	F21,F20,F19,G22,G21,G20,G19,H22
SM_CSn1 / GPIOC[15]	D22

Pad Name	NUC910
LCD	**(23 pins)**
VD [17:0]	L20,L19,M22,M21,M20,M19,N22,N21,N20,N19,P22,P21, P20,R22,R21,R20,R19,T22
HSYNC	L21
VSYNC	K21
VDEN	L22
VICLK	K19
VOCLK	K20
IDE Interface	**(28 pins)**
IDECS0n / GPIOI[0]	D2
IDECS1n / GPIOI[1]	D1
IDEDA [2:0] / GPIOI[4:2]	E2,E3,E4
IDEINTRQ / GPIOI[5]	E1
IDEDMACKn / GPIOI[6]	F4
IDEIORDY / GPIOI[7]	F3
IDEIORn / GPIOI[8]	F2
IDEIOWn / GPIOI[9]	F1
IDEDMARQ / GPIOI[10]	G4
IDEDD[15:12] / GPIOI[14:11]	L3,L4,K1,K2
IDERESETn / GPIOI[15]	L2
IDEDD[7:0] / KPI_COL[7:0]	J3,H1,H2,H3,H4,G1,G2,G3
IDEDD[11:8] / KPI_ROW[3:0]	K3,K4,J1,J2

Pad Name	NUC910
ADC Interface	**(18 pins)**
ADC[7:0]	W22, W21, W20, Y22, Y21, Y20, AA22, AA20
AVREFp	V20
AVREFn	V19
AVO[3:0]	U20,U19,V22,V21
ASW[3:0]	T21,T20,U22,U21
Miscellaneous	**(10 pins)**
nIRQ [7:0] / GPIOH[7:0]	N1,N2,N3,N4,A18,B18,C18,A19
nWDOG / GPIOI[16]	B2
Power/Ground	**(73 pins)**
VDD18	J11,J12,L9,L14,M9,M14,P11,P12
VDD33	A22,C3,C20,D4,D9,D14,D19,J4,J19,P4,P19,W4,W7,W9, W14,AB1
VSS	J9,J10,J13,J14,K9–K14,L10–L13,M10–M13,N9-N14,P9, P10,P13,P14
USBVDDC0 (3.3V)	C7
USBVSSC0	A7
USBVDDT0 (3.3V)	C5,D6,
USBVSST0	B4,B5,B6
USBVDDC1 (3.3V)	C9
USBVSSC1	A10
USBVDDT1 (3.3V)	D7,D8
USBVSST1	B8,B9,B10
AVDD33	T19
AVSS	W19
RTCVDD18	AA21
PLLVDD18	W17,W18
PLLVSS	AA17,AB22
NC	A1,C4,B7,B11, D18

5. PIN DESCRIPTION

5.1 Pin Description for Interface

Pin Name	IO Type	Description
Clock & Reset (9)		
EXTAL15M	I	15MHz External Clock / Crystal Input for Both PLLs
XTAL15M	O	15MHz Crystal Output
EXTAL48M0	O	48MHz Crystal Output for USB2.0 PHY0
XTAL48M0	I	48MHz Crystal Input for USB2.0 PHY0
EXTAL48M1	O	48MHz Crystal Output for USB2.0 PHY1 (Optional)
XTAL48M1	I	48MHz Crystal Input for USB2.0 PHY1 (Optional)
EXTAL32K	I	32768Hz External Clock / Crystal Input for RTC
XTAL32K	O	32768Hz Crystal Output for RTC
nRESET	I	System Reset (Low active)
TAP Interface (5)		
TCK	ID	JTAG Test Clock, internal pull-down
TMS	IU	JTAG Test Mode Select, internal pull-up
TDI	IU	JTAG Test Data in, internal pull-up
TDO	O	JTAG Test Data out
nTRST	IU	JTAG Reset, active-low, internal pull-up
External Bus Interface (76)		
MA [24:0]	O	Address Bus of external memory and IO devices. (MA[21:13] are set to input mode when nRESET low active)
MD [31:0]	IO (D)	Data Bus of external memory and IO device (Pull-down are programmable)
nWBE [3:0] / SDQM [3:0]	O	Write Byte Enable for specific device (nECS [4:0]). Data Bus Mask signal for SDRAM (nSCS [1:0]), (Low active)
nSCS [1:0]	O	SDRAM chip select for two external banks, (Low active)
nSRAS	O	Row Address Strobe for SDRAM, (Low active)
nSCAS	O	Column Address Strobe for SDRAM, (Low active)
nSWE	O	SDRAM Write Enable, (Low active)
MCKE	O	SDRAM Clock Enable
MCLK	O	System Master Clock Out, SDRAM clock
nWAIT	IU	External Wait, (Low active), internal pull-up
nBTCS	O	ROM/Flash Chip Select, (Low active)
nECS [4:0]	O	External I/O Chip Select, (Low active)

nOE	O	ROM/Flash, External Memory Output Enable, (Low active)
Ethernet RMII Interface (10)		
PHY_MDC	O(IS)	RMII Management Data Clock
PHY_MDIO	IO(D)	RMII Management Data I/O (Pull-down is programmable)
PHY_TXD [1:0]	O(ID)	RMII Transmit Data bus (Pull-down are programmable)
PHY_TXEN	O(ID)	RMII Transmit Enable (Pull-down is programmable)
PHY_REFCLK	O(ID)	RMII Reference Clock. (Pull-down is programmable)
PHY_RXD [1:0]	I(OD)	RMII Receive Data bus (Pull-down are programmable)
PHY_CRSDV	I(OD)	RMII Carrier Sense / Receive Data Valid (Pull-down is programmable)
PHY_RXERR	I(OD)	RMII Receive Data Error (Pull-down is programmable)

AC97/I2S/PWM (5)		
AC97_nRESET / I2S_SYSCLK	O(ID)	AC97 Controller RESET Output. I2S Controller System Clock Output. (Pull-down is programmable)
AC97_DATAI / I2S_DATAI / PWM [0]	IO(D)	AC97 Controller Data Input. I2S Controller Data Input. PWM Channel 0 Output. (Pull-down is programmable)
AC97_DATAO / I2S_DATAO / PWM [1]	O(ID)	AC97 Controller Data Output. I2S Controller Data Output. PWM Channel 1 Output. (Pull-down is programmable)
AC97_SYNC / I2S_WS / PWM [2]	IO(D)	AC97 Controller Synchronous Pulse Output. I2S Controller Word Select. PWM Channel 2 Output. (Pull-down is programmable)
AC97_BITCLK / I2S_BITCLK / PWM [3]	IOSD	AC97 Controller Bit Clock Input. I2S Controller Bit Clock. PWM Channel 3 Output. (Pull-down with Schmitt trigger input)
USB Interface (11)		
DP0	IO	Differential Positive USB Port0 IO signal

DN0	IO	Differential Negative USB Port0 IO signal
REXT0	A	External Resister Connect for Port0
UATEST0	A	USB PHY 0 Analog Test pin (NC in normal operation)
DP1	IO	Differential Positive USB Port1 IO signal
DN1	IO	Differential Negative USB Port1 IO signal
REXT1	A	External Resister Connect for Port1
UPWR1	O	USB Port1 Power Control signal
OVI	I	USB Over Current Detection signal
HDS	I	USB PHY 0 Device/Host Mode Select Control signal
UPWR	O	USB Port0 Power Control signal This pin is always driven to Low when USB Port0 is at Device mode (the HDS pin at high state)
I2C/USI(SPI/MW) Interface (4)		
SCL0 / SFRM	IOS	I2C Serial Clock Line 0. USI Serial Frame. (Input with Schmitt trigger)
SDA0 / SSPTXD	IOS	I2C Serial Data Line 0. USI Serial Transmit Data. (Input with Schmitt trigger)
SCL1 / SCLK	IOS	I2C Serial Clock Line 1. USI Serial Clock. (Input with Schmitt trigger)
SDA1 / SSPRXD	IOS	I2C Serial Data Line 1. USI Serial Receive Data. (Input with Schmitt trigger)

PS2 Keyboard/Mouse/SD1 Interface (4)		
PS2CLK0 / SD1_DAT0 / MS1_DAT0	IOS	PS2 Port0 Clock SD/SDIO Mode #1 – Data Line Bit 0 Memory Stick Mode #1 – Data Line Bit 0 (Input with Schmitt trigger)
PS2DATA0 / SD1_DAT1 / MS1_DAT1	IO(U)	PS2 Port0 Data SD/SDIO Mode #1 – Data Line Bit 1 Memory Stick Mode #1 – Data Line Bit 1 (Pull-up is programmable)
PS2CLK1 / SD1_DAT2 / MS1_DAT2	IOS	PS2 Port1 Clock SD/SDIO Mode #1 – Data Line Bit 2 Memory Stick Mode #1 – Data Line Bit 2 (Input with Schmitt trigger)
PS2DATA1 / SD1_DAT3 / MS1_DAT3	IO(U)	PS2 Port1 Data SD/SDIO Mode #1 – Data Line Bit 3 Memory Stick Mode #1 – Data Line Bit 3 (Pull-up is programmable)
Keypad Interface (KPI) (12)		
KPI_COL[7:0]	I	Keypad Column Scan Input Bus This bus is shared with NAND Flash Interface or IDE Interface, which is programmable setting.
KPI_ROW[3:0]	O	Keypad Row Scan Output Bus This bus is shared with NAND Flash Interface or IDE Interface, which is programmable setting.
UART0/UART1/UART2/UART3/UART4 Interface (14)		
TXD0	IO(D)	UART0 Transmit Data. (Pull-down is programmable)
RXD0	IO(D)	UART0 Receive Data. (Pull-down is programmable)
TXD1(B)	IO(D)	UART1 Transmit Data for Bluetooth (Pull-down is programmable)
RXD1(B)	IO(D)	UART1 Receive Data for Bluetooth (Pull-down is programmable)
CTS1 (B)	IO(D)	UART1 Clear To Send for Bluetooth (Pull-down is programmable)
RTS1 (B)	IO(D)	UART1 Request To Send for Bluetooth (Pull-down is programmable)
TXD2(IrDA) / DTR1	IO(D)	UART2 Transmit Data supporting SIR IrDA. UART1 Data Terminal Ready (Pull-down is programmable)

RXD2(IrDA) / DSR1	IO(D)	UART2 Receive Data supporting SIR IrDA. UART1 Data Set Ready
TXD3(M)	IO(U)	UART3 Transmit Data for Micro Printer (Pull-up is programmable)
RXD3(M)	IO(U)	UART3 Receive Data for Micro Printer (Pull-up is programmable)
DTR3(M)	IO(U)	UART3 Data Terminal Ready for Micro Printer (Pull-up is programmable)
DSR3(M)	IO(U)	UART3 Data Set Ready for Micro Printer (Pull-up is programmable)
TXD4 / RIn1	IO(U)	UART4 Transmit Data. UART1 Ring Indicator (Pull-up is programmable)
RXD4 / CDn1	IO(U)	UART4 Receive Data. UART1 Carrier Detector (Pull-up is programmable)
Smart Card/SD/SDIO/Memory Stick Interface (10)		
SC0_DAT / SD0_CMD / MS0_BS	IO(U)	Smart Card I/O Contact to Card 0. SD/SDIO Mode #0 – Command/Response (SPI Mode – Data In) Memory Stick Mode #0 – Bus State. (Pull-up is programmable)
SC0_CLK / SD0_CLK / MS0_CLK	IO(U)	Smart Card Clock Output to Card 0. SD/SDIO Mode #0 – Clock; (SPI Mode – Clock) Memory Stick Mode #0 – Clock (Pull-up is programmable)
SC0_RST / SD0_DAT0 / MS0_DAT0	IO(U)	Smart Card Reset Output to Card 0. SD/SDIO Mode #0 – Data Line Bit 0; Memory Stick Mode #0 – Data Line Bit 0; (Pull-up is programmable)
SC0_PRES / SD0_DAT1 / MS0_DAT1	IO(U)	Smart Card 0 Presence Contact Input. SD/SDIO Mode #0 – Data Line Bit 1; Memory Stick Mode #0 – Data Line Bit 1; (Pull-up is programmable)
SC0_nPWR / SD0_DAT2 / MS0_DAT2	IO(U)	Smart Card 0 Power FET Control Signal Output. SD/SDIO Mode #0 – Data Line Bit 2; Memory Stick Mode #0 – Data Line Bit 2; (Pull-up is programmable)

SC1_DAT / SD0_DAT3 / MS0_DAT3	IO(U)	Smart Card I/O Contact to Card 1. SD/SDIO Mode #0 – Data Line Bit 3; Memory Stick Mode #0 – Data Line Bit 3; (Pull-up is programmable)
SC1_CLK	IO(U)	Smart Card Clock Output to Card 1. (Pull-up is programmable)
SC1_RST / SD0_CDn / MS0_CDn	IO(U)	Smart Card Reset Output to Card 1. SD/SDIO Mode #0 – Card Detect. Memory Stick Mode #0 – Card Detect. (Pull-up is programmable)
SC1_PRES	IO(U)	Smart Card 1 Presence Contact Input. (Pull-up is programmable)
SC1_nPWR	IO(U)	Smart Card 1 Power FET Control Signal Output. (Pull-up is programmable)
NAND Flash Interface (16)		
SM_CSn	O(IU)	NAND Flash Chip Select (Pull-up is programmable)
SM_CS1n	O(IU)	NAND Flash Chip Select #1 (Pull-up is programmable)
SM_ALE	O(IU)	NAND Flash Address Latch Enable (Pull-up is programmable)
SM_CLE	O(IU)	NAND Flash Command Latch Enable (Pull-up is programmable)
SM_WEn	O(IU)	NAND Flash Write Enable (Low active) (Pull-up is programmable)
SM_REn	O(IU)	NAND Flash Read Enable (Low active) (Pull-up is programmable)
SM_WPn	O(IU)	NAND Flash Write Protect (Low active) (Pull-up is programmable)
SM_RBn	I(OU)	NAND Flash Busy (Low active) (Pull-up is programmable)
SM_D[7:0]	IO(U)	NAND Flash Data Bus (Pull-up is programmable)
ADC Interface (18)		
ADC[7:0]	AI	ADC Analog Input
AVO[3:0]	AO	Reference Voltage Ouput
ASW[3:0]	AO	ADC Switch Ouput
AVREFp	A	ADC Positive Reference Voltage Input
AVREFn	A	ADC Negative Reference Voltage Input

ATAPI Interface (28)		
IDECS0n	O(IU)	IDE Chip Select 0 (Low active) (Pull-up is programmable)
IDECS1n	O(IU)	IDE Chip Select 1 (Low active) (Pull-up is programmable)
IDEDD[15:0]	IO(U)	IDE Data Bus (Pull-up is programmable)
IDEDA[2:0]	O(IU)	IDE Address Bus (Pull-up is programmable)
IDEINTRQ	I(OD)	IDE Interrupt Request (Pull-down is programmable)
IDEDMARQ	I(OD)	IDE DMA Request (Pull-down is programmable)
IDEDMACKn	O(IU)	IDE DMA Acknowledge (Low active) (Pull-up is programmable)
IDEIORDY	I(OU)	IDE IO Ready (Pull-up is programmable)
IDEIORn	O(IU)	IDE IO Read (Low active) (Pull-up is programmable)
IDEIOWn	O(IU)	IDE IO Write (Low active) (Pull-up is programmable)
IDERESETn	O(IU)	IDE Reset (Low active) (Pull-up is programmable)
LCD Interface (29)		
VD [23:0]	O(IU)	LCD Pixel Data Output. (Pull-up is programmable)
HSYNC	O	Horizontal Sync or Line Sync.
VSYNC	O	Vertical Sync or Frame Sync.
VDEN	O	Data Enable or Display Control Signal.
VICLK	IU	Pixel Clock Input.
VOCLK	O	Pixel Clock Output.

Miscellaneous(14)		
nXDREQ[0] / SD1_CDn / MS1_CDn	I(OU)	External DMA #0 Request SD/SDIO Mode #1 – Card Detect Memory Stick Mode #1 – Card Detect (Pull-up is programmable)
nXDREQ[1] / SD1_CMD / MS1_BS	I(OU)	External DMA #1 Request SD/SDIO Mode #1 – Command/Response (SPI Mode #1 – Data In) Memory Stick Mode #1 – Bus State (Pull-up is programmable)
nXDACK[0] / SD1_nPWR / MS1_nPWR	O(IU)	External DMA #0 Acknowledge SD/SDIO Mode #1 – Power Control Memory Stick Mode #1 – Power Control (Pull-up is programmable)
nXDACK[1] / SD1_CLK / MS1_CLK	O(IU)	External DMA #1 Acknowledge SD/SDIO Mode #1 – Clock (SPI Mode #1 – Clock) Memory Stick Mode #1 – Clock (Pull-up is programmable)
nIRQ[7:0]	I(OU)	External Interrupt Request (Pull-up is programmable)
nWDOG	O	Watchdog Timer Timeout Flag (Low active)
Power/Ground		
VDD18	P	Core Logic power (1.8V)
VDD33	P	IO Buffer power (3.3V)
VSS	G	IO Buffer and Core ground (0V)
USBVDDC0	P	USB Port0 PHY power (3.3V)
USBVSSC0	G	USB Port0 PHY ground (0V)
USBVDDT0	P	USB Port0 PHY Transceiver power (3.3V)
USBVSST0	G	USB Port0 PHY Transceiver ground (0V)
USBVDDC1	P	USB Port1 PHY power (3.3V)
USBVSSC1	G	USB Port1 PHY ground (0V)
USBVDDT1	P	USB Port1 PHY Transceiver power (3.3V)
USBVSST1	G	USB Port1 PHY Transceiver ground (0V)
PLLVDD18	P	PLL power (1.8V)
PLLVSS18	G	PLL ground (0V)
AVDD33	P	ADC Analog power (3.3V)
AVSS	G	ADC Analog ground (0V)
RTCVDD18	P	RTC Battery power (1.8V)

5.2 GPIO Share Pin Description

In this chip, there are GPIOC~GPIOI groups for general IO control. All of GPIO pins are shared with the other interface and define as the following

GPIO Group	Shared pin function
GPIOC (16 pins)	NAND Flash / KPI / LCD Interface
GPIOC[0]	SM_CSn / KPI_ROW[0] / VD[18]
GPIOC[1]	SM_ALE / KPI_ROW[1] / VD[19]
GPIOC[2]	SM_CLE / KPI_ROW[2] / VD[20]
GPIOC[3]	SM_WEn / KPI_ROW[3] / VD[21]
GPIOC[4]	SM_REn / VD[22]
GPIOC[5]	SM_WPn / VD[23]
GPIOC[6]	SM_RBn
GPIOC[7]	SM_D[0] / KPI_COL[0]
GPIOC[8]	SM_D[1] / KPI_COL[1]
GPIOC[9]	SM_D[2] / KPI_COL[2]
GPIOC[10]	SM_D[3] / KPI_COL[3]
GPIOC[11]	SM_D[4] / KPI_COL[4]
GPIOC[12]	SM_D[5] / KPI_COL[5]

GPIOC[13]	SM_D[6] / KPI_COL[6]
GPIOC[14]	SM_D[7] / KPI_COL[7]
GPIOC[15]	SM_CS1n /
GPIOD (10 pins)	SC/ SD(SDIO) / Memory Stick 1 Interface
GPIOD[0]	SC0_DAT/ SD0_CMD / MS0_BS
GPIOD[1]	SC0_CLK / SD0_CLK / MS0_CLK
GPIOD[2]	SC0_RST / SD0_DAT0 / MS0_DAT0
GPIOD[3]	SC0_PRES / SD0_DAT1 / MS0_DAT1
GPIOD[4]	SC0_nPWR / SD0_DAT2 / MS0_DAT2
GPIOD[4]	SC0_nPWR / SD0_DAT2 / MS0_DAT2
GPIOD[5]	SC1_DAT / SD0_DAT3 / MS0_DAT3
GPIOD[6]	SC1_RST / SD0_CDn / MS0_CDn
GPIOD[7]	SC1_nPWR
GPIOD[8]	SC1_CLK / SD0_nPWR / MS0_nPWR
GPIOD[9]	SC1_PRES

GPIOE (14 pins)	UART Interface
GPIOE[0]	TXD0
GPIOE[1]	RXD0
GPIOE[2]	TXD1(B)
GPIOE[3]	RXD1(B)
GPIOE[4]	RTS1 (B)
GPIOE[5]	CTS1 (B)
GPIOE[6]	TXD2(IrDA) / DTR1
GPIOE[7]	RXD2(IrDA) / DSR1
GPIOE[8]	TXD3(M)
GPIOE[9]	RXD3(M)
GPIOE[10]	DTR3(M)
GPIOE[11]	DSR3(M)
GPIOE[12]	TXD4 / RIn1
GPIOE[13]	RXD4 / CDn1
GPIOF (10 pins)	**RMII Interface**
GPIOF[0]	PHY_MDC
GPIOF[1]	PHY_MDIO
GPIOF[3:2]	PHY_TXD [1:0]
GPIOF[4]	PHY_TXEN
GPIOF[5]	PHY_REFCLK
GPIOF[7:6]	PHY_RXD [1:0]
GPIOF[8]	PHY_CRSDV
GPIOF[9]	PHY_RXERR
GPIOG (17 pins)	**I2C/USI XDMA, PS2/SD1/MS1, AC97/I2S/PWM Interface**
GPIOG[0]	SCL0 / SFRM
GPIOG[1]	SDA0 / SSPTXD
GPIOG[2]	SCL1 / SCLK

GPIOG[3]	SDA1 / SSPRXD
GPIOG[4]	nXDREQn[0] / SD1_CDn / MS1_CDn
GPIOG[5]	nXDACKn[0] / SD1_nPWR / MS1_nPWR
GPIOG[6]	nXDREQn[1] / SD1_CMD / MS1_BS
GPIOG[7]	nXDACKn[1] / SD1_CLK / MS1_CLK
GPIOG[8]	PS2CLK0 / SD1_DAT0 / MS1_DAT0
GPIOG[9]	PS2DATA0 / SD1_DAT1 / MS1_DAT1
GPIOG[10]	PS2CLK1 / SD1_DAT2 / MS1_DAT2
GPIOG[11]	PS2DATA1 / SD1_DAT3 / MS1_DAT3
GPIOG[12]	AC97_nRESET / I2S_SYSCLK /
GPIOG[13]	AC97_DATAI / I2S_DATAI / PWM [0]
GPIOG[14]	AC97_DATAO / I2S_DATAO / PWM [1]
GPIOG[15]	AC97_SYNC / I2S_WS / PWM [2]
GPIOG[16]	AC97_BITCLK / I2S_BITCLK / PWM [3]

GPIOH (8 pins)	nIRQ Interface
GPIOH[7:0]	nIRQ[7:0]
GPIOI (17 pins)	**ATAPI**
GPIOI[0]	IDECS0n
GPIOI[1]	IDECS1n
GPIOI[4:2]	IDEDA[2:0]
GPIOI[5]	IDEINTRQ
GPIOI[6]	IDEDMACKn
GPIOI[7]	IORDY
GPIOI[8]	IDEIORn
GPIOI[9]	IDEIOWn
GPIOI[10]	IDEDMARQ
GPIOI[14:11]	IDEDD[15:12]
GPIOI[15]	IDERESETn
GPIOI[16]	nWDOG
IDEDD (12 pins)	**ATAPI / KPI Interface**
IDEDD[7:0] / KPI_COL[7:0]	IDEDD[7:0] / KPI_COL[7:0]
IDEDD[11:8] / KPI_ROW[3:0]	IDEDD[11:8] / KPI_ROW[3:0]

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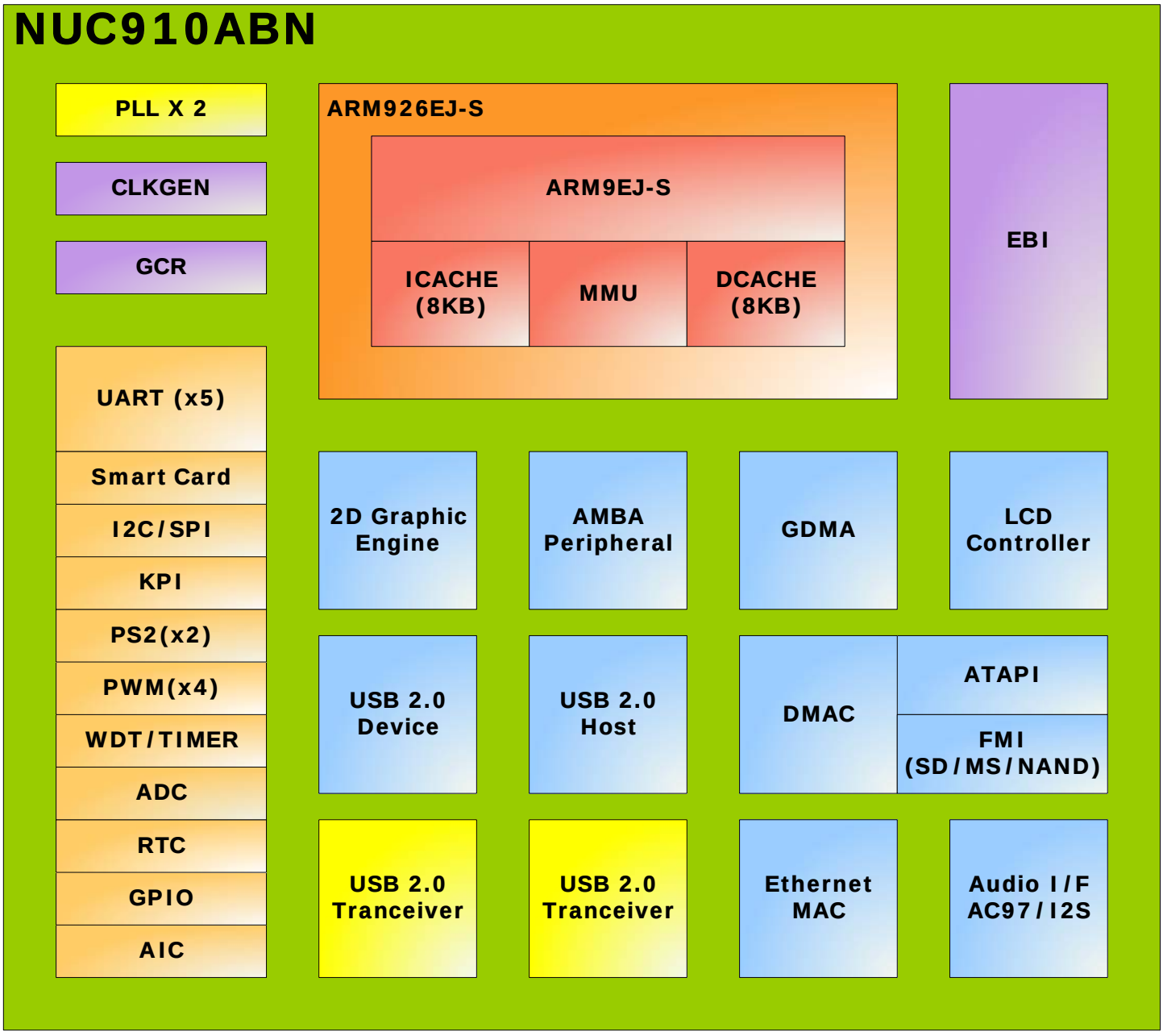
32-BIT ARM926EJS-BASED MCU

6. FUNCTIONAL BLOCK



7. ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Ambient temperature	-40 °C ~ 85 °C
Storage temperature	-50 °C ~ 125°C
Voltage on any pin	-0.5V ~ 6V
Power supply voltage (Core logic)	-0.5V ~ 2.5V
Power supply voltage (IO Buffer)	-0.5V ~ 4.6V
Injection current (latch-up testing)	100mA
Crystal Frequency	4MHz ~ 30MHz

7.2 DC Specifications

7.2.1 Digital DC Characteristics

(Normal test conditions: VDD33/AVDD33 = 3.3V+/-10%, VDD18/RTCVDD18/PLLVDD18 = 1.8V+/-10%, USBVDDC0/USBVDDC1/USBVDDT0/USBVDDT1= 3.3V+/-5%, TA = -40 °C ~ 85 °C unless otherwise specified)

Symbol	Parameter	Condition	Min	TYP	Max	Unit
VDD33/ AVDD33	Power Supply		2.97	-	3.63	V
VDD18/ RTCVDD18/ PLLVDD18	Power Supply		1.62	-	1.98	V
USBVDDC0/ USBVDDC1/ USBVDDT0/ USBVDDT1	Power Supply		3.13	-	3.46	V
V_{IL}	Input Low Voltage		-0.3	-	0.8	V
V_{IH}	Input High Voltage		2.0	-	5.5	V
VT+	Schmitt Trigger positive-going threshold		1.5	-	1.62	V
VT-	Schmitt trigger negative-going threshold		1.14	-	1.27	V
V_{OL}	Output Low Voltage	Depend on driving	-	-	0.4	V
V_{OH}	Output High Voltage	Depend on driving	2.4	-	-	V
I_{IH}	Input High Current	V_{IN} = 2.4 V	-1	-	1	uA
I_{IL}	Input Low Current	V_{IN} = 0.4 V	-1	-	1	uA
I_{OC}	Operation Current	Note 1	-	340	-	mA
I_{SC}	Standby Current	Note 2	-	50	-	uA

Note1:

This operation current is measured on VDD18 @ 1.8V, and all of IP clocks are enable with CPU clock/system clock @ 200MHz / 100MHz.

Note2:

The standby current is measured on VDD18 @1.8V, and all of IP clocks are disabling with power-down mode, all of GPIO pins are set to output and clock pins keep at 0V.

7.2.2 USB Low-/Full-Speed DC Electrical Specifications

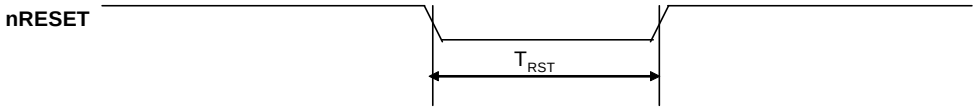
Symbol	Parameter	Conditions	MIN	TYP	MAX
V_{IH}	Pad input high voltage		2.0V		
V_{IL}	Pad input low voltage				0.8V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2V		
V_{CM}	Common mode voltage range	include V_{DI} range	0.8V		2.5V
V_{SE}	Single-ended receiver threshold		0.8V		2.0V
V_{OL}	Pad output low voltage		0V		0.3V
V_{OH}	Pad output high voltage		2.8V		3.6V
V_{CRS}	Differential output signal cross-point voltage		1.3V		2.0V
R_{PU}	Internal pull-up resistor	Bus idle	900Ω		1575Ω
		Receiving	1425Ω		3090Ω
R_{PD}	Internal pull-down resistor		14.25KΩ		24.80KΩ
Z_{DRV}	Driver output resistance‡	Steady state drive		10Ω	
C_{IN}	Transceiver pad capacitance	Pad to ground			20pF

7.2.3 USB High-Speed DC Electrical Specifications

Symbol	Parameter	Conditions	MIN	TYP	MAX
V_{HSDI}	High-speed differential input signal level	|PADP-PADM|	150mV		
V_{HSSQ}	High-speed SQ detection threshold	|PADP-PADM|	100mV		150mV
V_{HSCM}	High-speed common mode voltage range		-50mV		500mV
V_{HSOH}	High-speed data signaling high		360mV		440mV
V_{HSOL}	High-speed data signaling low		-10mV		10mV
V_{CHIRPJ}	Chirp J level		700mV		1100mV
V_{CHIRPK}	Chirp K level		-900mV		-500mV
Z_{HSDRV}	High-speed driver output resistance	45Ω±10%	40.5Ω		49.5Ω

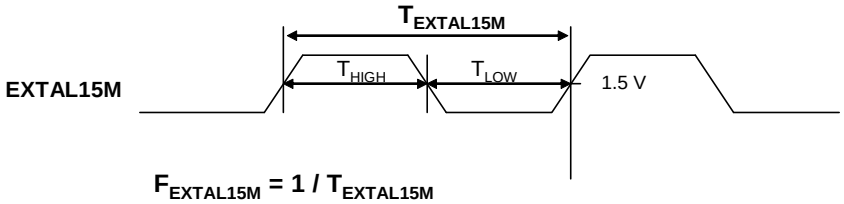
7.3 AC Specifications

7.3.1 RESET AC Characteristics



Symbol	Parameter	MIN	MAX	Unit
T_{RST}	Reset Pulse Width after Power stable	1.0	-	ms

7.3.2 Clock Input Characteristics

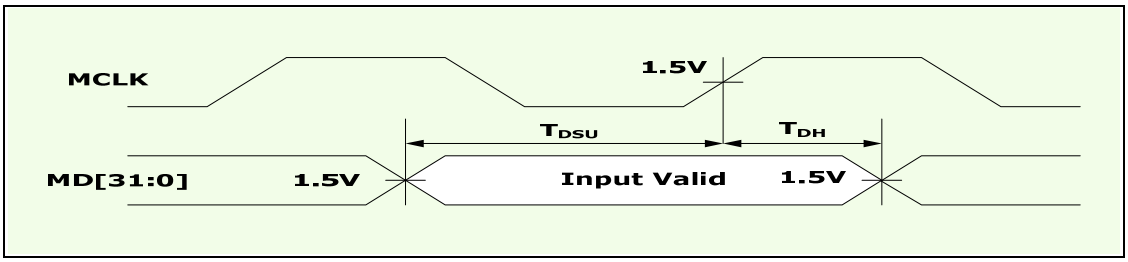


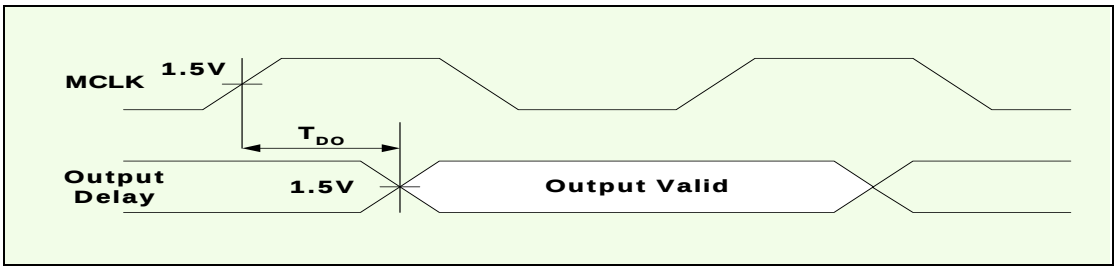
$F_{EXTAL15M} = 1 / T_{EXTAL15M}$

$EXTAL15M_{DUTY} = T_{HIGH} / (T_{HIGH} + T_{LOW})$

Symbol	Parameter	MIN	TYP	MAX	Unit
$F_{EXTAL15M}$	Clock Input Frequency	-	15.0	-	MHz
$EXTAL15M_{DUTY}$	Clock Input Duty Cycle	45	50	55	%
V_{IL} (EXTAL15M)	EXTAL15M Input Low Voltage	0	-	0.8	V
V_{IH} (EXTAL15M)	EXTAL15M Input High Voltage	2.0	-	VDD33 + 0.3	V

7.3.3 EBI/SDRAM Interface AC Characteristics

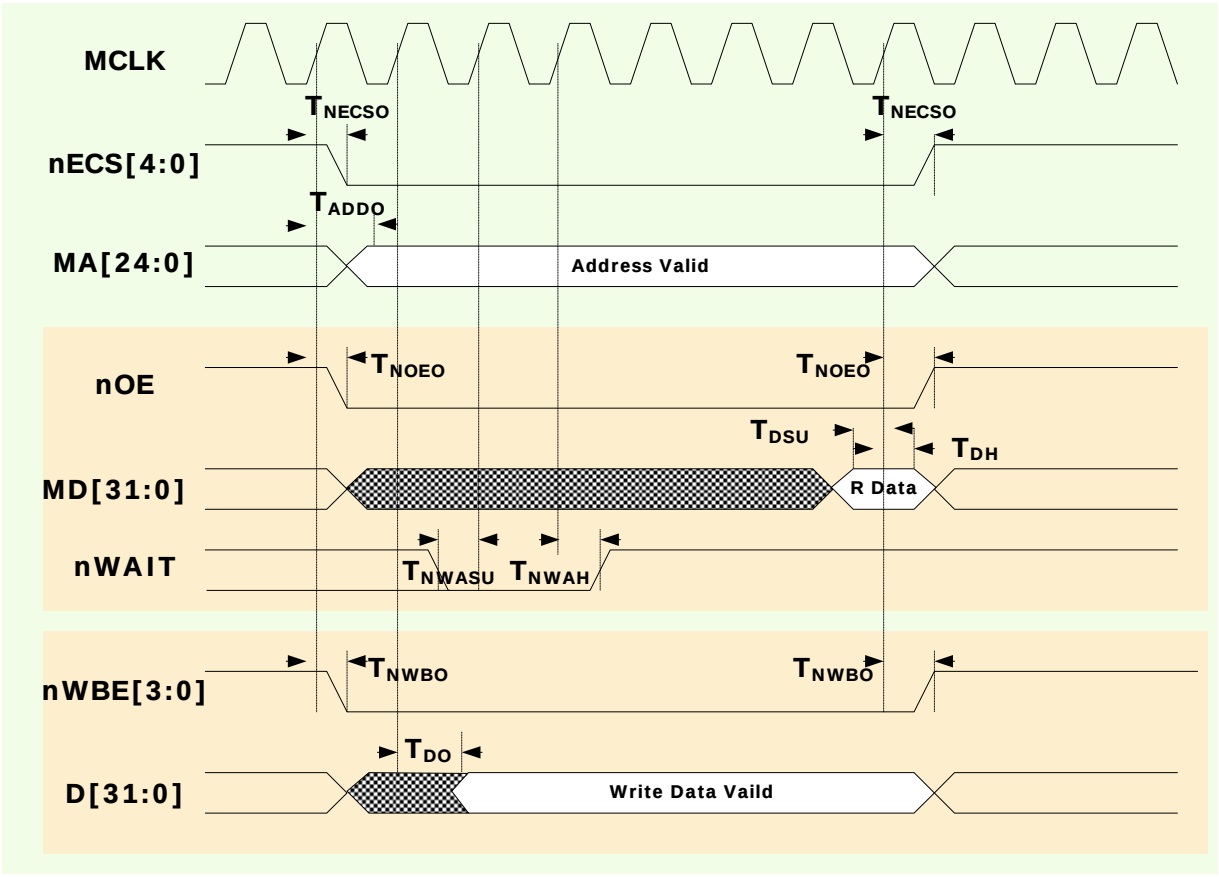




Symbol	Parameter	MIN	MAX	Unit
F_{MCLK}	SDRAM Clock Output Frequency	-	100	MHz
T_{DSU}	MD[31:0]] Input Setup Time	2	-	ns
T_{DH}	MD[31:0] Input Hold Time	2	-	ns
T_{OSU}	SDRAM Output Signal Valid Delay Time	2*	5*	ns

* The above T_{OSU} is based on the EBI CKSKEW register default setting on 0x48 and F_{MCLK} at 100MHz

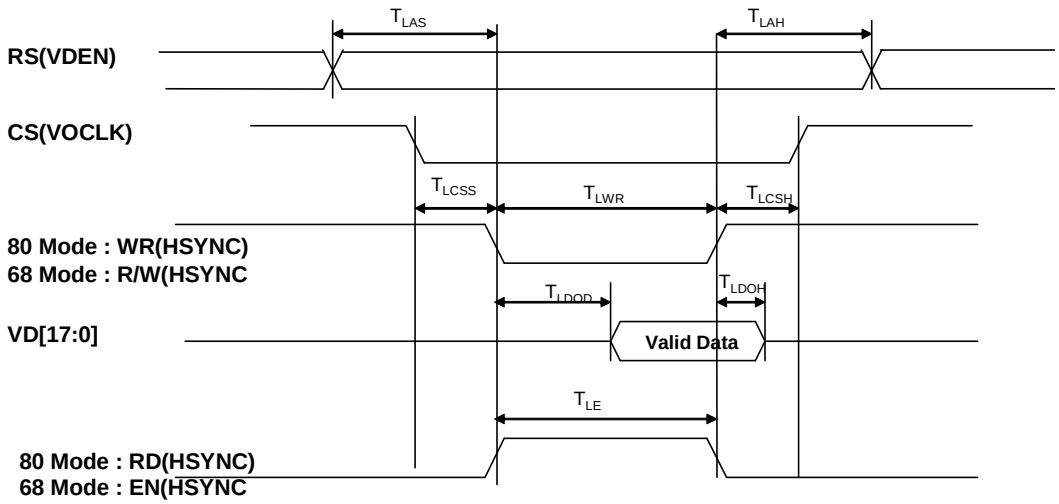
7.3.4 EBI(ROM/SRAM/External I/O) AC Characteristics



Symbol	Parameter	MIN	MAX	Unit
T_{ADDO}	Address Output Delay Time	2*	7*	ns
T_{NCSO}	ROM/SRAM/Flash or External I/O Chip Select Delay Time	2*	7*	ns
T_{NOEO}	ROM/SRAM or External I/O Bank Output Enable Delay	2*	7*	ns
T_{NWBO}	ROM/SRAM or External I/O Bank Write Byte Enable Delay	2*	7*	ns
T_{DH}	Read Data Hold Time	5		ns
T_{DSU}	Read Data Setup Time	1		ns
T_{DO}	Write Data Output Delay Time (SRAM or External I/O)	2*	7*	ns
T_{NWASU}	External Wait Setup Time	3		ns
T_{NWAH}	External Wait Hold Time	1		ns

* The above data are based on the EBI CKSKEW register default setting on 0x48 and F_{MCLK} at 100MH

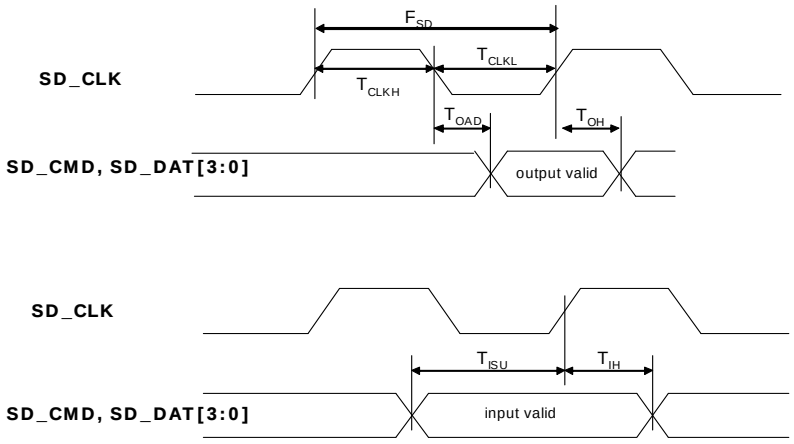
7.3.5 LCD Interface: MPU Type AC Characteristics



Symbol	Parameter	Conditions	MIN	MAX	Unit
T_{LCSS}	Chip Select Set-up Time	-	1/2	-	*PCLK
T_{LCSH}	Chip Select Hold Time	-	1/2	-	*PCLK
T_{LAS}	Address Set-up Time	-	1	-	*PCLK
T_{LAH}	Address Hold Time	-	1	-	*PCLK
T_{LDOD}	Write Data Active Delay	-	0	1/2	*PCLK
T_{LDOH}	Write Data Hold Time	-	1/2	-	*PCLK
T_{LWR}	WR Pulse Width	80 Mode	1	-	*PCLK
T_{LE}	LE Pulse Width	68 Mode	1/2	-	*PCLK

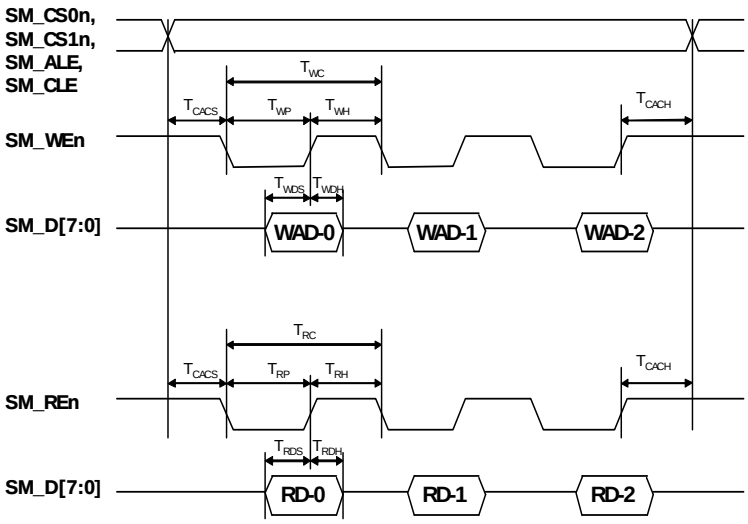
*PCLK is the engine clock of the LCD Controller

7.3.6 SD Host Interface AC Characteristics



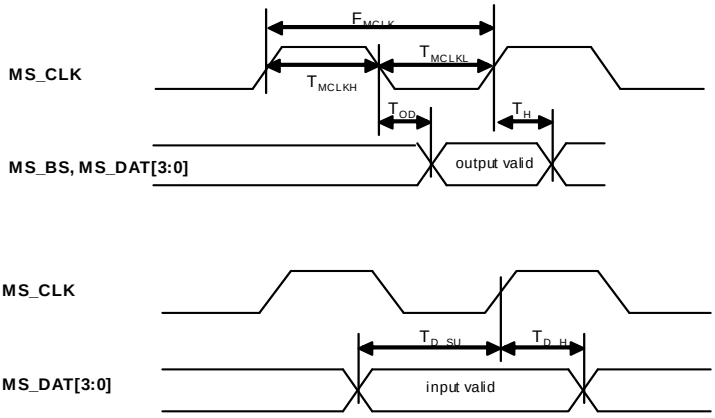
Symbol	Parameter	Conditions	MIN	MAX	Unit
F_{SD}	SD Clock Frequency	Identification Mode	**100**	**400**	KHz
F_{SD}	SD Clock Frequency	Data Transfer Mode	-	**50**	MHz
T_{CLKH}	SD Clock High Time	-	**10**	-	ns
T_{CLKL}	SD Clock Low Time	-	**10**	-	ns
T_{ISU}	SD CMD & Data Input Setup Time	-	**5**	-	ns
T_{IH}	SD CMD & Data Input Hold Time	-	**5**	-	ns
T_{OAD}	SD Output Active Delay (Falling Edge)	-	-	**14**	ns
T_{OH}	SD Output Hold Time	-	**0**	-	ns

7.3.7 NAND Flash Memory Interface AC Characteristics



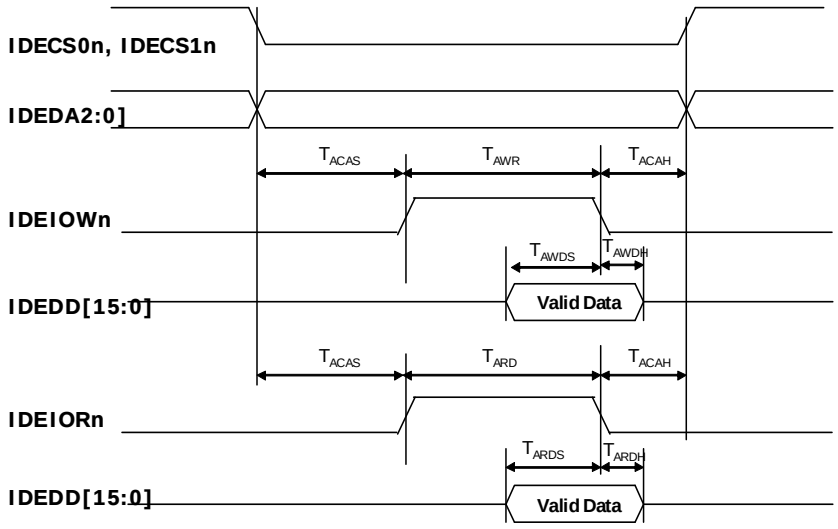
Symbol	Parameter	MIN	MAX	Unit
T_{CACS}	SM_CS0n, SM_CS1n, SM_ALE, SM_CLE Setup Time before SM_WEn, SM_REn Low	20	-	ns
T_{CACH}	SM_CS0n, SM_CS1n, SM_ALE, SM_CLE Hold Time after SM_WEn, SM_REn High	40	-	ns
T_{WP}	Write Pulse Width	40	-	ns
T_{WH}	SM_WEn High Time	20	-	ns
T_{WC}	Write Cycle Time	80	-	ns
T_{WDS}	Write Data Output Setup Time	30	-	ns
T_{WDH}	Write Data Output Hold Time	20	-	ns
T_{RP}	Read Pulse Width	60	-	ns
T_{RH}	SM_REn High Time	20	-	ns
T_{RC}	Read Cycle Time	80	-	ns
T_{RDS}	Read Data Input Setup Time	6	-	ns
T_{RDH}	Read Data Input Hold Time	20	-	ns

7.3.8 Memory Stick Interface AC Characteristics



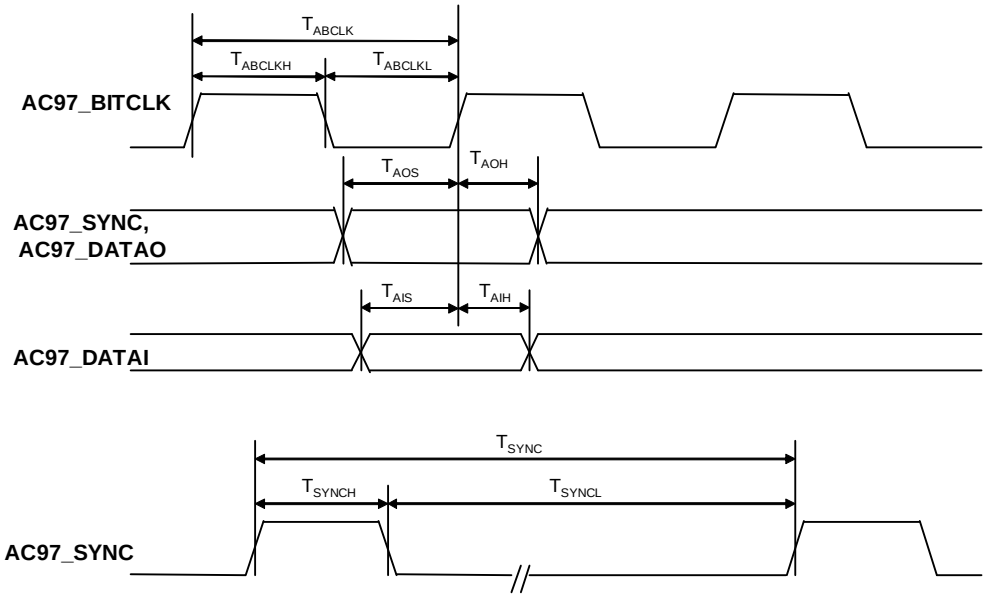
Symbol	Parameter	Conditions	MIN	MAX	Unit
F_{MCLK}	MS_CLK Clock Frequency	Serial Mode	**5**	**20**	MHz
F_{MCLK}	MS_CLK Clock Frequency	Parallel Mode	**10**	**40**	MHz
T_{MCLKH}	MS_CLK Clock High Time		**5**	-	ns
T_{MCLKL}	MS_CLK Clock Low Time		**5**	-	ns
T_{BS_OD}	MS_BS Output Delay (Falling Edge)		**5**	**15**	ns
T_{BS_H}	MS_BS Output Hold Time		**1**	-	ns
T_{D_SU}	Data Input Setup Time		**8**	-	ns
T_{D_H}	Data input Hold Time		**1**	-	ns
T_{D_OD}	Data Output Delay (Falling Edge)		**8**	**15**	ns
T_{D_OD}	Data Output Hold Time		**1**	-	ns

7.3.9 ATAPI Interface AC Characteristic



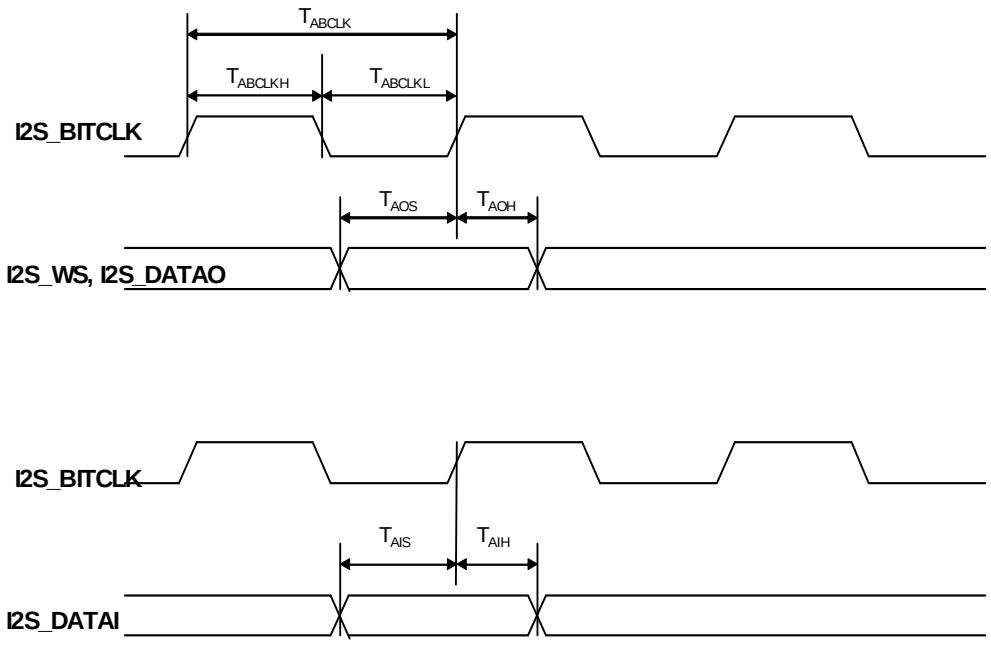
Symbol	Parameter	MIN	MAX	Unit
T_{ACAS}	Set-up time, IDECS0n, IDECS1n and IDEDA[2:0] valid before IDEIORn or IDEIOWn low	**25**	-	ns
T_{ACAH}	Hold time, IDECS0n, IDECS1n and IDEDA[2:0] valid after IDEIORn or IDEIOWn high	**10**	-	ns
T_{AWDS}	Write Data Set-up Time	**20**	-	ns
T_{AWDH}	Write Data Hold Time	**10**	-	ns
T_{AWR}	IDEIOWn Pulse Width	**70**	-	ns
T_{ARDS}	Read Data Set-up Time	**20**	-	ns
T_{ARDH}	Read Data Hold Time	**5**	-	ns
T_{ARD}	IDEIORn Pulse Width	**70**	-	ns
T_{CYC}	Command (IDEIOWn or IDEIORn) Cycle Time	**120**	-	ns

7.3.10 Audio AC-Link Interface AC Characteristics



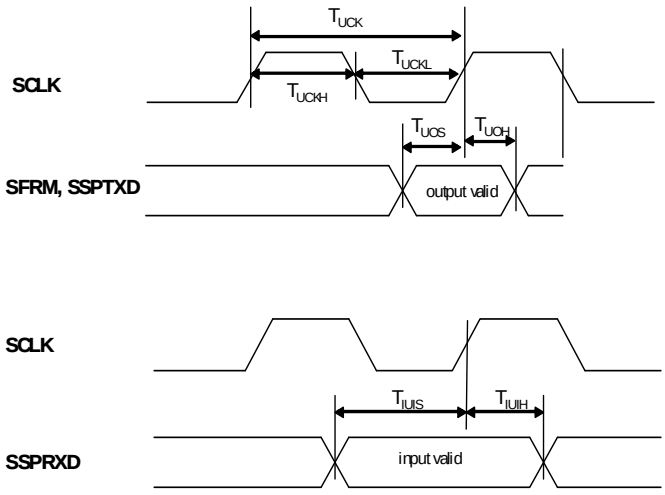
Symbol	Parameter	MIN	TYP	MAX	Unit
T_{ABCLKH}	Audio Bit Clock Input High Time	**36.6**	**40.7**	**44.8**	ns
T_{ABCLKH}	Audio Bit Clock Input Low Time	**36.6**	**40.7**	**44.8**	ns
T_{ABCLK}	Audio Bit Clock Input Cycle Time	-	**81.4**	-	ns
T_{AOS}	Audio Output Signal (AC97_SYNC, AC97_DATAO) Setup Time	**15**	-	-	ns
T_{AOH}	Audio Output Signal (AC97_SYNC, AC97_DATAO) Hold Time	**5**	-	-	ns
T_{AIS}	Audio Data Input Setup Time	**15**	-	-	ns
T_{AIH}	Audio Data Input Hold Time	**5**	-	-	ns
T_{SYNCH}	Sync Signal Output High Time	-	**20.8**	-	ns
T_{SYNCH}	Sync Signal Output Low Time	-	**1.3**	-	ns
T_{SYNC}	Sync Signal Output Cycle Time	-	**19.5**	-	ns

7.3.11 Audio I2S Interface AC Characteristics



Symbol	Parameter	MIN	MAX	Unit
T_{ABCLKH}	Audio Bit Clock Output High Time	**18.3**	-	ns
T_{ABCLKH}	Audio Bit Clock Output Low Time	**18.3**	-	ns
T_{ABCLK}	Audio Bit Clock Output Cycle Time	**40.7**	-	ns
T_{AOS}	Audio Data Output Setup Time	**4.5**	-	ns
T_{AOH}	Audio Data Output Hold Time	**4.5**	-	ns
T_{AIS}	Audio Data Input Setup Time	**4.5**	-	ns
T_{AIH}	Audio Data Input Hold Time	**4.5**	-	ns

7.3.12 USI(SPI/MW) Interface AC Characteristics



Symbol	Parameter	MIN	MAX	Unit
T_{CLKH}	Clock Output High Time	**14.6**	-	ns
T_{CLKL}	Clock Output Low Time	**15.8**	-	ns
T_{CLK}	Clock Cycle Time	**30.4**	**-**	ns
T_{UOS}	SFRM, SSPTXD Output Setup Time	**15**	-	ns
T_{UOH}	SFRM, SSPTXD Output Hold Time	**13**	-	ns
T_{UIS}	SSPRXD Input Setup Time	**10**	-	ns
T_{UIH}	SSPRXD Input Hold Time	**10**	-	ns

7.3.13 USB Transceiver AC Characteristics

USB Transceiver: Low-Speed AC Electrical Specifications

Symbol	Parameter	Conditions	MIN	TYP	MAX
T_{LR}	Low-speed driver rise time	C_L=50pF	75ns		300ns
T_{LF}	Low-speed driver fall time	C_L=50pF	75ns		300ns
T_{LRFM}	Low-speed rise/fall time matching	$T_{LRFM} = T_{LR} / T_{LF}$	80%		125%

USB Transceiver: Full-Speed AC Electrical Specifications

Symbol	Parameter	Conditions	MIN	TYP	MAX
T_{FR}	Full-speed driver rise time	C_L=50pF	4ns		20ns
T_{FF}	Full-speed driver fall time	C_L=50pF	75ns		20ns
T_{FRFM}	Full-speed rise/fall time matching	$T_{FRFM} = T_{FR} / T_{FF}$	90%		111.11 %

USB Transceiver: High-Speed AC Electrical Specifications

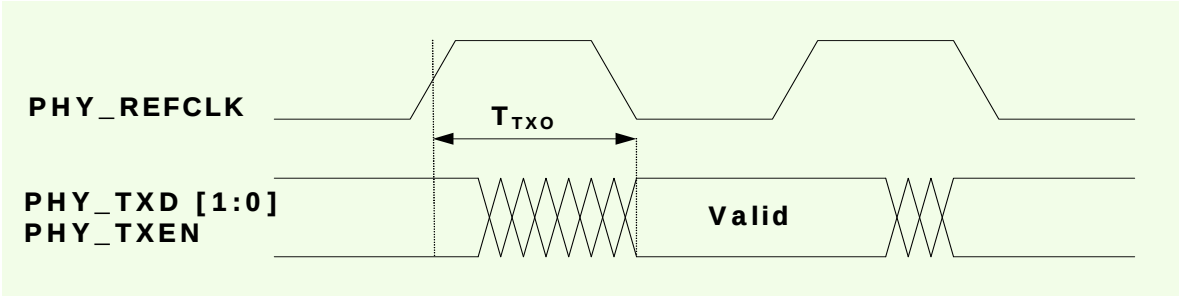
Symbol	Parameter	Conditions	MIN	TYP	MAX
T_{HSR}	High-speed driver rise time	Z_{HSDRV}=45Ω	500ps		900ps
T_{HSF}	High-speed driver fall time	Z_{HSDRV}=45Ω	500ps		900ps
	High-speed driver waveform requirement		Eye diagram of template 1**		
	High-speed receiver waveform requirement		Eye diagram of template 4††		
	High-speed jitter requirement	Data source end	Eye diagram of template 1**		
		Receiver end	Eye diagram of template 4††		

** Check "Universal Serial Bus Specification Revision 2.0" page 133.

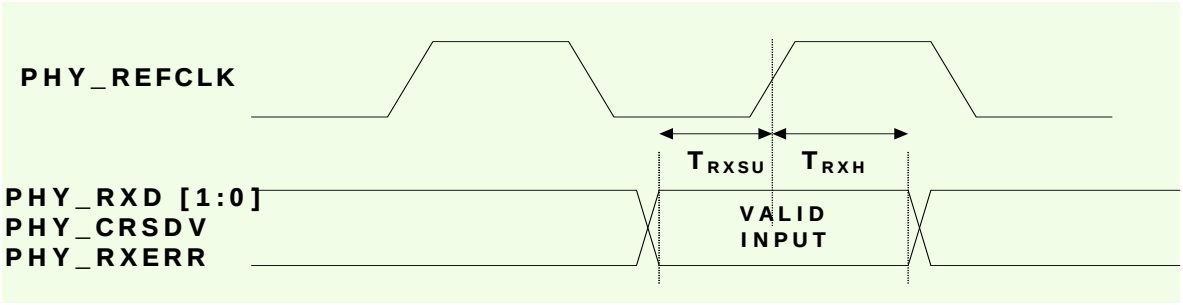
†† Check "Universal Serial Bus Specification Revision 2.0" page 136.

7.3.14 EMC RMII AC Characteristics

The signal timing characteristics conforms to the guidelines specified in IEEE Std. 802.3.

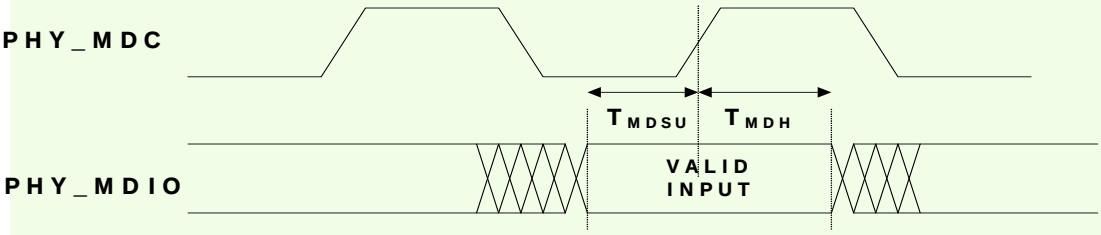


Transmit Signal Timing Relationships at RMII

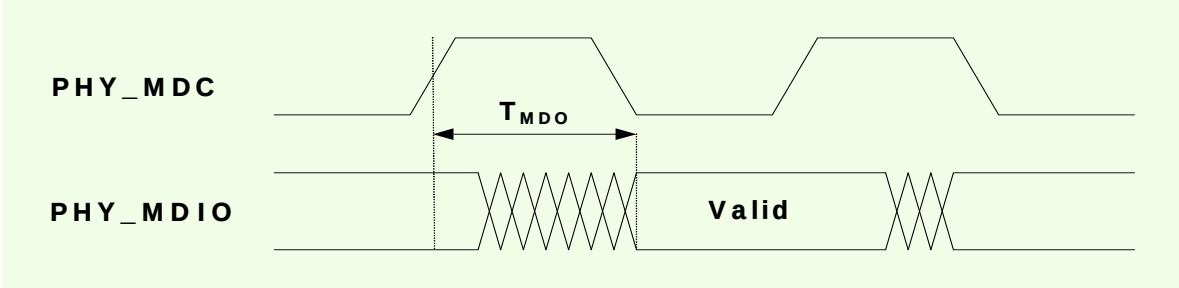


Receive Signal Timing Relationships at RMII

Symbol	Parameter	MIN	MAX	Unit
T_{TxO}	Transmit Output Delay Time	7	14	ns
T_{RxSU}	Receive Setup Time	4		ns
T_{RxH}	Receive Hold Time	2		ns



PHY_MDIO Read from PHY Timing



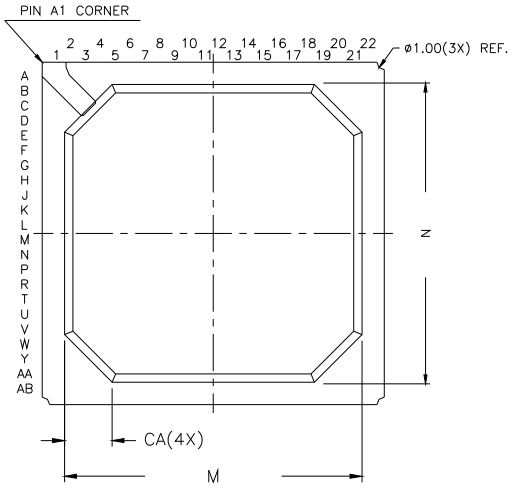
PHY_MDIO Write to PHY Timing

Symbol	Parameter	MIN	MAX	Unit
T_{MDO}	PHY_MDIO Output Delay Time	0	15	ns
T_{MDSU}	PHY_MDIO Setup Time	5		ns
T_{MDH}	PHY_MDIO Hold Time	5		ns

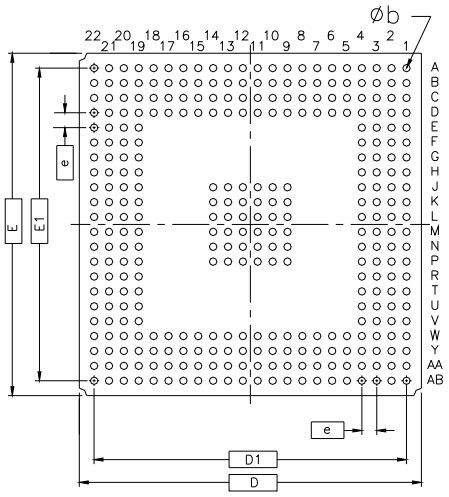
8. PACKAGE SPECIFICATIONS

NUC910ABN PBGA324Ball (23X23mm,Ball pitch:1.0mm ,Ø=0.6mm)

TOP VIEW



BOTTOM VIEW

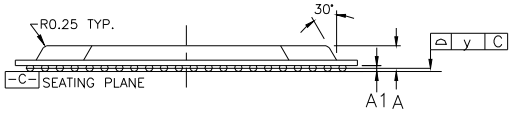


Controlling Dimension :Millimeters

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.60	1.73	1.86	0.0629	0.0681	0.0732
A1	0.30	–	0.50	0.0118	–	0.0196
D	23			0.9055		
D1	21			0.8267		
E	23			0.9055		
E1	21			0.8267		
y	0.2			0.0078		
øb	0.5	0.6	0.7	0.0157	0.0196	0.0236
e	–	1.0	–	–	0.0393	–
M	–	20	–	–	0.7874	–
N	–	20	–	–	0.7874	–
CA	3.2 REF.			0.1259 REF.		

Note:1.Ball Land: 0.65mm / Ball opening: 0.55mm
2.PCB Solder Ball Land Suggested<=0.55mm

SIDE VIEW (FOR TOP VIEW)



9. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	March 03, 2009	-	Initial Issued

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