32-BIT ARM926EJS-BASED MCU

NUC950ADN
32-bit ARM926EJ-S Based Microcontroller
Product Data Sheet

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1. GENERAL DESCRIPTION

This chip is built around an outstanding CPU core: the 16/32 ARM926EJ-S RISC processor designed by Advanced RISC Machines, Ltd. The ARM926EJ-S core, offers 8K-byte I-cache and 8K-byte D-cache with MMU, is a low power, general-purpose integrated circuits. One 10/100 Mb MAC of Ethernet controller is built-in to reduce total system cost. A TFT type LCD controller and 2D graphics engine with various integrated on chip functions, this micro-controller is suitable for a high end, high performance and low cost related products as well as general purpose applications.

The following integrated on-chip functions are described in detail in this document.

	Main Function
CPU	• ARM926EJ-S
Platform	• Programmable PLL System Clock Synthesizer
	• AMBA Peripherals
	• Timer, Watchdog Timer
	• Advanced Interrupt Controller
	• General DMA Controller
	• External Bus Interface Controller
Networking	• Ethernet MAC Controller
Display Interface	• LCD Controller
Graphics	• 2D Graphic Engine
Audio Interface	• 2-Channel I2S Controller
	• 2-Channel AC97 Controller
USB Interface	• USB 1.1/2.0 High/Full/Low Speed Host Controller
	• USB 2.0 High/Full Speed Device Controller
Storage Interface	• NAND Flash Controller with ECC1/ECC4
	• SD/SDIO/MMC Controller
	• Memory Stick (MS) Controller
Peripheral & Misc.	• GPIO
	• 4-Channel PWM
	• UART/HS-UART
	• USI (SPI/uWire)
	• I2C (Master) Controller
	• Keypad Scan Controller

2. FEATURES

Architecture

- Efficient and powerful ARM926EJ-S core with fully 16/32-bit RISC architecture
- Little Endian mode supported
- 8K-byte I-cache and 8K-byte D-cache with MMU
- Cost-effective JTAG-based debug solution

Power management

- Programmable clock enable for individual peripherals
- IDLE mode to halt ARM Core and keep peripheral working
- Power-Down mode to stop all clocks included external crystal oscillator.
- Exit IDLE/Power-Down by interrupts

PLL

- Supports two on-chip PLLs
- The external clock can be multiplied by on-chip PLL to provide high frequency system clock
- The input frequency range is 4-30MHz; 15MHz is preferred.
- Programmable clock frequency
- Wakeup by interrupt, USB device.

Advanced Interrupt Controller

- 31 interrupt sources, including 3 external interrupt sources
- Programmable normal or fast interrupt mode (IRQ, FIQ)
- Programmable as either edge-triggered or level-sensitive for 3 external interrupt sources
- Programmable as either low-active or high-active for 3 external interrupt sources
- Priority methodology is encoded to allow for interrupt daisy-chaining
- Automatically mask out the lower priority interrupt during interrupt nesting
- Automatically clear the interrupt flag when the interrupt source is programmed to be edge-triggered

General DMA Controller

- 2-channel General DMA for memory-to-memory data transfers without CPU intervention
- Increments or decrements a source or destination address in 8-bit, 16-bit or 32-bit data transfers
- 8-data burst mode

External Bus Interface

- 8/16/32-bit external bus support for ROM/SRAM, flash memory, SDRAM and external I/Os
- Programmable access cycle (0-7 wait cycle)
- Four-word depth write buffer

Ethernet MAC Controller

- 100/10-Mbps operation
- DMA engine with burst mode
- MAC Tx/Rx buffers (256 bytes Tx, 256 bytes Rx)
- Full compliance with IEEE standard 802.3
- RMII interface only
- Station Management Signaling
- On-Chip CAM (up to 16 destination addresses)
- Full-duplex mode with PAUSE feature
- Long/short packet modes

LCD Controller

- Support the 8/12/16/18-bit data interface to connect with 80/68 series MPU type LCM module
- Convert RGB-565, YUV-422 display data to RGB-444, RGB-565, RGB-666, YUV-422 color format for display output
- Support CCIR-656(with vsync / hsync / data enable sync signal) 8/16-bit YUV data output format to connect with external TV encoder
- Support 8/16 bpp OSD data with image overlay function to facilitate the diverse graphic UI.
- Support linear 1X – 8X image scaling up function.
- Support Picture-In-Picture display function
- Support hardware cursor.

2-D Graphics Engine

- Color depth 8-bit/16-bit/32-bit in RGB domain or RGB332/RGB565/RGB888 are supported
- Contains 2D Bit Block Transfer (BitBLT) functions as defined in Microsoft GDI. It includes HostBLT, Pattern BLT, Color/Font Expanding BLT, Transparent BLT, Tile BLT, Block Move BLT, Copy File BLT, Color/Font Expansion, and Rectangle Fill, etc.
- Supports fore/background colors and all Microsoft 256 ternary raster-operation codes (ROP)
- Clipping window can be defined as inside or outside clipping
- Implements the alpha-blending function for source/destination picture overlaying
- Fast Bresenham line drawing algorithm is used to draw solid/textured lines
- Supports rectangular border or frame drawing

- Supports picture re-sizing by 1/255 ~ 254/255 down-scaling and 1 ~ 1.996 up-scaling (1+254/255).
- Supports object rotations in different degrees, that is L45/L90/R45/R90/M180/F180/X180, where
  - L45/L90 means rotate left 45/90 degrees,
  - R45/R90 means rotate right 45/90 degrees,
  - M180 means mirror (flop),
  - F180 means up-side-down (flip) and X180 for rotations by 180 degrees

2-Channel AC97 / I2S Controller

- Support I2S interface.
- Support AC97 interface.
- Built-in an 8x32 bits internal buffer.
- Support DMA function for data transfer between internal buffer and system memory.
- Support 16-bit I2S and MSB-justified format.

USB Host Controller with transceiver

- Fully compliant with USB Revision 2.0 specification.
- Enhanced Host Controller Interface (EHCI) Revision 1.0 compatible.
- Open Host Controller Interface (OHCI) Revision 1.0 compatible.
- Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt, Isochronous and Split transfers.
- Built-in DMA for real-time data transfer.
- Support two ports (one port transceiver is shared with USB Device Controller)

USB Device Controller with transceiver

- Compliant with USB version 2.0 specification.
- Software control for device remote-wakeup.
- Supports 6 configurable IN/OUT endpoints in addition to Control Endpoint. Each of these endpoints can be configures as IN or OUT with Isochronous, Bulk or Interrupt transfer.
- Three different modes of operation of an in-endpoint (Auto validation mode, manual validation mode, Fly mode.
- Supports Endpoint Maximum Packet Size up to 1024 bytes.

Flash Memory Interface (FMI)

- Directly connect to Secure Digital (SD, MMC and SDIO) flash memory card, Memory Stick (Memory stick PRO) and NAND type flash memory.
- Supports DMA function to accelerate the data transfer between the internal buffer, external SDRAM, and flash memory card.

- Two 512 bytes internal buffers are embedded inside

I2C Master

- Compatible with I^2C standard, support master mode only
- Multi Master Operation
- Clock stretching and wait state generation
- Provide multi-byte transmit operation, up to 4 bytes can be transmitted in a single transfer
- Software programmable acknowledge bit
- Arbitration lost interrupt, with automatic transfer cancellation
- Start/Stop/Repeated Start/Acknowledge generation
- Start/Stop/Repeated Start detection
- Bus busy detection
- Supports 7 bit addressing mode
- Software mode I^2C

Universal Serial Interface (USI)

- Support MICROWIRE/SPI master mode
- Support full/half duplex synchronous serial data transfer
- Variable length of transfer word up to 32 bits
- Provide burst mode operation, transmit/receive can be executed up to four times in one transfer
- MSB or LSB first data transfer
- Receive and Transmit on both rising or falling edge of serial clock independently

UART

- Three UART (serial I/O) blocks with interrupt-based operation
- Support for 5-bit, 6-bit, 7-bit or 8-bit serial data transmit and receive
- Programmable baud rates
- 1,1½ or 2 stop bits
- Odd or even parity
- Break generation and detection
- Parity, overrun and framing error detection
- X16 clock mode
- Support for IrDA and two debug ports

Timers

- Five programmable 24-bit timers with 8-bit pre-scalar
- One programmable 20-bit Watchdog timer
- One-short mode, period mode or toggle mode operation

4-Channel PWM

- Four 16-bit timers
- Two 8-bit pre-scalars & Two 4-bit divider
- Programmable duty control of output waveform (PWM)
- Auto reload mode or one-shot pulse mode
- Dead-zone generator

Keypad Scan Interface

- Scan up to 16x8 with an external 4 to 16 decoder; or 4x8 array without auxiliary component
- Programmable de-bounce time
- One or two keys scan with interrupt and three keys reset function.
- Support low power wakeup function

Programmable I/Os

- Pins individually configurable to input, output or I/O mode for dedicated signals
- I/O ports are Programmable and Configurable for Multiple functions

Operation Voltage Range

- VDD18 for IO Buffer: 1.8V+/-10%
- VDD33 for Core Logic: 3.3V+/-10%
- USBVDDC0/USBVDDC1/USBVDDT0/USBVDDT1 for USB: 3.3V+/-5%
- PLLVDD18 for PLL: 1.8V+/-10%

Operation Temperature Range

- -20 ° ~ 70 °C

Operating Frequency

- Up to 200 MHz for ARM926EJ-S CPU

Package Type

- 216-Pin LQFP, Pb free, Halogen free

3. PIN DIAGRAM

NUC950 Pin Diagram

4. PIN ASSIGNMENT

Table 4.1 NUC950 Pins Assignment

Pad Name	NUC950
Clock & Reset	**(5 pins)**
EXTAL15M	102
XTAL15M	103
EXTAL48M0	209
XTAL48M0	208
nRESET	1
TAP Interface	**(5 pins)**
TMS	10
TDI	11
TDO	12
TCK	13
nTRST	14
External Bus Interface	**(71 pins)**
MA [21:0]	60-48,46-38
MD [31:0]	100-98,95-88,86,84-78,75-63
nWBE [3:0] / SDQM [3:0]	32-29
nSCS [1:0]	23-22
nSRAS	35
nSCAS	36
MCKE	33
nSWE	34
MCLK	25
nWAIT	16
nBTCS	21
nECS [2:0]	20-18
nOE	17

Pad Name	NUC950
Ethernet Interface	**(10 pins)**
PHY_MDC / GPIOF[0]	172
PHY_MDIO / GPIOF[1]	173
PHY_TXD [1:0] / GPIOF[3:2]	175-174
PHY_TXEN / GPIOF[4]	176
PHY_REFCLK / GPIOF[5]	177
PHY_RXD [1:0] / GPIOF[7:6]	179-178
PHY_CRSDV / GPIOF[8]	180
PHY_RXERR / GPIOF[9]	181
AC97/I2S/PWM	**(5 pins)**
AC97_nRESET / I2S_SYSCLK / - / GPIOG[12]	184
AC97_DATAI / I2S_DATAI / PWM [0] / GPIOG[13]	185
AC97_DATAO / I2S_DATAO / PWM [1] / GPIOG[14]	186
AC97_SYNC / I2S_WS / PWM [2] / GPIOG[15]	187
AC97_BITCLK / I2S_BITCLK / PWM [3] / GPIOG[16]	188

USB Interface	(10 pins)
DP0	215
DN0	214
REXT0	212
UPWR0	195
OVI	196
HDS	198
DP1	206
DN1	205
REXT1	203
UPWR1	200
Pad Name	**NUC950**
I2C/USI(SPI/MW)	(4 pins)
SCL0 / SFRM / GPIOG[0]	3
SDA0 / SSPTXD / GPIOG[1]	4
SCL1 / SCLK / GPIOG[2]	5
SDA1 / SSPRXD / GPIOG[3]	6
Pad Name	**NUC950**
UART	(6 pins)
TXD0 / GPIOE[0]	189
RXD0 / GPIOE[1]	190
TXD1(B) / GPIOE[2]	191
RXD1(B) / GPIOE[3]	192
TXD2(IrDA) / GPIOE[6]	193
RXD2(IrDA) / GPIOE[7]	194
Pad Name	**NUC950**

SDIO(SD) / Memory Stick	(8 pins)
SD_CMD / MS_BS / GPIOD[0]	156
SD_CLK / MS_CLK / GPIOD[1]	157
SD_DAT0 / MS_DAT0 / GPIOD[2]	158
SD_DAT1 / MS_DAT1 / GPIOD[3]	159
SD_DAT2 / MS_DAT2 / GPIOD[4]	160
SD_DAT3 / MS_DAT3 / GPIOD[5]	161
SD_CDn / MS_CDn / GPIOD[6]	163
SD_nPWR / MS_nPWR / GPIOD[8]	164
Pad Name	**NUC950**
NAND Flash(SM) / KPI	(15pins)
SM_CS0n / KPI_ROW[0] / GPIOC[0]	142
SM_ALE / KPI_ROW[1] GPIOC[1]	140
SM_CLE / KPI_ROW[2] GPIOC[2]	141
SM_WEn / KPI_ROW[3] GPIOC[3]	143

SM_REn / GPIOC[4]	144
SM_WPn / GPIOC[5]	145
SM_RBn / GPIOC[6]	146
SM_D[7:0] / KPI_COL[7:0] / GPIOC[14:7]	154–147
Pad Name	**NUC950**
LCD	**(23 pins)**
VD [17:0]	130–122,120,118-117,114-109
HSYNC	131
VSYNC	139
VDEN	132
VICLK	133
VOCLK	137
Pad Name	**NUC950**
Miscellaneous	**(6 pins)**
nIRQ [2:0] / GPIOH[2:0]	169-167
nWDOG / GPIOI[16]	2
GPIOE13	165
TEST	166
Power/Ground	**(48 pins)**
VDD18	9,27,76,96,115,135,170,197
VDD33	15,26,47,62,87,101,119,136,162,182
VSS	7,8,24,28,37,61,77,85,97,104,116,121,134,138,155,171,183,199
USBVDDC0 (3.3V)	211
USBVSSC0	210
USBVDDT0 (3.3V)	216
USBVSST0	213
USBVDDC1 (3.3V)	202
USBVSSC1	201
USBVDDT1 (3.3V)	207
USBVSST1	204
PLLVDD18	108,105
PLLVSS	107,106

5. PIN DESCRIPTION

5.1 Pin Description for Interface

Pin Name	IO Type	Description
Clock & Reset (5)		
EXTAL15M	I	15MHz External Clock / Crystal Input for PLL
XTAL15M	O	15MHz Crystal Output
EXTAL48M0	O	48MHz Crystal Output for USB2.0 PHY
XTAL48M0	I	48MHz Crystal Input for USB2.0 PHY
nRESET	I	System Reset (Low active)
TAP Interface (5)		
TCK	ID	JTAG Test Clock, internal pull-down
TMS	IU	JTAG Test Mode Select, internal pull-up
TDI	IU	JTAG Test Data in, internal pull-up
TDO	O	JTAG Test Data out
nTRST	IU	JTAG Reset, active-low, internal pull-up
External Bus Interface (72)		
MA [21:0]	O	Address Bus of external memory and IO devices. (MA[21:13] are set to input mode when nRESET low active)
MD [31:0]	IO (D)	Data Bus of external memory and IO device (Pull-down are programmable)
nWBE [3:0] / SDQM [3:0]	O	Write Byte Enable for specific device (nECS [2:0]). Data Bus Mask signal for SDRAM (nSCS [1:0]), (Low active)
nSCS [1:0]	O	SDRAM chip select for two external banks, (Low active)
nSRAS	O	Row Address Strobe for SDRAM, (Low active)
nSCAS	O	Column Address Strobe for SDRAM, (Low active)
nSWE	O	SDRAM Write Enable, (Low active)
MCKE	O	SDRAM Clock Enable
MCLK	O	System Master Clock Out, SDRAM clock
nWAIT	IU	External Wait, (Low active), internal pull-up
nBTCS	O	ROM/Flash Chip Select, (Low active)
nECS [2:0]	O	External I/O Chip Select, (Low active)
nOE	O	ROM/Flash, External Memory Output Enable, (Low active)
Ethernet RMII Interface (10)		
PHY_MDC	O(IS)	RMII Management Data Clock

PHY_MDIO	IO(D)	RMII Management Data I/O (Pull-down is programmable)
PHY_TXD [1:0]	O(IU)	RMII Transmit Data bus (Pull-up are programmable)
PHY_TXEN	O(ID)	RMII Transmit Enable (Pull-down is programmable)
PHY_REFCLK	O(ID)	RMII Reference Clock. (Pull-down is programmable)
PHY_RXD [1:0]	I(OU)	RMII Receive Data bus (Pull-up are programmable)
PHY_CRSDV	I(OD)	RMII Carrier Sense / Receive Data Valid (Pull-down is programmable)
PHY_RXERR	I(OD)	RMII Receive Data Error (Pull-down is programmable)
AC97/I2S/PWM (5)		
AC97_nRESET / I2S_SYSCLK	O(ID)	AC97 Controller RESET Output. I2S Controller System Clock Output. (Pull-down is programmable)
AC97_DATAI / I2S_DATAI / PWM [0]	IO(D)	AC97 Controller Data Input. I2S Controller Data Input. PWM Channel 0 Output. (Pull-down is programmable)
AC97_DATAO / I2S_DATAO / PWM [1]	O(ID)	AC97 Controller Data Output. I2S Controller Data Output. PWM Channel 1 Output. (Pull-down is programmable)
AC97_SYNC / I2S_WS / PWM [2]	IO(D)	AC97 Controller Synchronous Pulse Output. I2S Controller Word Select. PWM Channel 2 Output. (Pull-down is programmable)
AC97_BITCLK / I2S_BITCLK / PWM [3]	IOSD	AC97 Controller Bit Clock Input. I2S Controller Bit Clock. PWM Channel 3 Output. (Pull-down with Schmitt trigger input)
USB Interface (10)		
DP0	IO	Differential Positive USB Port0 IO signal
DN0	IO	Differential Negative USB Port0 IO signal
REXT0	A	External Resister Connect for Port0
DP1	IO	Differential Positive USB Port1 IO signal
DN1	IO	Differential Negative USB Port1 IO signal
REXT1	A	External Resister Connect for Port1

UPWR1	O	USB Port1 Power Control signal
OVI	I	USB Over Current Detection signal
HDS	I	USB PHY 0 Device/Host Mode Select Control signal
UPWR0	O	USB Port0 Power Control signal This pin is always driven to Low when USB Port0 is at Device mode (the HDS pin at high state)
I2C/USI(SPI/MW) Interface (4)		
SCL0 / SFRM	IOS	I2C Serial Clock Line 0. USI Serial Frame. (Input with Schmitt trigger)
SDA0 / SSPTXD	IOS	I2C Serial Data Line 0. USI Serial Transmit Data. (Input with Schmitt trigger)
SCL1 / SCLK	IOS	I2C Serial Clock Line 1. USI Serial Clock. (Input with Schmitt trigger)
SDA1 / SSPRXD	IOS	I2C Serial Data Line 1. USI Serial Receive Data. (Input with Schmitt trigger)
UART0/UART1/UART2 Interface (6)		
TXD0	IO(D)	UART0 Transmit Data. (Pull-down is programmable)
RXD0	IO(D)	UART0 Receive Data. (Pull-down is programmable)
TXD1	IO(D)	UART1 Transmit Data (Pull-down is programmable)
RXD1	IO(D)	UART1 Receive Data (Pull-down is programmable)
TXD2(IrDA)	IO(D)	UART2 Transmit Data supporting SIR IrDA. (Pull-down is programmable)
RXD2(IrDA)	IO(D)	UART2 Receive Data supporting SIR IrDA. (Pull-down is programmable)
SD/SDIO/Memory Stick Interface (8)		
SD0_CMD / MS0_BS	IO(U)	SD/SDIO Mode – Command/Response (SPI Mode – Data In) Memory Stick Mode – Bus State. (Pull-up is programmable)
SD0_CLK / MS0_CLK	IO(U)	SD/SDIO Mode – Clock; (SPI Mode – Clock) Memory Stick Mode – Clock (Pull-up is programmable)

SD0_DAT0 / MS0_DAT0	IO(U)	SD/SDIO Mode – Data Line Bit 0; Memory Stick Mode – Data Line Bit 0; (Pull-up is programmable)
SD0_DAT1 / MS0_DAT1	IO(U)	SD/SDIO Mode – Data Line Bit 1; Memory Stick Mode – Data Line Bit 1; (Pull-up is programmable)
SD0_DAT2 / MS0_DAT2	IO(U)	SD/SDIO Mode – Data Line Bit 2; Memory Stick Mode – Data Line Bit 2; (Pull-up is programmable)
SD0_DAT3 / MS0_DAT3	IO(U)	SD/SDIO Mode – Data Line Bit 3; Memory Stick Mode – Data Line Bit 3; (Pull-up is programmable)
SD0_CDn / MS0_CDn	IO(U)	SD/SDIO Mode – Card Detect. Memory Stick Mode – Card Detect. (Pull-up is programmable)
SD_nPWR	IO(U)	SD/SDIO Power FET Control Signal Output. (Pull-up is programmable)
NAND Flash Interface (15)		
SM_CS0n	O(IU)	NAND Flash Chip Select #0 (Pull-up is programmable)
SM_ALE	O(IU)	NAND Flash Address Latch Enable (Pull-up is programmable)
SM_CLE	O(IU)	NAND Flash Command Latch Enable (Pull-up is programmable)
SM_WEn	O(IU)	NAND Flash Write Enable (Low active) (Pull-up is programmable)
SM_REn	O(IU)	NAND Flash Read Enable (Low active) (Pull-up is programmable)
SM_WPn	O(IU)	NAND Flash Write Protect (Low active) (Pull-up is programmable)
SM_RBn	I(OU)	NAND Flash Busy (Low active) (Pull-up is programmable)
SM_D[7:0]	IO(U)	NAND Flash Data Bus (Pull-up is programmable)
Keypad Interface (KPI) (12)		
KPI_COL[7:0]	I	Keypad Column Scan Input Bus This bus is shared with NAND Flash Interface, which is programmable setting.
KPI_ROW[3:0]	O	Keypad Row Scan Output Bus This bus is shared with NAND Flash Interface, which is programmable setting.
LCD Interface (23)		

VD [17:0]	O(IU)	LCD Pixel Data Output. (Pull-up is programmable)
HSYNC	O	Horizontal Sync or Line Sync.
VSYNC	O	Vertical Sync or Frame Sync.
VDEN	O	Data Enable or Display Control Signal.
VOCLK	O	Pixel Clock Output.
VICLK	IU	Pixel Clock Input.
Miscellaneous(6)		
nIRQ[2:0]	I(OU)	External Interrupt Request (Pull-up is programmable)
nWDOG	O	Watchdog Timer Timeout Flag (Low active)
GPIOE13	IO(U)	Bit 13 of the GPIOE port
TEST	I	Test Mode This pin has to pull low in normal operation.
Power/Ground		
VDD18	P	Core Logic power (1.8V)
VDD33	P	IO Buffer power (3.3V)
VSS	G	IO Buffer and Core ground (0V)
USBVDDC0	P	USB Port0 PHY power (3.3V)
USBVSSC0	G	USB Port0 PHY ground (0V)
USBVDDT0	P	USB Port0 PHY Transceiver power (3.3V)
USBVSST0	G	USB Port0 PHY Transceiver ground (0V)
USBVDDC1	P	USB Port1 PHY power (3.3V)
USBVSSC1	G	USB Port1 PHY ground (0V)
USBVDDT1	P	USB Port1 PHY Transceiver power (3.3V)
USBVSST1	G	USB Port1 PHY Transceiver ground (0V)
PLLVDD18	P	PLL power (1.8V)
PLLVSS18	G	PLL ground (0V)

5.2 GPIO Share Pin Description

In this chip, there are GPIOC~GPIOI groups for general IO control. All of GPIO pins are shared with the other interface and define as the following

GPIO Group	Shared pin function
GPIOC (15 pins)	NAND Flash Interface / KPI
GPIOC[0]	SM_CS0n / KPI_ROW[0]
GPIOC[1]	SM_ALE / KPI_ROW[1]
GPIOC[2]	SM_CLE / KPI_ROW[2]
GPIOC[3]	SM_WEn / KPI_ROW[3]
GPIOC[4]	SM_REn
GPIOC[5]	SM_WPn
GPIOC[6]	SM_RBn
GPIOC[7]	SM_D[0] / KPI_COL[0]
GPIOC[8]	SM_D[1] / KPI_COL[1]
GPIOC[9]	SM_D[2] / KPI_COL[2]
GPIOC[10]	SM_D[3] / KPI_COL[3]
GPIOC[11]	SM_D[4] / KPI_COL[4]
GPIOC[12]	SM_D[5] / KPI_COL[5]
GPIOC[13]	SM_D[6] / KPI_COL[6]
GPIOC[14]	SM_D[7] / KPI_COL[7]

GPIOD (8 pins)	SD(SDIO) / Memory Stick Interface

GPIOD[0]	SD_CMD / MS_BS
GPIOD[1]	SD_CLK / MS_CLK
GPIOD[2]	SD_DAT0 / MS_DAT0
GPIOD[3]	SD_DAT1 / MS_DAT1
GPIOD[4]	SD_DAT2 / MS_DAT2
GPIOD[5]	SD_DAT3 / MS_DAT3
GPIOD[6]	SD_CDn / MS_CDn
GPIOD[8]	SD_nPWR / MS_nPWR

GPIOE (7 pins)	UART Interface
GPIOE[0]	TXD0
GPIOE[1]	RXD0
GPIOE[2]	TXD1
GPIOE[3]	RXD1
GPIOE[6]	TXD2(IrDA)
GPIOE[7]	RXD2(IrDA)
GPIOE[13]	GPIOE13

GPIOF (10 pins)	RMII Interface
GPIOF [0]	PHY_MDC
GPIOF [1]	PHY_MDIO
GPIOF [3:2]	PHY_TXD [1:0]
GPIOF [4]	PHY_TXEN
GPIOF [5]	PHY_REFCLK
GPIOF [7:6]	PHY_RXD [1:0]
GPIOF [8]	PHY_CRSDV
GPIOF [9]	PHY_RXERR

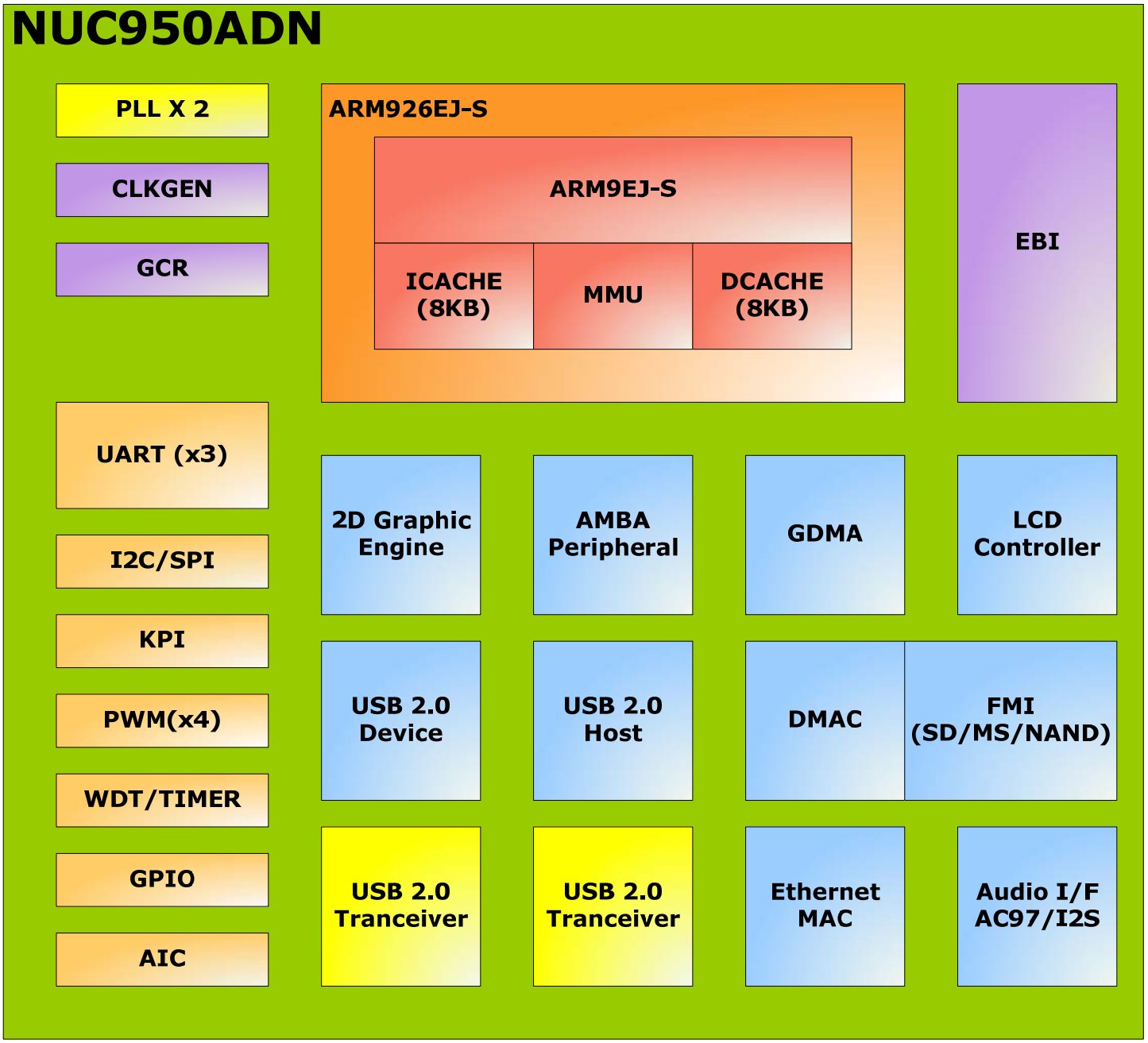
GPIOG (9 pins)	I2C/USI XDMA, AC97/I2S/PWM Interface

GPIOG[0]	SCL0 / SFRM
GPIOG[1]	SDA0 / SSPTXD
GPIOG[2]	SCL1 / SCLK
GPIOG[3]	SDA1 / SSPRXD
GPIOG[12]	AC97_nRESET I2S_SYSCLK
GPIOG[13]	AC97_DATAI / I2S_DATAI / PWM [0]
GPIOG[14]	AC97_DATAO / I2S_DATAO / PWM [1]
GPIOG[15]	AC97_SYNC / I2S_WS / PWM [2]
GPIOG[16]	AC97_BITCLK / I2S_BITCLK / PWM [3]

GPIOH (3 pins)	nIRQ Interface
GPIOH[2:0]	nIRQ[2:0]

GPIOI (1 pin)	Watch Dog Signal
GPIOI[16]	nWDOG

6. FUNCTIONAL BLOCK



7. ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Ambient temperature	-20 °C ~ 70 °C
Storage temperature	-50 °C ~ 125°C
Voltage on any pin	-0.5V ~ 6V
Power supply voltage (Core logic)	-0.5V ~ 2.5V
Power supply voltage (IO Buffer)	-0.5V ~ 4.6V
Injection current (latch-up testing)	100mA
Crystal Frequency	4MHz ~ 30MHz

7.2 DC Specifications

7.2.1 Digital DC Characteristics

(Normal test conditions: VDD33 = 3.3V+/- 10%, VDD18/PLLVDD18 = 1.8V+/- 10%, USBVDDC0/USBVDDC1/USBVDDT0/USBVDDT1= 3.3V+/-5%, TA = -20 °C ~ 70 °C unless otherwise specified)

Symbol	Parameter	Condition	Min	TYP	Max	Unit
VDD33	Power Supply		2.97	-	3.63	V
VDD18/ PLLVDD18	Power Supply		1.62	-	1.98	V
USBVDDC0/ USBVDDC1/ USBVDDT0/ USBVDDT1	Power Supply		3.13	-	3.46	V
V_{IL}	Input Low Voltage		-0.3	-	0.8	V
V_{IH}	Input High Voltage		2.0	-	5.5	V
VT+	Schmitt Trigger positive-going threshold		1.5	-	1.62	V
VT-	Schmitt trigger negative-going threshold		1.14	-	1.27	V
V_{OL}	Output Low Voltage	Depend on driving	-	-	0.4	V
V_{OH}	Output High Voltage	Depend on driving	2.4	-	-	V
I_{IH}	Input High Current	V_{IN} = 2.4 V	-1	-	1	uA
I_{IL}	Input Low Current	V_{IN} = 0.4 V	-1	-	1	uA

I_{OC}	Operation Current	Note 1	-	340	-	mA
I_{SC}	Standby Current	Note 2	-	100	-	uA

Note1:

This operation current is measured on VDD18 @ 1.8V, and all of IP clocks are enable with CPU clock/system clock @ 200MHz / 100MHz.

Note2:

The standby current is measured on VDD18 @1.8V, and all of IP clocks are disabled with power-down mode, all of GPIO pins are set to output and clock pins keep at 0V.

7.2.2 USB Low-/Full-Speed DC Electrical Specifications

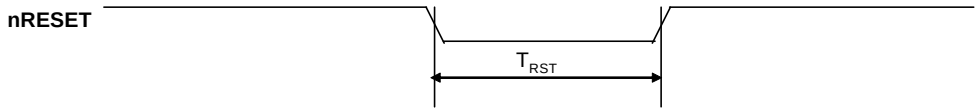
Symbol	Parameter	Conditions	Min	Nom	Max
V_{IH}	Pad input high voltage		2.0V		
V_{IL}	Pad input low voltage				0.8V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2V		
V_{CM}	Common mode voltage range	include V_{DI} range	0.8V		2.5V
V_{SE}	Single-ended receiver threshold		0.8V		2.0V
V_{OL}	Pad output low voltage		0V		0.3V
V_{OH}	Pad output high voltage		2.8V		3.6V
V_{CRS}	Differential output signal cross-point voltage		1.3V		2.0V
R_{PU}	Internal pull-up resistor	Bus idle	900Ω		1575Ω
		Receiving	1425Ω		3090Ω
R_{PD}	Internal pull-down resistor		14.25KΩ		24.80KΩ
Z_{DRV}	Driver output resistance‡	Steady state drive		10Ω	
C_{IN}	Transceiver pad capacitance	Pad to ground			20pF

7.2.3 USB High-Speed DC Electrical Specifications

Symbol	Parameter	Conditions	Min	Typ	Max
V_{HSDI}	High-speed differential input signal level	|PADP-PADM|	150mV		
V_{HSSQ}	High-speed SQ detection threshold	|PADP-PADM|	100mV		150mV
V_{HSCM}	High-speed common mode voltage range		-50mV		500mV
V_{HSOH}	High-speed data signaling high		360mV		440mV
V_{HSOL}	High-speed data signaling low		-10mV		10mV
V_{CHIRPJ}	Chirp J level		700mV		1100mV
V_{CHIRPK}	Chirp K level		-900mV		-500mV
Z_{HSDRV}	High-speed driver output resistance	45Ω±10%	40.5Ω		49.5Ω

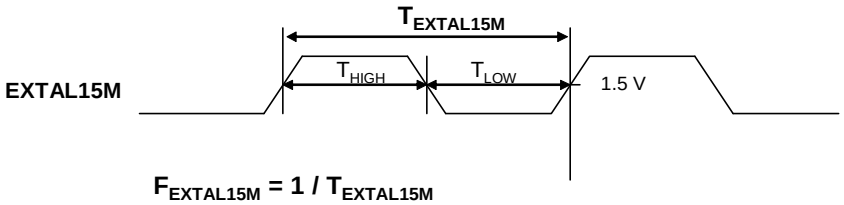
7.3 AC Specifications

7.3.1 RESET AC Characteristics



Symbol	Parameter	Min.	Max.	Unit
T_{RST}	Reset Pulse Width after Power stable	1.0	-	ms

7.3.2 Clock Input Characteristics

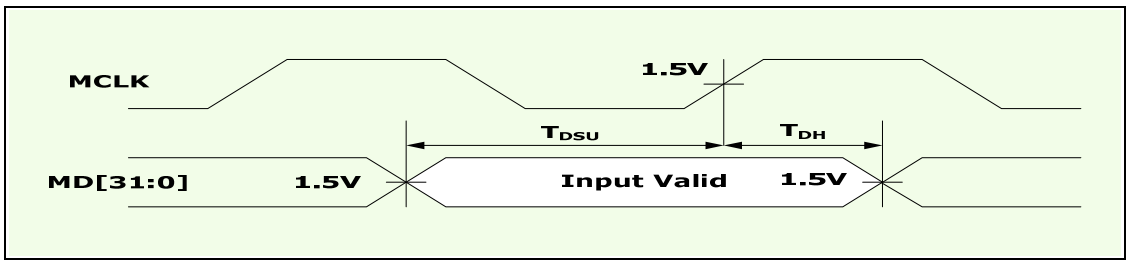


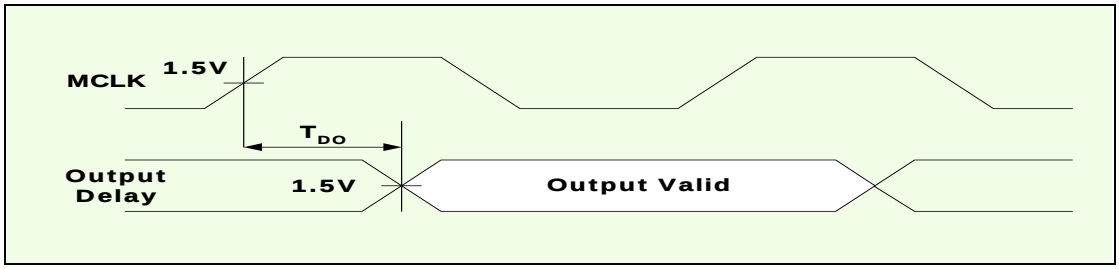
$F_{EXTAL15M} = 1 / T_{EXTAL15M}$

$EXTAL15M_{DUTY} = T_{HIGH} / (T_{HIGH} + T_{LOW})$

Symbol	Parameter	Min.	Typ.	Max.	Unit
$F_{EXTAL15M}$	Clock Input Frequency	-	15.0	-	MHz
$EXTAL15M_{DUTY}$	Clock Input Duty Cycle	45	50	55	%
V_{IL} (EXTAL15M)	EXTAL15M Input Low Voltage	0	-	0.8	V
V_{IH} (EXTAL15M)	EXTAL15M Input High Voltage	2.0	-	VDD33+0.3	V

7.3.3 EBI/SDRAM Interface AC Characteristics

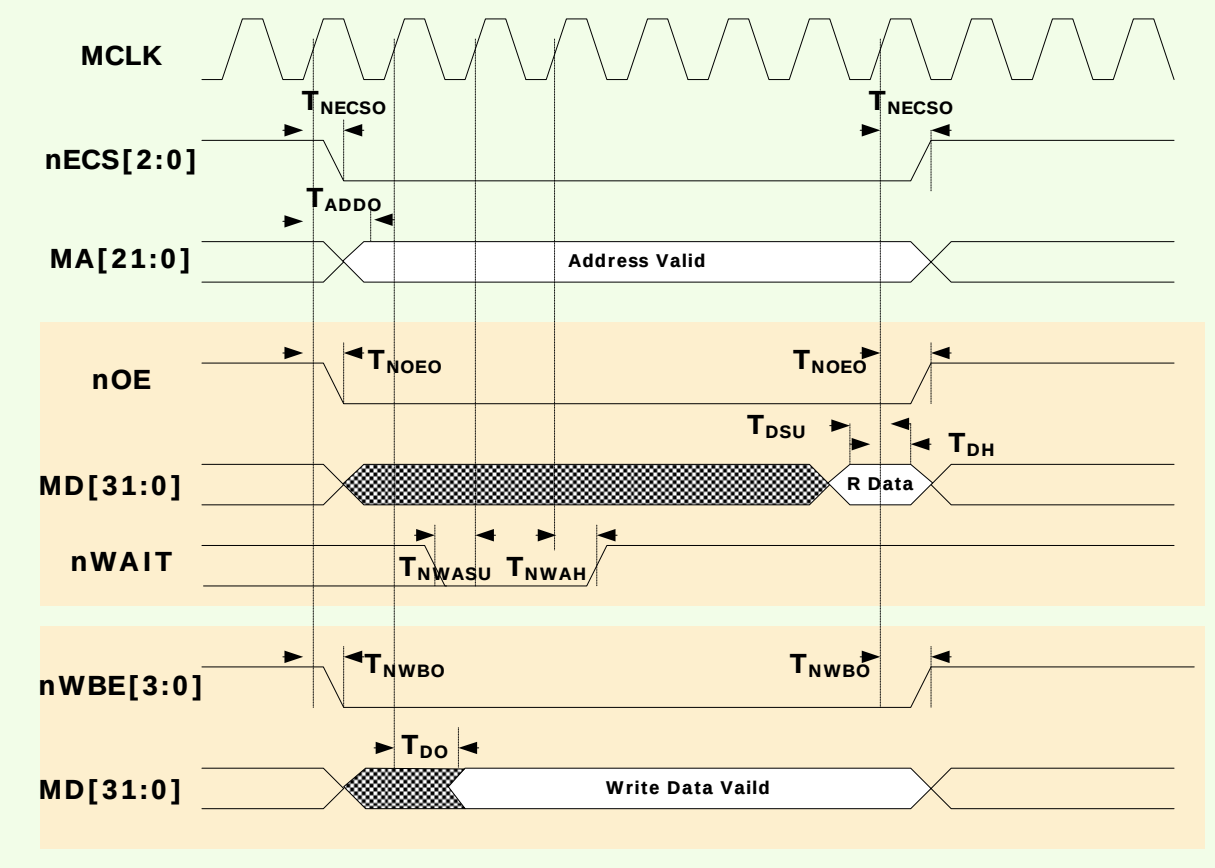




Symbol	Parameter	Min.	Max.	Unit
F_{MCLK}	SDRAM Clock Output Frequency	-	100	MHz
T_{DSU}	MD[31:0]] Input Setup Time	2	-	ns
T_{DH}	MD[31:0] Input Hold Time	2	-	ns
T_{OSU}	SDRAM Output Signal Valid Delay Time	2*	7*	ns

* The above T_{OSU} is based on the EBI CKSKEW register default setting on 0x48 and F_{MCLK} at 100MHz

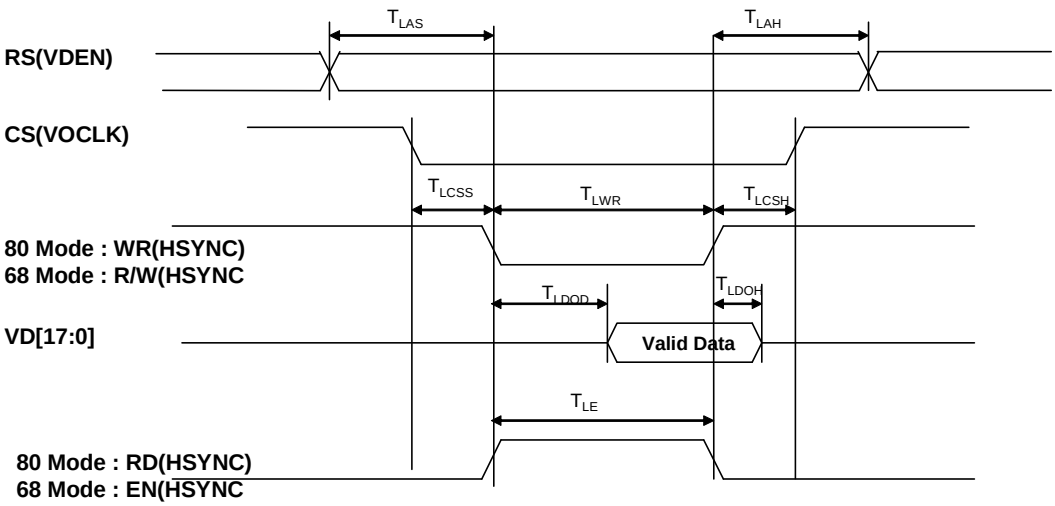
7.3.4 EBI/ (ROM/SRAM/External I/O) AC Characteristics



Symbol	Parameter	Min.	Max.	Unit
T_{ADDO}	Address Output Delay Time	2*	7*	ns
T_{NCSO}	ROM/SRAM/Flash or External I/O Chip Select Delay Time	2*	7*	ns
T_{NOEO}	ROM/SRAM or External I/O Bank Output Enable Delay	2*	7*	ns
T_{NWBO}	ROM/SRAM or External I/O Bank Write Byte Enable Delay	2*	7*	ns
T_{DH}	Read Data Hold Time	5		ns
T_{DSU}	Read Data Setup Time	1		ns
T_{DO}	Write Data Output Delay Time (SRAM or External I/O)	2*	7*	ns
T_{NWASU}	External Wait Setup Time	3		ns
T_{NWAH}	External Wait Hold Time	1		ns

The above data are based on the EBI CKSKEW register default setting on 0x48 and F_{MCLK} at 100MHz

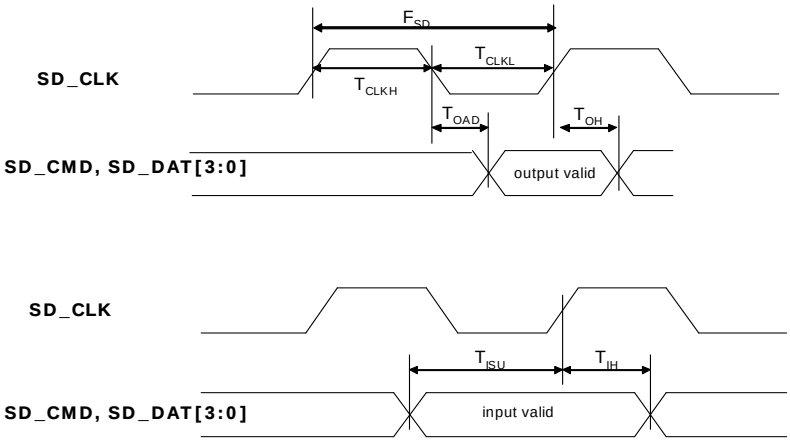
7.3.5 LCD Interface: MPU Type AC Characteristics



Symbol	Parameter	Conditions	Min.	Max.	Unit
T_{LCSS}	Chip Select Set-up Time	-	1/2	-	*PCLK
T_{LCSH}	Chip Select Hold Time	-	1/2	-	*PCLK
T_{LAS}	Address Set-up Time	-	1	-	*PCLK
T_{LAH}	Address Hold Time	-	1	-	*PCLK
T_{LDOD}	Write Data Active Delay	-	0	1/2	*PCLK
T_{LDOH}	Write Data Hold Time	-	1/2	-	*PCLK
T_{LWR}	WR Pulse Width	80 Mode	1	-	*PCLK
T_{LE}	LE Pulse Width	68 Mode	1/2	-	*PCLK

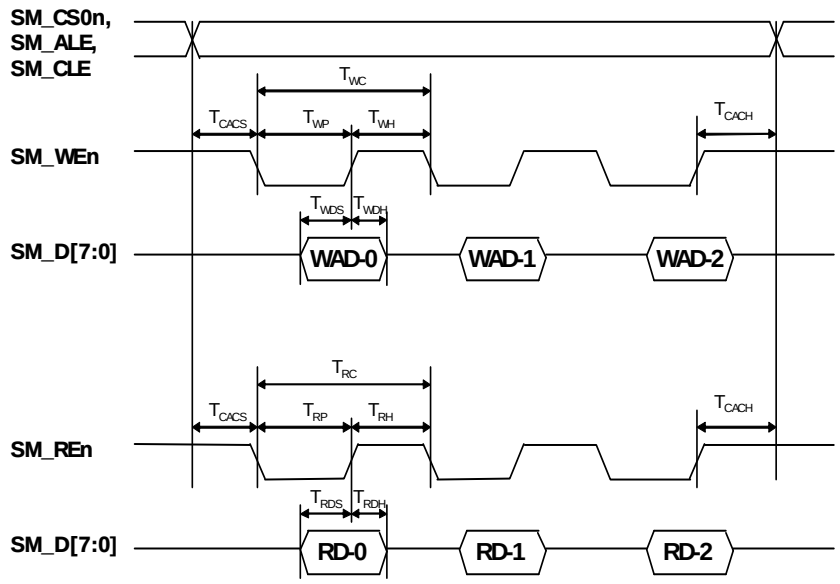
*PCLK is the engine clock of the LCD Controller

7.3.6 SD Host Interface AC Characteristics



Symbol	Parameter	Conditions	Min.	Max.	Unit
F_{SD}	SD Clock Frequency	Identification Mode	**100**	**400**	KHz
F_{SD}	SD Clock Frequency	Data Transfer Mode	-	**50**	MHz
T_{CLKH}	SD Clock High Time	-	**10**	-	ns
T_{CLKL}	SD Clock Low Time	-	**10**	-	ns
T_{ISU}	SD CMD & Data Input Setup Time	-	**5**	-	ns
T_{IH}	SD CMD & Data Input Hold Time	-	**5**	-	ns
T_{OAD}	SD Output Active Delay (Falling Edge)	-	-	**14**	ns
T_{OH}	SD Output Hold Time	-	**0**	-	ns

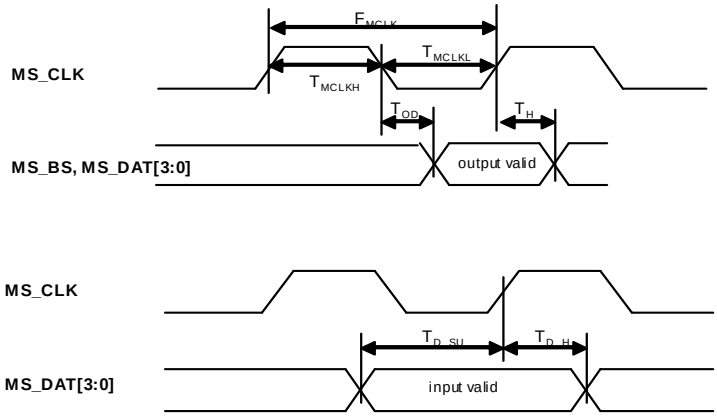
7.3.7 NAND Flash Memory Interface AC Characteristics



Symbol	Parameter	Min.	Max.	Unit
T_{CACS}	SM_CS0n, SM_ALE, SM_CLE Setup Time before SM_WEn, SM_REn Low	**20**	-	ns
T_{CACH}	SM_CS0n, SM_ALE, SM_CLE Hold Time after SM_WEn, SM_REn High	**40**	-	ns
T_{WP}	Write Pulse Width	**40**	-	ns
T_{WH}	SM_WEn High Time	**20**	-	ns
T_{WC}	Write Cycle Time	**80**	-	ns
T_{WDS}	Write Data Output Setup Time	**30**	-	ns
T_{WDH}	Write Data Output Hold Time	**20**	-	ns
T_{RP}	Read Pulse Width	**60**	-	ns
T_{RH}	SM_REn High Time	**20**	-	ns
T_{RC}	Read Cycle Time	**80**	-	ns
T_{RDS}	Read Data Input Setup Time	**6**	-	ns

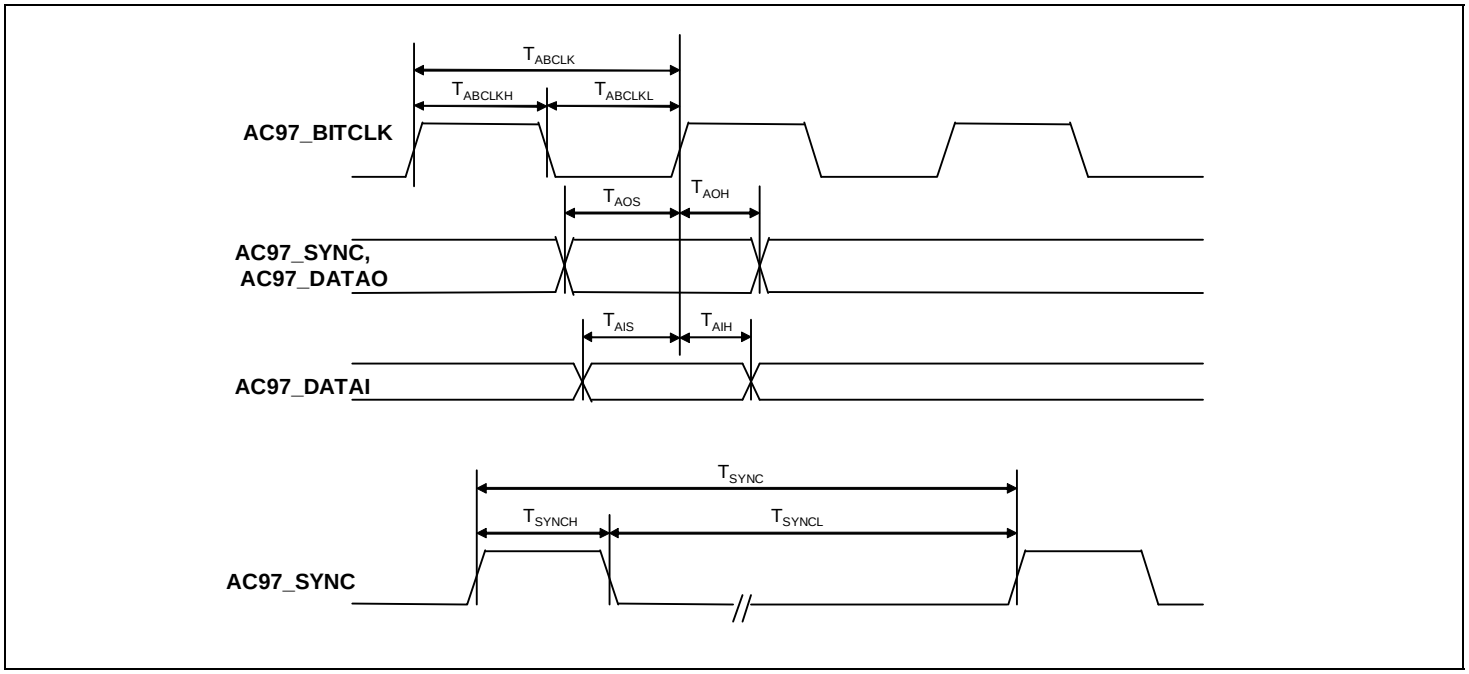
T_{RDH}	Read Data Input Hold Time	**20**	-	ns

7.3.8 Memory Stick Interface AC Characteristics



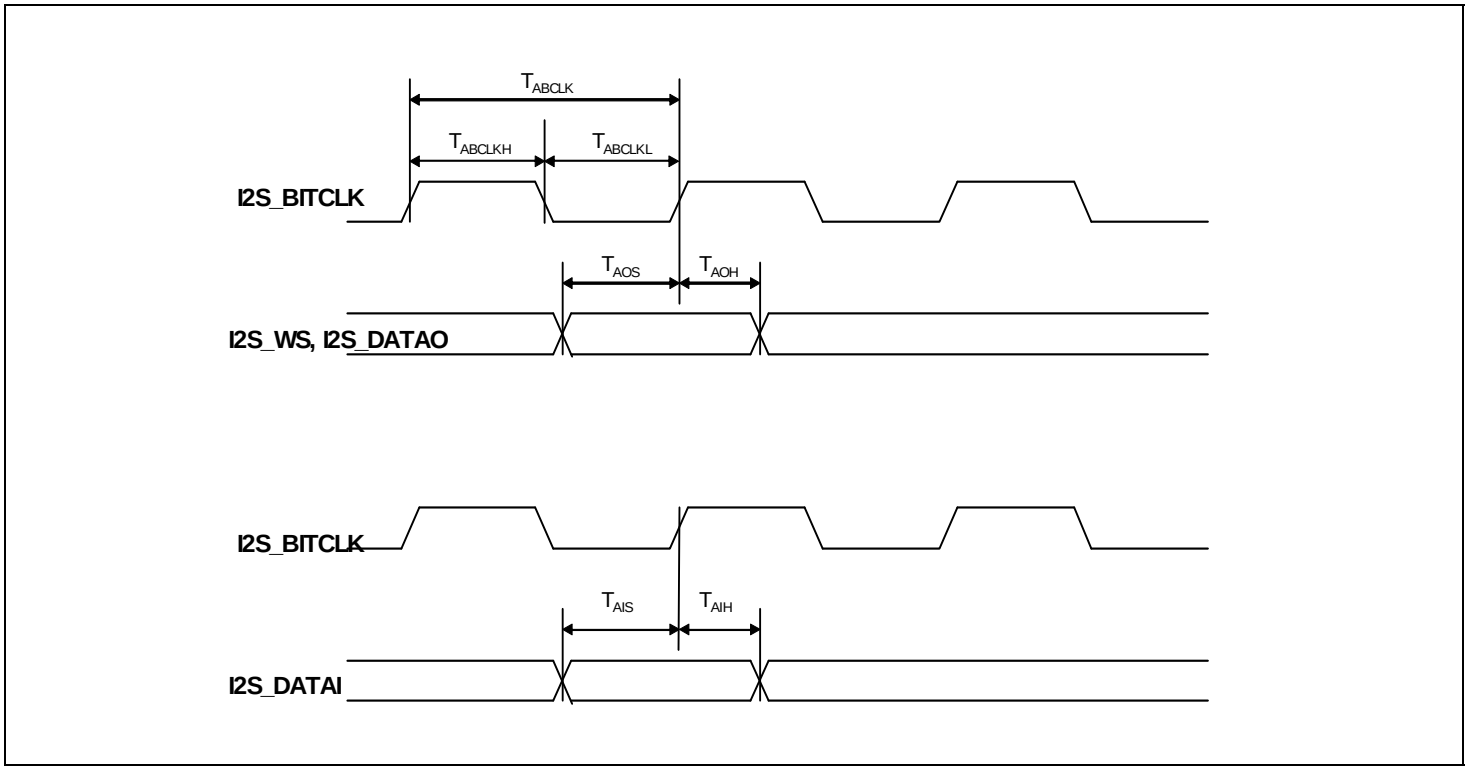
Symbol	Parameter	Conditions	Min.	Max.	Unit
F_{MCLK}	MS_CLK Clock Frequency	Serial Mode	**5**	**20**	MHz
F_{MCLK}	MS_CLK Clock Frequency	Parallel Mode	**10**	**40**	MHz
T_{MCLKH}	MS_CLK Clock High Time		**5**	-	ns
T_{MCLKL}	MS_CLK Clock Low Time		**5**	-	ns
T_{BS_OD}	MS_BS Output Delay (Falling Edge)		**5**	**15**	ns
T_{BS_H}	MS_BS Output Hold Time		**1**	-	ns
T_{D_SU}	Data Input Setup Time		**8**	-	ns
T_{D_H}	Data input Hold Time		**1**	-	ns
T_{D_OD}	Data Output Delay (Falling Edge)		**8**	**15**	ns
T_{D_OD}	Data Output Hold Time		**1**	-	ns

7.3.9 Audio AC-Link Interface AC Characteristics



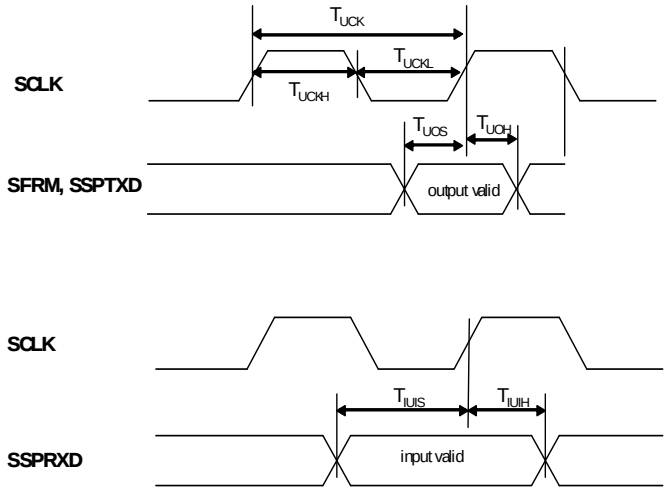
Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{ABCLKH}	Audio Bit Clock Input High Time	**36.6**	**40.7**	**44.8**	ns
T_{ABCLKH}	Audio Bit Clock Input Low Time	**36.6**	**40.7**	**44.8**	ns
T_{ABCLK}	Audio Bit Clock Input Cycle Time	-	**81.4**	-	ns
T_{AOS}	Audio Output Signal (AC97_SYNC, AC97_DATAO) Setup Time	**15**	-	-	ns
T_{AOH}	Audio Output Signal (AC97_SYNC, AC97_DATAO) Hold Time	**5**	-	-	ns
T_{AIS}	Audio Data Input Setup Time	**15**	-	-	ns
T_{AIH}	Audio Data Input Hold Time	**5**	-	-	ns
T_{SYNCH}	Sync Signal Output High Time	-	**20.8**	-	ns
T_{SYNCH}	Sync Signal Output Low Time	-	**1.3**	-	ns
T_{SYNC}	Sync Signal Output Cycle Time	-	**19.5**	-	ns

7.3.10 Audio I2S Interface AC Characteristics



Symbol	Parameter	Min.	Max.	Unit
T_{ABCLKH}	Audio Bit Clock Output High Time	**18.3**	-	ns
T_{ABCLKH}	Audio Bit Clock Output Low Time	**18.3**	-	ns
T_{ABCLK}	Audio Bit Clock Output Cycle Time	**40.7**	-	ns
T_{AOS}	Audio Data Output Setup Time	**4.5**	-	ns
T_{AOH}	Audio Data Output Hold Time	**4.5**	-	ns
T_{AIS}	Audio Data Input Setup Time	**4.5**	-	ns
T_{AIH}	Audio Data Input Hold Time	**4.5**	-	ns

7.3.11 USI (SPI/MW) Interface AC Characteristics



Symbol	Parameter	Min.	Max.	Unit
T_{CLKH}	Clock Output High Time	**14.6**	-	ns
T_{CLKL}	Clock Output Low Time	**15.8**	-	ns
T_{CLK}	Clock Cycle Time	**30.4**	**-**	ns
T_{UOS}	SFRM, SSPTXD Output Setup Time	**15**	-	ns
T_{UOH}	SFRM, SSPTXD Output Hold Time	**13**	-	ns
T_{UIS}	SSPRXD Input Setup Time	**10**	-	ns
T_{UIH}	SSPRXD Input Hold Time	**10**	-	ns

7.3.12 USB Transceiver AC Characteristics

USB Transceiver: Low-Speed AC Electrical Specifications

Symbol	Parameter	Conditions	Min	Typ	Max
T_{LR}	Low-speed driver rise time	C_L=50pF	75ns		300ns
T_{LF}	Low-speed driver fall time	C_L=50pF	75ns		300ns
T_{LRFM}	Low-speed rise/fall time matching	$T_{LRFM} = T_{LR} / T_{LF}$	80%		125%

USB Transceiver: Full-Speed AC Electrical Specifications

Symbol	Parameter	Conditions	Min	Typ	Max
T_{FR}	Full-speed driver rise time	C_L=50pF	4ns		20ns
T_{FF}	Full-speed driver fall time	C_L=50pF	75ns		20ns
T_{FRFM}	Full-speed rise/fall time matching	$T_{FRFM} = T_{FR} / T_{FF}$	90%		111.11 %

USB Transceiver: High-Speed AC Electrical Specifications

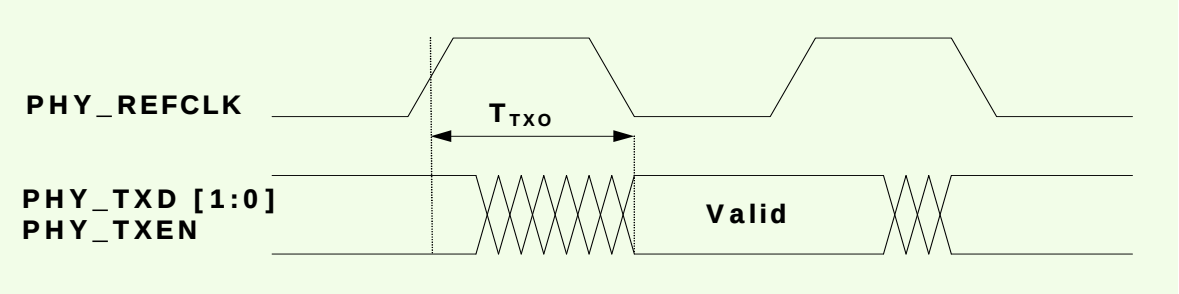
Symbol	Parameter	Conditions	Min	Typ	Max
T_{HSR}	High-speed driver rise time	Z_{HSDRV}=45Ω	500ps		900ps
T_{HSF}	High-speed driver fall time	Z_{HSDRV}=45Ω	500ps		900ps
	High-speed driver waveform requirement		Eye diagram of template 1**		
	High-speed receiver waveform requirement		Eye diagram of template 4††		
	High-speed jitter requirement	Data source end	Eye diagram of template 1**		
		Receiver end	Eye diagram of template 4††		

** Check "Universal Serial Bus Specification Revision 2.0" in page 133.

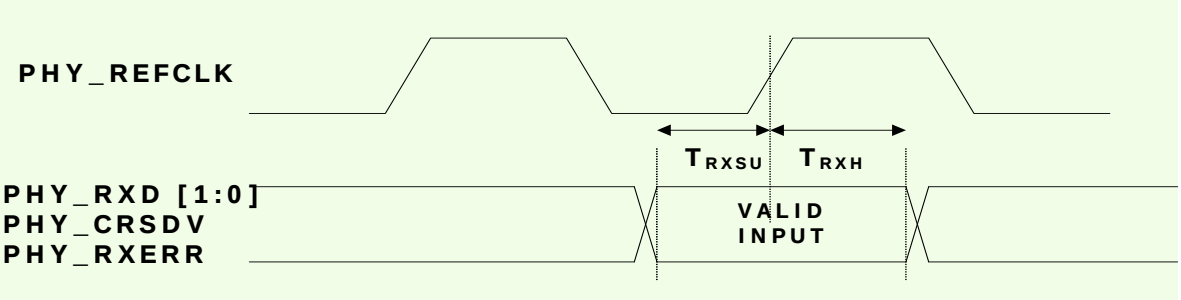
†† Check "Universal Serial Bus Specification Revision 2.0" in page 136.

7.3.13 EMC RMII AC Characteristics

The signal timing characteristics conforms to the guidelines specified in IEEE Std. 802.3.

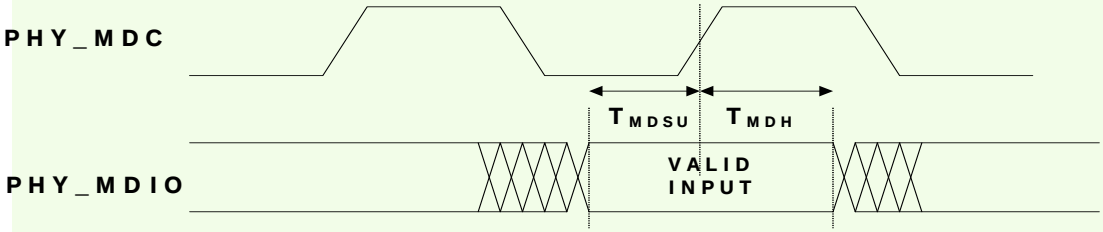


Transmit Signal Timing Relationships at RMII

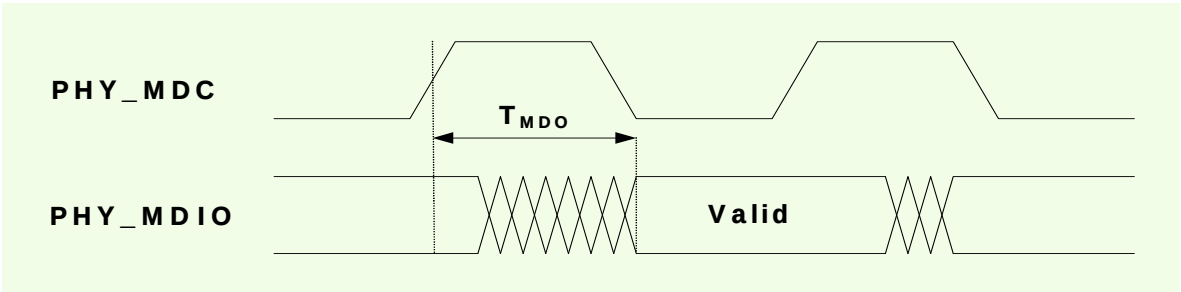


Receive Signal Timing Relationships at RMII

Symbol	Parameter	Min	Max	Unit
T_{TxO}	Transmit Output Delay Time	7	14	ns
T_{RxSU}	Receive Setup Time	4		ns
T_{RxH}	Receive Hold Time	2		ns



PHY_MDIO Read from PHY Timing

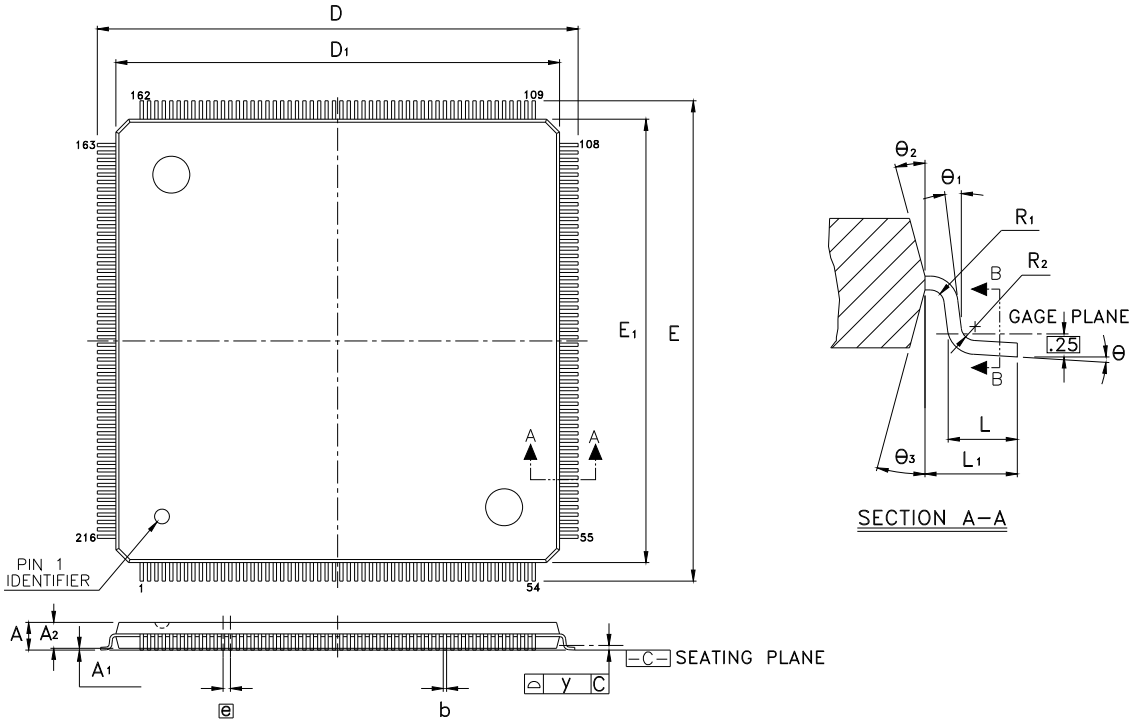


PHY_MDIO Write to PHY Timing

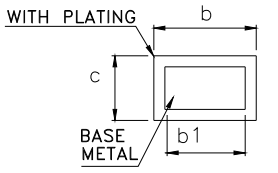
Symbol	Parameter	Min	Max	Unit
T_{MDO}	PHY_MDIO Output Delay Time	0	15	ns
T_{MDSU}	PHY_MDIO Setup Time	5		ns
T_{MDH}	PHY_MDIO Hold Time	5		ns

8. PACKAGE SPECIFICATIONS

NUC950ADN LQFP216L (24X24X1.4 mm, footprint 2.0mm)



SECTION A–A



SECTION B–B

Controlling Dimension :Millimeters

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	0.14	0.20	0.004	0.006	0.008
D	25.85	26.00	26.15	1.018	1.024	1.030
D1	23.90	24.00	24.10	0.941	0.945	0.949
E	25.85	26.00	26.15	1.018	1.024	1.030
E1	23.90	24.00	24.10	0.941	0.945	0.949
e	0.40 BSC			0.0157 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
y	0.08			0.00314		

9. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	March 03, 2009	-	Initial Issued

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