



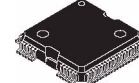
MC9S08AC128 8-Bit Microcontroller Data Sheet

MC9S08AC128

917A-03

840B-01

824D-02



8-Bit HCS08 Central Processor Unit (CPU)

- 40-MHz HCS08 CPU (central processor unit)
- 20-MHz internal bus frequency
- HC08 instruction set with added BGND, CALL and RTC instructions
- Memory Management Unit to support paged memory.
- Linear Address Pointer to allow direct page data accesses of the entire memory map

Development Support

- Background debugging system
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- On-chip in-circuit emulator (ICE) Debug module containing three comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow addresses and event-only data. Supports both tag and force breakpoints.

Memory Options

- Up to 128K FLASH — read/program/erase over full operating voltage and temperature
- Up to 8K Random-access memory (RAM)
- Security circuitry to prevent unauthorized access to RAM and FLASH contents

Clock Source Options

- Clock source options include crystal, resonator, external clock, or internally generated clock with precision NVM trimming using ICG module

System Protection

- Optional computer operating properly (COP) reset with option to run from independent internal clock source or bus clock
- CRC module to support fast cyclic redundancy checks on system memory
- Low-voltage detection with reset or interrupt
- Illegal opcode detection with reset
- Master reset pin and power-on reset (POR)

Power-Saving Modes

- Wait plus two stops

Peripherals

- **ADC** — 16-channel, 10-bit resolution, 2.5 μ s conversion time, automatic compare function, temperature sensor, internal bandgap reference channel
- **SCIx** — Two serial communications interface modules supporting LIN 2.0 Protocol and SAE J2602 protocols; Full duplex non-return to zero (NRZ); Master extended break generation; Slave extended break detection; Wakeup on active edge
- **SPIx** — One full and one master-only serial peripheral interface modules; Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting
- **IIC** — Inter-integrated circuit bus module; Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 10 bit addressing
- **TPMx** — One 2-channel and two 6-channel 16-bit timer/pulse-width modulator (TPM) modules: Selectable input capture, output compare, and edge-aligned PWM capability on each channel. Each timer module may be configured for buffered, centered PWM (CPWM) on all channels
- **KBI** — 8-pin keyboard interrupt module

Input/Output

- Up to 70 general-purpose input/output pins
- Software selectable pullups on input port pins
- Software selectable drive strength and slew rate control on ports when used as outputs

Package Options

- 80-pin low-profile quad flat package (LQFP)
- 64-pin quad flat package (QFP)
- 48-pin quad flat no-lead package (QFN)
- 44-pin low-profile quad flat package (LQFP)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Table of Contents

| | | | |
|--|----|--|--|
| Chapter 1 | | | |
| Device Overview | 3 | | |
| 1.1 MCU Block Diagram | 3 | | |
| Chapter 2 | | | |
| Pins and Connections | 5 | | |
| 2.1 Device Pin Assignment | 5 | | |
| Chapter 3 | | | |
| Electrical Characteristics and Timing Specifications | 11 | | |
| 3.1 Introduction | 11 | | |
| 3.2 Parameter Classification | 11 | | |
| 3.3 Absolute Maximum Ratings | 11 | | |
| 3.4 Thermal Characteristics | 13 | | |
| 3.5 ESD Protection and Latch-Up Immunity | 14 | | |
| 3.6 DC Characteristics | 14 | | |
| 3.7 Supply Current Characteristics | 18 | | |
| 3.8 ADC Characteristics | 21 | | |
| 3.9 Internal Clock Generation Module Characteristics | 24 | | |
| 3.9.1 ICG Frequency Specifications | 25 | | |
| 3.10 AC Characteristics | 27 | | |
| 3.10.1 Control Timing | 27 | | |
| 3.10.2 Timer/PWM (TPM) Module Timing | 28 | | |
| 3.11 SPI Characteristics | 30 | | |
| 3.12 FLASH Specifications | 33 | | |
| 3.13 EMC Performance | 34 | | |
| 3.13.1 Radiated Emissions | 34 | | |
| Chapter 4 | | | |
| Ordering Information and Mechanical Drawings | 35 | | |
| 4.1 Ordering Information | 35 | | |
| 4.2 Orderable Part Numbering System | 35 | | |
| 4.3 Mechanical Drawings | 35 | | |
| Chapter 5 | | | |
| Revision History | 37 | | |

Related Documentation

MC9S08AC128 Series Reference Manual (MC9S08AC128RM)

contains extensive product information including modes of operation, memory, resets and interrupts, register definitions, port pins, CPU, and all peripheral module information.

For the latest version of the documentation, check our website at:

<http://www.freescale.com>

Chapter 1

Device Overview

The MC9S08AC128 is a member of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). The MC9S08AC128 uses the enhanced HCS08 core.

1.1 MCU Block Diagram

The block diagram in [Figure 1-1](#) shows the structure of the MC9S08AC128 Series MCU.

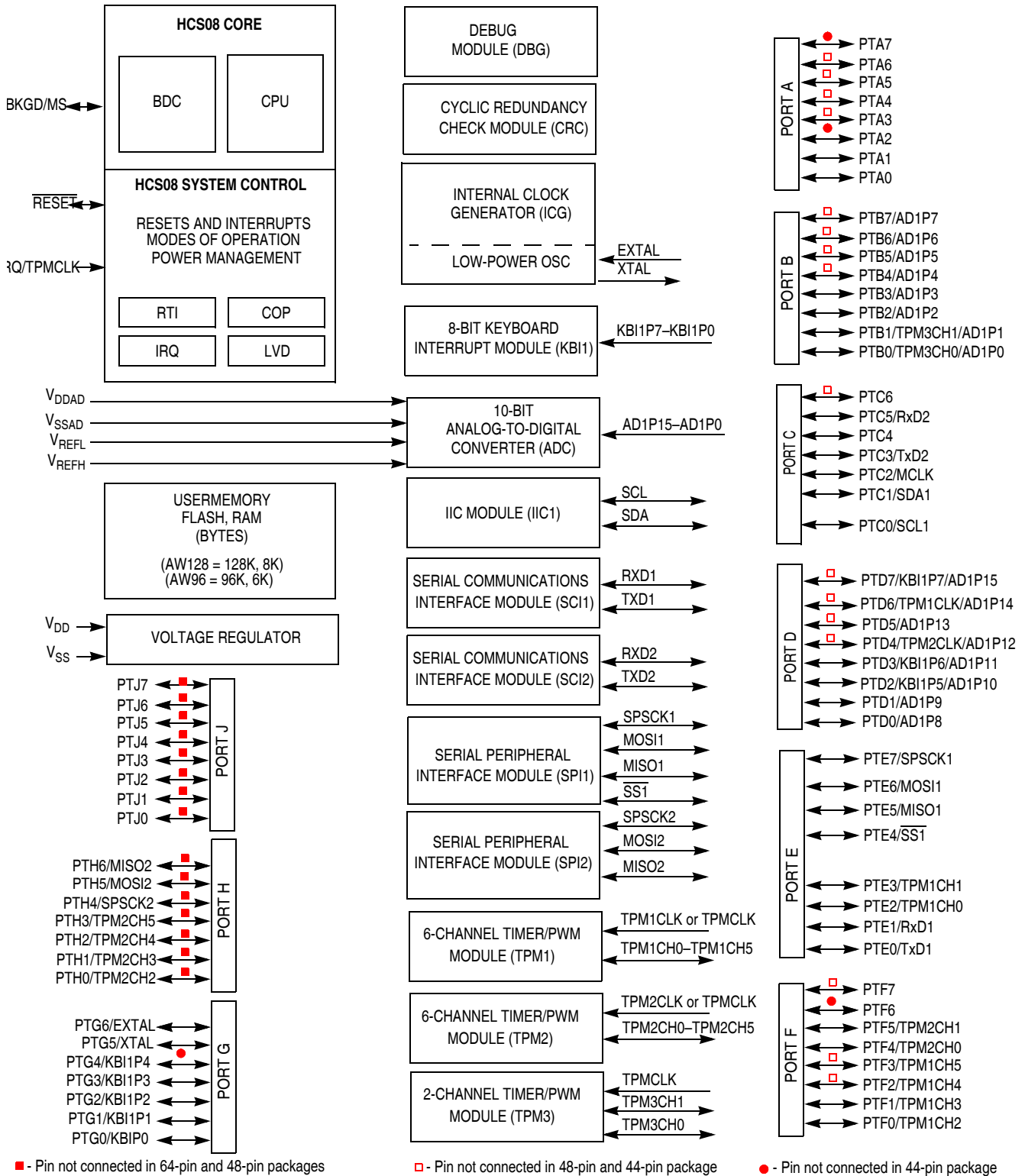


Figure 1-1. MC9S08AC128 Series Block Diagram

Chapter 2

Pins and Connections

This section describes signals that connect to package pins. It includes pinout diagrams, recommended system connections, and detailed discussions of signals.

2.1 Device Pin Assignment

Figure 2-1 shows the 80-pin LQFP package pin assignments for the MC9S08AC128 Series device.

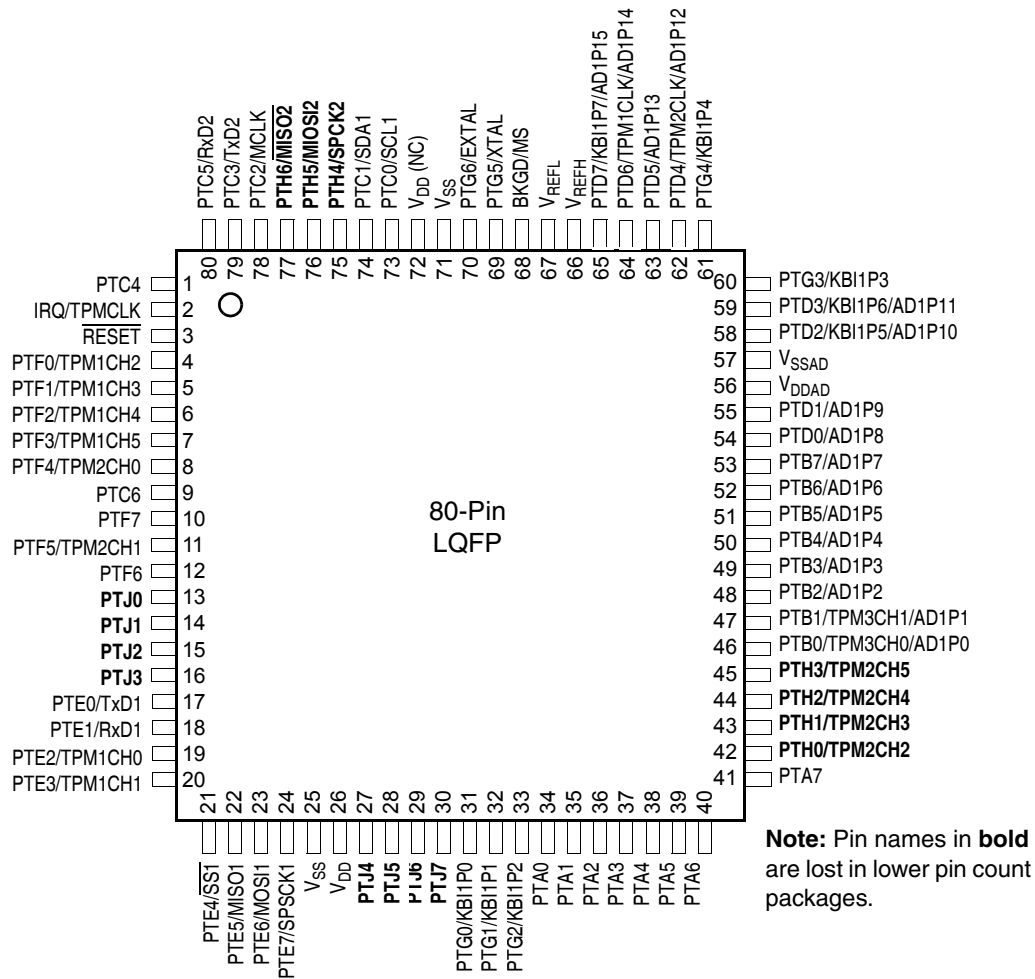


Figure 2-1. MC9S08AC128 Series in 80-Pin LQFP Package

Figure 2-2 shows the 64-pin package assignments for the MC9S08AC128 Series devices.

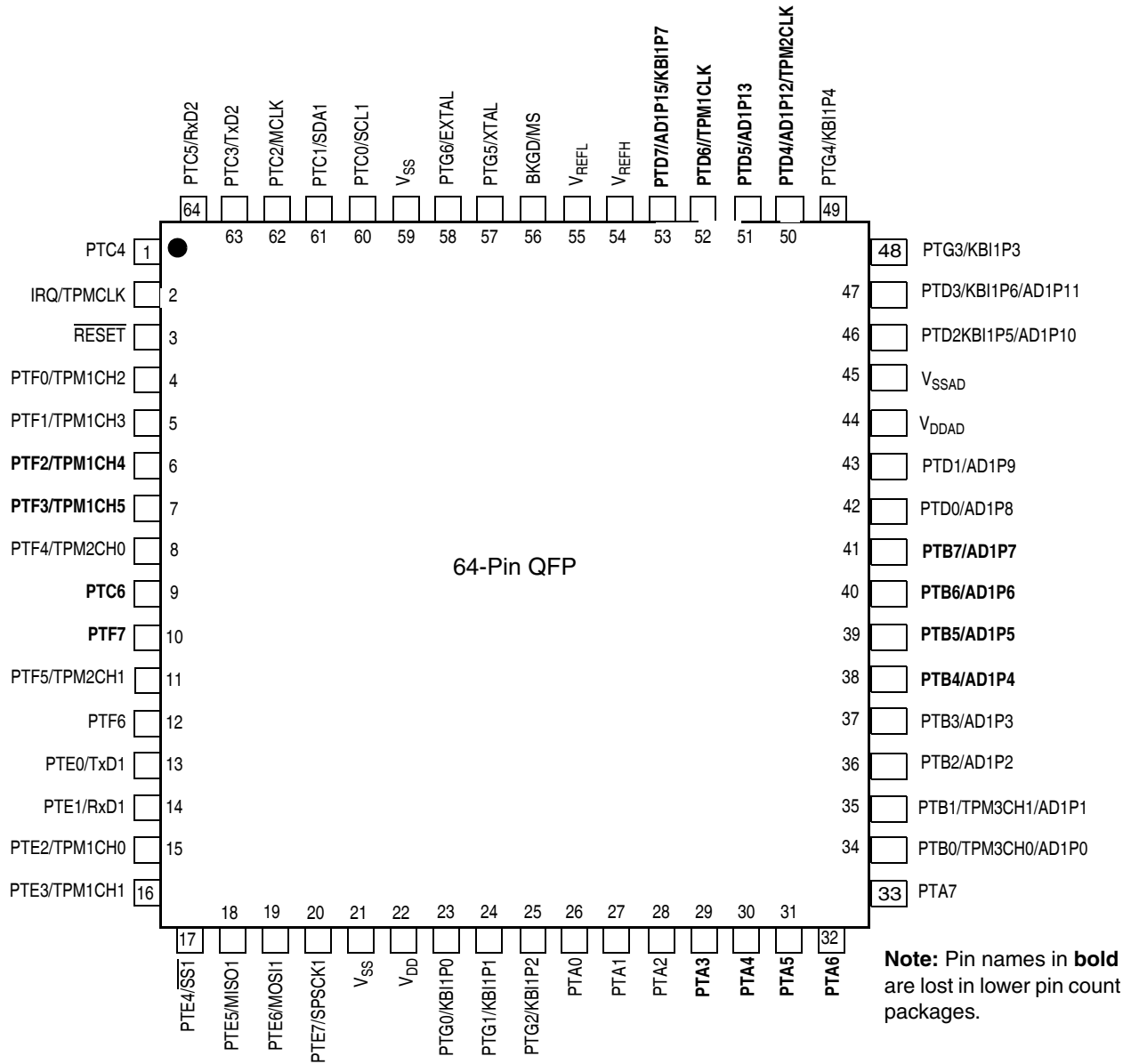
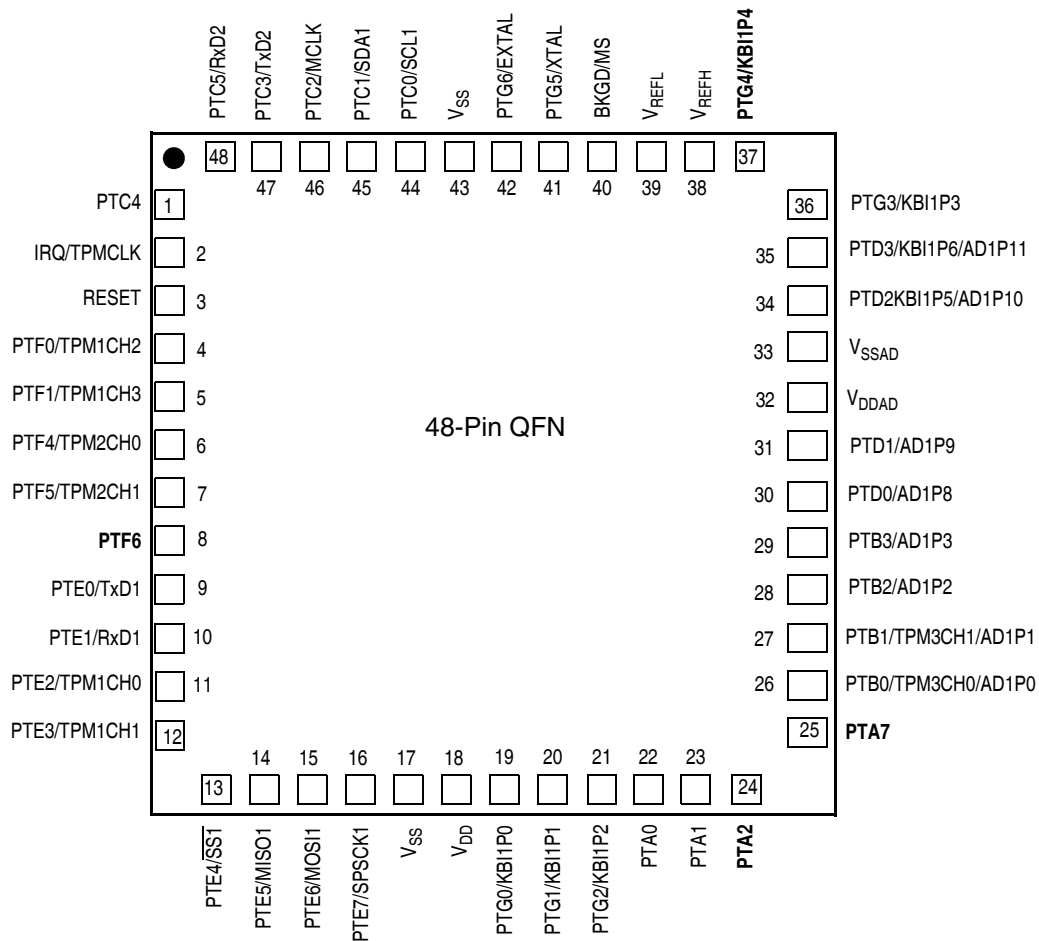


Figure 2-2. MC9S08AC128 Series in 64-Pin QFP Package

Figure 2-1 shows the 48-pin package assignments for the MC9S08AC128 Series devices.



Note: Pin names in bold are lost in lower pin count packages.

Figure 2-1. MC9S08AC128 Series in 48-Pin QFN Package

Figure 2-3 shows the 44-pin LQFP pin assignments for the MC9S08AC128 Series device.

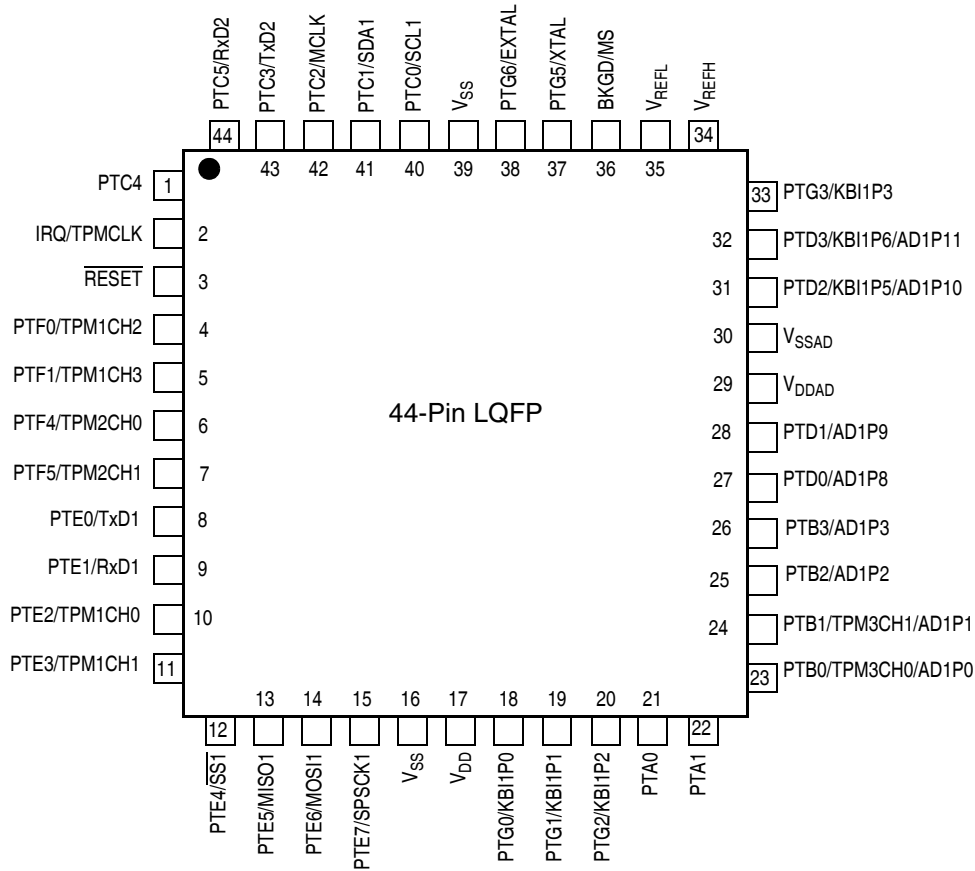


Figure 2-3. MC9S08AC128 Series in 44-Pin LQFP Package

Table 2-4. Pin Availability by Package Pin-Count

| Pin Number | | | | Lowest <-- | Priority | --> Highest |
|------------|----|----|----|------------|---------------------|-------------|
| 80 | 64 | 48 | 44 | Port Pin | Alt 1 | Alt 2 |
| 1 | 1 | 1 | 1 | PTC4 | | |
| 2 | 2 | 2 | 2 | IRQ | TPMCLK ¹ | |
| 3 | 3 | 3 | 3 | RESET | | |
| 4 | 4 | 4 | 4 | PTF0 | TPM1CH2 | |
| 5 | 5 | 5 | 5 | PTF1 | TPM1CH3 | |
| 6 | 6 | — | — | PTF2 | TPM1CH4 | |
| 7 | 7 | — | — | PTF3 | TPM1CH5 | |
| 8 | 8 | 6 | 6 | PTF4 | TPM2CH0 | |
| 9 | 9 | — | — | PTC6 | | |
| 10 | 10 | — | — | PTF7 | | |
| 11 | 11 | 7 | 7 | PTF5 | TPM2CH1 | |
| 12 | 12 | 8 | — | PTF6 | | |

Table 2-4. Pin Availability by Package Pin-Count (continued)

| Pin Number | | | | Lowest <-- | Priority | --> Highest |
|------------|----|----|----|-----------------|------------------|-------------|
| 80 | 64 | 48 | 44 | Port Pin | Alt 1 | Alt 2 |
| 13 | — | — | — | PTJ0 | | |
| 14 | — | — | — | PTJ1 | | |
| 15 | — | — | — | PTJ2 | | |
| 16 | — | — | — | PTJ3 | | |
| 17 | 13 | 9 | 8 | PTE0 | TxD1 | |
| 18 | 14 | 10 | 9 | PTE1 | RxD1 | |
| 19 | 15 | 11 | 10 | PTE2 | TPM1CH0 | |
| 20 | 16 | 12 | 11 | PTE3 | TPM1CH1 | |
| 21 | 17 | 13 | 12 | PTE4 | $\overline{SS1}$ | |
| 22 | 18 | 14 | 13 | PTE5 | MISO1 | |
| 23 | 19 | 15 | 14 | PTE6 | MOSI1 | |
| 24 | 20 | 16 | 15 | PTE7 | SPSCK1 | |
| 25 | 21 | 17 | 16 | V _{SS} | | |
| 26 | 22 | 18 | 17 | V _{DD} | | |
| 27 | — | — | — | PTJ4 | | |
| 28 | — | — | — | PTJ5 | | |
| 29 | — | — | — | PTJ6 | | |
| 30 | — | — | — | PTJ7 | | |
| 31 | 23 | 19 | 18 | PTG0 | KBI1P0 | |
| 32 | 24 | 20 | 19 | PTG1 | KBI1P1 | |
| 33 | 25 | 21 | 20 | PTG2 | KBI1P2 | |
| 34 | 26 | 22 | 21 | PTA0 | | |
| 35 | 27 | 23 | 22 | PTA1 | | |
| 36 | 28 | 24 | — | PTA2 | | |
| 37 | 29 | — | — | PTA3 | | |
| 38 | 30 | — | — | PTA4 | | |
| 39 | 31 | — | — | PTA5 | | |
| 40 | 32 | — | — | PTA6 | | |
| 41 | 33 | 25 | — | PTA7 | | |
| 42 | — | — | — | PTH0 | TPM2CH2 | |
| 43 | — | — | — | PTH1 | TPM2CH3 | |
| 44 | — | — | — | PTH2 | TPM2CH4 | |
| 45 | — | — | — | PTH3 | TPM2CH5 | |
| 46 | 34 | 26 | 23 | PTB0 | TPM3CH0 | AD1P0 |
| 47 | 35 | 27 | 24 | PTB1 | TPM3CH1 | AD1P1 |
| 48 | 36 | 28 | 25 | PTB2 | AD1P2 | |
| 49 | 37 | 29 | 26 | PTB3 | AD1P3 | |
| 50 | 38 | — | — | PTB4 | AD1P4 | |
| 51 | 39 | — | — | PTB5 | AD1P5 | |
| 52 | 40 | — | — | PTB6 | AD1P6 | |
| 53 | 41 | — | — | PTB7 | AD1P7 | |

Table 2-4. Pin Availability by Package Pin-Count (continued)

| Pin Number | | | | Lowest <-- | Priority | --> Highest |
|------------|----|----|----|---------------------|----------|-------------|
| 80 | 64 | 48 | 44 | Port Pin | Alt 1 | Alt 2 |
| 54 | 42 | 30 | 27 | PTD0 | AD1P8 | |
| 55 | 43 | 31 | 28 | PTD1 | AD1P9 | |
| 56 | 44 | 32 | 29 | V _{DDAD} | | |
| 57 | 45 | 33 | 30 | V _{SSAD} | | |
| 58 | 46 | 34 | 31 | PTD2 | KBI1P5 | AD1P10 |
| 59 | 47 | 35 | 32 | PTD3 | KBI1P6 | AD1P11 |
| 60 | 48 | 36 | 33 | PTG3 | KBI1P3 | |
| 61 | 49 | 37 | — | PTG4 | KBI1P4 | |
| 62 | 50 | — | — | PTD4 | TPM2CLK | AD1P12 |
| 63 | 51 | — | — | PTD5 | AD1P13 | |
| 64 | 52 | — | — | PTD6 | TPM1CLK | AD1P14 |
| 65 | 53 | — | — | PTD7 | KBI1P7 | AD1P15 |
| 66 | 54 | 38 | 34 | V _{REFH} | | |
| 67 | 55 | 39 | 35 | V _{REFL} | | |
| 68 | 56 | 40 | 36 | BKGD | MS | |
| 69 | 57 | 41 | 37 | PTG5 | XTAL | |
| 70 | 58 | 42 | 38 | PTG6 | EXTAL | |
| 71 | 59 | 43 | 39 | V _{SS} | | |
| 72 | — | — | — | V _{DD(NC)} | | |
| 73 | 60 | 44 | 40 | PTC0 | SCL1 | |
| 74 | 61 | 45 | 41 | PTC1 | SDA1 | |
| 75 | — | — | — | PTH4 | SPSCK2 | |
| 76 | — | — | — | PTH5 | MOSI2 | |
| 77 | — | — | — | PTH6 | MISO2 | |
| 78 | 62 | 46 | 42 | PTC2 | MCLK | |
| 79 | 63 | 47 | 43 | PTC3 | TxD2 | |
| 80 | 64 | 48 | 44 | PTC5 | RxD2 | |

¹ TPMCLK, TPM1CLK, and TPM2CLK options are configured via software; out of reset, TPM1CLK, TPM2CLK, and TPMCLK are available to TPM1, TPM2, and TPM3 respectively.

Chapter 3

Electrical Characteristics and Timing Specifications

3.1 Introduction

This section contains electrical and timing specifications.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 3-1. Parameter Classifications

| | |
|----------|--|
| P | Those parameters are guaranteed during production testing on each individual device. |
| C | Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. |
| T | Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category. |
| D | Those parameters are derived mainly from simulations. |

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in [Table 3-2](#) may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Table 3-2. Absolute Maximum Ratings

| Rating | Symbol | Value | Unit |
|---|-----------|-------------------------|------|
| Supply voltage | V_{DD} | -0.3 to + 5.8 | V |
| Input voltage | V_{In} | - 0.3 to $V_{DD} + 0.3$ | V |
| Instantaneous maximum current Single pin limit (applies to all port pins) ^{1, 2, 3} | I_D | ± 25 | mA |
| Maximum current into V_{DD} | I_{DD} | 120 | mA |
| Storage temperature | T_{stg} | -55 to +150 | °C |

¹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

² All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

³ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 3-3. Thermal Characteristics

| Rating | Symbol | Value | Unit | |
|--|---------------|------------------------------|------|--|
| Operating temperature range (packaged) | T_A | T_L to T_H -40 to 125 | °C | |
| Maximum junction temperature | T_J | 150 | °C | |
| Thermal resistance ^{1,2,3,4} | | | | |
| 80-pin LQFP | | | | |
| 1s | | 61 | | |
| 2s2p | | 47 | | |
| 64-pin QFP | | | | |
| 1s | θ_{JA} | 57 | °C/W | |
| 2s2p | | 43 | | |
| 48-pin QFN | | | | |
| 1s | | 81 | | |
| 2s2p | | 28 | | |
| 44-pin LQFP | | | | |
| 1s | | 73 | | |
| 2s2p | | 56 | | |

¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

² Junction to Ambient Natural Convection

³ 1s - Single Layer Board, one signal layer

⁴ 2s2p - Four Layer Board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 3-1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad \text{Eqn. 3-2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3-3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving equations 1 and 2 iteratively for any value of T_A .

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits and JEDEC Standard for Non-Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 3-4. ESD and Latch-up Test Conditions

| Model | Description | Symbol | Value | Unit |
|------------|-----------------------------|--------|-------|----------|
| Human Body | Series Resistance | R1 | 1500 | Ω |
| | Storage Capacitance | C | 100 | pF |
| | Number of Pulse per pin | – | 3 | |
| Machine | Series Resistance | R1 | 0 | Ω |
| | Storage Capacitance | C | 200 | pF |
| | Number of Pulse per pin | – | 3 | |
| Latch-up | Minimum input voltage limit | | – 2.5 | V |
| | Maximum input voltage limit | | 7.5 | V |

Table 3-5. ESD and Latch-Up Protection Characteristics

| Num | C | Rating | Symbol | Min | Max | Unit |
|-----|---|---|-----------|------------|-----|------|
| 1 | C | Human Body Model (HBM) | V_{HBM} | ± 2000 | – | V |
| 2 | C | Machine Model (MM) | V_{MM} | ± 200 | – | V |
| 3 | C | Charge Device Model (CDM) | V_{CDM} | ± 500 | – | V |
| 4 | C | Latch-up Current at $T_A = 125^\circ\text{C}$ | I_{LAT} | ± 100 | – | mA |

3.6 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 3-6. DC Characteristics

| Num | C | Parameter | Symbol | Min | Typ ¹ | Max | Unit | |
|-----|---|---|------------|------------------------------|------------------|----------------------|------------|---|
| 1 | — | Operating Voltage | V_{DD} | 2.7 | — | 5.5 | V | |
| 2 | P | Output high voltage — Low Drive (PTxDSn = 0) 5 V, $I_{Load} = -2$ mA 3 V, $I_{Load} = -0.6$ mA 5 V, $I_{Load} = -0.4$ mA 3 V, $I_{Load} = -0.24$ mA | V_{OH} | $V_{DD} - 1.5$ | — | — | V | |
| | P | Output high voltage — High Drive (PTxDSn = 1) 5 V, $I_{Load} = -10$ mA 3 V, $I_{Load} = -3$ mA 5 V, $I_{Load} = -2$ mA 3 V, $I_{Load} = -0.4$ mA | | $V_{DD} - 1.5$ | — | — | | |
| 3 | P | Output low voltage — Low Drive (PTxDSn = 0) 5 V, $I_{Load} = 2$ mA 3 V, $I_{Load} = 0.6$ mA 5 V, $I_{Load} = 0.4$ mA 3 V, $I_{Load} = 0.24$ mA | V_{OL} | — | — | 1.5 | V | |
| | P | Output low voltage — High Drive (PTxDSn = 1) 5 V, $I_{Load} = 10$ mA 3 V, $I_{Load} = 3$ mA 5 V, $I_{Load} = 2$ mA 3 V, $I_{Load} = 0.4$ mA | | — | — | 1.5 | | |
| 4 | P | Output high current — Max total I_{OH} for all ports 5V 3V | I_{OHT} | — — | — — | 100 60 | mA | |
| 5 | P | Output low current — Max total I_{OL} for all ports 5V 3V | I_{OLT} | — — | — — | 100 60 | mA | |
| 6 | P | Input high voltage; all digital inputs | V_{IH} | $2.7v \leq V_{DD} < 4.5v$ | — | — | V | |
| | | | | $4.5v \leq V_{DD} \leq 5.5v$ | 0.70x V_{DD} | — | | — |
| 7 | P | Input low voltage; all digital inputs | V_{IL} | — | — | $0.35 \times V_{DD}$ | | |
| 8 | P | Input hysteresis; all digital inputs | V_{hys} | $0.06 \times V_{DD}$ | | | mV | |
| 9 | P | Input leakage current; input only pins ² | $ I_{In} $ | — | 0.1 | 1 | μA | |
| 10 | P | High Impedance (off-state) leakage current ² | $ I_{OZ} $ | — | 0.1 | 1 | μA | |
| 11 | P | Internal pullup resistors ³ | R_{PU} | 20 | 45 | 65 | k Ω | |
| 12 | P | Internal pulldown resistors ⁴ | R_{PD} | 20 | 45 | 65 | k Ω | |
| 13 | C | Input Capacitance; all non-supply pins | C_{In} | — | — | 8 | pF | |
| 14 | D | RAM retention voltage | V_{RAM} | — | 0.6 | 1.0 | V | |
| 15 | P | POR rearm voltage | V_{POR} | 0.9 | 1.4 | 2.0 | V | |
| 16 | D | POR rearm time | t_{POR} | 10 | — | — | μs | |
| 17 | P | Low-voltage detection threshold — high range | V_{LVDH} | V_{DD} falling | 4.2 | 4.3 | 4.4 | V |
| | | | | V_{DD} rising | 4.3 | 4.4 | 4.5 | |
| 18 | P | Low-voltage detection threshold — low range | V_{LVDL} | V_{DD} falling | 2.48 | 2.56 | 2.64 | V |
| | | | | V_{DD} rising | 2.54 | 2.62 | 2.7 | |

Table 3-6. DC Characteristics (continued)

| Num | C | Parameter | Symbol | Min | Typ ¹ | Max | Unit |
|-----|---|---|-------------------|--------------|------------------|-------------|------|
| 19 | P | Low-voltage warning threshold — high range V _{DD} falling V _{DD} rising | V _{LVWH} | 4.2 4.3 | 4.3 4.4 | 4.4 4.5 | V |
| 20 | P | Low-voltage warning threshold — low range V _{DD} falling V _{DD} rising | V _{LVWL} | 2.48 2.54 | 2.56 2.62 | 2.64 2.7 | V |
| 21 | P | Low-voltage inhibit reset/recover hysteresis 5V 3V | V _{hys} | — — | 100 60 | — — | mV |
| 22 | P | Bandgap Voltage Reference ⁵ | V _{BG} | 1.170 | 1.200 | 1.230 | V |

¹ Typical values are based on characterization data at 25°C unless otherwise stated.

² Measured with V_{In} = V_{DD} or V_{SS}.

³ Measured with V_{In} = V_{SS}.

⁴ Measured with V_{In} = V_{DD}.

⁵ Factory trimmed at V_{DD} = 3.0 V, Temperature = 25 °C.

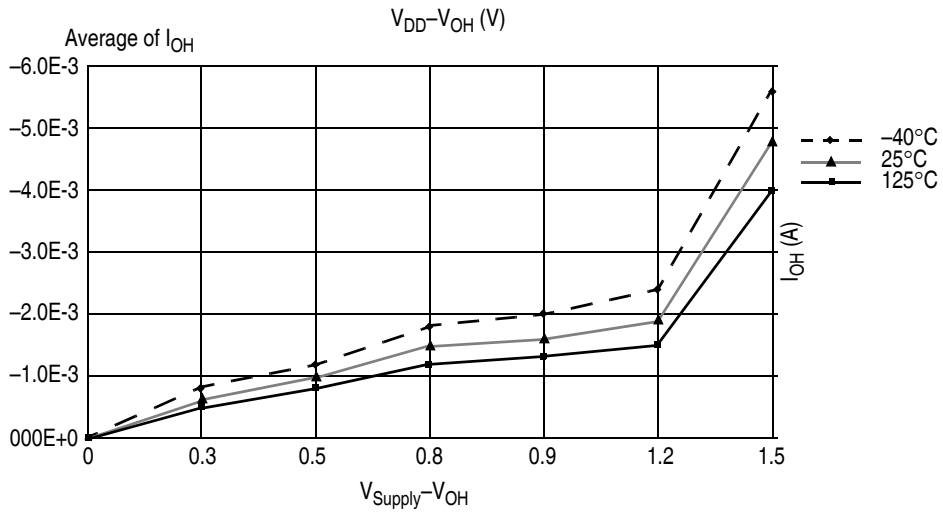


Figure 3-1. Typical I_{OH} (Low Drive) vs V_{DD}-V_{OH} at V_{DD} = 3 V

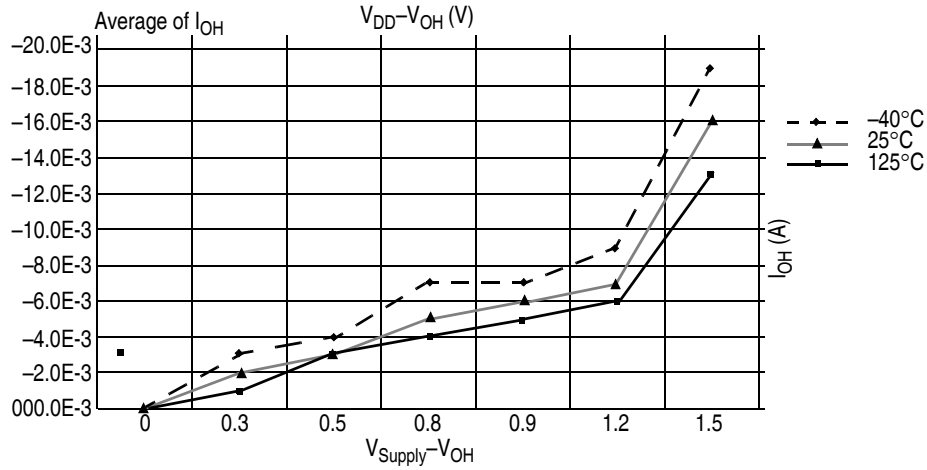


Figure 3-2. Typical I_{OH} (High Drive) vs $V_{DD}-V_{OH}$ at $V_{DD} = 3$ V

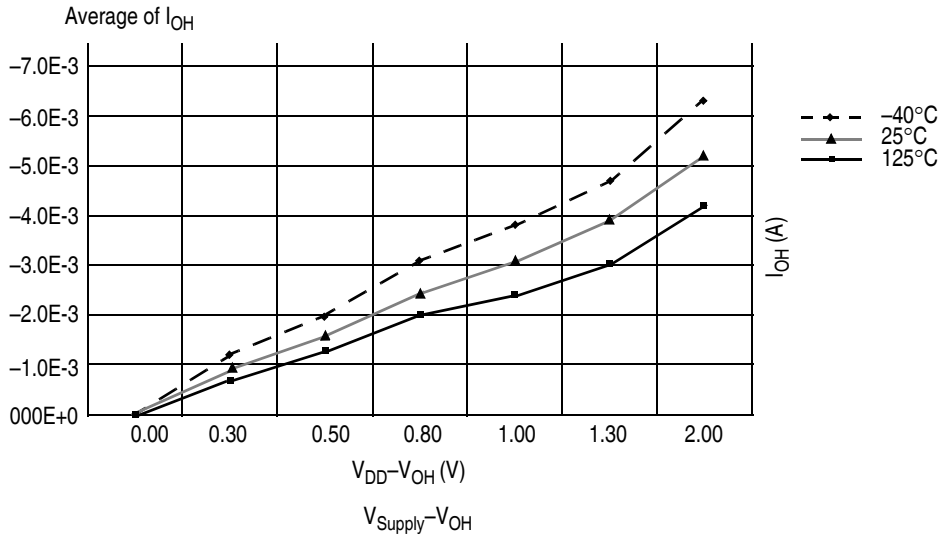


Figure 3-3. Typical I_{OH} (Low Drive) vs $V_{DD}-V_{OH}$ at $V_{DD} = 5$ V

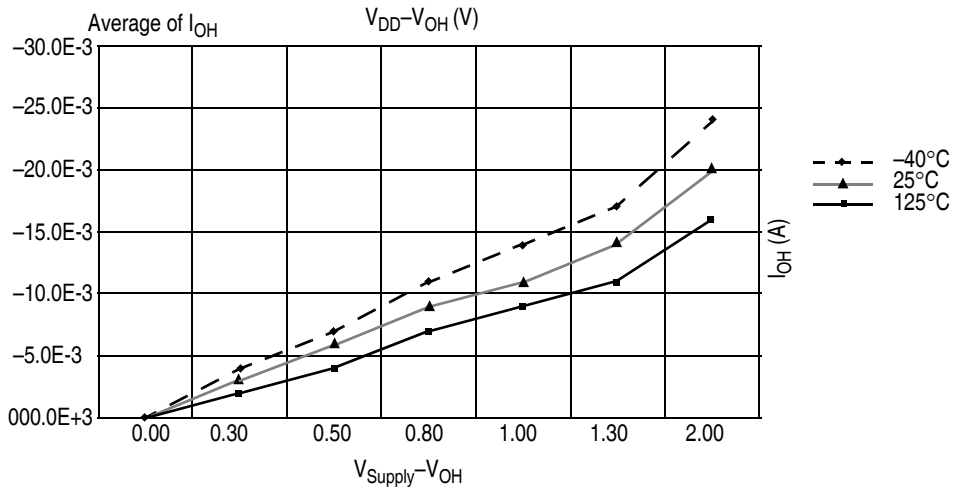


Figure 3-4. Typical I_{OH} (High Drive) vs $V_{DD}-V_{OH}$ at $V_{DD} = 5$ V

3.7 Supply Current Characteristics

Table 3-7. Supply Current Characteristics

| Num | C | Parameter | Symbol | V _{DD} (V) | Typ ¹ | Max | Unit | Temp (°C) |
|-----|---|---|------------------------|------------------------|------------------|------------------------|----------|-----------------------------|
| 1 | C | Run supply current ² measured at (CPU clock = 2 MHz, f _{Bus} = 1 MHz) | R _I DD | 5 | 1.1 | 1.4 ³ | mA | -40 to 125°C |
| | | | | 3 | 1.0 | 1.2 | | |
| 2 | C | Run supply current ⁴ measured at (CPU clock = 16 MHz, f _{Bus} = 8 MHz) | R _I DD | 5 | 6.7 | 8.0 ⁵ | mA | -40 to 125°C |
| | | | | 3 | 6 | 7.5 | | |
| 3 | C | Stop2 mode supply current | S2 _I DD | 5 | 1.0 | 25 160 | μA | -40 to 85°C -40 to 125°C |
| | | | | 3 | 0.8 | 23 150 | μA | -40 to 85°C -40 to 125°C |
| 4 | C | Stop3 mode supply current | S3 _I DD | 5 | 1.2 | 27 180 ³ | μA | -40 to 85°C -40 to 125°C |
| | | | | 3 | 1.0 | 25 170 | μA | -40 to 85°C -40 to 125°C |
| 5 | C | RTI adder to stop2 or stop3 ⁶ | S23 _I DDRTI | 5 | 300 | 500 500 | nA | -40 to 85°C -40 to 125°C |
| | | | | 3 | 300 | 500 500 | nA | -40 to 85°C -40 to 125°C |
| 6 | C | LVD adder to stop3 (LVDE = LVDSE = 1) | S3 _I DDLVD | 5 | 110 | 180 180 | μA | -40 to 85°C -40 to 125°C |
| | | | | 3 | 90 | 160 160 | μA | -40 to 85°C -40 to 125°C |
| 7 | C | Adder to stop3 for oscillator enabled ⁷ (OSCSTEN = 1) | S3 _I DDOSC | 5,3 | 5 | 8 8 | μA μA | -40 to 85°C -40 to 125°C |

¹ Typical values are based on characterization data at 25°C unless otherwise stated. See Figure 3-5 through Figure 3-7 for typical curves across voltage/temperature.

² All modules except ADC active, ICG configured for FBE, and does not include any dc loads on port pins

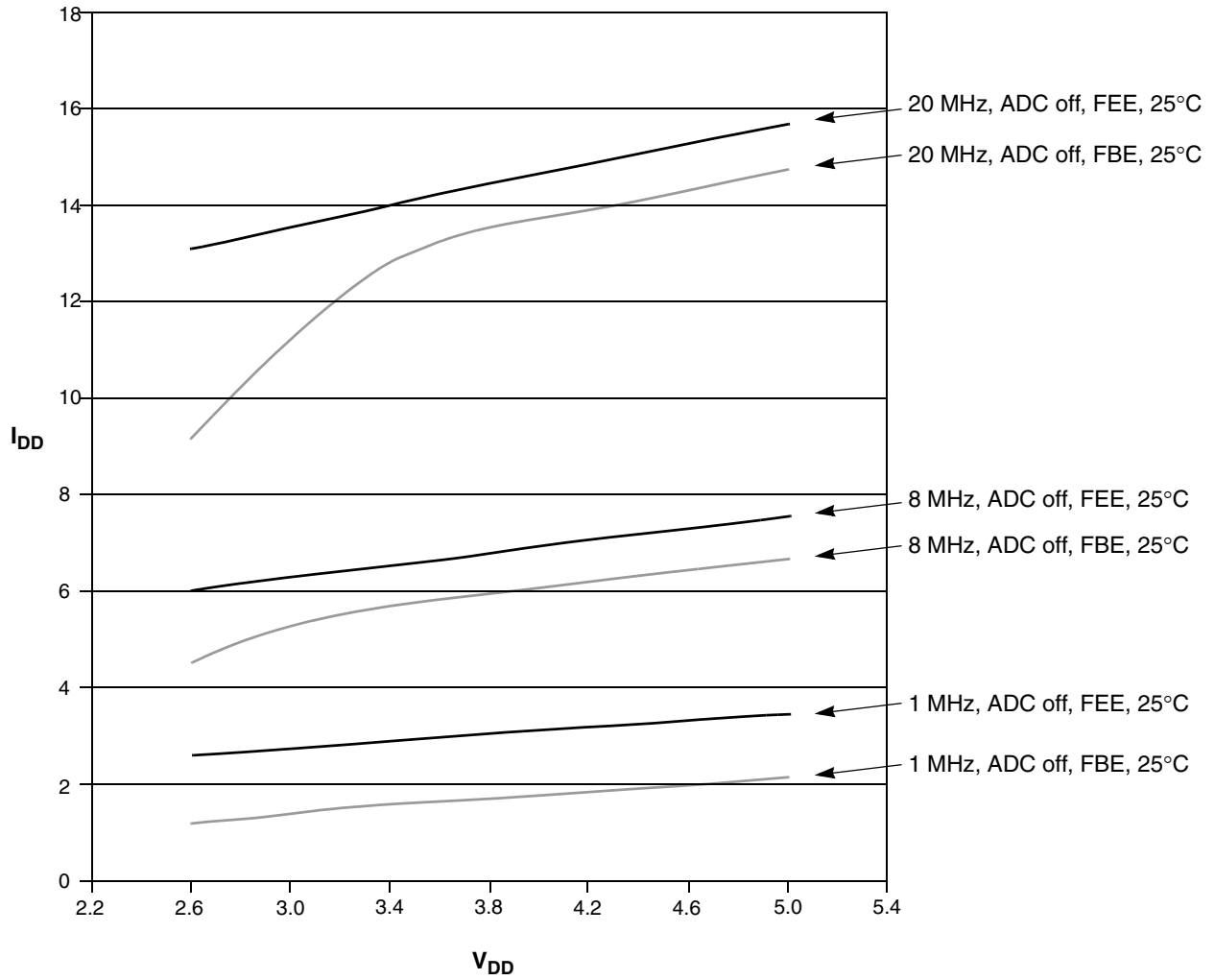
³ Every unit tested to this parameter. All other values in the Max column are guaranteed by characterization.

⁴ All modules except ADC active, ICG configured for FBE, and does not include any dc loads on port pins

⁵ Every unit tested to this parameter. All other values in the Max column are guaranteed by characterization.

⁶ Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode. Wait mode typical is 560 μA at 3 V with f_{Bus} = 1 MHz.

⁷ Values given under the following conditions: low range operation (RANGE = 0) with a 32.768kHz crystal, low power mode (HGO = 0), clock monitor disabled (LOCD = 1).



Note: External clock is square wave supplied by function generator. For FEE mode, external reference frequency is 4 MHz

Figure 3-5. Typical Run I_{DD} for FBE and FEE Modes, I_{DD} vs. V_{DD}

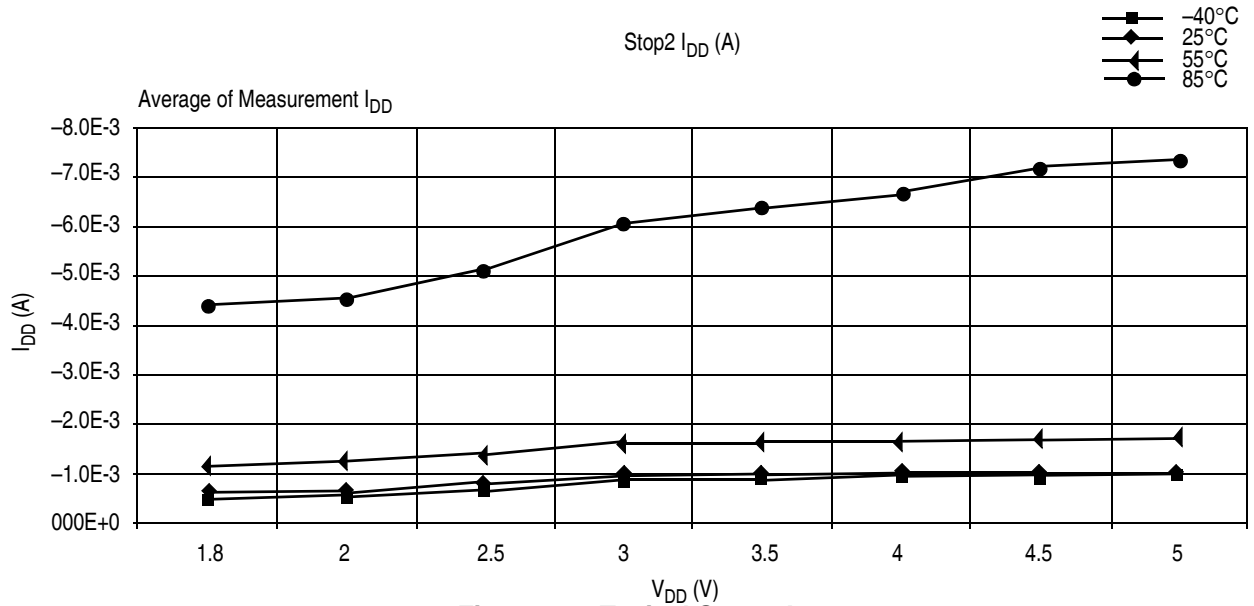


Figure 3-6. Typical Stop 2 I_{DD}

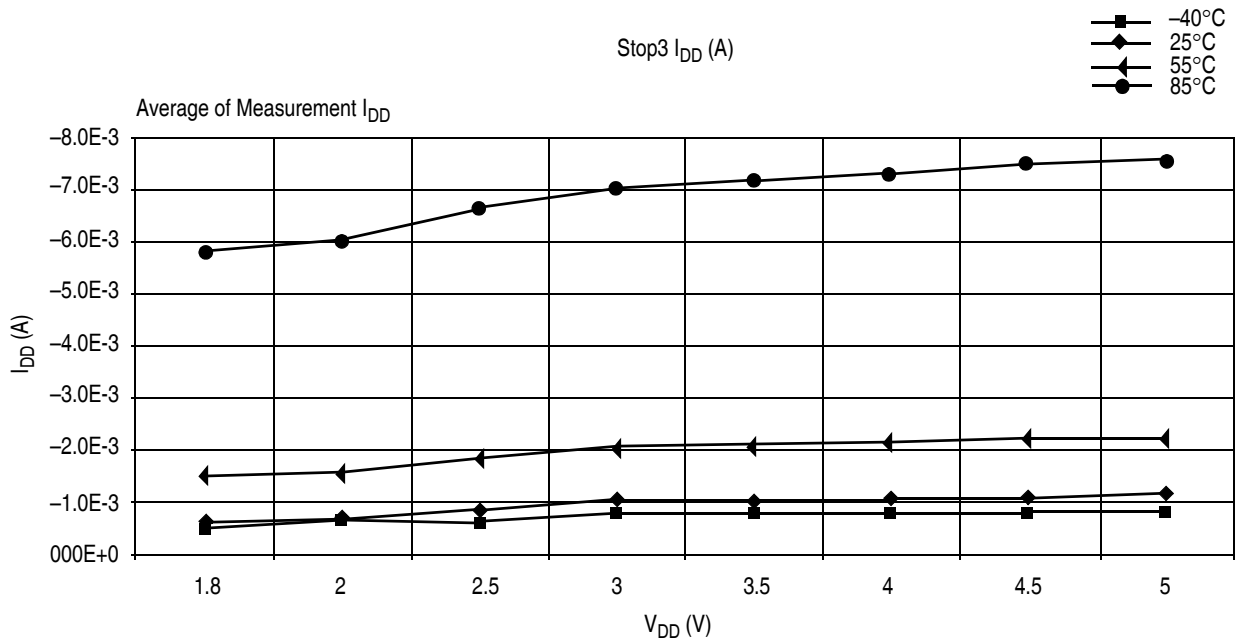


Figure 3-7. Typical Stop 3 I_{DD}

3.8 ADC Characteristics

Table 3-8. 5 Volt 10-bit ADC Operating Conditions

| Characteristic | Conditions | Symb | Min | Typ ¹ | Max | Unit |
|---|---|-------------------|------------|------------------|------------|------------------|
| Supply voltage | Absolute | V_{DDAD} | 2.7 | — | 5.5 | V |
| | Delta to V_{DD} ($V_{DD}-V_{DDAD}$) ² | ΔV_{DDAD} | -100 | 0 | +100 | mV |
| Ground voltage | Delta to V_{SS} ($V_{SS}-V_{SSAD}$) ² | ΔV_{SSAD} | -100 | 0 | +100 | mV |
| Ref voltage high | | V_{REFH} | 2.7 | V_{DDAD} | V_{DDAD} | V |
| Ref voltage low | | V_{REFL} | V_{SSAD} | V_{SSAD} | V_{SSAD} | V |
| Supply current | Stop, reset, module off | I_{DDAD} | — | 0.011 | 1 | μ A |
| Input voltage | | V_{ADIN} | V_{REFL} | — | V_{REFH} | V |
| Input capacitance | | C_{ADIN} | — | 4.5 | 5.5 | pF |
| Input resistance | | R_{ADIN} | — | 3 | 5 | k Ω |
| Analog source resistance External to MCU | 10-bit mode $f_{ADCK} > 4$ MHz $f_{ADCK} < 4$ MHz | R_{AS} | — | — | 5 | k Ω |
| | 8-bit mode (all valid f_{ADCK}) | | — | — | 10 | |
| ADC conversion clock frequency | High speed (ADLPC = 0) | f_{ADCK} | 0.4 | — | 8.0 | MHz |
| | Low power (ADLPC = 1) | | 0.4 | — | 4.0 | |
| Temp Sensor Slope | -40°C to 25°C | m | — | 3.266 | — | mV/ $^{\circ}$ C |
| | 25°C to 125°C | | — | 3.638 | — | |
| Temp Sensor Voltage | 25°C | V_{TEMP25} | — | 1.396 | — | V |

¹ Typical values assume $V_{DDAD} = 5.0$ V, Temp = 25°C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

² dc potential difference.

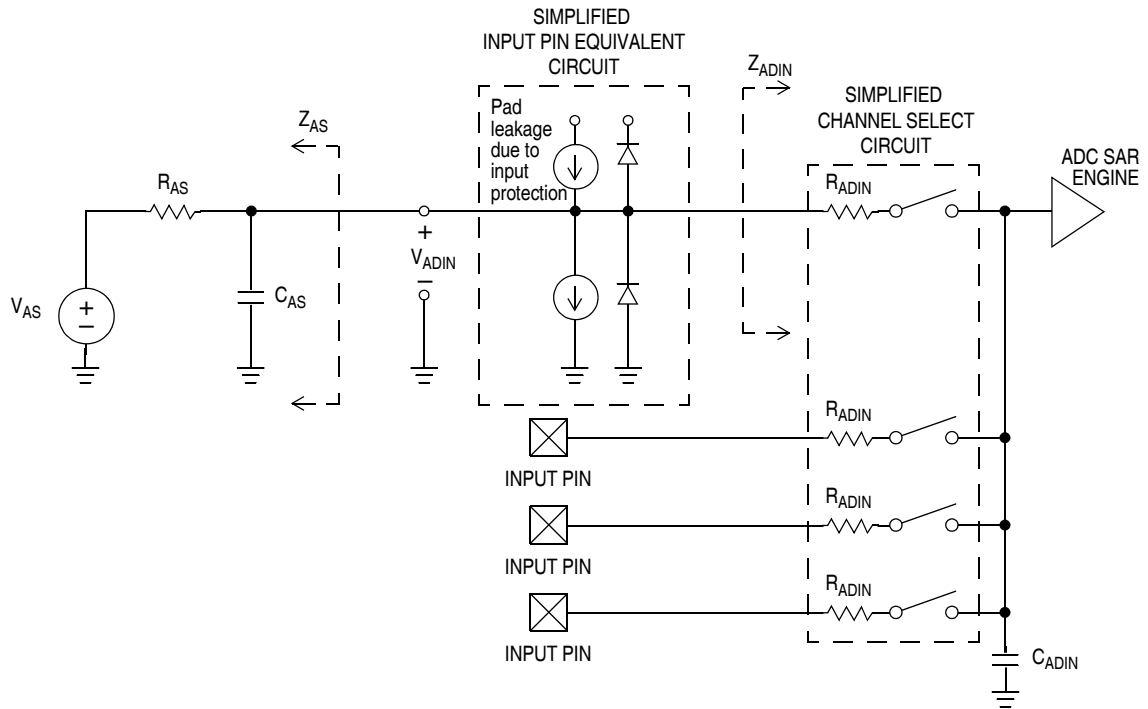


Figure 3-8. ADC Input Impedance Equivalency Diagram

Table 3-9. 5 Volt 10-bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

| Characteristic | Conditions | C | Symb | Min | Typ ¹ | Max | Unit |
|--|--|---|-------------|------|------------------|-----------|----------------|
| Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1 | | T | I_{DDAD} | — | 133 | — | μA |
| Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1 | | T | I_{DDAD} | — | 218 | — | μA |
| Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1 | | T | I_{DDAD} | — | 327 | — | μA |
| Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1 | | T | I_{DDAD} | — | 582 | — | μA |
| | $V_{DDAD} \leq 5.5 \text{ V}$ | P | | — | — | 1 | mA |
| ADC asynchronous clock source $t_{ADACK} = 1/f_{ADACK}$ | High speed (ADLPC = 0) | P | f_{ADACK} | 2 | 3.3 | 5 | MHz |
| | Low power (ADLPC = 1) | | | 1.25 | 2 | 3.3 | |
| Conversion time (Including sample time) | Short sample (ADLSMP = 0) | P | t_{ADC} | — | 20 | — | ADCK cycles |
| | Long sample (ADLSMP = 1) | | | — | 40 | — | |
| Sample time | Short sample (ADLSMP = 0) | P | t_{ADS} | — | 3.5 | — | ADCK cycles |
| | Long sample (ADLSMP = 1) | | | — | 23.5 | — | |
| Total unadjusted error Includes quantization | 10-bit mode | P | E_{TUE} | — | ± 1 | ± 2.5 | LSB^2 |
| | 8-bit mode | | | — | ± 0.5 | ± 1.0 | |
| Differential non-linearity | 10-bit mode | P | DNL | — | ± 0.5 | ± 1.0 | LSB^2 |
| | 8-bit mode | | | — | ± 0.3 | ± 0.5 | |
| | Monotonicity and no-missing-codes guaranteed | | | | | | |
| Integral non-linearity | 10-bit mode | C | INL | — | ± 0.5 | ± 1.0 | LSB^2 |
| | 8-bit mode | | | — | ± 0.3 | ± 0.5 | |
| Zero-scale error $V_{ADIN} = V_{SSA}$ | 10-bit mode | P | E_{ZS} | — | ± 0.5 | ± 1.5 | LSB^2 |
| | 8-bit mode | | | — | ± 0.5 | ± 0.5 | |
| Full-scale error $V_{ADIN} = V_{DDA}$ | 10-bit mode | P | E_{FS} | — | ± 0.5 | ± 1.5 | LSB^2 |
| | 8-bit mode | | | — | ± 0.5 | ± 0.5 | |
| Quantization error | 10-bit mode | D | E_Q | — | — | ± 0.5 | LSB^2 |
| | 8-bit mode | | | — | — | ± 0.5 | |

Table 3-9. 5 Volt 10-bit ADC Characteristics ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

| Characteristic | Conditions | C | Symb | Min | Typ ¹ | Max | Unit |
|---|-------------|---|-----------------|-----|------------------|------|------------------|
| Input leakage error Pad leakage ³ * R _{AS} | 10-bit mode | D | E _{IL} | — | ±0.2 | ±2.5 | LSB ² |
| | 8-bit mode | | | — | ±0.1 | ±1 | |

¹ Typical values assume $V_{DDAD} = 5.0V$, Temp = 25C, $f_{ADCK}=1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

² 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

³ Based on input pad leakage current. Refer to pad electricals.

3.9 Internal Clock Generation Module Characteristics

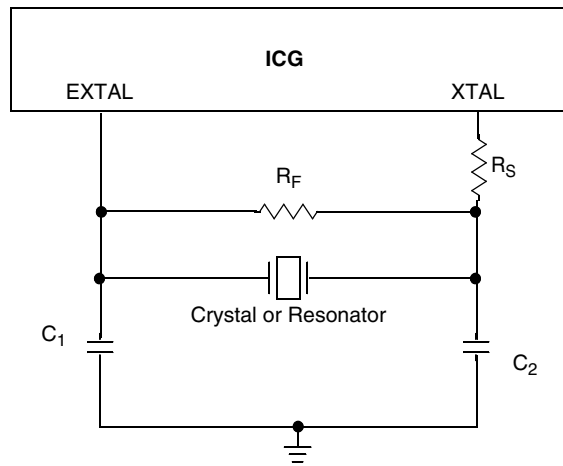


Table 3-10. ICG DC Electrical Specifications (Temperature Range = -40 to 125°C Ambient)

| Characteristic | Symbol | Min | Typ ¹ | Max | Unit |
|----------------------------|----------------------------------|-----------------------|------------------|-----|------|
| Load capacitors | C ₁ C ₂ | See Note ² | | | |
| Feedback resistor | R _F | | 10 | | MΩ |
| Low range (32k to 100 kHz) | | | 1 | | MΩ |
| High range (1M – 16 MHz) | | | | | |
| Series resistor | R _S | | | | kΩ |
| Low range | | | | | |
| Low Gain (HGO = 0) | | — | 0 | — | |
| High Gain (HGO = 1) | | — | 100 | — | |
| High range | | | | | |
| Low Gain (HGO = 0) | | — | 0 | — | |
| High Gain (HGO = 1) | | — | | | |
| ≥ 8 MHz | — | 0 | — | | |
| 4 MHz | — | 10 | — | | |
| 1 MHz | — | 20 | — | | |

¹ Typical values are based on characterization data at $V_{DD} = 5.0V$, 25°C or is typical recommended value.

² See crystal or resonator manufacturer’s recommendation.

3.9.1 ICG Frequency Specifications

Table 3-11. ICG Frequency Specifications

($V_{DDA} = V_{DDA}(\text{min})$ to $V_{DDA}(\text{max})$, Temperature Range = -40 to 125°C Ambient)

| Num | C | Characteristic | Symbol | Min | Typ ¹ | Max | Unit | |
|-----|---|--|-------------------------|--------------------------|------------------|-------------------------------|--------------------|-----|
| 1 | | Oscillator crystal or resonator (REFS = 1) (Fundamental mode crystal or ceramic resonator) Low range | f _{lo} | 32 | — | 100 | kHz | |
| | | High range | | | | | | |
| | | High Gain, FBE (HGO = 1, CLKS = 10) | f _{hi_byp} | 1 | — | 16 | | MHz |
| | | High Gain, FEE (HGO = 1, CLKS = 11) | f _{hi_eng} | 2 | — | 10 | | MHz |
| | | Low Power, FBE (HGO = 0, CLKS = 10) | f _{lp_byp} | 1 | — | 8 | | MHz |
| | | Low Power, FEE (HGO = 0, CLKS = 11) | f _{lp_eng} | 2 | — | 8 | MHz | |
| 2 | | Input clock frequency (CLKS = 11, REFS = 0) Low range | f _{lo} | 32 | — | 100 | kHz | |
| | | High range | f _{hi_eng} | 2 | — | 10 | | MHz |
| 3 | | Input clock frequency (CLKS = 10, REFS = 0) | f _{Extal} | 0 | — | 40 | MHz | |
| 4 | | Internal reference frequency (untrimmed) | f _{ICGIRCLK} | 182.25 | 243 | 303.75 | kHz | |
| 5 | | Duty cycle of input clock (REFS = 0) | t _{dc} | 40 | — | 60 | % | |
| 6 | | Output clock ICGOUT frequency CLKS = 10, REFS = 0 | f _{ICGOUT} | f _{Extal (min)} | — | f _{Extal (max)} | MHz | |
| | | All other cases | | f _{lo (min)} | — | f _{ICGDCLKmax (max)} | | |
| 7 | | Minimum DCO clock (ICGDCLK) frequency | f _{ICGDCLKmin} | 3 | — | | MHz | |
| 8 | | Maximum DCO clock (ICGDCLK) frequency | f _{ICGDCLKmax} | | — | 40 | MHz | |
| 9 | | Self-clock mode (ICGOUT) frequency ² | f _{Self} | f _{ICGDCLKmin} | | f _{ICGDCLKmax} | MHz | |
| 10 | | Self-clock mode reset (ICGOUT) frequency | f _{Self_reset} | 5.5 | 8 | 10.5 | MHz | |
| 11 | | Loss of reference frequency ³ Low range | f _{LOR} | 5 | | 25 | kHz | |
| | | High range | | 50 | | 500 | | |
| 12 | | Loss of DCO frequency ⁴ | f _{LOD} | 0.5 | | 1.5 | MHz | |
| 13 | | Crystal start-up time ^{5, 6} Low range | t _{CSTL} | — | 430 | — | ms | |
| | | High range | t _{CSTH} | — | 4 | — | | |
| 14 | | FLL lock time ⁷ Low range | t _{Lockl} | — | | 2 | ms | |
| | | High range | t _{Lockh} | — | | 2 | | |
| 15 | | FLL frequency unlock range | n _{Unlock} | -4*N | | 4*N | counts | |
| 16 | | FLL frequency lock range | n _{Lock} | -2*N | | 2*N | counts | |
| 17 | | ICGOUT period jitter, ⁸ measured at f _{ICGOUT} Max Long term jitter (averaged over 2 ms interval) | C _{Jitter} | — | | 0.2 | % f _{ICG} | |
| 18 | | Internal oscillator deviation from trimmed frequency ⁹ | ACC _{int} | — | ±0.5 | ±2 | % | |
| | | V _{DD} = 2.7 – 5.5 V, (constant temperature) V _{DD} = 5.0 V ±10%, -40° C to 125° C | | — | ±0.5 | ±2 | | |

¹ Typical values are based on characterization data at V_{DD} = 5.0V, 25°C unless otherwise stated.

² Self-clocked mode frequency is the frequency that the DCO generates when the FLL is open-loop.

- 3 Loss of reference frequency is the reference frequency detected internally, which transitions the ICG into self-clocked mode if it is not in the desired range.
- 4 Loss of DCO frequency is the DCO frequency detected internally, which transitions the ICG into FLL bypassed external mode (if an external reference exists) if it is not in the desired range.
- 5 This parameter is characterized before qualification rather than 100% tested.
- 6 Proper PC board layout procedures must be followed to achieve specifications.
- 7 This specification applies to the period of time required for the FLL to lock after entering FLL engaged internal or external modes. If a crystal/resonator is being used as the reference, this specification assumes it is already running.
- 8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{ICGOUT} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DDA} and V_{SSA} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.
- 9 See [Figure 3-9](#)

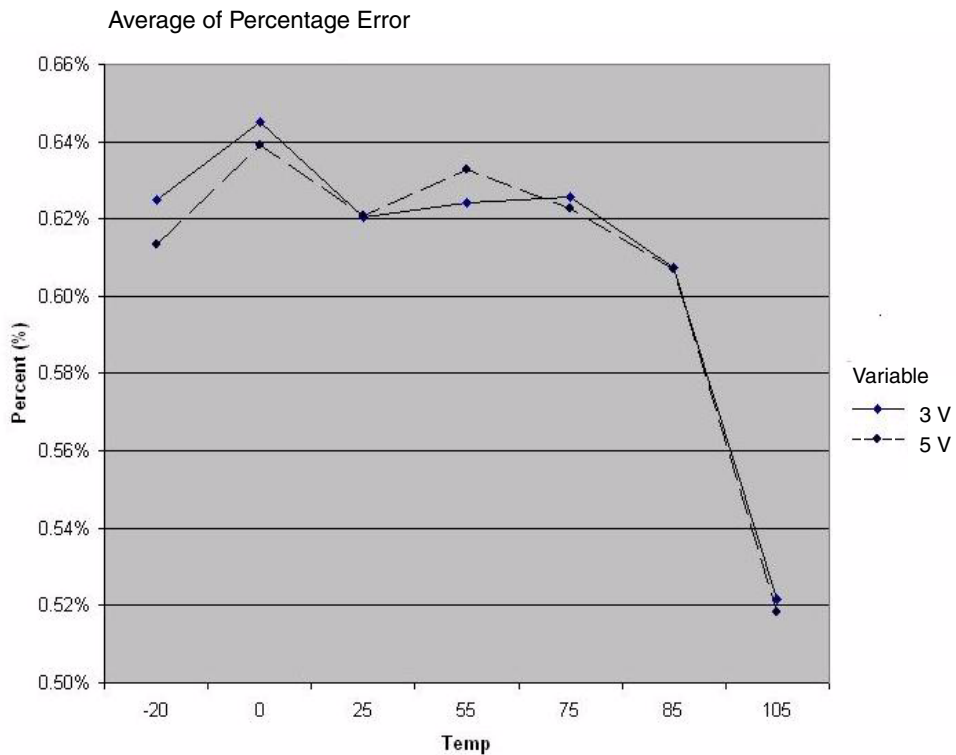


Figure 3-9. Internal Oscillator Deviation from Trimmed Frequency

3.10 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 3-12. Control Timing

| Num | C | Parameter | Symbol | Min | Typ ¹ | Max | Unit |
|-----|---|--|----------------------|----------------------------|------------------|------|---------|
| 1 | | Bus frequency ($t_{cyc} = 1/f_{Bus}$) | f_{Bus} | dc | — | 20 | MHz |
| 2 | | Real-time interrupt internal oscillator period | t_{RTI} | 600 | | 1500 | μs |
| 3 | | External reset pulse width ² ($t_{cyc} = 1/f_{Self_reset}$) | t_{extrst} | 1.5 x t_{Self_reset} | | — | ns |
| 4 | | Reset low drive ³ | t_{rstdrv} | 34 x t_{cyc} | | — | ns |
| 5 | | Active background debug mode latch setup time | t_{MSSU} | 25 | | — | ns |
| 6 | | Active background debug mode latch hold time | t_{MSH} | 25 | | — | ns |
| 7 | | IRQ pulse width Asynchronous path ² Synchronous path ⁴ | t_{LIH}, t_{HIL} | 100 1.5 x t_{cyc} | — | — | ns |
| 8 | | KBIPx pulse width Asynchronous path ² Synchronous path ³ | t_{LIH}, t_{HIL} | 100 1.5 x t_{cyc} | — | — | ns |
| 9 | | Port rise and fall time (load = 50 pF) ⁵ Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1) | t_{Rise}, t_{Fall} | — — | 3 30 | | ns |

¹ Typical values are based on characterization data at $V_{DD} = 5.0V$, $25^{\circ}C$ unless otherwise stated.

² This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

³ When any reset is initiated, internal circuitry drives the reset pin low for about 34 bus cycles and then samples the level on the reset pin about 38 bus cycles later to distinguish external reset requests from internal requests.

⁴ This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

⁵ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range $-40^{\circ}C$ to $125^{\circ}C$.

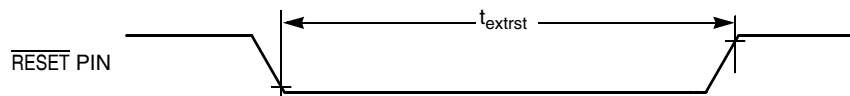


Figure 3-10. Reset Timing

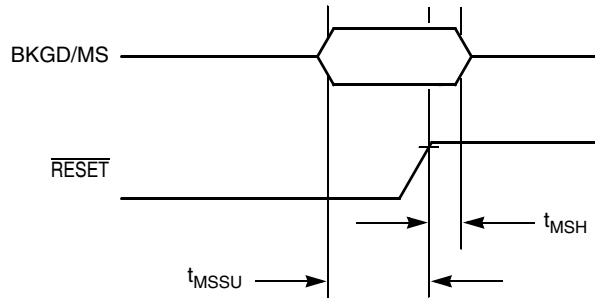


Figure 3-11. Active Background Debug Mode Latch Timing

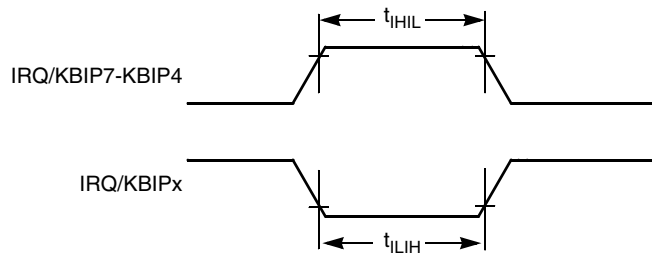


Figure 3-12. IRQ/KBIPx Timing

3.10.2 Timer/PWM (TPM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 3-13. TPM Input Timing

| Function | Symbol | Min | Max | Unit |
|---------------------------|--------------|-----|-------------|-----------|
| External clock frequency | f_{TPMext} | dc | $f_{Bus}/4$ | MHz |
| External clock period | t_{TPMext} | 4 | — | t_{cyc} |
| External clock high time | t_{clkh} | 1.5 | — | t_{cyc} |
| External clock low time | t_{clkl} | 1.5 | — | t_{cyc} |
| Input capture pulse width | t_{ICPW} | 1.5 | — | t_{cyc} |

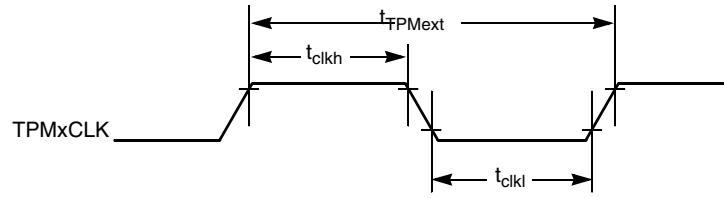


Figure 3-13. Timer External Clock

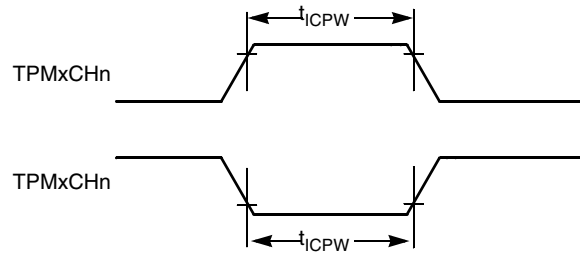


Figure 3-14. Timer Input Capture Pulse

3.11 SPI Characteristics

Table 3-14 and Figure 3-15 through Figure 3-18 describe the timing requirements for the SPI system.

Table 3-14. SPI Electrical Characteristic

| Num ¹ | C | Characteristic ² | Symbol | Min | Max | Unit |
|------------------|---|---|-------------|--------------------|-------------|-----------|
| | | Operating frequency ³ | | | | |
| | | Master | f_{op} | $f_{Bus}/2048$ | $f_{Bus}/2$ | Hz |
| | | Slave | f_{op} | dc | $f_{Bus}/4$ | |
| 1 | | Cycle time | | | | |
| | | Master | t_{SCK} | 2 | 2048 | t_{cyc} |
| | | Slave | t_{SCK} | 4 | — | t_{cyc} |
| 2 | | Enable lead time | | | | |
| | | Master | t_{Lead} | — | 1/2 | t_{SCK} |
| | | Slave | t_{Lead} | 1/2 | — | t_{SCK} |
| 3 | | Enable lag time | | | | |
| | | Master | t_{Lag} | — | 1/2 | t_{SCK} |
| | | Slave | t_{Lag} | 1/2 | — | t_{SCK} |
| 4 | | Clock (SPSCK) high time Master and Slave | t_{SCKH} | $1/2 t_{SCK} - 25$ | — | ns |
| 5 | | Clock (SPSCK) low time Master and Slave | t_{SCKL} | $1/2 t_{SCK} - 25$ | — | ns |
| 6 | | Data setup time (inputs) | | | | |
| | | Master | $t_{SI(M)}$ | 30 | — | ns |
| | | Slave | $t_{SI(S)}$ | 30 | — | ns |
| 7 | | Data hold time (inputs) | | | | |
| | | Master | $t_{HI(M)}$ | 30 | — | ns |
| | | Slave | $t_{HI(S)}$ | 30 | — | ns |
| 8 | | Access time, slave ⁴ | t_A | 0 | 40 | ns |
| 9 | | Disable time, slave ⁵ | t_{dis} | — | 40 | ns |
| 10 | | Data setup time (outputs) | | | | |
| | | Master | t_{SO} | 25 | — | ns |
| | | Slave | t_{SO} | 25 | — | ns |
| 11 | | Data hold time (outputs) | | | | |
| | | Master | t_{HO} | -10 | — | ns |
| | | Slave | t_{HO} | -10 | — | ns |

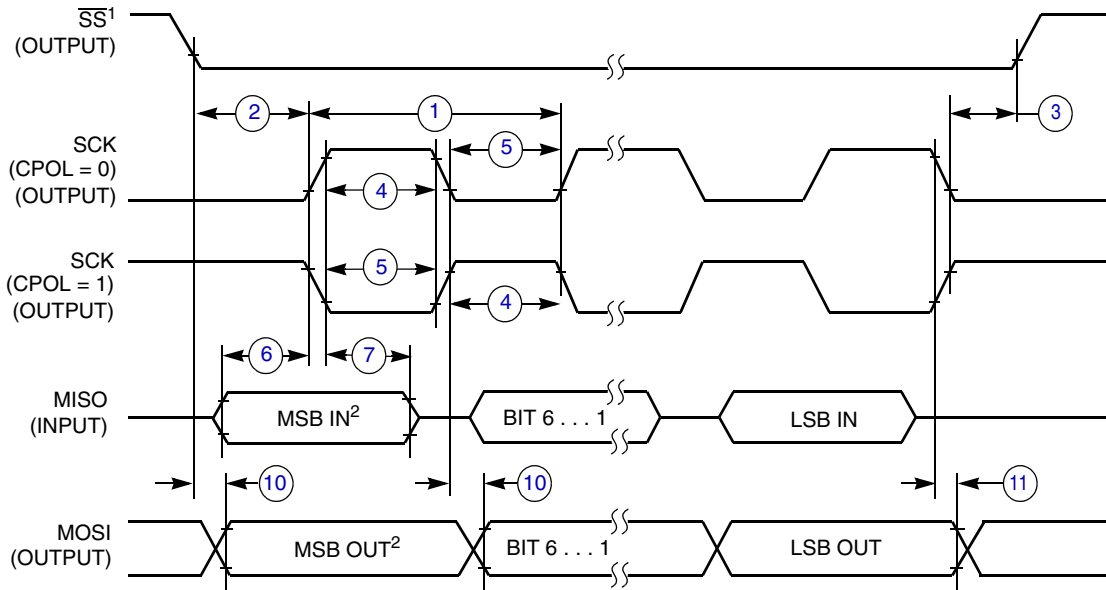
¹ Refer to Figure 3-15 through Figure 3-18.

² All timing is shown with respect to 20% V_{DD} and 70% V_{DD} , unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

³ Maximum baud rate must be limited to 5 MHz due to pad input characteristics.

⁴ Time to data active from high-impedance state.

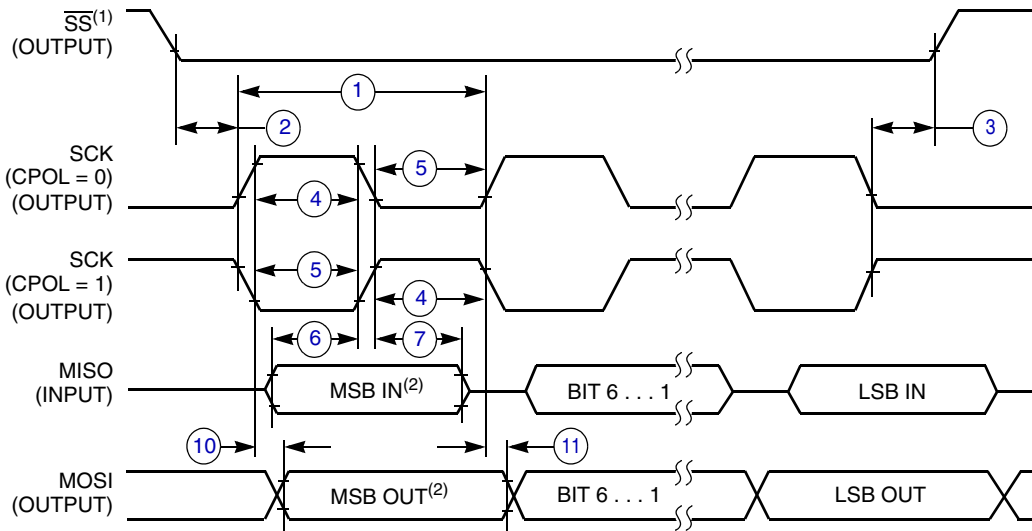
⁵ Hold time to high-impedance state.



NOTES:

1. \overline{SS} output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

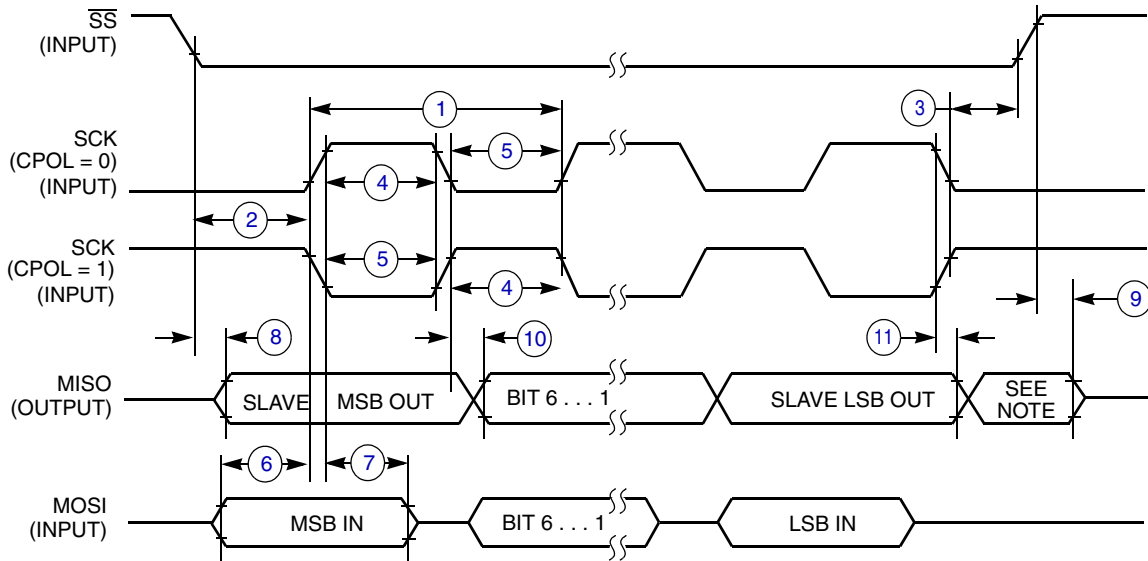
Figure 3-15. SPI Master Timing (CPHA = 0)



NOTES:

1. \overline{SS} output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

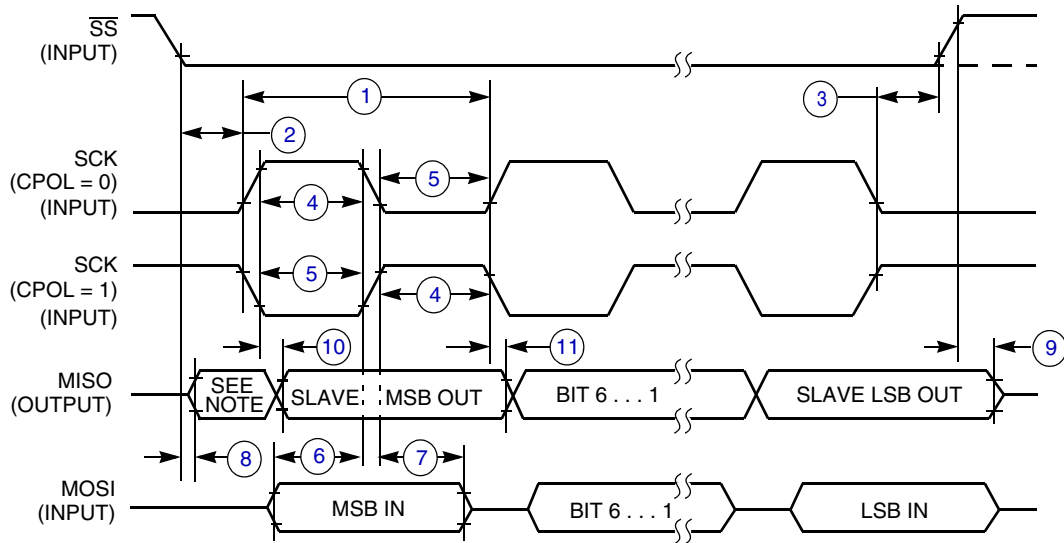
Figure 3-16. SPI Master Timing (CPHA = 1)



NOTE:

- 1. Not defined but normally MSB of character just received

Figure 3-17. SPI Slave Timing (CPHA = 0)



NOTE:

- 1. Not defined but normally LSB of character just received

Figure 3-18. SPI Slave Timing (CPHA = 1)

3.12 FLASH Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply.

Table 3-15. Flash Characteristics

| Num | C | Characteristic | Symbol | Min | Typ ¹ | Max | Unit |
|-----|---|--|-------------------------|-------------|------------------|--------|------------------|
| 1 | P | Supply voltage for program/erase | $V_{\text{prog/erase}}$ | 2.7 | | 5.5 | V |
| 2 | P | Supply voltage for read operation | V_{Read} | 2.7 | | 5.5 | V |
| 3 | P | Internal FCLK frequency ² | f_{FCLK} | 150 | | 200 | kHz |
| 4 | P | Internal FCLK period (1/FCLK) | t_{Fcy}^2 | 5 | | 6.67 | μs |
| 5 | P | Byte program time (random location) ⁽²⁾ | t_{prog} | | 9 | | t_{Fcy} |
| 6 | C | Byte program time (burst mode) ⁽²⁾ | t_{Burst} | | 4 | | t_{Fcy} |
| 7 | P | Page erase time ³ | t_{Page} | | 4000 | | t_{Fcy} |
| 8 | P | Mass erase time ⁽²⁾ | t_{Mass} | | 20,000 | | t_{Fcy} |
| 9 | C | Program/erase endurance ⁴ T_L to $T_H = -40^\circ\text{C}$ to $+125^\circ\text{C}$ $T = 25^\circ\text{C}$ | | 10,000 — | — 100,000 | — — | cycles |
| 10 | C | Data retention ⁵ | $t_{\text{D-ret}}$ | 15 | 100 | — | years |

¹ Typical values are based on characterization data at $V_{DD} = 5.0$ V, 25°C unless otherwise stated.

² The frequency of this clock is controlled by a software setting.

³ These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

⁴ **Typical endurance for Flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.

⁵ **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory*.

3.13 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

3.13.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

Table 3-16. Radiated Emissions

| Parameter | Symbol | Conditions | Frequency | f_{osc}/f_{BUS} | Level ¹ (Max) | Unit |
|--|---------------|---|----------------|----------------------------|-----------------------------|------------|
| Radiated emissions, electric field and magnetic field | V_{RE_TEM} | $V_{DD} = 5.0\text{ V}$ $T_A = +25^\circ\text{C}$ package type 80 LQFP | 0.15 – 50 MHz | 32kHz crystal 20MHz Bus | 30 | dB μ V |
| | | | 50 – 150 MHz | | 32 | |
| | | | 150 – 500 MHz | | 19 | |
| | | | 500 – 1000 MHz | | 7 | |
| | | | IEC Level | | I^2 | — |
| | | | SAE Level | | I^2 | — |

¹ Data based on laboratory test results.

² IEC and SAE Level Maximums: $I=36\text{ dBuV}$.

Chapter 4

Ordering Information and Mechanical Drawings

4.1 Ordering Information

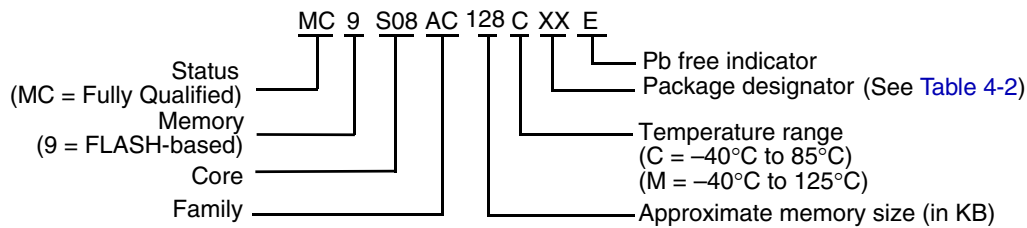
This section contains ordering numbers for MC9S08AC128 Series devices. See below for an example of the device numbering system.

Table 4-1. Device Numbering System

| Device Number | Memory | | Available Packages ¹ |
|---------------|--------|-----|----------------------------------|
| | FLASH | RAM | Type |
| MC9S08AC128 | 128K | 8K | 80 LQFP, 64 QFP, 48-QFN, 44-LQFP |
| MC9S08AC96 | 96K | 6K | 80 LQFP, 64 QFP, 48-QFN, 44-LQFP |

¹ See [Table 4-2](#) for package information.

4.2 Orderable Part Numbering System



4.3 Mechanical Drawings

[Table 4-2](#) provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08AC128 Series Product Summary pages at <http://www.freescale.com>.

To view the latest drawing, either:

- Click on the appropriate link in [Table 4-2](#), or
- Open a browser to the Freescale® website (<http://www.freescale.com>), and enter the appropriate document number (from [Table 4-2](#)) in the “Enter Keyword” search box at the top of the page.

Table 4-2. Package Information

| Pin Count | Type | Designator | Document No. |
|-----------|------|------------|-----------------------------|
| 80 | LQFP | LK | 98ASS23237W |
| 64 | QFP | FU | 98ASB42844B |
| 48 | QFN | FT | 98ARH99048A |
| 44 | LQFP | FG | 98ASS23225W |

Chapter 5

Revision History

To provide the most up-to-date information, the version of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

The following revision history table summarizes changes contained in this document.

| Revision Number | Revision Date | Description of Changes |
|-----------------|---------------|---|
| 1 | 9/2008 | Initial release of a separate data sheet and reference manual. Removed PTH7, clarified SPI as one full and one master-only, added missing RoHS logo, updated back cover addresses, and incorporated general release edits and updates. Added some finalized electrical characteristics. |
| 2 | 6/2009 | Added the parameter “Bandgap Voltage Reference” in Table 3-6 Updated Section 3.13, “EMC Performance” and corrected Table 3-16 . Updated disclaimer page. |
| 3 | 9/2010 | Added 48-pin QFN package information. |
| 4 | 8/2011 | Updated the t_{RTI} in the Table 3-12 . Updated the R_{IDD} in the Table 3-7 . |



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