

LC898123F40XC

IRIS or Auto Focus (AF) Controller & Driver with 40 KB Flash Memory

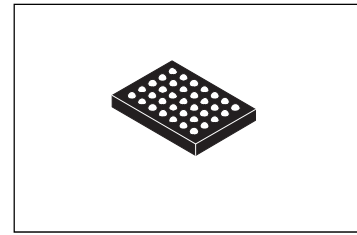


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1. Overview

LC898123F40XC is a system LSI integrating an onchip 32bit DSP, a Flash Memory and peripherals including analog circuits for IRIS or AF (Auto Focus) control and H-bridge and linear drivers.



WLCSP35, 3.22x2.3

2. Features

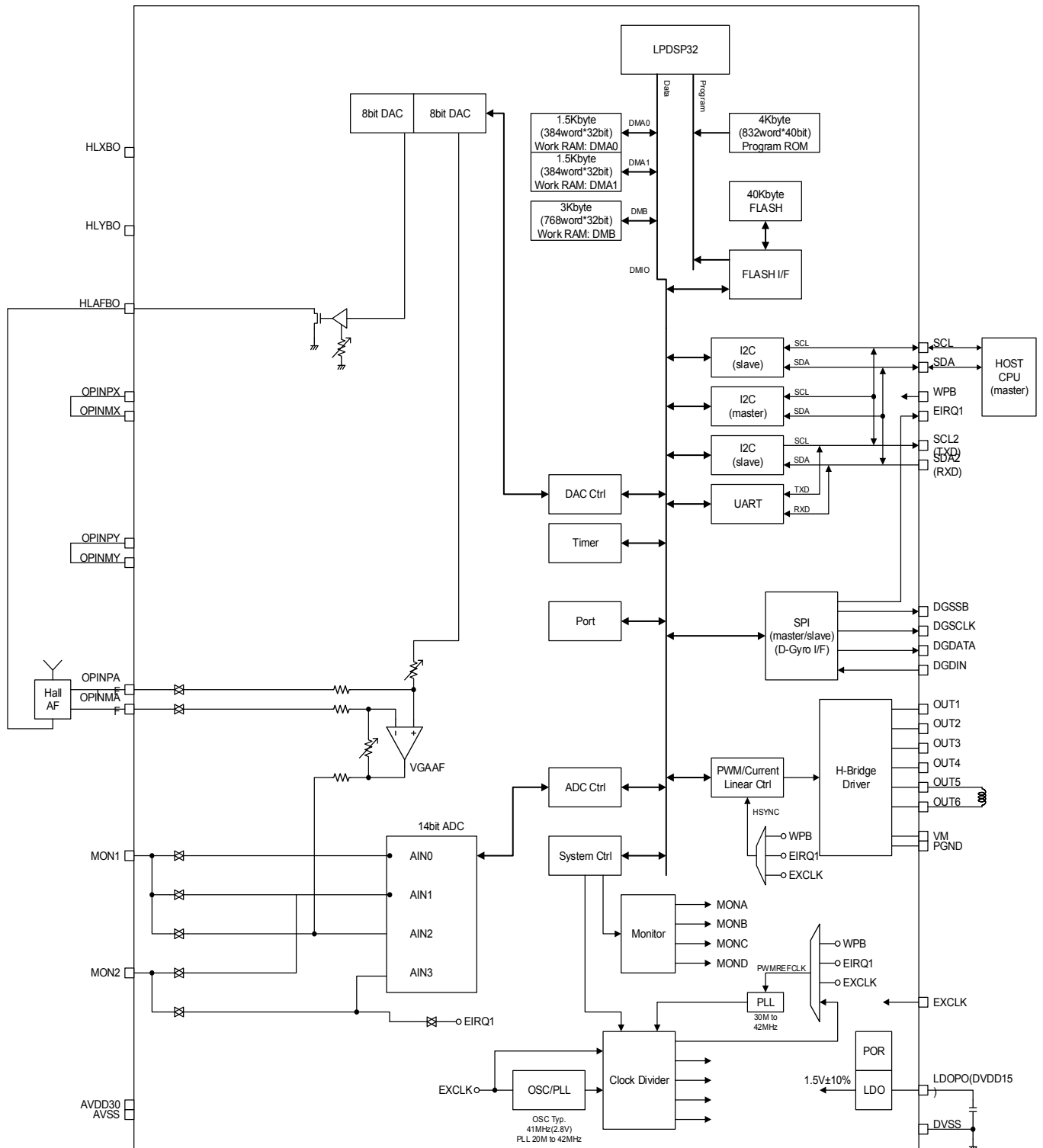
- Onchip 32 bit DSP
 - Built-in software digital servo filter
 - Built-in software Gyro filter
- Flash Memory
 - 40 kByte Flash memory to store data and DSP program
- Peripherals
 - Hall AD converter
 - 14 bit
 - Input 4 ch
 - DA converter for Hall Offset setting
 - 8 bit / 1 ch
 - DA converter for Hall Bias
 - 8 bit
 - Output 1 ch
 - Built-in Serial I/F circuit (2-wire Bus with clock stretch function) (1MHz)
 - Built-in Hall Amp (Gain of Opamp : ×5, ×10, ×13, ×20, ×40, ×60)
 - Built-in OSC(Oscillator)
 - typ 41 MHz
 - Built-in LDO (Low Drop-Out regulator)
 - Digital Gyro I/F for various types of gyro (SPI Bus)
- Package
 - WLP35 (3.22mm × 2.30mm , thickness : 0.45mm w/ BC)
 - Pb-Free
 - Halogen Free
- Motor Driver
 - OP-AF(unidirection)
 - Constant current linear driver (×1 ch, $I_{full} = 150\text{ mA}$)
 - OP-AF(bidirection)
 - Constant current linear driver (×1 ch, $I_{full} = 150\text{ mA}$)
 - CL-AF
 - Constant current linear driver (×1 ch, $I_{full} = 150\text{ mA}$)
 - H-bridge PWM driver (×1 ch, $I_{max} 150\text{ mA}$)
- Power supply voltage
 - AD/DA/VGA/LDO/OSC :
 - AVDD30 = 2.6V to 3.3V
 - Digital I/O (except Gyro I/F) :
 - AVDD30 = 2.6V to 3.3V
 - Driver :
 - VM = Constant current : 1.75 to 3.3V
 - H Bridge PWM : 2.6 to 3.3V
 - Core Logic / Gyro I/F IO :
 - generated by onchip LDO
 - DVDD15 = typ 1.55V output

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

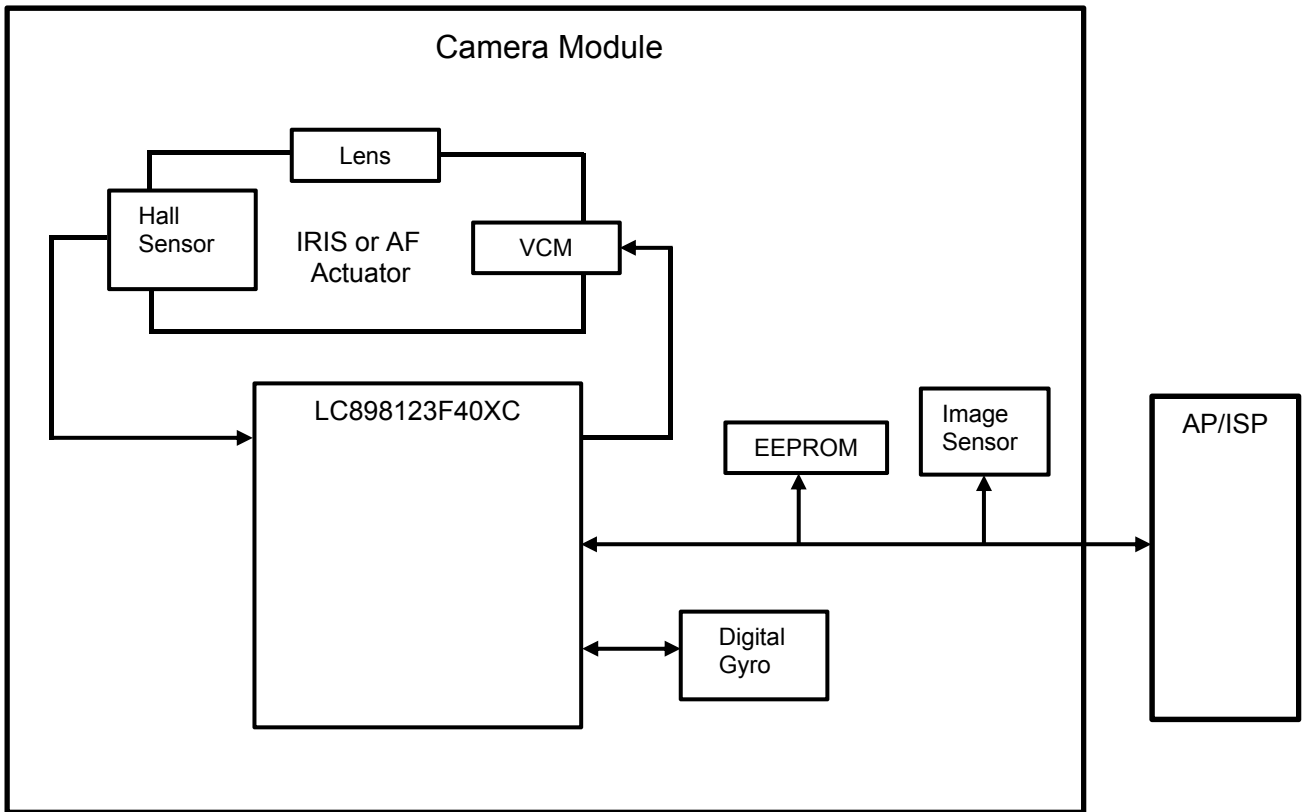
LC898123F40XC

3. Block Diagram



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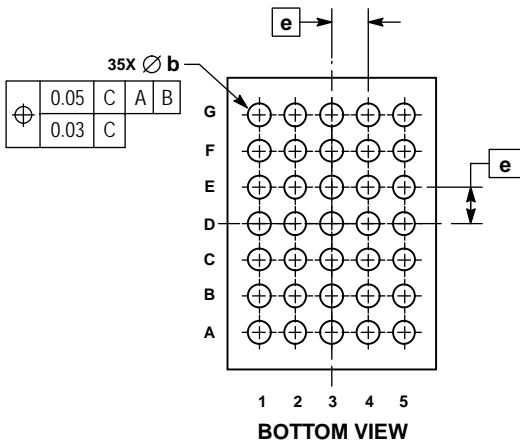
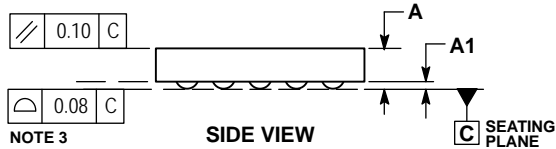
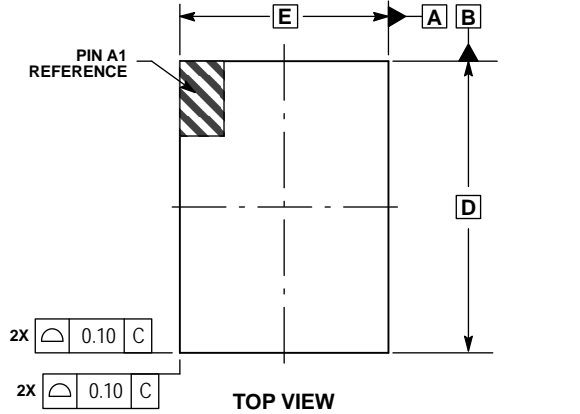
4. Application Diagram



LC898123F40XC

5. Package Dimensions unit : mm

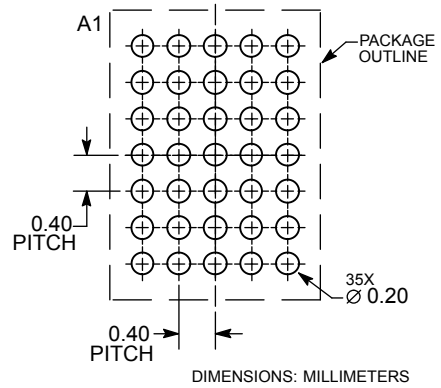
WLCSP35, 3.22x2.3
CASE 567LJ
ISSUE O



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.45
A1	0.03	0.13
b	0.15	0.25
D	3.22 BSC	
E	2.30 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

LC898123F40XC

6. Pin Assign

	OUT4	OUT3	OUT2	OUT1	VM
G					
	MON1	SDA2 (RXD)	WPB	PGND	OUT6
F					
	MON2	SCL2 (TXD)	DVSS	EXCLK	OUT5
E					
	DVDD15	EIRQ1	AVSS	SDA	SCL
D					
	AVDD30	HLAFBO	AVSS	HLYBO	HLXBO
C					
	DGDATA	DGSSB	OPINMAF	OPINMY	OPINMX
B					
	DGCLK	DGDIN	OPINPAF	OPINPY	OPINPX
A					
	1	2	3	4	5

BOTTOM VIEW

	Driver output		Analog V _{DD}
	Driver V _{DD}		Analog GND
	Driver GND		Digital GND
			Logic Core V _{DD} (Output)

LC898123F40XC

7. Pin Description

Pin Num	Pin	I/O Atr	I/O Pwr (V)	Primary Function (just after Reset)	Sub Functions	Init
A1	DGSCLK	B	1.55	Digital Gyro I/F Clock Input	Digital Gyro Clock Output	Z
				Digital Gyro I/F Clock Output	Internal Signal Monitor	
A2	DGDIN	B	1.55	Digital Gyro Data Input (4 Wired)	I2C Data I/O for DAC Monitor	Z
					Internal Signal Monitor	
A3	OPINPA F	I	2.8	AF Hall Opamp Input Plus	–	–
A4	OPINPY	I	2.8	connect to OPINMY (B4)	–	–
A5	OPINPX	I	2.8	connect to OPINMX (B5)	–	–
B1	DGDATA	B	1.55	GPIO Input	Digital Gyro I/F Data Output (4 Wired)	Z
					Digital Gyro I/F Data I/O (3 Wired)	
					Internal Signal Monitor	
B2	DGSSB	B	1.55	Digital Gyro I/F Chip Select Input	Digital Gyro I/F Chip Select Output	Z
				Digital Gyro I/F Chip Select Output	Internal Signal Monitor	
B3	OPINMA F	I	2.8	AF Hall OpAmp Input Minus	–	–
B4	OPINMY	I	2.8	connect to OPINPY (A4)	–	–
B5	OPINMX	I	2.8	connect to OPINPX (A5)	–	–
C1	AVDD30	P	–	Analog Power (2.6 to 3.3V)	–	–
C2	HLAFBO	O	2.8	AF Hall Bias Output	–	–
C3	AVSS	P	–	Analog GND	–	–
C4	HLYBO	O	2.8	Open	–	–
C5	HLXBO	O	2.8	Open	–	–
D1	DVDD15	P	–	Internal LDO Power Output	–	–
D2	EIRQ1	B	2.8	External IRQ1	I2C Data I/O for DAC Monitor	D
					UART Data Output (TXD)	
					SPI I/F Chip Select Output	
				External Clock Input	Internal Signal Monitor	
					Servo Monitor Analog Input	
D3	AVSS	P	–	Analog GND	–	–
D4	SDA	B	2.8	I2C Data	–	Z
D5	SCL	B	2.8	I2C Clock	–	Z
E1	MON2	B	2.8	(Debugger Data Input)	I2C Data I/O for DAC Monitor	Z
					UART Data Input (RXD)	
					Servo Monitor Analog Out	
					Internal Signal Monitor	
E2	SCL2 (TXD)	B	2.8	I2C Clock for 2nd I2C	I2C Data I/O for DAC Monitor	Z
					UART Data Output	
					Internal Signal Monitor	
E3	DVSS	P	–	Logic GND	–	–
E4	EXCLK	B	2.8	External Clock Input	I2C Data I/O for DAC Monitor	D
				External IRQ1	Internal Signal Monitor	
E5	OUT5	O	2.8	AF Driver Output (H-Bridge, Linear)	–	–
F1	MON1	B	2.8	(Debugger Data Output)	I2C Data I/O for DAC Monitor	L
					UART Data Output (TXD)	
					Servo Monitor Analog Out	
					Internal Signal Monitor	
F2	SDA2 (RXD)	B	2.8	I2C Data for 2nd I2C	I2C Data I/O for DAC Monitor	Z
					UART Data Input	
					Internal Signal Monitor	
F3	WPB	I	2.8	Write Protect for Flash	–	D
F4	PGND	P	–	Driver GND	–	–
F5	OUT6	O	2.8	AF Driver Output (H-Bridge, Linear)	–	–
G1	OUT4	O	2.8	Open	–	–
G2	OUT3	O	2.8	Open	–	–
G3	OUT2	O	2.8	Open	–	–
G4	OUT1	O	2.8	Open	–	–
G5	VM	P	–	Driver Power (2.6V to 3.3V)	–	–

LC898123F40XC

8. Electrical Characteristics

8-1 Logic

1) Absolute Maximum Rating at $V_{SS}=0V$

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	$V_{AD30\ max}$	$T_a \leq 25^\circ C$	-0.3 to +4.6	V
Input voltage (Except DGDATA, DGSSB, DGSCCLK, DGDIN)	V_{AI30}	$T_a \leq 25^\circ C$	-0.3 to $V_{AI30}+0.3$	V
Input voltage (DGDATA, DGSSB, DGSCCLK, DGDIN)	V_{LDO18}	$T_a = -30\ to\ +85^\circ C$	-0.3 to +1.872	V
Storage temperature	Tstg		-55 to +125	°C
Operating temperature	Topt		-30 to +85	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2) Allowable Operating Ratings at $T_a=-30\ to\ +85^\circ C$, $V_{SS}=0V$

3.0V Power Supply (AVDD30)

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{AD30}	2.6	2.8	3.3	V
Input voltage range	V_{IN}	0	-	V_{AD30}	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

LC898123F40XC

3) DC Characteristics : Input/Output level at V_{SS}= 0V, V_{DD}=2.6 to 3.6V, T_a = -30 to +85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Applicable Pin
High-level voltage input	VIH	CMOS schmitt	1.36			V	SCL2(TXD), SDA2(RXD), EXCLK
Low-level voltage input	VIL				0.39	V	
High-level voltage input	VIH	CMOS schmitt	1.26			V	DGDIN, DGSSB, DGSCCLK, DGDATA
Low-level voltage input	VIL				0.35		
High-level voltage input	VIH	CMOS schmitt	1.40				SCL, SDA
Low-level voltage input	VIL				0.40	V	
High-level voltage input	VIH	CMOS schmitt	1.48				EIRQ1, WPB
Low-level voltage input	VIL				0.37		
High-level voltage input	VIH	CMOS supported	1.40				MON1, MON2
Low-level voltage input	VIL				0.51		
High-level voltage output	VOH	IOH=-2mA	AVDD30-0.4			V	SCL2(TXD), SDA2(RXD), EXCLK, EIRQ1, MON1, MON2
High-level voltage output	VOH	IOH=-0.1mA	1.32			V	DGDIN, DGSSB, DGSCCLK, DGDATA
Low-level voltage output	VOL	IOL=2mA			0.2	V	SCL2(TXD), SDA2(RXD), DGDIN, DGSSB, DGSCCLK, DGDATA, EXCLK, SDA, SCL
Low-level voltage output	VOL	IOL=2mA			0.4	V	MON1, MON2, EIRQ1
Analog input voltage	VAI		AVSS		AVDD30	V	OPINPAF, OPINMAF
PullUp resistor	Rup		50		200	kΩ	MON1, MON2, EIRQ1, SCL2(TXD), SDA2(RXD)
PullUp resistor	Rup		180		800	kΩ	DGDATA, DGDIN, DGSSB, DGSCCLK
PullDown resistor	Rdn		50		220	kΩ	MON1, MON2, EIRQ1, SCL2(TXD), SDA2(RXD), EXCLK, WPB
PullDown resistor	Rdn		120		500	kΩ	DGDATA, DGDIN, DGSSB, DGSCCLK

4) Non-volatile Memory Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Endurance	EN				1000	Cycles
Data retention	RT		10			Years

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

LC898123F40XC

8-2 Driver

1) Absolute Maximum Rating

Parameter	Symbol	Condition	Ratings	Unit
Power supply voltage	VMmax		4.6	V
Output peak current	Iopeak	OUT5, OUT6 t ≤ 10ms, ON-duty ≤ 20%	200	mA
Output continuous current	Iomax	OUT5, OUT6	157.5	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2) Allowable Operating Ratings

Parameter	Symbol	Condition	Ratings	Unit
Ambient temperature	Topg		-30 to +85	°C
Power supply voltage	VM	Constant Current	1.75 to 3.3	V
		H-Bridge PWM	2.6 to 3.3	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3) H-Bridge Driver Output at Ta=25°C, AVDD30=VM=2.8V

Parameter	Symbol	Condition	typ	Unit
Output ON resistance OUT1 to OUT4	Ronu		0.5	Ω
	Rond		1.0 (*1)	Ω
Output ON resistance OUT5, OUT6	Ronu		1.1	Ω
	Rond		1.3 (*1)	Ω

4) Constant Current Driver Output at Ta=25°C, AVDD30=VM=2.8V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Current OUT5, OUT6	I _{full}	OP-AF (unidirection) Full code	142.5	150	157.5	mA
		OP-AF (bidirection) CL-AF Full code	142.5	150	157.5	mA
		Compliance Voltage OUT5, OUT6	V _{comp}	OP-AF (unidirection)	0.4	
OP-AF (bidirection) CL-AF	0.5			V		

OP-AF (unidirection)

$$\text{VCM resistance (RvcM)} = (\text{VM} - \text{Vcomp_Min}) / \text{Io} [\Omega]$$

OP-AF(bidirection) / CL-AF

$$\text{VCM resistance (RvcM)} = (\text{VM} - (\text{Ronu} * \text{Io} + \text{Vcomp_Min})) / \text{Io} [\Omega]$$

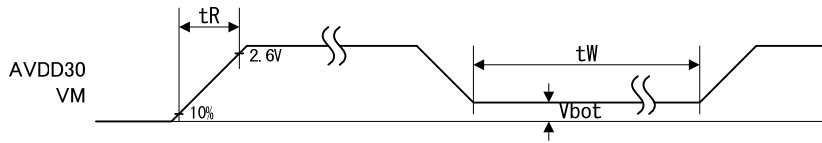
$$\text{Output ON resistance (Ron)} = \text{VM}/\text{Io} - \text{RvcM} [\Omega]$$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

LC898123F40XC

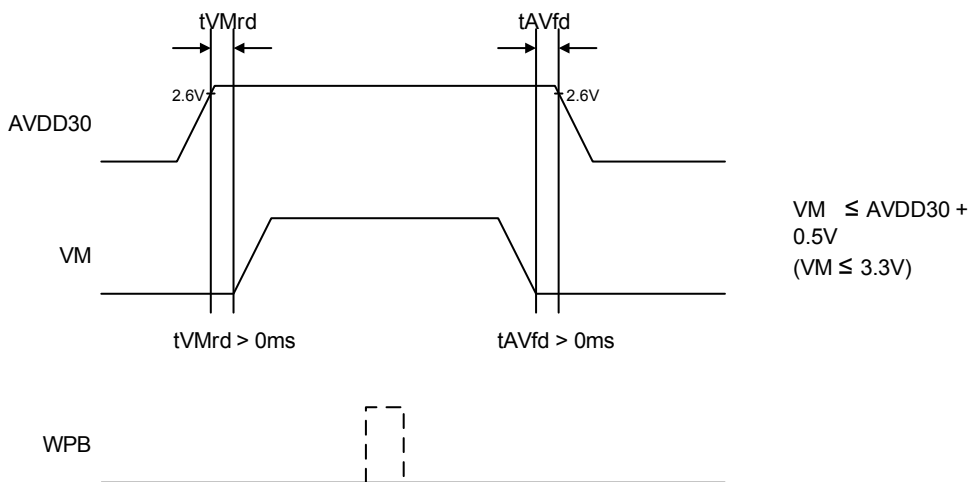
9. AC Characteristics

9-1 Power Sequence



Item	Symbol	Min	Typ	Max	Units
Rise time	t_R			3	ms
Wait time	t_W	100			ms
Bottom Voltage	V_{bot}			0.2	V

Injection order between AVDD30 and VM is below.



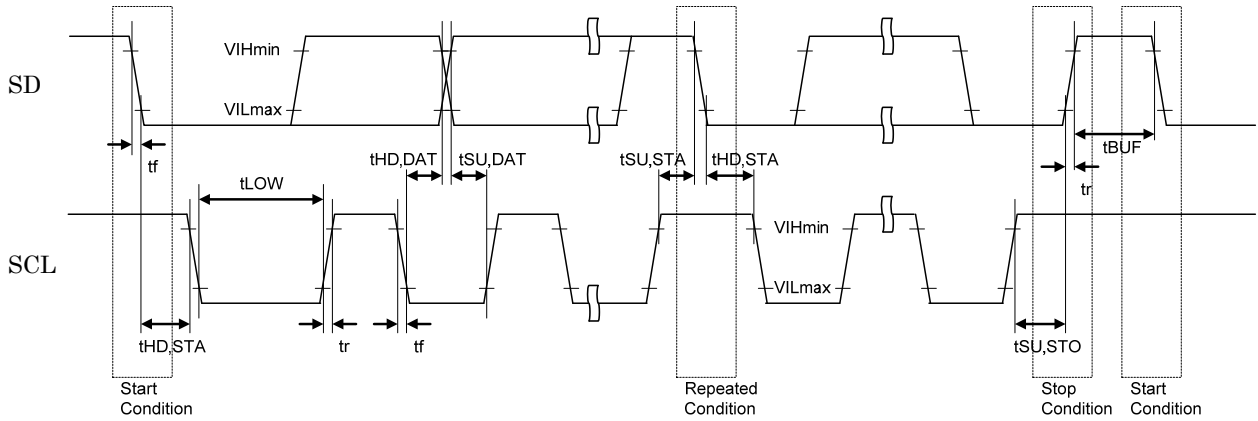
WPB must be open or pull down normally. When Erase or Program is made to Flash, WPB have to be High. SDA, SCL, EXCLK, WPB tolerate 3V input at the time of power off.

The data in the flash memory may be rewritten unintentionally if you do not keep specifications. And it is forbidden to power off during flash access. The data in the flash memory may be rewritten unintentionally.

LC898123F40XC

9-2 Two Wire Serial Interface Timing

The communication protocol is compatible with I²C (Fast mode Plus).
This circuit has clock stretch function.



Item	Symbol	Pin name	Min	Typ	Max	Units
SCL clock frequency	Fscl	SCL			1000	kHz
START condition hold time	tHD,STA	SCL SDA	0.26			μs
SCL clock Low period	tLOW	SCL	0.5			μs
SCL clock High period	tHIGH	SCL	0.26			μs
Setup time for repetition START condition	tSU,STA	SCL SDA	0.26			μs
Data hold time	tHD,DAT	SCL SDA	0 (*1)		0.9	μs
Data setup time	tSU,DAT	SCL SDA	50			ns
SDA, SCL rising time	tr	SCL SDA			120	ns
SDA, SCL falling time	tf	SCL SDA			120	ns
STOP condition setup time	tSU,STO	SCL SDA	0.26			μs
Bus free time between STOP and START	tBUF	SCL SDA	0.5			μs

(*1) Although the I²C specification defines a condition that 300 ns of hold time is required internally, LC898123F40XC is designed for a condition with typ. 40 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resistor.

LC898123F40XC

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC898123F40XC-VH	WLCSP35, 3.22x2.3 (Pb-Free / Halogen Free)	4000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

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