

NCP81149

Single-Phase Voltage Regulator with SVID Interface for Computing Applications

High Switching Frequency, High Efficiency, Integrated Power MOSFETs

The NCP81149, a single-phase synchronous buck regulator, integrates power MOSFETs to provide a high-efficiency and compact-footprint power management solution for new generation computing CPUs. The device is able to deliver up to 14 A TDC output current on an adjustable output with SVID interface. Operating in high switching frequency up to 1.2 MHz allows employing small size inductors and capacitors while maintaining high efficiency due to integrated solution with high performance power MOSFETs. Current-mode RPM control with feedforward from both input power supply and output voltage ensures stable operation over wide operation condition. The NCP81149 is in a QFN48 6 x 6 mm package.

Features

- Meets Intel® VR12.6 and VR12.6+ Specifications
- Support 11.5 W and 15 W ULT Platforms
- 4.5 V to 25 V Input Voltage Range
- Adjustable Output Voltage with SVID Interface
- Integrated Gate Driver and Power MOSFETs
- 0 V, 1.65 V, 1.7 V, 1.75 V Boot Up Voltage
- 500 kHz ~ 1.2 MHz Switching Frequency
- Current-Mode RPM Control
- Adaptive Voltage Positioning (AVP)
- Programmable DVID Feed-Forward to Support Fast DVID
- Feedforward Operation for Input Supply Voltage and Output Voltage
- Output Over-Voltage and Under-Voltage Protections
- External Current Limitation Programming with Inductor Current Sense
- QFN48, 6x6 mm, 0.4 mm Pitch Package
- This is a Pb-Free Device

Typical Applications

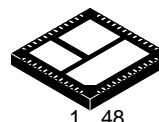
- Ultrabook Applications
- Notebook Applications



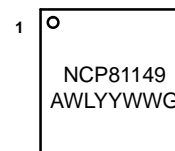
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MARKING DIAGRAM



QFN48
CASE 485CJ



NCP81149 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP81149MNTXG	QFN48 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NCP81149

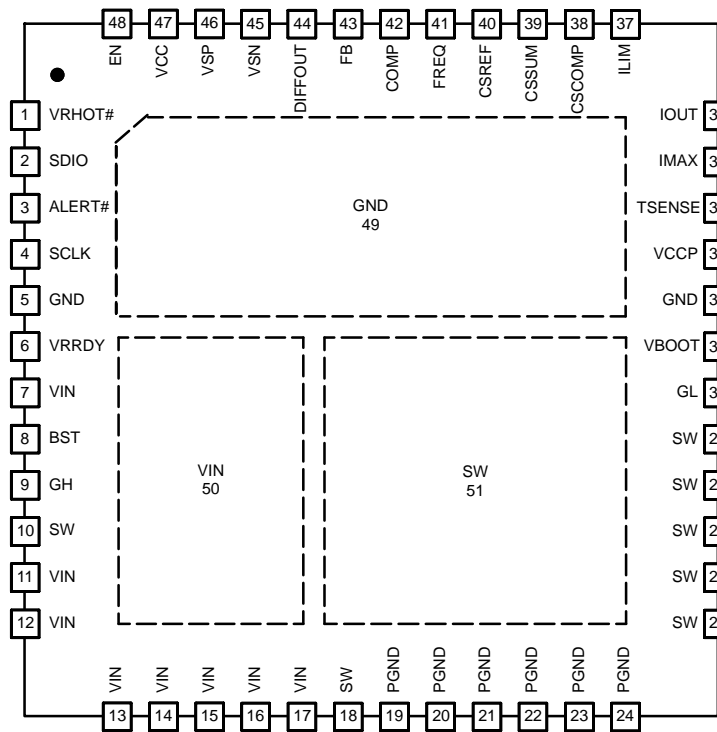


Figure 1. Pin Configuration
(Top View)

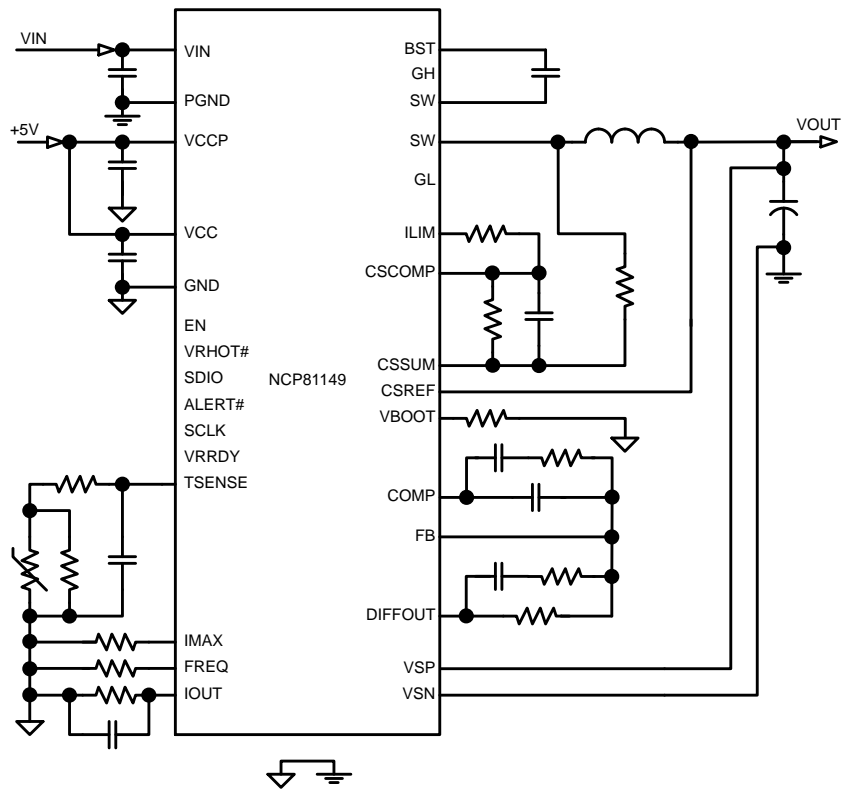


Figure 2. Typical Application Circuit

NCP81149

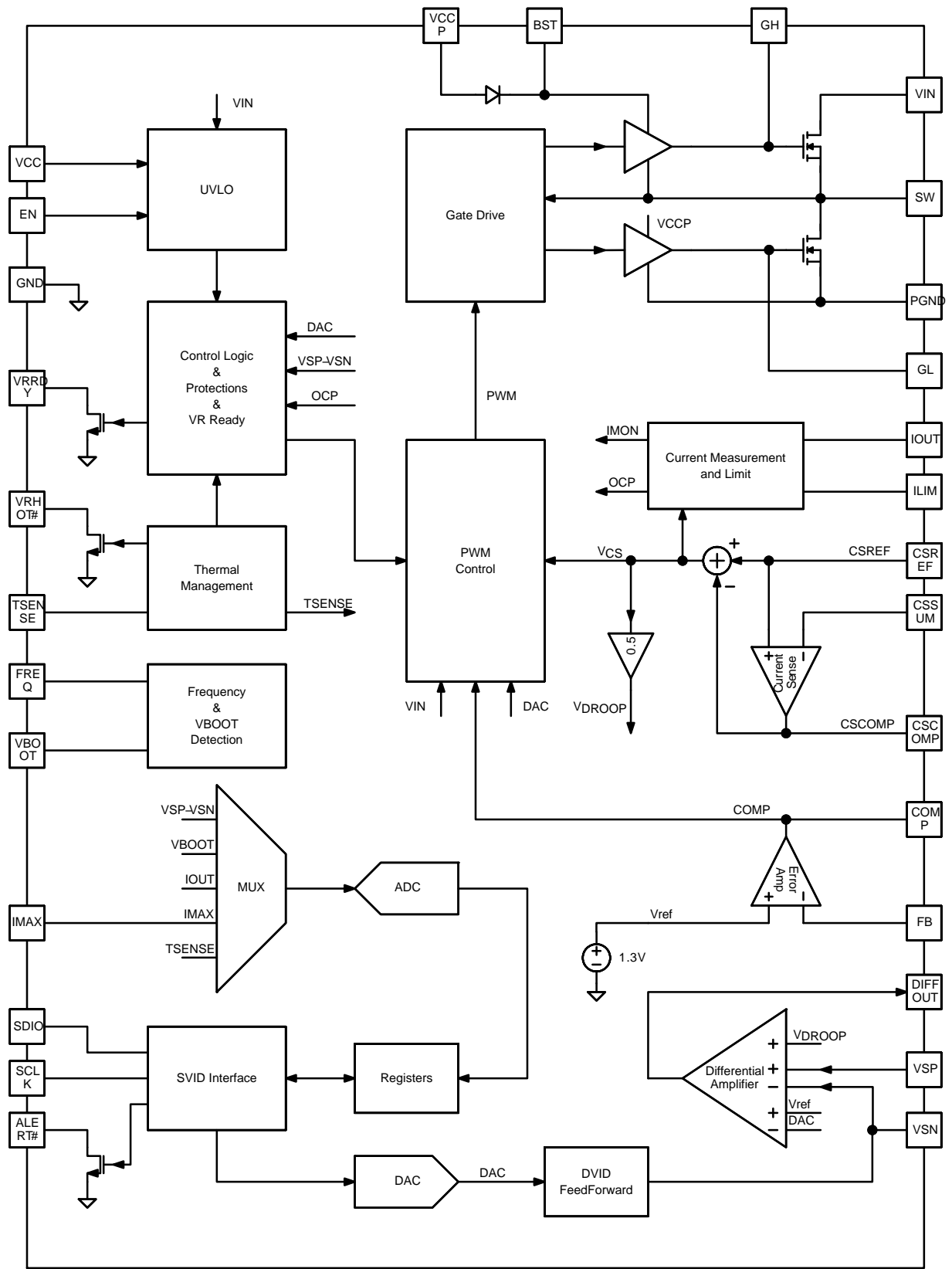


Figure 3. Functional Block Diagram

NCP81149

PIN DESCRIPTION

Pin	Name	Type	Description
1	VRHOT#	Logic Output	VR HOT. Logic low output represents over temperature.
2	SDIO	Logic Bidirectional	Serial Data IO Port. Data port of SVID interface.
3	ALERT#	Logic Output	ALERT. Open–drain output. Provides a logic low valid alert signal of SVID interface.
4	SCLK	Logic Input	Serial Clock. Clock input of SVID interface.
5, 32, 49	GND	Analog Ground	Analog Ground. Ground of internal control circuits. Must be connected to the system ground.
6	VRRDY	Logic Output	Voltage Regulator Ready. Open–drain output. Provides a logic high valid power good output signal, indicating the regulator's output is in regulation window.
7, 11–17, 50	VIN	Power Input	Power Supply Input. These pins are the power supply input pins of the device, which are connected to drain of internal high–side power MOSFET. 22 μ F or more ceramic capacitors must bypass this input to power ground. The capacitors should be placed as close as possible to these pins.
8	BST	Power Bidirectional	Bootstrap. Provides bootstrap voltage for the high–side gate driver. A 0.1 μ F ~ 1 μ F ceramic capacitor is required from this pin to SW (pin 10). A 1 Ω ~ 2 Ω resistor may be employed in series with the BST cap to reduce switching noise and ringing when needed.
9	GH	Analog Output	Gate of High–Side MOSFET. Directly connected with the gate of the high–side power MOSFET.
10	SW	Power Return	Switching Node. Provides a return path for integrated high–side gate driver. It is internally connected to source of high–side MOSFET.
18, 25–29, 51	SW	Power Output	Switch Node. Pins to be connected to an external inductor. These pins are interconnection between internal high–side MOSFET and low–side MOSFET.
19–24	PGND	Power Ground	Power Ground. These pins are the power supply ground pins of the device, which are connected to source of internal low–side power MOSFET. Must be connected to the system ground.
30	GL	Analog Output	Gate of Low–Side MOSFET. Directly connected with the gate of the low–side power MOSFET.
31	VBOOT	Analog Input	Boot–Up Voltage. A resistor from this pin to ground programs boot–up voltage.
33	VCCP	Analog Power	Voltage Supply of Gate Driver. Power supply input pin of internal gate driver. A 4.7 μ F or larger ceramic capacitor bypasses this input to ground. This capacitor should be placed as close as possible to this pin.
34	TSENSE	Analog	Temperature Sense. An external temperature sense network is connected to this pin.
35	IMAX	Analog Input	Current Maximum. A resistor from this pin to ground programs IMAX.
36	IOUT	Analog Output	OUT Current Monitor. Provides output signal representing output current by connecting a resistor from this pin to ground. Shorting this pin to ground disables IMON function.
37	ILIM	Analog Output	Limit of Current. A resistor from this pin to CSCOMP programs over–current threshold with inductor current sense.
38	CSCOMP	Analog Output	Current Sense COMP. Output pin of current sense amplifier.
39	CSSUM	Analog Input	Current Sense SUM. Inverting input of current sense amplifier.
40	CSREF	Analog Input	Current Sense Reference. Non–Inverting input of current sense amplifier.
41	FREQ	Analog Input	Frequency. A resistor from this pin to ground programs switching frequency.
42	COMP	Analog	Compensation. Output pin of error amplifier.
43	FB	Analog Input	Feedback. Inverting input to error amplifier.
44	DIFFOUT	Analog Output	Differential Amplifier Output. Output pin of differential voltage sense amplifier.
45	VSN	Analog Input	Voltage Sense Negative Input. Inverting input of differential voltage sense amplifier. It is also used for DVID feed forward function with an external resistor.
46	VSP	Analog Input	Voltage Sense Positive Input. Non–inverting input of differential voltage sense amplifier.

NCP81149

PIN DESCRIPTION

Pin	Name	Type	Description
47	VCC	Analog Power	Voltage Supply of Controller. Power supply input pin of control circuits. A 1 μ F or larger ceramic capacitor bypasses this input to ground. This capacitor should be placed as close as possible to this pin.
48	EN	Logic Input	Enable. Logic high enables the device and logic low makes the device in standby mode.

MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		Min	Max	
Power Supply Voltage to PGND	V_{VIN}		30	V
Switch Node to PGND	V_{SW}		30	V
Analog Supply Voltage to GND	V_{CC}, V_{CCP}	-0.3	6.5	V
BST to PGND	BST_PGND	-0.3	33 38 (<50 ns)	V
BST to SW	BST_SW	-0.3	6.5	V
GH to SW	GH	-0.3 -2 (<200 ns)	BST + 0.3	V
GL to GND	GL	-0.3 -2 (<200 ns)	$V_{CCP} + 0.3$	V
VSN to GND	VSN	-0.3	0.3	V
IOUT	IOUT	-0.3	2.5	V
PGND to GND	PGND	-0.3	0.3	V
Other Pins		-0.3	$V_{CC} + 0.3$	V
Latch up Current: (Note 1) All pins, except digital pins Digital pins	I_{LU}	-100 -10	100 10	mA
Operating Junction Temperature Range	T_J	-40	150	$^{\circ}$ C
Operating Ambient Temperature Range	T_A	-40	125	$^{\circ}$ C
Storage Temperature Range	T_{STG}	-55	150	$^{\circ}$ C
Thermal Resistance Junction to Board (Note 2)	$R_{\theta JB}$	8.2		$^{\circ}$ C/W
Thermal Resistance Junction to Ambient (Note 2)	$R_{\theta JA}$	21.8		$^{\circ}$ C/W
Power Dissipation at $T_A = 25^{\circ}$ C (Note 3)	P_D	4.59		W
Moisture Sensitivity Level (Note 4)	MSL	3		-

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Latch up Current per JEDEC standard: JESD78 class II.
- The thermal resistance values are dependent of the internal losses split between devices and the PCB heat dissipation. This data is based on a typical operation condition with a 4-layer FR-4 PCB board, which has two, 1-ounce copper internal power and ground planes and 2-ounce copper traces on top and bottom layers with approximately 80% copper coverage. No airflow and no heat sink applied (reference EIA/JEDEC 51.7). It also does not account for other heat sources that may be present on the PCB next to the device in question (such as inductors, resistors etc.)
- The maximum power dissipation (P_D) is dependent on input voltage, output voltage, output current, external components selected, and PCB layout. The reference data is obtained based on $T_{JMAX} = 125^{\circ}$ C and $R_{\theta JA} = 21.8^{\circ}$ C/W.
- Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020A.

NCP81149

ELECTRICAL CHARACTERISTICS

($V_{IN} = 8.4\text{ V}$, $V_{CC} = V_{CCP} = 5\text{ V}$, $V_{OUT} = 1.8\text{ V}$, typical values are referenced to $T_J = 25^\circ\text{C}$, Min and Max values are referenced to T_J from -40°C to 125°C , unless otherwise noted.)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
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SUPPLY VOLTAGE

Supply Voltage V_{IN} Range	(Note 5)	V_{IN}		8.4		V
Supply Voltage V_{CC} Range	(Note 5)	V_{CC}	4.75	5	5.25	V
Supply Voltage V_{CCP} Range	(Note 5)	V_{CCP}	4.75	5	5.25	V

SUPPLY VOLTAGE MONITOR

V_{IN} UVLO	Falling Threshold	V_{INUV-}	3.0	3.25	3.5	V
	Hysteresis	V_{INHYS}		650	–	mV
V_{CC} UVLO	Falling Threshold	V_{CCUV-}	3.8	4.08	–	V
	Rising Threshold	V_{CCUV+}	–	4.34	4.5	V
	Hysteresis	V_{CCHYS}	–	260	–	mV

SUPPLY CURRENT

V_{IN} Quiescent Supply Current (Power MOSFETs)	EN high, no load, PS0,1,2 Modes	I_Q	–	1.5	3	mA
	EN high, no load, PS3 Mode		–	1.5	3	mA
	EN high, PS4 Mode (Note 6)		–	–	1	μA
V_{IN} Shutdown Current	EN low (Note 6)	I_{SD}	–	–	1	μA
V_{CC} Quiescent Supply Current (Controller)	EN high, no load, PS0,1,2 Modes	I_{QCC}	–	8.0	12	mA
	EN high, no load, PS3 Mode		–	7.5	12	mA
	EN high, PS4 Mode (Note 6)		–	170	194	μA
V_{CC} Shutdown Current	EN low (Note 6)	I_{SDCC}	–	–	100	μA
V_{CCP} Quiescent Supply Current (Gate Driver)	EN high, no load, PS0,1,2 Modes	I_{QCCP}	–	0.7	1.25	mA
	EN high, no load, PS3 Mode		–	0.7	1.25	mA
	EN high, PS4 Mode (Note 6)		–	–	2	μA
V_{CCP} Shutdown Current	EN low	I_{SDCCP}	–	–	2	μA

OUTPUT VOLTAGE

Output Voltage Range	(Note 5)	V_{OUT}	0	–	2.3	V
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REGULATION ACCURACY

System Voltage Accuracy	$1.5\text{ V} < \text{DAC} < 2.3\text{ V}$		–0.7	0.7	%
	$1.0\text{ V} < \text{DAC} < 1.5\text{ V}$		–11	11	mV
	$0.5\text{ V} < \text{DAC} < 1.0\text{ V}$		–11	11	mV

DVID

Fast Slew Rate	Default	FSR		48		mV/ μs
Soft Start Slew Rate		SSSR		FSR/4		mV/ μs
Slow Slew Rate		SSR		FSR/2 FSR/4 (default) FSR/8 FSR/16		mV/ μs

DIFFERENTIAL VOLTAGE–SENSE AMPLIFIER

DC Gain	$V_{SP} - V_{SN} = 0.5\text{ V to } 2.3\text{ V}$	GAIN_DVA		1.0		V/V
–3dB Gain Bandwidth	$CL = 20\text{ pF to GND}$, $RL = 10\text{ k}\Omega$ to GND (Note 5)	BW_DVA		10		MHz
V_{SP} Input Voltage Range	(Note 5)	V_{SP}	–0.3	–	3.0	V
V_{SN} Input Voltage Range	(Note 5)	V_{SN}	–0.3	–	0.3	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Guaranteed by design, not tested in production.

6. $T_J = 25^\circ\text{C}$.

NCP81149

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = 8.4\text{ V}$, $V_{CC} = V_{CCP} = 5\text{ V}$, $V_{OUT} = 1.8\text{ V}$, typical values are referenced to $T_J = 25^\circ\text{C}$, Min and Max values are referenced to T_J from -40°C to 125°C , unless otherwise noted.)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
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DIFFERENTIAL VOLTAGE-SENSE AMPLIFIER

Input Bias Current	$V_{SP,CSREF} = 1.3\text{ V}$	I_{VSP} I_{VSN}	-15 -100		15 100	μA nA
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DIFFERENTIAL CURRENT-SENSE AMPLIFIER

DC Gain	(Note 5)	GAIN_DCA		80		dB
-3dB Gain Bandwidth	$CL = 20\text{ pF}$ to GND, $RL = 10\text{ k}\Omega$ to GND (Note 5)	BW_DCA		10		MHz
Input Offset Voltage		V_{OS_CS}	-300	-	300	μV
Input Bias Current	$CSSUM = CSREF = 1\text{ V}$	I_{CSSUM} I_{CSREF}	-7.5 -10		7.5 10	nA μA

ERROR AMPLIFIER

DC Gain	$CL = 20\text{ pF}$ to GND, $RL = 10\text{ k}\Omega$ to GND (Note 5)	GAIN_EA		80		dB
Unity Gain Bandwidth	$CL = 20\text{ pF}$ to GND, $RL = 10\text{ k}\Omega$ to GND (Note 5)	BW_EA		20		MHz
Slew Rate	$\Delta V_{in} = 100\text{ mV}$, $G = -10\text{ V/V}$, $\Delta V_{out} = 1.5\text{ V} - 2.5\text{ V}$, $CL = 20\text{ pF}$ to GND, $RL = 10\text{ k}\Omega$ to GND (Note 5)	SR_EA		25		$\text{V}/\mu\text{s}$
Output Voltage Swing	$I_{source_EA} = 2\text{ mA}$	V_{max_EA}	3.5	-	-	V
	$I_{sink_EA} = 2\text{ mA}$	V_{min_EA}	-	-	1	V
FB Voltage		V_{FB}		1.3		V
Input Bias Current	$V_{FB} = 1.3\text{ V}$	I_{FB}	-1.5		1.5	μA

SWITCHING FREQUENCY

Normal Operation Frequency (Programmed by a resistor at FREQ pin)	(Note 5)	FSW	500		1200	kHz
FREQ Output Voltage		VFREQ	1.95	2.0	2.05	V

CONTROL LOGIC

ENABLE Input High Voltage		VEN_H	0.8	-	-	V
ENABLE Input Low Voltage		VEN_L	-	-	0.3	V
ENABLE Input Hysteresis		VEN_HYS	-	300	-	mV
ENABLE Input Bias Current		IEN_BIAS	-		1.0	μA

SCLK, SDIO

Input High Voltage		V_{IH}	0.65			V
Input Low Voltage		V_{IL}			0.45	V
Input Threshold Hysteresis		V_{HYS}		50		mV
Output High Voltage	(Note 5)	V_{OH}		1.05		V
Output Low Voltage	SDIO	V_{OL}			0.3	V
Buffer On Resistance (data line, ALERT#, and VR_HOT#)		R_{ON}	3		13	Ω
Input Leakage Current	Pin voltage between 0 and 1.05 V		-100		100	μA

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NCP81149

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Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
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SCLK, SDIO

Input Capacitance	Die capacitance only (Note 5)				4.0	pF
VR Clock to Data Delay	Time between SCLK rising edge and valid SDIO level (Note 5)	Tco	4		8.3	ns
Setup Time	Time before SCLK falling (sampling) edge that SDIO level must be valid (Note 5)	Tsu	7			ns
Hold Time	Time after SCLK falling edge that the SDIO level remains valid (Note 5)	Thld	14			ns

ALERT#

Output Low Voltage	I_ALERT# = -4 mA		-	-	0.3	V
Output Leakage Current	High Impedance State, ALERT# = 3.3 V		-1.0	-	1.0	μA

VR_HOT#

Output Low Voltage	I_VRHOT# = -4 mA		-	-	0.3	V
Output Leakage Current	High Impedance State, VRHOT# = 3.3 V		-1.0	-	1.0	μA

TSENSE

Alert# Assert Threshold				491		mV
Alert# De-assert Threshold				513		mV
VR_HOT# Assert Threshold				472		mV
VR_HOT# De-assert Threshold				494		mV
TSENSE Bias Current	VTSENSE = 0.4 V		112	120	128	μA

VBOOT

Sensing Current	VVBOOT = GND			10		μA
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IMAX

Sensing Current	VIMAX = GND			10		μA
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ADC

Voltage Range			0		2.0	V
Total Unadjusted Error (TUE)			-1		1	%
Differential Nonlinearity (DNL)	8-bit				1	LSB
Power Supply Sensitivity				± 1		%
Conversion Time				30		μs
Round Robin				90		μs

VR_READY (VRRDY Output)

Rise Time	External 1 k Ω pull-up to 3.3 V, CTOT = 45 pF, $\Delta V_o = 10\%$ to 90%			100		ns
Fall Time	External 1 k Ω pull-up to 3.3 V, CTOT = 45 pF, $\Delta V_o = 90\%$ to 10%			10		ns
Output Voltage at Power-Up	Pulled up to 5 V via 2 k Ω		-	-	1.0	V
VR_READY Delay (Rising)	DAC = Target to VR_READY			50		μs

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NCP81149

ELECTRICAL CHARACTERISTICS (continued)

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Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
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VR_READY (VRRDY Output)

VR_READY Delay (Falling)	From OCP or OVP			5		μs
VRRDY Pin Low Voltage	Voltage at VRRDY pin with 4mA sink current	VPG_L	–	–	0.3	V
VRRDY Pin Leakage Current	VRRDY = 5 V	PG_LK	–1.0	–	1.0	μA

OVER VOLTAGE PROTECTION

Absolute Over Voltage Threshold During Soft-Start			2.8	2.9	3.0	V
Over Voltage Threshold Above DAC	VSP rising		350	400	425	mV
Over Voltage Delay	VSP rising to GH low			50		ns

UNDER VOLTAGE PROTECTION

Under Voltage Threshold Below DAC	VSP falling		250	300	350	mV
Under-voltage Delay				5		μs

OVER CURRENT PROTECTION

ILIM Threshold Current (OCP shutdown after 50 μs delay)		I _{LIMTH_SLOW}	8.5	10.0	12.0	μA
ILIM Threshold Current (immediate OCP shutdown)		I _{LIMTH_FAST}	12.0	15.0	18.0	μA

IOUT OUTPUT

Current Gain	(I _{OUTCURRENT}) / (I _{LIMCURRENT}); R _{ILIM} = 20 k Ω ; R _{IOUT} = 5.0 k Ω ; DAC = 0.8 V, 1.25 V, 1.52 V		9.5	10	10.5	A/A
Input Referred Offset Voltage	ILIM – CSREF		–5.5	–	5.5	mV
Output Source Current	ILIM sink current = 80 μA			800		μA

HIGH-SIDE MOSFET

Drain-to-Source ON Resistance	$V_{GS} = 4.5\text{ V}$, $I_D = 10\text{ A}$	R _{ON_H}	–	8.0	–	m Ω
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LOW-SIDE MOSFET

Drain-to-Source ON Resistance	$V_{GS} = 4.5\text{ V}$, $I_D = 10\text{ A}$	R _{ON_L}	–	4.0	–	m Ω
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HIGH-SIDE GATE DRIVE

Pull-High Drive ON Resistance	$V_{BST} - V_{SW} = 5\text{ V}$	R _{DRV_HH}	–	1.2	2.9	Ω
Pull-Low Drive ON Resistance	$V_{BST} - V_{SW} = 5\text{ V}$	R _{DRV_HL}	–	0.8	2.2	Ω
GH Propagation Delay Time	From GL falling to GH rising	T _{GH_d}		15		ns

LOW-SIDE GATE DRIVE

Pull-High Drive ON Resistance	$V_{CCP} - V_{PGND} = 5\text{ V}$	R _{DRV_LH}	–	0.9	3.0	Ω
Pull-Low Drive ON Resistance	$V_{CCP} - V_{PGND} = 5\text{ V}$	R _{DRV_LL}	–	0.4	1.25	Ω
GL Propagation Delay Time	From GH falling to GL rising	T _{GL_d}		10		ns

SW to PGND RESISTANCE

SW to PGND Pull-Down Resistance	(Note 5)	R _{SW}	–	1.88	–	k Ω
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BOOTSTRAP RECTIFIER SWITCH

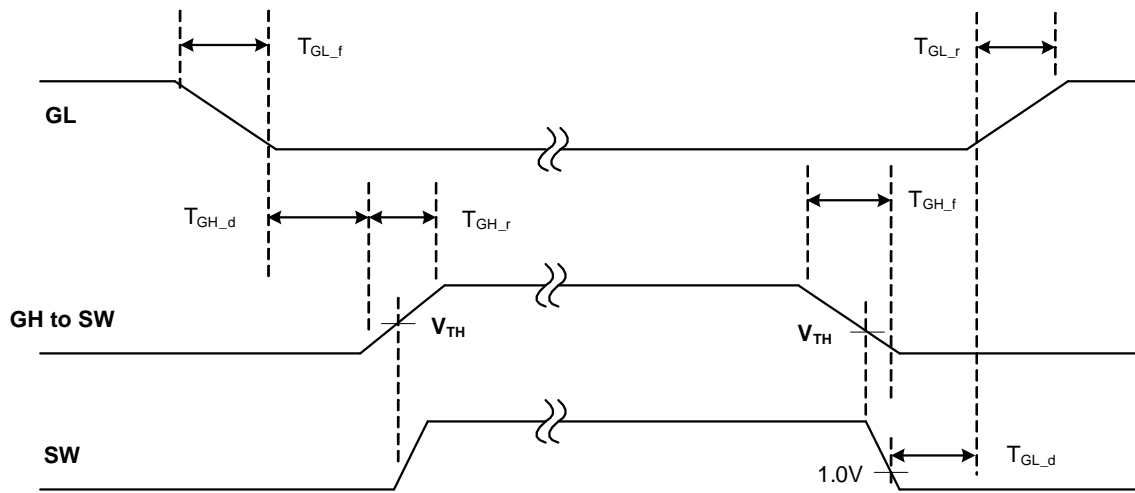
On Resistance	EN = L or EN = H and DRVL = H	R _{on_BST}	5	13	22	Ω
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6. $T_J = 25^\circ\text{C}$.

NCP81149



NOTE: Timing is referenced to the 90% and 10% points, unless otherwise noted.

Figure 4. Timing Diagram of Gate Drivers

Table 1. STATE TRUTH TABLE

STATE	VR_RDY Pin	Error AMP Comp Pin	OVP & UVP	Method of Reset
POR $0 < V_{CC} < UVLO$	N/A	N/A	N/A	
Disabled EN < threshold UVLO > threshold	Low	Low	Disabled	
Start up Delay & Calibration EN > threshold UVLO > threshold	Low	Low	Disabled	
Soft Start EN > threshold UVLO > threshold	Low	Operational	Active / No latch	
Normal Operation EN > threshold UVLO > threshold	High	Operational	Active / Latching	N/A
Over Voltage	Low	N/A	DAC + 400 mV	
Over Current	Low	Operational	Last DAC Code	
VID Code = 00h	Low: if Reg34h:bit0=0; High:if Reg34h:bit0=1	Clamped at 0.9 V	Disabled	

NCP81149

Table 2. VR12.6 VID CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	0	0	0	0	0	0	0	OFF	00
0	0	0	0	0	0	0	1	0.5	01
0	0	0	0	0	0	1	0	0.51	02
0	0	0	0	0	0	1	1	0.52	03
0	0	0	0	0	1	0	0	0.53	04
0	0	0	0	0	1	0	1	0.54	05
0	0	0	0	0	1	1	0	0.55	06
0	0	0	0	0	1	1	1	0.56	07
0	0	0	0	1	0	0	0	0.57	08
0	0	0	0	1	0	0	1	0.58	09
0	0	0	0	1	0	1	0	0.59	0A
0	0	0	0	1	0	1	1	0.6	0B
0	0	0	0	1	1	0	0	0.61	0C
0	0	0	0	1	1	0	1	0.62	0D
0	0	0	0	1	1	1	0	0.63	0E
0	0	0	0	1	1	1	1	0.64	0F
0	0	0	1	0	0	0	0	0.65	10
0	0	0	1	0	0	0	1	0.66	11
0	0	0	1	0	0	1	0	0.67	12
0	0	0	1	0	0	1	1	0.68	13
0	0	0	1	0	1	0	0	0.69	14
0	0	0	1	0	1	0	1	0.7	15
0	0	0	1	0	1	1	0	0.71	16
0	0	0	1	0	1	1	1	0.72	17
0	0	0	1	1	0	0	0	0.73	18
0	0	0	1	1	0	0	1	0.74	19
0	0	0	1	1	0	1	0	0.75	1A
0	0	0	1	1	0	1	1	0.76	1B
0	0	0	1	1	1	0	0	0.77	1C
0	0	0	1	1	1	1	0	0.78	1D
0	0	0	1	1	1	1	1	0.79	1E
0	0	0	1	1	1	1	1	0.8	1F
0	0	1	0	0	0	0	0	0.81	20
0	0	1	0	0	0	0	1	0.82	21

NCP81149

Table 2. VR12.6 VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	0	1	0	0	0	1	0	0.83	22
0	0	1	0	0	0	1	1	0.84	23
0	0	1	0	0	1	0	0	0.85	24
0	0	1	0	0	1	0	1	0.86	25
0	0	1	0	0	1	1	0	0.87	26
0	0	1	0	0	1	1	1	0.88	27
0	0	1	0	1	0	0	0	0.89	28
0	0	1	0	1	0	0	1	0.9	29
0	0	1	0	1	0	1	0	0.91	2A
0	0	1	0	1	0	1	1	0.92	2B
0	0	1	0	1	1	0	0	0.93	2C
0	0	1	0	1	1	0	1	0.94	2D
0	0	1	0	1	1	1	0	0.95	2E
0	0	1	0	1	1	1	1	0.96	2F
0	0	1	1	0	0	0	0	0.97	30
0	0	1	1	0	0	0	1	0.98	31
0	0	1	1	0	0	1	0	0.99	32
0	0	1	1	0	0	1	1	1	33
0	0	1	1	0	1	0	0	1.01	34
0	0	1	1	0	1	0	1	1.02	35
0	0	1	1	0	1	1	0	1.03	36
0	0	1	1	0	1	1	1	1.04	37
0	0	1	1	1	0	0	0	1.05	38
0	0	1	1	1	0	0	1	1.06	39
0	0	1	1	1	0	1	0	1.07	3A
0	0	1	1	1	0	1	1	1.08	3B
0	0	1	1	1	1	0	0	1.09	3C
0	0	1	1	1	1	0	1	1.1	3D
0	0	1	1	1	1	1	0	1.11	3E
0	0	1	1	1	1	1	1	1.12	3F
0	1	0	0	0	0	0	0	1.13	40
0	1	0	0	0	0	0	1	1.14	41
0	1	0	0	0	0	1	0	1.15	42
0	1	0	0	0	0	1	1	1.16	43

NCP81149

Table 2. VR12.6 VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	1	0	0	0	1	0	0	1.17	44
0	1	0	0	0	1	0	1	1.18	45
0	1	0	0	0	1	1	0	1.19	46
0	1	0	0	0	1	1	1	1.2	47
0	1	0	0	1	0	0	0	1.21	48
0	1	0	0	1	0	0	1	1.22	49
0	1	0	0	1	0	1	0	1.23	4A
0	1	0	0	1	0	1	1	1.24	4B
0	1	0	0	1	1	0	0	1.25	4C
0	1	0	0	1	1	0	1	1.26	4D
0	1	0	0	1	1	1	0	1.27	4E
0	1	0	0	1	1	1	1	1.28	4F
0	1	0	1	0	0	0	0	1.29	50
0	1	0	1	0	0	0	1	1.3	51
0	1	0	1	0	0	1	0	1.31	52
0	1	0	1	0	0	1	1	1.32	53
0	1	0	1	0	1	0	0	1.33	54
0	1	0	1	0	1	0	1	1.34	55
0	1	0	1	0	1	1	0	1.35	56
0	1	0	1	0	1	1	1	1.36	57
0	1	0	1	1	0	0	0	1.37	58
0	1	0	1	1	0	0	1	1.38	59
0	1	0	1	1	0	1	0	1.39	5A
0	1	0	1	1	0	1	1	1.4	5B
0	1	0	1	1	1	0	0	1.41	5C
0	1	0	1	1	1	0	1	1.42	5D
0	1	0	1	1	1	1	0	1.43	5E
0	1	0	1	1	1	1	1	1.44	5F
0	1	1	0	0	0	0	0	1.45	60
0	1	1	0	0	0	0	1	1.46	61
0	1	1	0	0	0	1	0	1.47	62
0	1	1	0	0	0	1	1	1.48	63
0	1	1	0	0	1	0	0	1.49	64
0	1	1	0	0	1	0	1	1.5	65

NCP81149

Table 2. VR12.6 VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	1	1	0	0	1	1	0	1.51	66
0	1	1	0	0	1	1	1	1.52	67
0	1	1	0	1	0	0	0	1.53	68
0	1	1	0	1	0	0	1	1.54	69
0	1	1	0	1	0	1	0	1.55	6A
0	1	1	0	1	0	1	1	1.56	6B
0	1	1	0	1	1	0	0	1.57	6C
0	1	1	0	1	1	0	1	1.58	6D
0	1	1	0	1	1	1	0	1.59	6E
0	1	1	0	1	1	1	1	1.6	6F
0	1	1	1	0	0	0	0	1.61	70
0	1	1	1	0	0	0	1	1.62	71
0	1	1	1	0	0	1	0	1.63	72
0	1	1	1	0	0	1	1	1.64	73
0	1	1	1	0	1	0	0	1.65	74
0	1	1	1	0	1	0	1	1.66	75
0	1	1	1	0	1	1	0	1.67	76
0	1	1	1	0	1	1	1	1.68	77
0	1	1	1	1	0	0	0	1.69	78
0	1	1	1	1	0	0	1	1.7	79
0	1	1	1	1	0	1	0	1.71	7A
0	1	1	1	1	0	1	1	1.72	7B
0	1	1	1	1	1	0	0	1.73	7C
0	1	1	1	1	1	0	1	1.74	7D
0	1	1	1	1	1	1	0	1.75	7E
0	1	1	1	1	1	1	1	1.76	7F
1	0	0	0	0	0	0	0	1.77	80
1	0	0	0	0	0	0	1	1.78	81
1	0	0	0	0	0	1	0	1.79	82
1	0	0	0	0	0	1	1	1.8	83
1	0	0	0	0	1	0	0	1.81	84
1	0	0	0	0	1	0	1	1.82	85
1	0	0	0	0	1	1	0	1.83	86
1	0	0	0	0	1	1	1	1.84	87

NCP81149

Table 2. VR12.6 VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	0	0	0	1	0	0	0	1.85	88
1	0	0	0	1	0	0	1	1.86	89
1	0	0	0	1	0	1	0	1.87	8A
1	0	0	0	1	0	1	1	1.88	8B
1	0	0	0	1	1	0	0	1.89	8C
1	0	0	0	1	1	0	1	1.9	8D
1	0	0	0	1	1	1	0	1.91	8E
1	0	0	0	1	1	1	1	1.92	8F
1	0	0	1	0	0	0	0	1.93	90
1	0	0	1	0	0	0	1	1.94	91
1	0	0	1	0	0	1	0	1.95	92
1	0	0	1	0	0	1	1	1.96	93
1	0	0	1	0	1	0	0	1.97	94
1	0	0	1	0	1	0	1	1.98	95
1	0	0	1	0	1	1	0	1.99	96
1	0	0	1	0	1	1	1	2	97
1	0	0	1	1	0	0	0	2.01	98
1	0	0	1	1	0	0	1	2.02	99
1	0	0	1	1	0	1	0	2.03	9A
1	0	0	1	1	0	1	1	2.04	9B
1	0	0	1	1	1	0	0	2.05	9C
1	0	0	1	1	1	0	1	2.06	9D
1	0	0	1	1	1	1	0	2.07	9E
1	0	0	1	1	1	1	1	2.08	9F
1	0	1	0	0	0	0	0	2.09	A0
1	0	1	0	0	0	0	1	2.1	A1
1	0	1	0	0	0	1	0	2.11	A2
1	0	1	0	0	0	1	1	2.12	A3
1	0	1	0	0	1	0	0	2.13	A4
1	0	1	0	0	1	0	1	2.14	A5
1	0	1	0	0	1	1	0	2.15	A6
1	0	1	0	0	1	1	1	2.16	A7
1	0	1	0	1	0	0	0	2.17	A8
1	0	1	0	1	0	0	1	2.18	A9

NCP81149

Table 2. VR12.6 VID CODES (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	0	1	0	1	0	1	0	2.19	AA
1	0	1	0	1	0	1	1	2.2	AB
1	0	1	0	1	1	0	0	2.21	AC
1	0	1	0	1	1	0	1	2.22	AD
1	0	1	0	1	1	1	0	2.23	AE
1	0	1	0	1	1	1	1	2.24	AF
1	0	1	1	0	0	0	0	2.25	B0
1	0	1	1	0	0	0	1	2.26	B1
1	0	1	1	0	0	1	0	2.27	B2
1	0	1	1	0	0	1	1	2.28	B3
1	0	1	1	0	1	0	0	2.29	B4
1	0	1	1	0	1	0	1	2.3	B5

NCP81149

DETAILED DESCRIPTION

General

The NCP81149, a single-phase synchronous buck regulator, integrates power MOSFETs to provide a high-efficiency and compact-footprint power management solution for new generation computing CPUs. The device is able to deliver up to 14 A TDC output current on an adjustable output with SVID interface. Operating in high switching frequency up to 1.2 MHz allows employing small size inductors and capacitors while maintaining high efficiency due to integrated solution with high performance power MOSFETs. Current-mode RPM control with feedforward from both input power supply and output voltage ensures stable operation over wide operation condition.

Serial VID interface (SVID)

The NCP81149 supports Intel serial VID interface. It communicates with the microprocessor through three wires (SCLK, SDIO, ALERT#).

Boot Voltage

The NCP81149 has a Vboot voltage can be externally programmed by a resistor connected to the VBOOT pin. A 10 μ A current is sourced from the VBOOT pin and the resulting voltage is measured. Table 3 shows the boot voltage configuration. This value is set on power up and cannot be changed after the initial power up sequence is complete.

Table 3. BOOT VOLTAGE CONFIGURATION

Resistance at Vboot Pin	Boot Voltage
30.1k	0 V
49.9k	1.65 V
69.8k	1.70 V
90.9k	1.75 V

Current-Mode RPM Operation

The NCP81149 operates with the current-mode Ramp-Pulse-Modulation (RPM) scheme in PS0/1/2/3 operation modes. In forced CCM mode, the inductor current is always continuous and the device operates in quasi-fixed switching frequency, which has a typical value programmed by users through a resistor at pin FREQ. In auto CCM/DCM mode, the inductor current is continuous and the device operates in quasi-fixed switching frequency in medium and heavy load range, while the inductor current becomes discontinuous and the device automatically operates in PFM mode with an adaptive fixed on time and variable switching frequency in light load range.

Switching Frequency

Switching frequency is programmed by a resistor RFREQ to ground at the FREQ pin. The typical frequency range is from 500 kHz to 1.2 MHz. The FREQ pin provides approximately 2 V out and the source current is mirrored into the internal ramp generator. The switching frequency can be found in Figure 5 with a given RFREQ. The frequency shown in Figure 5 is under condition of 10 A output current at VID = 1.7 V. The frequency has a variation over VID voltage and loading current, which maintains similar output ripple voltage over different operation condition. Figure 6 shows frequency variations over the VID voltage range.

NCP81149

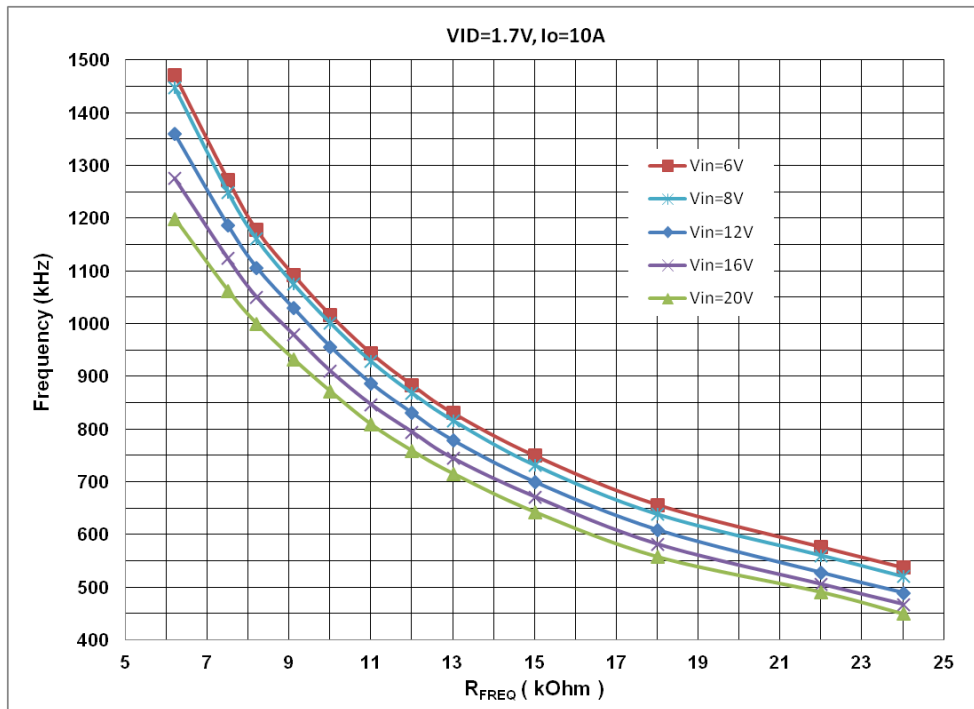


Figure 5. Switching Frequency vs. R_{FREQ}

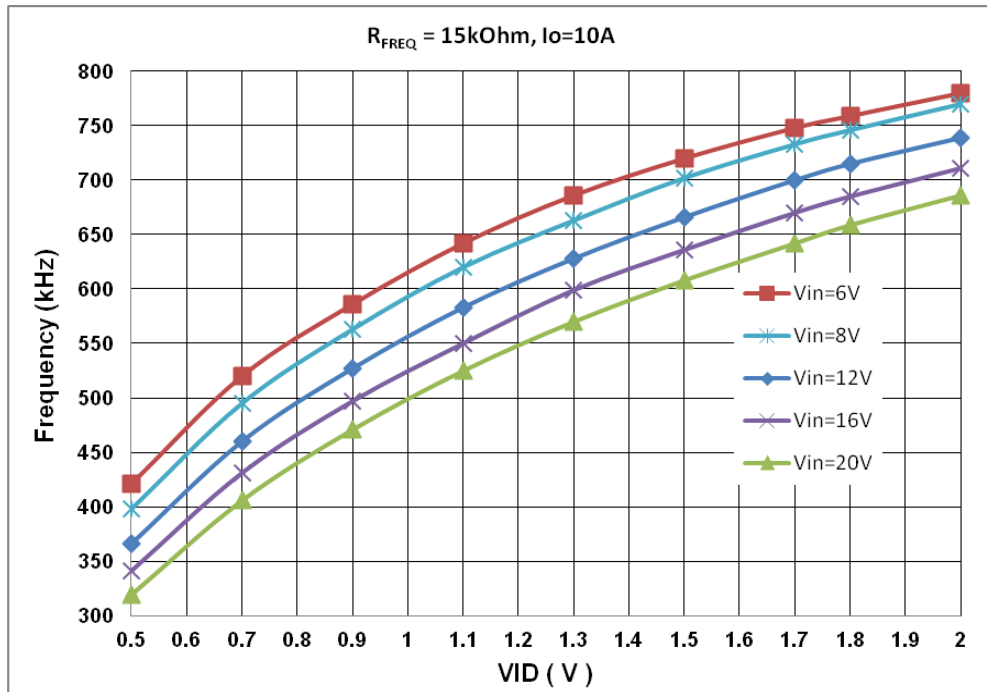


Figure 6. Switching Frequency vs. VID Voltage

Remote Voltage Sense

A high performance differential amplifier is provided to accurately sense the output voltage of the regulator. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The output (DIFOUT) of the

remote sense amplifier is a sum of the error voltage (between the output VSP-VSN and the DAC), a load-line voltage VDROOP, and a 1.3 V DC bias.

$$V_{DIFOUT} = (V_{VSP} - V_{VSN}) + (1.3V - V_{DAC}) + V_{DROOP} \quad (\text{eq. 1})$$

The VDROOP voltage is zero for non DC load line applications. In applications with a DC load line, the VDROOP voltage is a half of the voltage difference between the CSCOMP pin and the CSREF pin.

$$V_{DROOP} = 0.5 \cdot V_{CS} = 0.5 \cdot (V_{CSREF} - V_{CSCOMP}) \quad (\text{eq. 2})$$

The DIFOUT signal then goes through a compensation network and into the inverting input (FB pin) of an error amplifier. The non-inverting input of the error amplifier is connected to the same 1.3 V used for the differential sense amplifier output bias.

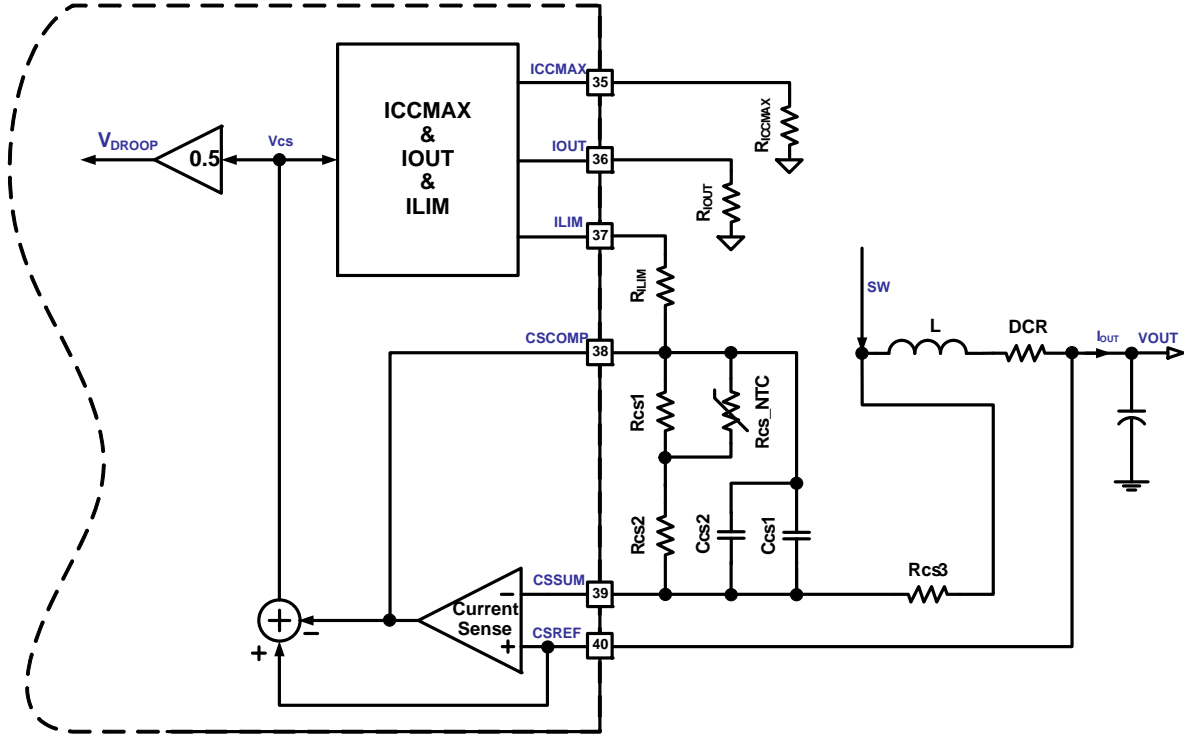


Figure 7. Differential Current-Sense Circuit Diagram

Differential Current Sense

The differential current-sense circuit diagram is shown in Figure 7. An internally-used voltage signal V_{cs} , representing the inductor current level, is the voltage difference between CSREF and CSCOMP. The output side of the inductor is used to create a low impedance virtual ground. The current-sense amplifier actively filters and gains up the voltage applied across the inductor to recover the voltage drop across the inductor's DC resistance (DCR). RCS_NTC is placed close to the inductor to sense the temperature. This allows the filter time constant and gain to be a function of the Rth_NTC resistor and compensate for the change in the DCR with temperature. The DC gain in the current sensing loop is

$$G_{CS} = \frac{V_{CS}}{V_{DCR}} = \frac{V_{CSREF} - V_{CSCOMP}}{I_{OUT} \cdot DCR} = \frac{R_{CS}}{R_{CS3}} \quad (\text{eq. 3})$$

Where

$$R_{CS} = R_{CS2} + \frac{R_{CS1} \cdot R_{CS_NTC}}{R_{CS1} + R_{CS_NTC}} \quad (\text{eq. 4})$$

The values of Rcs1 and Rcs2 are set based on a 220k NTC thermistor and the temperature effect of the inductor and

thus usually they should not need to be changed. The gain G_{cs} can be adjusted by the value change of the Rcs3 resistor. The internal V_{cs} voltage should be set to the output voltage droop in applications with a DC load line requirement. In no droop applications, the gain G_{cs} should be set to provide about 100mV across the current limit programming resistor at full load.

In order to recover the inductor DCR voltage drop current signal, the pole frequency in the CSCOMP filter should be set equal to the zero from the output inductor, that means

$$C_{CS1} + C_{CS2} = \frac{L}{DCR \cdot R_{CS}} \quad (\text{eq. 5})$$

Ccs1 and Ccs2 are in parallel to allow for a fine tuning of the time constant using commonly available values.

In applications with a droop voltage VDROOP, the DC load line LL can be obtained by

$$\begin{aligned} LL &= \frac{V_{DROOP}}{I_{OUT}} = \frac{0.5 \cdot (V_{CSREF} - V_{CSCOMP})}{I_{OUT}} \\ &= 0.5 \cdot \frac{R_{CS}}{R_{CS3}} \cdot DCR \end{aligned} \quad (\text{eq. 6})$$

Over Current Protection

The NCP81149 provides two different types of current limit protection. Current limits are programmed with a resistor RILIM between the CSCOMP pin and the ILIM pin. The current from the ILIM pin to this resistor is then compared to two internal currents (10 μA and 15 μA) corresponding to two different current limit thresholds ILIM and ILIM_Fast (150% of ILIM level). If the ILIM pin current exceeds the 10 μA level, an internal latch-off timer starts. The controller shuts down if the fault is not removed after 50 μs. If the current into the pin exceeds 15 μA the controller will shut down immediately. To recover from an OCP fault the EN pin must be cycled low.

The value of RILIM can be designed using the following equation with a required over current protection threshold ILIM and a known current-sense network.

$$R_{ILIM} = \frac{V_{CS@I_{LIM}}}{10\mu} = \frac{R_{CS}}{R_{CS3}} \cdot I_{LIM_PK} \cdot DCR \cdot 10^5 \quad (\text{eq. 7})$$

$$= \frac{R_{CS}}{R_{CS3}} \cdot \left(I_{LIM} + \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{2 \cdot L \cdot F_{SW} \cdot V_{IN}} \right) \cdot DCR \cdot 10^5$$

ICC_MAX

A resistor to ground is monitored on startup and this sets the ICCmax value. A 10 μA current is sourced from this pin to generate a voltage on the program resistor. The resistor value can be determined from the below equation. The resistor value should be no less than 10k.

$$ICC_MAX = \frac{R_{ICCMAX} \cdot 10\mu \cdot 64}{2} = R_{ICCMAX} \cdot 3.2 \cdot 10^{-4} \quad (\text{eq. 8})$$

IOUT

The IOUT pin sources a current equal to the ILIM sink current gained by the IOUT Current Gain (10 typ.). The voltage of the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to

ground such that a load equal to ICCMAX generates a 2 V signal on IOUT. A pull-up resistor to 5 V VCC can be used to offset the IOUT signal positive if needed.

$$R_{IOUT} = \frac{2}{10 \cdot V_{CS@ICC_MAX}} \cdot R_{ILIM}$$

$$= \frac{1}{5 \cdot \frac{R_{CS}}{R_{CS3}} \cdot ICC_MAX \cdot DCR} \cdot R_{ILIM} \quad (\text{eq. 9})$$

Input UVLO Protection

NCP81149 monitors supply voltages at the VCC pin and the VIN pins in order to provide under voltage protection. If either supply drops below its threshold, the controller will shut down the outputs. Upon recovery of the supplies, the controller reenters its startup sequence, and soft start begins.

Output Under-Voltage Protection

The output voltage is monitored by a dedicated differential amplifier. If the output falls below target by more than “Under Voltage Threshold below DAC-Droop”, the UVL comparator sends the VR_RDY signal low.

Output Over-Voltage Protection

During normal operation the output voltage is monitored at the differential inputs VSP and VSN. If the output voltage exceeds the DAC voltage by “Over Voltage Threshold above DAC”, GH will be forced low, and GL will go high. After the OVP trips, the DAC ramps slowly down to zero to avoid a negative output voltage spike during shutdown. If the DAC+OVP Threshold drops below the output, GL will again go high, and will toggle between low and high as the output voltage follows the DAC+OVP Threshold down. When the DAC gets to zero, the GH will be held low and the GL will remain high. To reset the part, the EN pin must be cycled low. During soft-start, the OVP threshold is set to 2.9 V. This allows the controller to start up without false triggering the OVP.

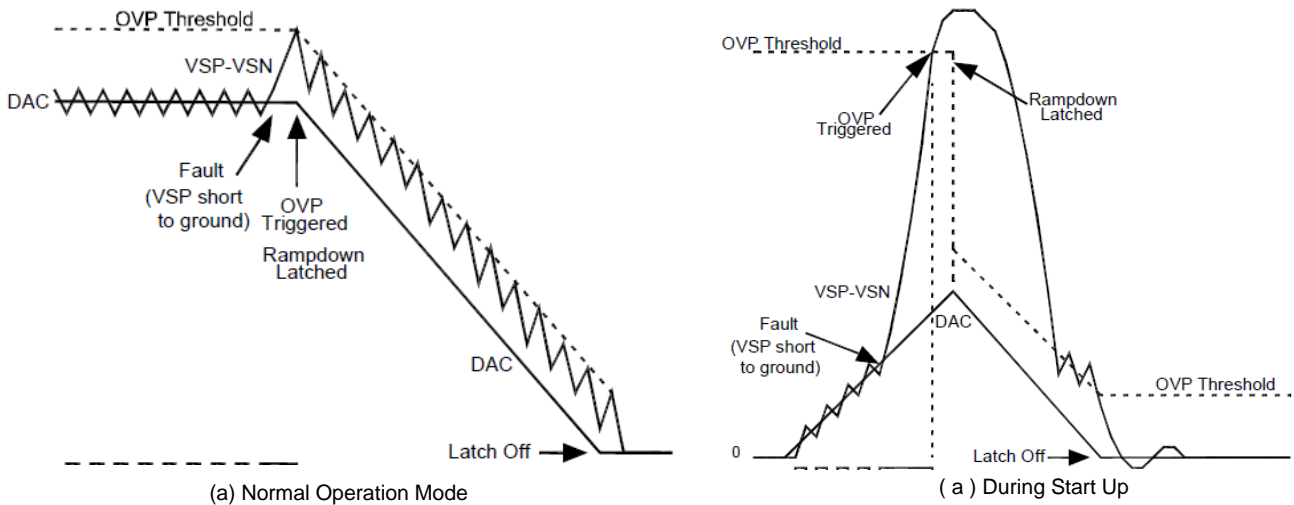


Figure 8. Function of Over Voltage Protection

Temperature Sense and Thermal Alert

The NCP81149 provides an external temperature sense and a thermal alert in normal operation mode. The temperature sense and thermal alert circuit diagram is shown in Figure 9. A precision current I_{TSENSE} is sourced out the output of the TSENSE pin to generate a voltage across the temperature sense network, which consists of a NTC thermistor R_{NTC} (100kOhm typ.), two resistors R_{COMP1} (0 Ω typ.) and R_{COMP2} (8.2 k Ω typ.), and a filter capacitor C_{Filter} (0.1 μ F typ.). The voltage on the temperature sense input is sampled by the internal A/D converter and then digitally converted to temperature and stored in SVID register 17h. Usually the thermistor is placed close to a hot spot like inductor or NCP81149 itself. A 100k NTC thermistor similar to the Murata NCP15WF104D03RC should be used. The NCP81149 also monitors the voltage at the TSENSE pin and compares the

voltage to internal thresholds and assert ALERT# or VRHOT# once it trips the thresholds. The DC voltage at TSENSE pin can be calculated by

$$V_{TSENSE} = I_{TSENSE} \cdot \left(R_{COMP1} + \frac{R_{COMP2} \cdot R_{NTC_T}}{R_{COMP2} + R_{NTC_T}} \right) \tag{eq. 10}$$

R_{NTC_T} is the resistance of R_{NTC} at an absolute temperature T, which is obtained by

$$R_{NTC_T} = R_{NTC_T0} \cdot \exp\left(B \cdot \left(\frac{1}{T} - \frac{1}{T_0} \right) \right) \tag{eq. 11}$$

where R_{NTC_T0} is a known resistance of R_{NTC} at an absolute temperature T_0 , and B is the B-constant of R_{NTC} .

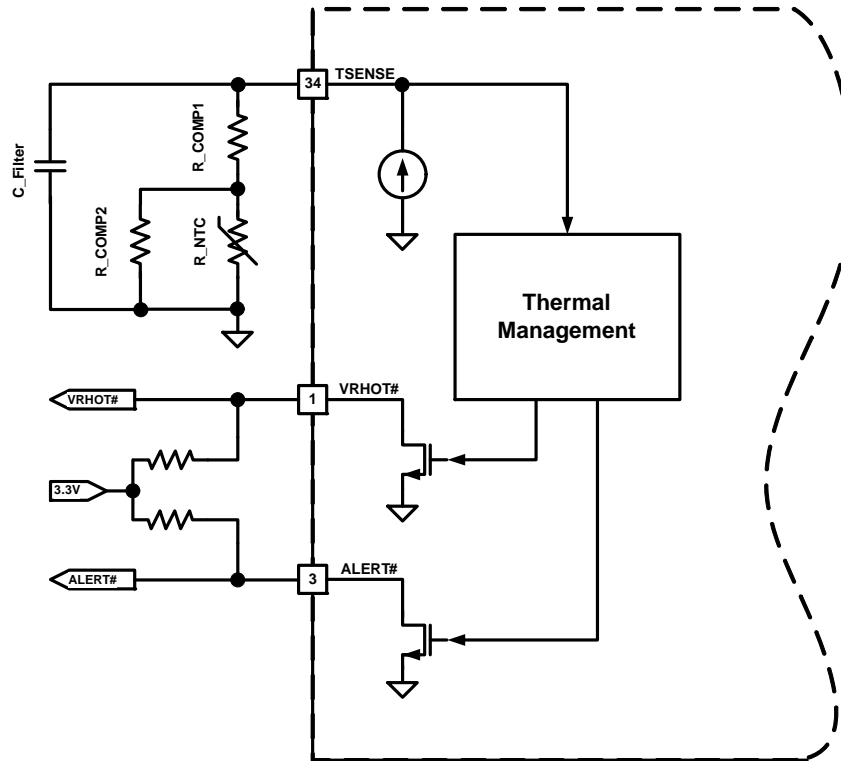


Figure 9. Temperature Sense and Thermal Alert Circuit Diagram

LAYOUT GUIDELINES

Electrical Layout Considerations

Good electrical layout is a key to make sure proper operation, high efficiency, and noise reduction. Electrical layout guidelines are:

- **Power Paths:** Use wide and short traces for power paths (such as VIN, VOUT, SW, and PGND) to reduce parasitic inductance and high-frequency loop area. It is also good for efficiency improvement.
- **Power Supply Decoupling:** The device should be well decoupled by input capacitors and input loop area should be as small as possible to reduce parasitic inductance, input voltage spike, and noise emission. Usually, a small low-ESL MLCC is placed very close to VIN and PGND pins.
- **VCC Decoupling:** Place decoupling caps as close as possible to the controller VCC and VCCP pins. The filter resistor at VCC pin should be not higher than 2.2 Ω to prevent large voltage drop.
- **Switching Node:** SW node should be a copper pour, but compact because it is also a noise source.
- **Bootstrap:** The bootstrap cap and an option resistor need to be very close and directly connected between pin 8 (BST) and pin 10 (SW). No need to externally connect pin 10 to SW node because it has been internally connected to other SW pins.
- **Ground:** It would be good to have separated ground planes for PGND and GND and connect the two planes at one point. Directly connect GND pin to the exposed pad and then connect to GND ground plane through vias.
- **Voltage Sense:** Use Kelvin sense pair and arrange a “quiet” path for the differential output voltage sense.
- **Current Sense:** Careful layout for current sensing is critical for jitter minimization, accurate current

limiting, and IOUT reporting. The filter cap from CSCOMP to CSREF should be close to the controller. The temperature compensating thermistor should be placed as close as possible to the inductor. The wiring path should be kept as short as possible and well away from the switch node.

- **Compensation Network:** The small feedback cap from COMP to FB should be as close to the controller as possible. Keep the FB traces short to minimize their capacitance to ground.
- **SVID Bus:** The Serial VID bus is a high speed data bus and the bus routing should be done to limit noise coupling from the switching node. The signals should be routed with the Alert# line in between the SVID clock and SVID data lines. The SVID lines must be ground referenced and each line’s width and spacing should be such that they have nominal 50 Ω impedance with the board stackup.

Thermal Layout Considerations

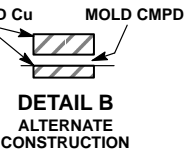
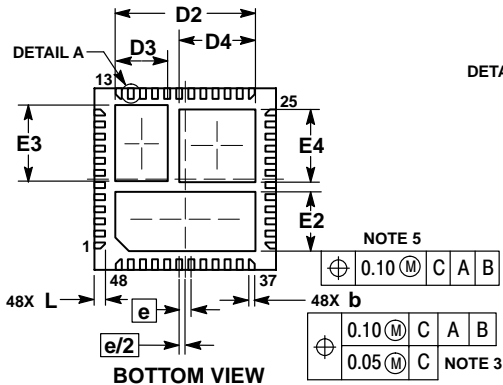
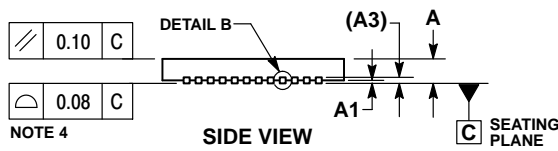
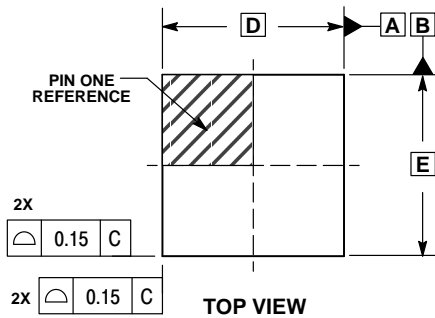
Good thermal layout helps high power dissipation from a small package with reduced temperature rise. Thermal layout guidelines are:

- The exposed pads must be well soldered on the board.
- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More free vias are welcome to be around IC and underneath the exposed pads to connect the inner ground layers to reduce thermal impedance.
- Use large area copper pour to help thermal conduction and radiation.
- Do not put the inductor to be too close to the IC, thus the heat sources are distributed.

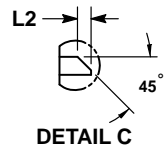
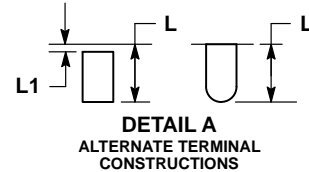
NCP81149

PACKAGE DIMENSIONS

QFN48 6x6, 0.4P
CASE 485CJ
ISSUE A

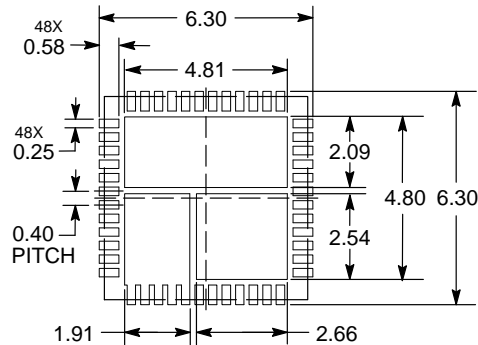


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSIONS: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
 5. POSITIONAL TOLERANCE APPLIES TO ALL THREE EXPOSED PADS IN BOTH X AND Y AXIS.



MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20	REF
b	0.15	0.25
D	6.00	BSC
D2	4.53	4.73
D3	1.64	1.84
D4	2.42	2.62
D5	4.58	4.78
E	6.00	BSC
E2	1.86	2.06
E3	2.41	2.61
E4	2.30	2.50
e	0.40	BSC
G3	1.45	BSC
G4	1.06	BSC
H2	1.40	BSC
H3	1.19	BSC
H4	1.10	BSC
L	0.25	0.45
L1	---	0.15
L2	0.15	REF


RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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