Operational Amplifier, Rail-to-Rail Output, 3 MHz BW

The NCx2007x series operational amplifiers provide rail–to–rail output operation, 3 MHz bandwidth, and are available in single, dual, and quad configurations. Rail–to–rail operation enables the user to make optimal use of the entire supply voltage range while taking advantage of 3 MHz bandwidth. The NCx2007x can operate on supply voltages as low as 2.7 V over the temperature range of –40°C to 125° C. At a 2.7 V supply, the high bandwidth provides a slew rate of 2.8 V/µs while only consuming 405 µA of quiescent current per channel. The wide supply range allows the NCx2007x to run on supply voltages as high as 36 V, making it ideal for a broad range of applications. Since this is a CMOS device, high input impedance and low bias currents make it ideal for interfacing to a wide variety of signal sensors. The NCx2007x devices are available in a variety of compact packages. Automotive qualified options are available under the NCV prefix.

Features

- Rail-To-Rail Output
- Wide Supply Range: 2.7 V to 36 V
- Wide Bandwidth: 3 MHz typical at $V_S = 2.7 \text{ V}$
- High Slew Rate: 2.8 V/ μ s typical at V_S = 2.7 V
- Low Supply Current: 405 μ A per channel at $V_S = 2.7 \text{ V}$
- Low Input Bias Current: 5 pA typical
- Wide Temperature Range: -40°C to 125°C
- Available in a variety of packages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Current Sensing
- Signal Conditioning
- Automotive

End Products

- Notebook Computers
- Portable Instruments
- Power Supplies

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.



ON Semiconductor®

www.onsemi.com





SOT-553 CASE 463B TSOP-5 CASE 483





Micro8™ CASE 846A SOIC-8 CASE 751





TSSOP-8 CASE 948S

TSSOP-14 CASE 948G



SOIC-14 NB CASE 751A

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 2 of this data sheet.

ORDERING INFORMATION

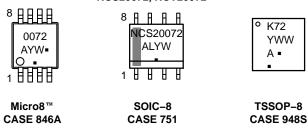
See detailed ordering and shipping information on page 4 of this data sheet.

MARKING DIAGRAMS

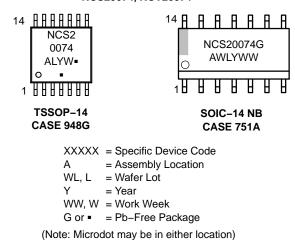
Single Channel Configuration NCS20071, NCV20071



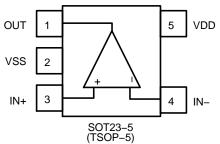
Dual Channel Configuration NCS20072, NCV20072

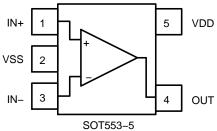


Quad Channel Configuration NCS20074, NCV20074

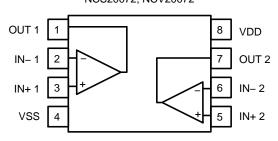


Single Channel Configuration NCS20071, NCV20071





Dual Channel Configuration NCS20072, NCV20072



Quadruple Channel Configuration NCS20074, NCV20074

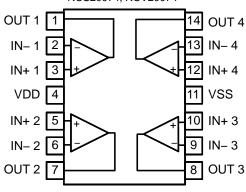


Figure 1. Pin Connections

ORDERING INFORMATION

Device	Configuration	Automotive	Marking	Package	Shipping [†]
NCS20071SN2T1G (In Development)**		No	TBD	TSOP-5 (Pb-Free)	3000 / Tape and Reel
NCS20071XV53T2G (In Development)**	Single	No Yes No Yes	TBD	SOT553-5 (Pb-Free)	4000 / Tape and Reel
NCV20071SN2T1G* (In Development)**	- Sirigle	Voc	TBD	TSOP-5 (Pb-Free)	3000 / Tape and Reel
NCV20071XV53T2G* (In Development)**		res	TBD	SOT553-5 (Pb-Free)	4000 / Tape and Reel
NCS20072DMR2G			0072	Micro8 (MSOP8) (Pb-Free)	4000 / Tape and Reel
NCS20072DR2G		Yes - No - No -	NCS20072	SOIC-8 (Pb-Free)	2500 / Tape and Reel
NCS20072DTBR2G	Post.		K72	TSSOP-8 (Pb-Free)	2500 / Tape and Reel
NCV20072DMR2G*	- Dual		0072	Micro8 (MSOP8) (Pb-Free)	4000 / Tape and Reel
NCV20072DR2G*			NCS20072	SOIC-8 (Pb-Free)	2500 / Tape and Reel
NCV20072DTBR2G*			K72	TSSOP-8 (Pb-Free)	2500 / Tape and Reel
NCS20074DR2G		N	NCS20074	SOIC-14 (Pb-Free)	2500 / Tape and Reel
NCS20074DTBR2G	Outd	NO	NCS2 0074	TSSOP-14 (Pb-Free)	2500 / Tape and Reel
NCV20074DR2G*	Quad	Va a	NCS20074	SOIC-14 (Pb-Free)	2500 / Tape and Reel
NCV20074DTBR2G*		Yes No No	NCS2 0074	TSSOP-14 (Pb-Free)	2500 / Tape and Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*}NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable.

**Contact local sales office for availability.

ABSOLUTE MAXIMUM RATINGS (Note 1)

	Rating	Symbol	Limit	Unit
Supply Voltage (V _{DD} – V _{SS}) (Note 2)	Vs	40	V
Input Voltage		V_{CM}	V _{SS} – 0.2 to V _{DD} + 0.2	V
Differential Input Voltage		V _{ID}	±V _S	V
Maximum Input Current		I _{IN}	±10	mA
Maximum Output Current		I _O	±100	mA
Continuous Total Power Dis	ssipation (Note 2)	P _D	200	mW
Maximum Junction Temper	ature	TJ	150	°C
Storage Temperature Rang	e	T _{STG}	-65 to 150	°C
Mounting Temperature (Infr	ared or Convection – 20 sec)	T _{mount}	260	°C
ESD Capability (Note 3) Human Body Model Machine Model Charged Device Model – NCS20072/NCV20072 Charged Device Model – NCS20074/NCV20074		HBM MM CDM CDM	2000 150 2000 (C6) 1000 (C6)	V
Latch-Up Current (Note 4)		I _{LU}	100	mA
Moisture Sensitivity Level (Note 5)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
- 2. Continuous short circuit operation to ground at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of the maximum output current rating over the long term may adversely affect reliability. Shorting output to either VDD or VSS will adversely affect reliability.
- 3. This device series incorporates ESD protection and is tested by the following methods:
 - ESD Human Body Model tested per ANSI/ANSI/ESDA/JEDEC JS-001-2010 (AEC-Q100-002)

 - ESD Machine Model tested per JESD22–A115 (AEC–Q100–003) ESD Charged Device Model tested per ANSI/ESD S5.3.1–2009 (AEC–Q100–011)
- 4. Latch-up Current tested per JEDEC standard: JESD78 (AEC-Q100-004)
- 5. Moisture Sensitivity Level tested per IPC/JEDEC standard: J-STD-020A

THERMAL INFORMATION

Parameter	Symbol	Package	Single Layer Board (Note 6)	Multi–Layer Board (Note 7)	Unit
		SOT23-5 / TSOP5			
		SOT553-5			
	θ_{JA}	Micro8 / MSOP8	236	167	
Junction-to-Ambient		SOIC-8	190	131	°C/W
		TSSOP-8	253	194	
		SOIC-14	142	101	
		TSSOP-14	179	128	

- 6. Values based on a 1S standard PCB according to JEDEC51-3 with 1.0 oz copper and a 300 mm² copper area
- 7. Values based on a 1S2P standard PCB according to JEDEC51-7 with 1.0 oz copper and a 100 mm² copper area

OPERATING RANGES

Parameter	Symbol	Min	Max	Unit
Operating Supply Voltage (Single Supply)	Vs	2.7	36	V
Operating Supply Voltage (Split Supply)	Vs	±1.35	±18	V
Differential Input Voltage	V _{ID}		V _S	V
Input Common Mode Voltage Range	V _{CM}	V _{SS}	V _{DD} – 1.35	V
Ambient Temperature	T _A	-40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS AT V_S = 2.7 V $T_A = 25^{\circ}C$; $R_L \ge 10$ kΩ; $V_{CM} = V_{OUT} = \text{mid}$ –supply unless otherwise noted. All limits are guaranteed by testing or statistical analysis. **Boldface** limits apply over the specified temperature range, $T_A = -40^{\circ}C$ to 125°C. (Notes 8, 9)

Parameter	Symbol	Cond	litions	Min	Тур	Max	Unit
INPUT CHARACTERISTICS							
Innut Offact Valtage	.,,				1.3	±3	mV
Input Offset Voltage	Vos					±4	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	T _A = 25°0	C to 125°C		2		μV/°C
Input Bias Current (Note 9)					5	200	nΛ
input bias current (Note 9)	I _{IB}					1500	рA
		NCv'	20072		2	75	
Input Offset Current (Note 9)	1	NOX	20072			500	pА
input Onset Current (Note 9)	los	NCv'	20074		2	75	рΑ
		NCX.	20074			200	
Channel Congretion	XTLK	DC	NCx20072		100		dB
Channel Separation	AILK	DC	NCx20074		115		uБ
Differential Input Resistance	R _{ID}				50		GΩ
Common Mode Input Resistance	R _{IN}				5		GΩ
Differential Input Capacitance	C _{ID}				1.5		pF
Common Mode Input Capacitance	C _{CM}				3.5		pF
		NCx2	20072,	90	110		
Common Mode Rejection Ratio	CMDD	$V_{CM} = V_{SS} + 0.2$	V to V _{DD} – 1.35 V	69			4D
	CMRR	NCx20074, $V_{CM} = V_{SS}$ to $V_{DD} - 1.35 \text{ V}$		90	110		dB
		NCX20074, V _{CM} =	V _{SS} to V _{DD} – 1.35 V	69			
OUTPUT CHARACTERISTICS							
Open Lean Voltage Cain	^			96	118		٩D
Open Loop Voltage Gain	A _{VOL}			86			dB
Output Current Canability		Op amp sir	nking current		70		m Λ
Output Current Capability	I _O	Op amp sou	rcing current		50		mA
Output Valtage High	\/	Voltage output qui	ng from positive rail		0.006	0.15	V
Output Voltage High	V _{OH}	voltage output swi	ng from positive rail			0.22	V
Outrot Valtage Law	V	Valta en autout audi	an financia na matika maji		0.005	0.15	
Output Voltage Low	V _{OL}	voltage output swir	ng from negative rail			0.22	V
AC CHARACTERISTICS							
Unity Gain Bandwidth	UGBW	C _L = 25 pF			3		MHz
Slew Rate at Unity Gain	SR	C _L = 20 pF	$R_L = 2 k\Omega$		2.8		V/µs
Phase Margin	φm	C _L =	25 pF		50		٥
Gain Margin	A _m	C _L =	25 pF		14		dB
Cattling Time		V _O = 1 Vpp,	Settling time to 0.1%		0.6		
Settling Time	t _S	Gain = 1, C _L = 20 pF Settling time to 0.01%			1.2		μS

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

^{8.} Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

^{9.} Performance guaranteed over the indicated operating temperature range by design and/or characterization.

ELECTRICAL CHARACTERISTICS AT V_S = 2.7 V

 $T_A = 25^{\circ}\text{C}$; $R_L \ge 10 \text{ k}\Omega$; $V_{CM} = V_{OUT} = \text{mid-supply}$ unless otherwise noted. All limits are guaranteed by testing or statistical analysis. **Boldface** limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to 125°C. (Notes 8, 9)

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
NOISE CHARACTERISTICS						
Total Harmonic Distortion plus Noise	THD+N	V _{IN} = 0.5 Vpp, f = 1 kHz, Av = 1		0.05		%
Leaved Defense d Valle as Ne's a	_	f = 1 kHz		30		-VI/1
Input Referred Voltage Noise	f = 1 kHz f = 10 kHz in f = 1 kHz	e _n	20		nV/√Hz	
Input Referred Current Noise	i _n	f = 1 kHz		0.25		fA/√Hz
SUPPLY CHARACTERISTICS						
Danier Orașile Daiaștia e Datia	DODD	Neteral	114	135		.ID
Power Supply Rejection Ratio	PSRR	No Load	100			dB
Davier County Orders and County		Den shannel and lead		405	525	μΑ
Power Supply Quiescent Current	I _{DD}	Per channel, no load			625	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS AT V_S = 5 V

 $T_A = 25^{\circ}\text{C}$; $R_L \ge 10 \text{ k}\Omega$; $V_{CM} = V_{OUT} = \text{mid-supply}$ unless otherwise noted. All limits are guaranteed by testing or statistical analysis. **Boldface** limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to 125°C. (Notes 10, 11)

Parameter	Symbol	Conditions		Min	Тур	Max	Unit
INPUT CHARACTERISTICS							
Innut Offset Voltage	V				1.3	±3	mV
Input Offset Voltage	V _{OS}					±4	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$T_A = 2$	25°C to 125 °C		2		μV/°C
Input Bias Current (Note 11)	_				5	200	nΛ
input bias Current (Note 11)	I _{IB}					1500	рA
		NCx20072			2	75	
Input Offset Current (Note 11)		IN	ICX20072			500]
input Onset Current (Note 11)	los	NCx20074			2	75	pA
						200	
Channel Congretion	XTLK	DC	NCx20072		100		dB
Channel Separation	AILK	DC	NCx20074		115		иь
Differential Input Resistance	R _{ID}				50		GΩ
Common Mode Input Resistance	R _{IN}				5		GΩ
Differential Input Capacitance	C _{ID}				1.5		pF
Common Mode Input Capacitance	C _{CM}				3.5		pF
		N	Cx20072,	102	125		
Common Mada Daigation Datia	CMDD	$V_{CM} = V_{SS} +$	0.2 V to V _{DD} – 1.35 V	80			dP
Common Mode Rejection Ratio	CIVIKK	CMRR NCx20074, $V_{CM} = V_{SS}$ to $V_{DD} - 1.35 \text{ V}$		105	125		dB
				80			

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

^{8.} Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

^{9.} Performance guaranteed over the indicated operating temperature range by design and/or characterization.

^{10.} Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

^{11.} Performance guaranteed over the indicated operating temperature range by design and/or characterization.

ELECTRICAL CHARACTERISTICS AT $V_S = 5 \text{ V}$

 $T_A = 25^{\circ}\text{C}$; $R_L \ge 10 \text{ k}\Omega$; $V_{CM} = V_{OUT} = \text{mid}$ -supply unless otherwise noted. All limits are guaranteed by testing or statistical analysis. **Boldface** limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to 125°C. (Notes 10, 11)

Parameter	Symbol	Cond	litions	Min	Тур	Max	Unit
OUTPUT CHARACTERISTICS							
Once Leen Walters Only	^			96	120		-ID
Open Loop Voltage Gain	A_{VOL}			86			dB
Output Compat Compatility		Op amp sir	king current		50		^
Output Current Capability	I _O	Op amp sou	rcing current		60		mA
Outrot Valta na Himb	V	Valta na autout aud			0.013	0.20	V
Output Voltage High	V _{OH}	voltage output swi	ng from positive rail			0.25]
Output Valtage Law	V	Voltage output out	ag from pagativa rail		0.01	0.10	V
Output Voltage Low	V_{OL}	voltage output swir	ng from negative rail			0.15]
AC CHARACTERISTICS							
Unity Gain Bandwidth	UGBW	C _L =	25 pF		3.2		MHz
Slew Rate at Unity Gain	SR	$C_{L} = 20 \text{ pF}$	$R_L = 2 k\Omega$		2.7		V/μs
Phase Margin	ϕ_{m}	C _L =	25 pF		50		٥
Gain Margin	A _m	C _L =	25 pF		14		dB
Cattling Times		$V_O = 3 \text{ Vpp},$	Settling time to 0.1%		1.2		_
Settling Time	t _S	Gain = 1, $C_L = 20 \text{ pF}$	Settling time to 0.01%		5.6		μS
NOISE CHARACTERISTICS							
Total Harmonic Distortion plus Noise	THD+N	V _{IN} = 2.5 Vpp, 1	f = 1 kHz, Av = 1		0.009		%
Lament Defermed Malterna Nation	_	f = 1	kHz		30		->/// II
Input Referred Voltage Noise	e _n	f = 1	0 kHz		20		nV/√ Hz
Input Referred Current Noise	i _n	f = 1	kHz		0.25		fA/√ Hz
SUPPLY CHARACTERISTICS							
Davier Comply Delegation Det	DODD	NI-	Land	114	135		40
Power Supply Rejection Ratio	PSKK	PSRR No Load		100			dB
Danier Comple Order and Order		D I	al as land		410	530	
Power Supply Quiescent Current	IDD	I _{DD} Per channel, no load				630	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

10. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

^{11.} Performance guaranteed over the indicated operating temperature range by design and/or characterization.

ELECTRICAL CHARACTERISTICS AT V_S = 10 V

 $T_A = 25^{\circ}\text{C}$; $R_L \ge 10 \text{ k}\Omega$; $V_{CM} = V_{OUT} = \text{mid}$ -supply unless otherwise noted. All limits are guaranteed by testing or statistical analysis. Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to 125°C. (Notes 12, 13)

Parameter	Symbol	Cond	litions	Min	Тур	Max	Unit
INPUT CHARACTERISTICS							
land Official Vallage	.,				1.3	±3	mV
Input Offset Voltage	Vos					±4	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	T _A = 25°0	C to 125°C		2		μV/°C
Janut Dies Coment (Note 42)	,				5	200	Λ
Input Bias Current (Note 13)	I _{IB}					1500	рA
		NCv	20072		2	75	
Input Offset Current (Note 13)	1	INCX.	20072			500	
input Offset Current (Note 13)	I _{OS}	NCv	20074		2	75	рA
		NCx20074				200	
Channel Congration	XTLK	DC	NCx20072		100		dB
Channel Separation	AILK	DC	NCx20074		115		uБ
Differential Input Resistance	R _{ID}				50		GΩ
Common Mode Input Resistance	R _{IN}				5		GΩ
Differential Input Capacitance	C _{ID}				1.5		pF
Common Mode Input Capacitance	C _{CM}				3.5		pF
		NCx2	20072,	110	130]
Common Mode Rejection Ratio	CMRR	$V_{CM} = V_{SS} + 0.2$	V to V _{DD} – 1.35 V	87			dB
	CIVIKK	NCx20074, $V_{CM} = V_{SS}$ to $V_{DD} - 1.35 \text{ V}$		110	130		
		NCX20074, V _{CM} =	VSS to VDD - 1.33 V	87			
OUTPUT CHARACTERISTICS							
Open Loop Voltage Gain	۸			98	120		dB
Open Loop Vollage Galli	A _{VOL}			88			uБ
Output Current Capability		Op amp sir	nking current		50		mA
Output Current Capability	I _O	Op amp sou	rcing current		65		IIIA
Output Voltage High	V	Voltago output swi	ng from positive rail		0.023	0.08	V
Output voltage riigii	V _{OH}	voltage output swi	ng nom positive rail			0.10	V
Output Voltage Low	V	Voltago output swir	ng from negative rail		0.022	0.3	V
Output voltage Low	V _{OL}	voltage output swii	ig itom negative fail			0.35	V
AC CHARACTERISTICS							
Unity Gain Bandwidth	UGBW	C _L = 25 pF			3.2		MHz
Slew Rate at Unity Gain	SR	C _L = 20 pF	$R_L = 2 k\Omega$		2.2		V/μs
Phase Margin	ϕ_{m}	C _L =	25 pF		50		0
Gain Margin	A _m	C _L =	25 pF		14		dB
Settling Time	+-	V _O = 8.5 Vpp,	Settling time to 0.1%		3.4		
Setting Time	t _S	Gain = 1, C _L = 20 pF Settling time to 0.01%			6.8		μS

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

^{12.} Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

^{13.} Performance guaranteed over the indicated operating temperature range by design and/or characterization.

ELECTRICAL CHARACTERISTICS AT V_S = 10 V

 $T_A = 25^{\circ}\text{C}$; $R_L \ge 10 \text{ k}\Omega$; $V_{CM} = V_{OUT} = \text{mid-supply}$ unless otherwise noted. All limits are guaranteed by testing or statistical analysis. Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to 125°C. (Notes 12, 13)

Parameter	Symbol	Conditions	Min	Тур	Max	Unit	
NOISE CHARACTERISTICS							
Total Harmonic Distortion plus Noise	THD+N	V _{IN} = 7.5 Vpp, f = 1 kHz, Av = 1		0.004		%	
Leaved Defense d Valle as Ne's a	_	f = 1 kHz		30		-VI/1	
Input Referred Voltage Noise	e _n	f = 1 kHz 30 f = 10 kHz 20 f = 1 kHz 0.25		nV/√ Hz			
Input Referred Current Noise	i _n	f = 1 kHz		0.25		fA/√Hz	
SUPPLY CHARACTERISTICS							
	D0DD		114	135			
Power Supply Rejection Ratio	PSRR	No Load	100			dB	
Daniel Original Original		Denote and an local		416	540		
Power Supply Quiescent Current	I _{DD}	Per channel, no load			640	μΑ	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS AT V_S = 36 V

 $T_A = 25^{\circ}\text{C}$; $R_L \ge 10 \text{ k}\Omega$; $V_{CM} = V_{OUT} = \text{mid-supply}$ unless otherwise noted. All limits are guaranteed by testing or statistical analysis. Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to 125°C. (Notes 14, 15)

Parameter	Symbol	Conditions		Min	Тур	Max	Unit
INPUT CHARACTERISTICS				•	•	•	
Innut Offert Veltere	N/				1.3	±3	mV
Input Offset Voltage	Vos					±4	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$T_A = 2$	25°C to 125°C		2		μV/°C
					5	200	
Input Bias Current (Note 15)	I _{IB}	NCx20072				2000	pА
		N			1500		
		NCx20072			2	75	
						1000	pA
Input Offset Current (Note 15)	los	NCx20074			2	75	
						200	
Observation	VTLV	D0	NCx20072		100		JD
Channel Separation	XTLK	DC	NCx20074		115		dB
Differential Input Resistance	R _{ID}		•		50		GΩ
Common Mode Input Resistance	R _{IN}				5		GΩ
Differential Input Capacitance	C _{ID}				1.5		pF
Common Mode Input Capacitance	C _{CM}				3.5		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

^{12.} Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

^{13.} Performance guaranteed over the indicated operating temperature range by design and/or characterization.

^{14.} Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

^{15.} Performance guaranteed over the indicated operating temperature range by design and/or characterization.

ELECTRICAL CHARACTERISTICS AT V_S = 36 V

 $T_A = 25^{\circ}\text{C}$; $R_L \ge 10 \text{ k}\Omega$; $V_{CM} = V_{OUT} = \text{mid}$ -supply unless otherwise noted. All limits are guaranteed by testing or statistical analysis. Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to 125°C. (Notes 14, 15)

Parameter	Symbol	Cond	itions	Min	Тур	Max	Unit
INPUT CHARACTERISTICS							
		NCx2	0072.	120	145		
		$V_{CM} = V_{SS} + 0.2 \text{ V to } V_{DD} - 1.35 \text{ V}$		95			- ID
Common Mode Rejection Ratio	CMRR			120	145		dB
		NCx20074, $V_{CM} = V_{CM}$	$V_{\rm SS}$ to $V_{\rm DD}$ – 1.35 V	95			
OUTPUT CHARACTERISTICS		•			•		
0 1 1/1 0:				98	120		
Open Loop Voltage Gain	A_{VOL}			88			dB
0 0		Op amp sin	king current		50		
Output Current Capability	I _O	Op amp sourcing current			65		- mA
					0.074	0.10	
Output Voltage High	V_{OH}	Voltage output swing from positive rail	NCx20072			0.15	V
		nom poom o ran	NCx20074			0.12	
0	.,				0.065	0.3	,,
Output Voltage Low	V_{OL}	Voltage output swing from negative rail				0.35	V
AC CHARACTERISTICS		•			•		
Unity Gain Bandwidth	UGBW	C _L = 25 pF			3.2		MHz
Slew Rate at Unity Gain	SR	C _L = 20 pF	$R_L = 2 k\Omega$		2.4		V/μs
Phase Margin	ϕ_{m}	C _L =	25 pF		50		۰
Gain Margin	A _m	C _L =	25 pF		14		dB
0.48		Vo = 10 Vpp.	Settling time to 0.1%		3.2		
Settling Time	t _S	$V_O = 10 \text{ Vpp},$ Gain = 1, $C_L = 20 \text{ pF}$	Settling time to 0.01%		6.8		μS
NOISE CHARACTERISTICS							
Total Harmonic Distortion plus Noise	THD+N	V _{IN} = 28.5 Vpp,	f = 1 kHz, Av = 1		0.001		%
1 15 (1)/ (1)		f = 1	kHz		30		\ //
Input Referred Voltage Noise	e _n	f = 10) kHz		20		nV/√Hz
Input Referred Current Noise	i _n	f = 1	kHz		0.25		fA/√ Hz
SUPPLY CHARACTERISTICS							
				114	135		
Power Supply Rejection Ratio	PSRR	No I	₋oad	100			dB
			NO 655-5		465	570	+
	Supply Quiescent Current I _{DD} Per channel, no load	NCx20072			700	1 .	
Power Supply Quiescent Current		Per channel, no load			465	600	μΑ
			NCx20074			700	1

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

14. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

^{15.} Performance guaranteed over the indicated operating temperature range by design and/or characterization.

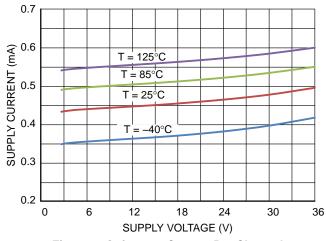


Figure 2. Quiescent Current Per Channel vs. **Supply Voltage**

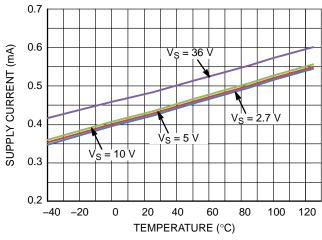


Figure 3. Quiescent Current vs. Temperature

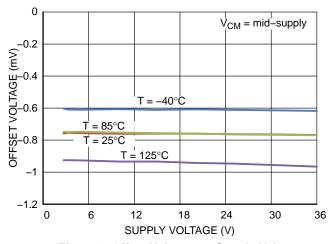


Figure 4. Offset Voltage vs. Supply Voltage

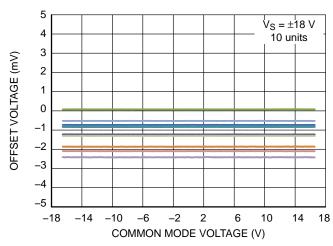


Figure 5. Input Offset Voltage vs. Common **Mode Voltage**

180

135

90

0 -45 DHASE

-90

-135

100M

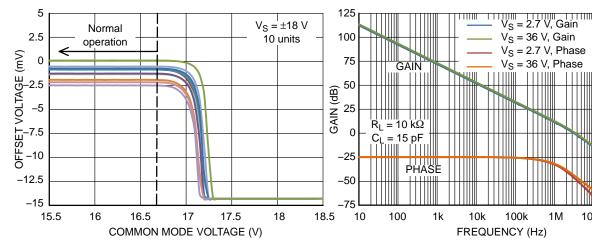


Figure 6. Input Offset Voltage vs. Common **Mode Voltage**

Figure 7. Gain and Phase vs. Frequency

1M

10M

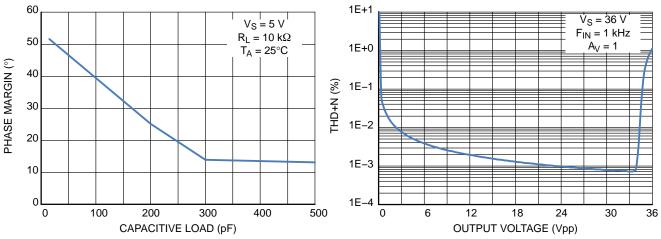


Figure 8. Phase Margin vs. Capacitive Load

Figure 9. THD+N vs. Output Voltage

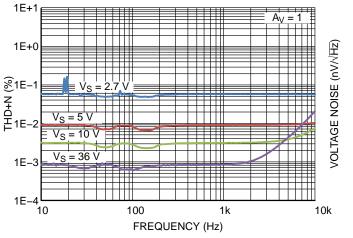


Figure 10. THD+N vs. Frequency

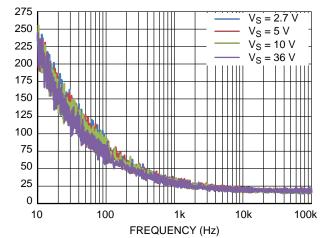


Figure 11. Input Voltage Noise vs. Frequency

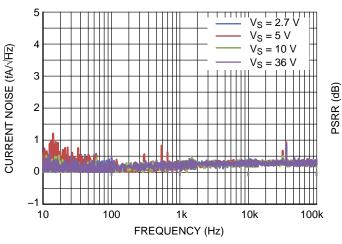


Figure 12. Input Current Noise vs. Frequency

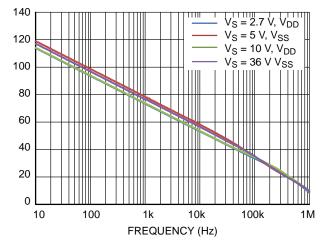
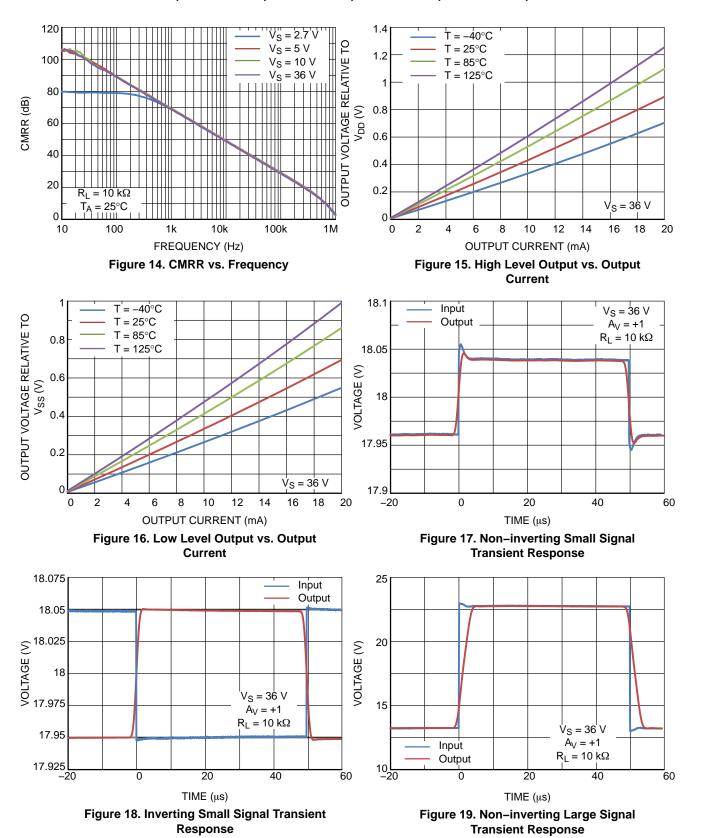


Figure 13. PSRR vs. Frequency



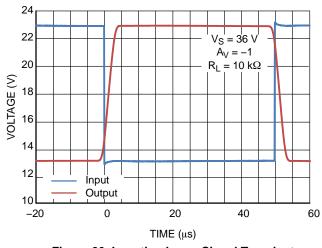


Figure 20. Inverting Large Signal Transient Response

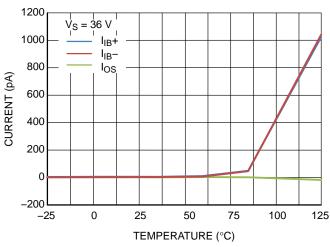


Figure 21. Input Bias and Offset Current vs.
Temperature

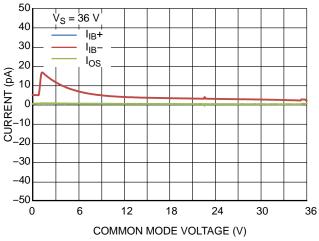


Figure 22. Input Bias Current vs. Common Mode Voltage

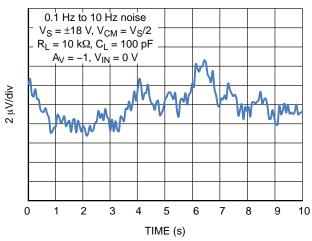


Figure 23. 0.1 Hz to 10 Hz Noise

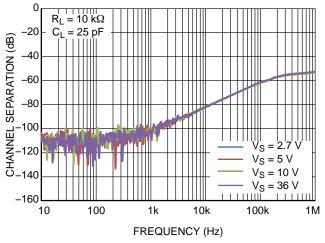


Figure 24. Channel Separation vs. Frequency

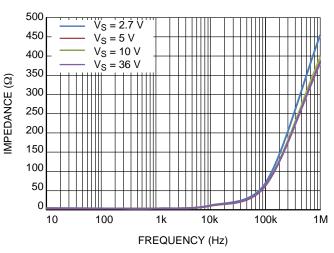
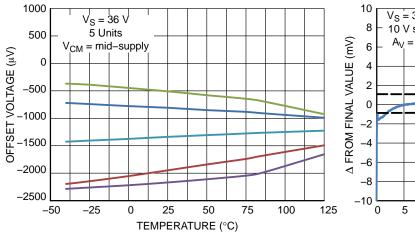


Figure 25. Open Loop Output Impedance



10 V_S = 36 V
8 10 V step
A_V = -1
12-bit Setting
12-bit Setting
12-bit Setting
12-bit Setting
12-bit Setting
12-bit Setting
13-bit Setting
14-color = 12-bit Setting
14-color = 12-bit Setting
15-color = 12-bit Setting
16-color = 12-bit Setting
17-color = 12-bit Setting
18-color = 12-bit Setting
18-color = 12-bit Setting
19-color = 12-bit Setting
19-co

Figure 26. Offset Voltage vs. Temperature

Figure 27. Large Signal Settling Time

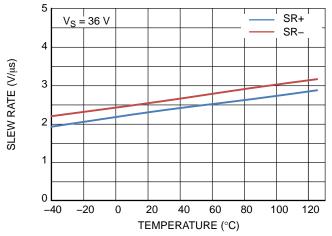
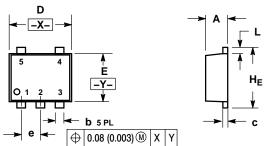


Figure 28. Slew Rate vs. Temperature

PACKAGE DIMENSIONS

SOT-553, 5 LEAD CASE 463B

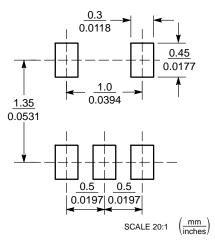
ISSUE C



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETERS
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH
 THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM
 THICKNESS. DIADET METER THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
С	0.08	0.13	0.18	0.003	0.005	0.007
D	1.55	1.60	1.65	0.061	0.063	0.065
E	1.15	1.20	1.25	0.045	0.047	0.049
е	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	1.55	1.60	1.65	0.061	0.063	0.065

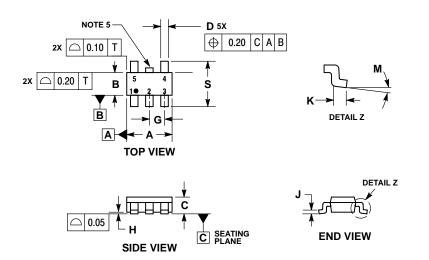
RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSOP-5 CASE 483-02 ISSUE K

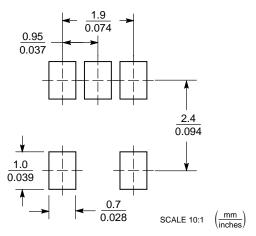


NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME
- Y14.5M, 1994. CONTROLLING DIMENSION: MILLIMETERS.
- 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
 4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
 5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS			
DIM	MIN	MAX		
Α	3.00	BSC		
В	1.50	BSC		
C	0.90	1.10		
D	0.25	0.50		
G	0.95 BSC			
Н	0.01	0.10		
J	0.10	0.26		
K	0.20	0.60		
М	0 °	10°		
S	2.50	3.00		

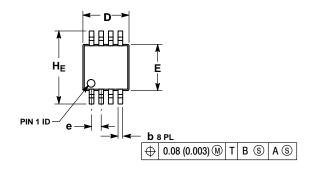
SOLDERING FOOTPRINT*

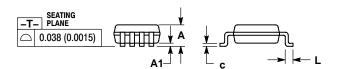


^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

Micro8™ CASE 846A-02 **ISSUE J**





- NOTES:

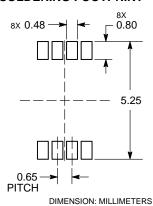
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE 3. DIMENSION A DUES NOT INCLUDE MOLLO FLASH, PHOTHOSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.06) PER SIDE.

 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

 5. 846A-01 OBSOLETE, NEW STANDARD 846A-02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α			1.10		-	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
С	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
е	0.65 BSC				0.026 BSC)
L	0.40	0.55	0.70	0.016	0.021	0.028
HE	4.75	4.90	5.05	0.187	0.193	0.199

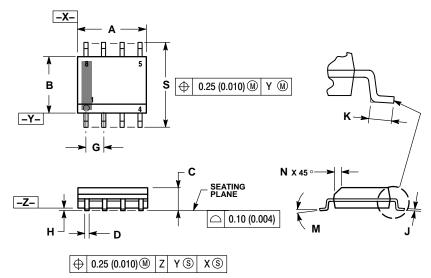
RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOIC-8 NB CASE 751-07 **ISSUE AK**

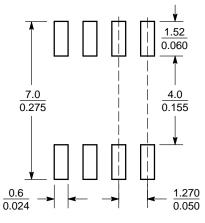


- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE

- MOLD PROTRUSION.
 MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.127 (0.005) TOTAL
 IN EXCESS OF THE D DIMENSION AT
 MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW
- STANDARD IS 751-07.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	4.80	5.00	0.189	0.197	
В	3.80	4.00	0.150	0.157	
C	1.35	1.75	0.053	0.069	
D	0.33	0.51	0.013	0.020	
G	1.27 BSC		0.050 BSC		
Η	0.10	0.25	0.004	0.010	
J	0.19	0.25	0.007	0.010	
K	0.40	1.27	0.016	0.050	
М	0 °	8 °	0 °	8 °	
Ν	0.25	0.50	0.010	0.020	
S	5.80	6.20	0.228	0.244	

SOLDERING FOOTPRINT*

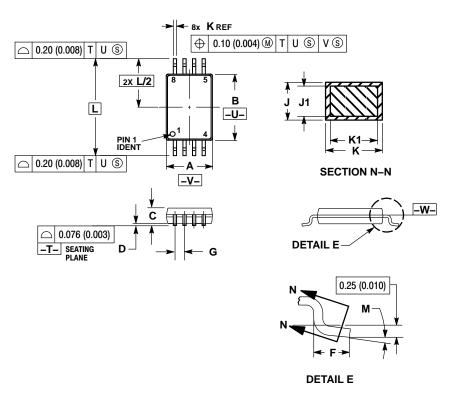


SCALE 6:1

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSSOP-8 **CASE 948S** ISSUE C



- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010)
- PER SIDE.

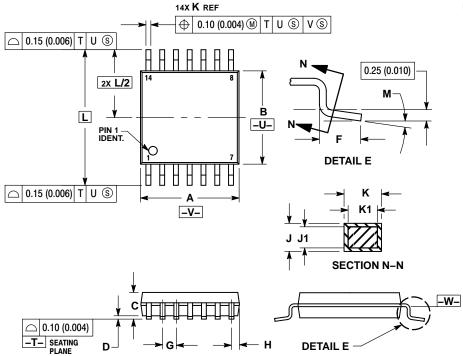
 5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

 6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W-.

	MILLIN	IETERS	INCHES	
DIM	MIN MAX		MIN	MAX
DIM				
Α	2.90	3.10	0.114	0.122
В	4.30	4.50	0.169	0.177
C		1.10		0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252	BSC
М	0°	8°	0°	8°

PACKAGE DIMENSIONS

TSSOP-14 CASE 948G ISSUE B



NOTES:

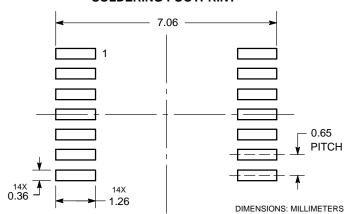
- DIMENSIONING AND TOLERANCING PER
 ANSI V14 5M 1982
- ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
- 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PEP SIDE
- EXCEED 0.15 (0.006) PER SIDE.

 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

 5. DIMENSION K DOES NOT INCLUDE DAMBAR
- DIMENSION K DOES NOT INCLUDE DAMBAI PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65 BSC		0.026 BSC		
Н	0.50	0.60	0.020	0.024	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
٦	6.40 BSC		0.252	BSC	
М	0 °	8 °	0 °	8 °	

SOLDERING FOOTPRINT*



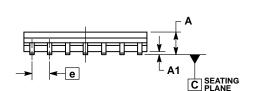
*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOIC-14 NB

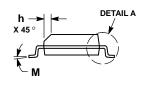
CASE 751A-03 ISSUE K В Н Н Н Н DETAIL A

⊕ 0.25 M C A S B S



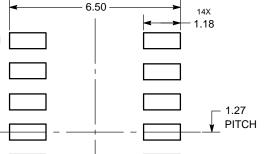
0.58

13X b



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
- 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
- 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
 5. MAXIMUM MOLD PROTRUSION 0.15 PER

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	1.35	1.75	0.054	0.068	
A1	0.10	0.25	0.004	0.010	
A3	0.19	0.25	0.008	0.010	
b	0.35	0.49	0.014	0.019	
D	8.55	8.75	0.337	0.344	
Е	3.80	4.00	0.150	0.157	
е	1.27 BSC		0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.019	
L	0.40	1.25	0.016	0.049	
М	0 °	7 °	0 °	7 °	



SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and the (III) are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT

| ⊕ | 0.25 (M | B (M

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA

Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

Europe, Middle East and Africa Technical Support: Phone: 421 33 790 2910 Japan Customer Focus Center

Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative