TLK10xL Industrial Temp, Single Port 10/100Mbs Ethernet Physical Layer Transceiver

1 Device Overview

1.1 Features

- Low-Power Consumption:
  - Single Supply: <205 mW PHY, 275 mW With Center Tap (Typical)
  - Dual Supplies: <126 mW PHY, 200 mW With Center Tap (Typical)
- Programmable Power Back Off to Reduce PHY Power up to 20% in Systems With Shorter Cables
- IEEE 1588 SFD Indication Enables Time Stamping by a Controller or Processor
- Low Deterministic Latency Supports IEEE1588 Implementation
- Cable Diagnostics
- Programmable Fast Link Down Modes, <10 µs Reaction Time
- Variable I/O voltage range: 3.3V, 2.5V, 1.8V
- MAC Interface I/O voltage range:
  - MII I/O voltage range: 3.3V, 2.5V, 1.8V
  - RMII I/O voltage range: 3.3V, 2.5V
- Fixed TX Clock to XI, With Programmable Phase Shift
- Auto-MDIX for 10/100Mbs
- Energy Detection Mode
- MII and RMII Capabilities
- IEEE 802.3u MII
- Error-Free 100Base-T Operation up to 150 Meters Under Typical Conditions
- Error-Free 10Base-T Operation up to 300 Meters Under Typical Conditions
- Serial Management Interface
- IEEE 802.3u Auto-Negotiation and Parallel Detection
- IEEE 802.3u ENDEC, 10Base-T Transceivers and Filters
- IEEE 802.3u PCS, 100Base-TX Transceivers
- Integrated ANSI X3.263 Compliant TP-PMD Physical Sublayer with Adaptive Equalization and Baseline Wander Compensation
- Programmable LED Support Link, Activity
- 10/100Mbs Packet BIST (Built in Self Test)
- HBM ESD Protection on RD± and TD± of 16 kV
- 32-pin VQFN (5 mm) × (5 mm)

1.2 Applications

- Industrial Networks and Factory Automation
- Motor and Motion Control
- General Embedded Applications

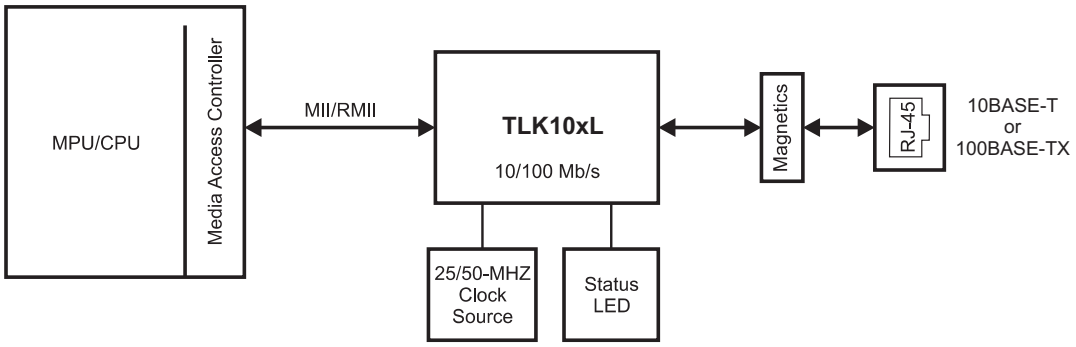
1.3 Description

The TLK10xL is a single-port Ethernet PHY for 10Base-T and 100Base TX signaling, integrating all the physical-layer functions needed to transmit and receive data on standard twisted-pair cables.
The device supports the standard Media Independent Interface (MII) and Reduced Media Independent Interface (RMII) for direct connection to a Media Access Controller (MAC).

The device is designed for power-supply flexibility, and can operate with a single 3.3-V power supply or with combinations of 3.3-V and 1.55-V power supplies for reduced power operation.

The TLK10xL uses mixed-signal processing to perform equalization, data recovery, and error correction to achieve robust operation over CAT 5 twisted-pair wiring. The TLK10xL not only meets the requirements of IEEE 802.3, but maintains high margins in terms of cross-talk and alien noise.

The TLK10xL Ethernet PHY has a special Power Back Off mode to conserve power in systems with relatively short cables. This mode provides the flexibility to reduce system power when the system is not required to drive the standard IEEE 802.3 100-m cable length, or the extended 150m, error-free cable reach of the TLK10xL. For more detail, see application note SLLA328.



Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
TLK10xL	VQFN (32)	5.00 mm × 5.00 mm

(1) For more information, see Section 8, *Mechanical Packaging and Orderable Information*.

1.4 Functional Block Diagram

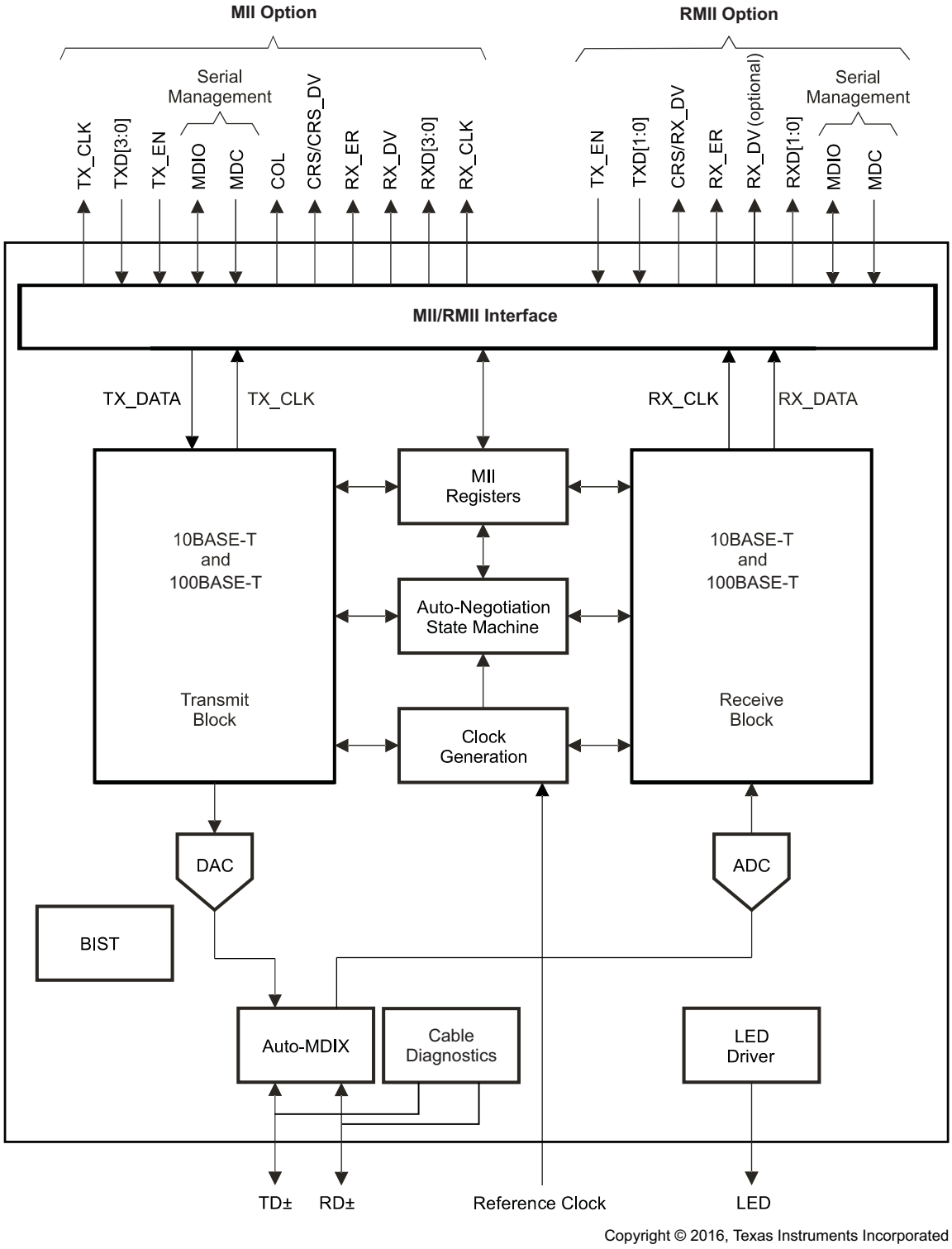


Figure 1-1. TLK10xL Functional Block Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (November 2014) to Revision D **Page**

- Changed description of I/O Voltage Range and MAC interfaces to clarify voltages. 1
- Changed QFN to VQFN 1
- Added package information 1
- Added note for oscillator voltage levels 10
- Changed and test conditions of t_2 16
- Added timing parameter for XI clock stability after power up. 16
- Deleted CLK25MHz_OUT 24
- Added note on impact of enabling Enhanced LED link on link blinking 26
- Changed format of table header. 34
- Added note that the default transmit link pulse polarity is reversed 38
- Changed Register Block to Register Maps 41
- Added Compliance Test register. 42
- Changed format of Register Table header row. 43
- Changed format of Register Table header row. 44
- Changed VRCR bits 3:0 to RESERVED. 45
- Added note that enabling Enhanced LED Link overrides the LED blinking functionality of PHYCR register bit 5 57
- Changed default to inverted polarity 58
- Added text in MLEDCR clarifying polarity of LED. 71
- Added Compliance Test register, address 0x0027 72
- Changed Power Back Off Levels 73
- Changed VRCR bits 3:0 to RESERVED 74
- Deleted partial list of recommended transformers 90
- Changed recommendation for common mode chokes to requirement. 90
- Deleted the amplitude of the oscillator should be a nominal voltage of 3.3V. 90
- Added notes on oscillator supply voltage. 90

Changes from Revision B (January 2014) to Revision C **Page**

- Deleted "(TLK106)" 1
- Deleted "IEEE 802.3u 100BASE-FX Fiber Interface" 1
- Deleted "Additionally, the TLK10xL supports 100Base-FX signaling via an external optical transceiver." 1
- Added note for oscillator voltage levels 10
- Deleted "SD_IN" 10
- Updated Handling Ratings to ESD Ratings and moved Storage temperature to Absolute Maximum Ratings 12
- Added parameters for dual-supply operation 12
- Deleted Redundant row "Power dissipation 200 mW" 12
- Changed Thermal Table format 13
- Deleted DC Characteristics, SD_IN 14
- V_{TH1} - max value deleted, 200-mV typ value added 14
- Added timing parameter for XI clock stability after power up. 16
- Deleted FX Timing 16
- Changed format of table header. 34
- Added note that the default transmit link pulse polarity is reversed 38
- Deleted FIBCR Register 42
- Deleted Fiber Mode Control 2 and Fiber Mode Control 3 42
- Deleted Fiber Mode Control 43
- Deleted Fiber Mode Control Register, Fiber Mode Control 2 and Fiber Mode Control 3 45
- Changed Speed Selection register bit to RW 46
- Changed Auto-Negotiation Enable register bit to RW 46
- Added Reserved bits 57
- Deleted Bit[14] Fiber Mode Control 57
- Added note that enabling Enhanced LED Link overrides the LED blinking functionality of PHYCR register bit 5 57
- Changed default to inverted polarity 58
- Changed "Active WOL" to "Active Energy Saving" 62
- Changed "Passive WOL" to "Passive Energy Saving" 62
- Changed "1" to "0" 71
- Added Compliance Test register, address 0x0027 72
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- Changed Power Back Off Levels 73
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- Deleted Fiber Mode Control Register 2 (FIBCR2) 74
- Deleted Fiber Mode Control Register 3 (FIBCR3) 74
- Changed "the same levels as the MII interface" to "operates at 3.3-V or 2.5-V VDD_IO levels" 81
- Changed "WOL (Wake-On LAN)" to "Energy Saving" 89
- Changed "WOL (Wake-On LAN)" to "Energy Saving" 89
- Deleted partial list of recommended transformers 90
- Changed recommendation for common mode chokes to requirement. 90
- Deleted the amplitude of the oscillator should be a nominal voltage of 3.3V. 90
- Added notes on oscillator supply voltage. 90

Changes from Revision A (November 2013) to Revision B **Page**

- Changed "Low Power Consumption: <205mW PHY and 275mW with Center Tap (Typical)" to "Low Power Consumption: <126mW PHY and 200mW with Center Tap (Typical, dual supplies)" 1
- Changed "MII and RMII Interfaces" to "MII and RMII Capabilities" 1
- Changed "Error-Free Operation up to 150 Meters Under Typical Conditions" to "Error-Free 100Base-T Operation up to 150 Meters Under Typical Conditions Error-Free 10Base-T Operation up to 300 Meters Under Typical Conditions" 1
- Added operating conditions for single and dual supplies 12
- Changed title from "Active Power" to "Active Power, Single Supply Operation" 15
- Added Dual Supply Operation table 15
- Added bit 10, Fast Link Down Mode enable, Drop the link based on descrambler link loss, adusted description of bits 3:0 to reflect 5 options instead of 4 58
- Deleted " Allow the system to reset the PHY using register access." 71
- Changed recommended transformer from Pulse HX1188 to Pulse HX1198 90

Changes from Original (August 2013) to Revision A **Page**

- Updated Pin Layout, changed "VDD33_IO" to "VDD_IO" 7
- Added maximum storage temperature 12
- Changed "... stable for minimum of 1ms ..." to "... stable for minimum of 1µs ..." (typo correction) 16
- Changed titles, "100Base-TX ... Timing" to "100Base-TX / FX ... Timing" 16
- Added Power Back Off Control Register (0AEh) 41
- Registers 0010h - 001Fh moved from extended-addressing space to direct-addressing space 46
- Changed default value for MDL_REV from 0001 to 0010 49
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- Updated RMII Control and Status Register bit 4 description 66

3 Pin Configuration and Functions

The TLK10xL pins fall into the following interface categories (subsequent sections describe each interface):

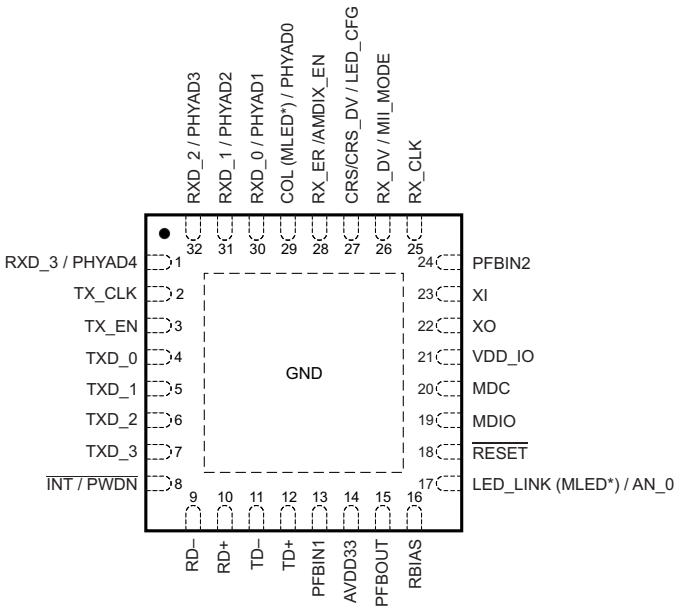
- Serial Management Interface
- MAC Data Interface
- Clock Interface
- LED Interface
- Reset and Power Down
- Bootstrap Configuration Inputs
- 10/100-Mbps PMD Interface
- Special Connect Pins
- Power and Ground pins

Note: Configuration pin option. See Section 5.1.1 for *Jumper Definitions*.

The definitions below define the functionality of each pin.

Type: I	Input	Type: OD	Open Drain
Type: O	Output	Type: PD, PU	Internal Pulldown/Pullup
Type: I/O	Input/Output	Type: S	Configuration Pin (All configuration pins have weak internal pullups or pulldowns. Use an external 2.2-kΩ resistor if you need a different default value. See Section 5.1.1 for details.)

3.1 Pin Diagram



* MLED can be routed via REG 0x0025 (MLEDCR Register), for further details see Section 5.1.8.

Figure 3-1. TLK10xL Pin Diagram, Top View

This document describes signals that take on different names depending on configuration. In such cases, the different names are placed together and separated by slash (/) characters. For example, "RXD_3 / PHYAD4". Active-low signals are represented by overbars.

3.2 Serial Management Interface (SMI)

PIN		TYPE	DESCRIPTION
NAME	NO.		
MDC	20	I	**MANAGEMENT DATA CLOCK:** Clock signal for the management data input/output (MDIO) interface. The maximum MDC rate is 25 MHz; there is no minimum MDC rate. MDC is **not** required to be synchronous to the TX_CLK or the RX_CLK.
MDIO	19	I/O	**MANAGEMENT DATA I/O:** Bidirectional command / data signal synchronized to MDC. Either the local controller or the TLK10xL may drive the MDIO signal. This pin requires a pullup resistor with value 2.2 kΩ.

3.3 MAC Data Interface

PIN		TYPE	DESCRIPTION
NAME	NO.		
COL (MLED)/ PHYAD0	29	S, O, PU	**COLLISION DETECT:** For MII mode in Full Duplex Mode this pin is always low. In 10Base-T and 100Base-TX half-duplex modes, this pin is asserted HIGH only when both transmit and receive media are non-idle. This pin is not used in RMII mode. **MLED:** The Multi LED can be routed to this pin via REG 0x0025 (MLEDCR Register), for further details see Section 5.1.8.
CRS / CRS_DV/ LED_CFG	27	S, O, PU	**CARRIER SENSE:** In MII mode this pin is asserted high when the receive medium is non-idle. **CARRIER SENSE/RECEIVE DATA VALID:** In RMII mode, this pin combines the RMII Carrier and Receive Data Valid indications.
RX_CLK	25	O	**RECEIVE CLOCK:** In MII mode it is the receive clock that provides either a 25-MHz or 2.5-MHz reference clock, depending on the speed, that is derived from the received data stream.
RX_DV / MII_MODE	26	S, O, PD	**RECEIVE DATA VALID:** This pin indicates valid data is present on the RXD [3:0] for MII mode or on RXD [1:0] for RMII mode, independently from Carrier Sense.
RX_ER / AMDIX_EN	28	S, O, PU	**RECEIVE ERROR**: This pin indicates that an error symbol has been detected within a received packet in both MII and RMII mode. In MII mode, RX_ER is asserted high synchronously to RX_CLK and in RMII mode, synchronously to XI (50 MHz). This pin is not required to be used by the MAC, in either MII or RMII, because the PHY is corrupting data on a receive error.
RXD_0 / PHYAD1 RXD_1 / PHYAD2 RXD_2 / PHYAD3 RXD_3 / PHYAD4	30 31 32 1	S, O, PD	**RECEIVE DATA:** Symbols received on the cable are decoded and presented on these pins synchronous to RX_CLK. They contain valid data when RX_DV is asserted. A nibble RXD [3:0] is received in the MII mode and 2-bits RXD[1:0] is received in the RMII Mode. PHY address pins PHYAD[4:1] are multiplexed with RXD [3:0], and are pulled down. PHYAD0 (LSB of the address) is multiplexed with COL on pin 29, and is pulled up. If no external pullup or pulldown is present, the default address is 0x01.
TX_CLK	2	O, PD	**MII TRANSMIT CLOCK:** MII Transmit Clock provides the 25-MHz or 2.5-MHz reference clock depending on the speed. Note that in MII mode, this clock has constant phase referenced to REF_CLK. Applications requiring such constant phase may use this feature. Unused in RMII mode. In RMII, X1 reference clock is used as the clock for both transmit and receive.
TX_EN	3	I, PD	**TRANSMIT ENABLE:** TX_EN is presented on the rising edge of the TX_CLK . TX_EN indicates the presence of valid data inputs on TXD[3:0] in MII mode, and on TXD [1:0] in the RMII mode. TX_EN is an active high signal.
TXD_0 TXD_1 TXD_2 TXD_3	4 5 6 7	I, PD	**TRANSMIT DATA:** In MII mode, the transmit data nibble received from the MAC is synchronous to the rising edge of the TX_CLK signal. In RMII mode, TXD [1:0] received from the MAC is synchronous to the 50-MHz reference clock on XI.

3.4 10-Mbps and 100-Mbps PMD Interface

PIN		TYPE	DESCRIPTION
NAME	NO.		
RD–, RD+	9, 10	I/O	**Differential receive input (PMD Input Pair):** These differential inputs are automatically configured to accept either 100Base-TX or 10Base-T signaling. In Auto-MDIX mode of operation, this pair can be used as the Transmit Output pair. These pins require 3.3-V bias for operation.
TD–, TD+	11, 12	I/O	**Differential common driver transmit output (PMD Output Pair):** These differential outputs are automatically configured to either 10Base-T or 100Base-TX signaling. In Auto-MDIX mode of operation, this pair can be used as the Receive Input pair. These pins require 3.3-V bias for operation.

3.5 Clock Interface

PIN		TYPE	DESCRIPTION
NAME	NO.		
XI	23	I	**CRYSTAL/OSCILLATOR INPUT:** **MII reference clock:** Reference clock. 25-MHz ±50 ppm tolerance crystal reference or oscillator input. The device supports either an external crystal resonator connected across pins XI and XO. Note that external CMOS level oscillator must have the same voltage reference as the VDD_IO supply. **RMII reference clock:** Primary clock reference input for the RMII mode. When using an external CMOS-level oscillator, the oscillator must have the same voltage reference as the VDD_IO supply. RMII is not supported with a 1.8-V reference clock.
XO	22	O	**CRYSTAL OUTPUT:** Reference Clock output. XO pin is used for crystal only. This pin should be left floating when an oscillator input is connected to XI.

3.6 LED Interface

(See Table 5-4 and Table 5-5 for LED Mode Selection)

PIN		TYPE	DESCRIPTION	
NAME	NO.			
LED_LINK (MLED[1]) / AN_0	17	S, O, PU	**LED Pin** to indicate status	
			Mode 1	**LINK Indication LED**: Indicates the status of the link. When the link is good, the LED is ON.
			Mode 2	**ACT indication LED**: Indicates transmit and receive activity in addition to the status of the Link. The LED is ON when Link is good. The LED blinks when the transmitter or receiver is active.

(1) The Multi LED can be routed to this pin or to the COL (MLED) / PHYADD (pin 29) pin via REG 0x0025 (MLEDCR Register). For further details see Section 5.1.8.

3.7 Reset and Power Down

PIN		TYPE	DESCRIPTION
NAME	NO.		
$\overline{\text{INT}}$ / $\overline{\text{PWDN}}$	8	IO, OD, PU	Register access is required for this pin to be configured either as power down or as an interrupt. The default function of this pin is power down. When this pin is configured for a power-down function, an active low signal on this pin places the device in power-down mode. When this pin is configured as an interrupt pin, then this pin is asserted low when an interrupt condition occurs. The pin has an open-drain output with a weak internal pullup. Some applications may require an external pullup resistor.
$\overline{\text{RESET}}$	18	I, PU	This pin is an active-low reset input that initializes or reinitializes all the internal registers of the TLK10xL. Asserting this pin low for at least 1 µs forces a reset process to occur. All jumper options are reinitialized as well.

3.8 Power and Bias Connections

PIN		TYPE	DESCRIPTION
NAME	NO.		
AVDD33	14	P	Analog 3.3-V power supply
GND	Ground Pad	P	Ground Pad
IOGND	35, 47	P	I/O ground

PIN		TYPE	DESCRIPTION
NAME	NO.		
PFBIN1 PFBIN2	13 24	I	**Power Feedback Input**: These pins are fed with power from PFBOUT (pin 15) in single-supply operation. In multiple-supply operation, connect a 1.55-V external power supply to these pins. Connect a small capacitor of 0.1 µF close to each pin. To power down the internal linear regulator, write to register 0x00d0.
PFBOUT	15	O	**Power Feedback Output**: Place 10-µf and 0.1-µF capacitors (ceramic preferred) close to PFBOUT. In single-supply operation, connect this pin to PFBIN1 and PFBIN2 (pin 13 and pin 24). See Figure 5-1 for proper placement. In multiple-supply operation, this pin is not used.
RBIAS	16	I	**Bias Resistor Connection**: Use a 4.87-kΩ 1% resistor connected from RBIAS to GND.
VDD_IO	21	P	I/O 3.3-V, 2.5-V, or 1.8-V Supply - For details, see Section 5.1.2.3

4 Specifications

All parameters are derived by test, statistical analysis, or design.

4.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
VDD_IO, AVDD33	Supply voltage	–0.3	3.8	V
PFBIN1, PFBIN2		–0.3	1.8	
XI	DC Input voltage	–0.3	3.8	V
TD-, TD+, RD-, RD+		–0.3	6	
Other Inputs		–0.3	3.8	
XO	DC Output voltage	–0.3	3.8	V
Other outputs		–0.3	3.8	
T_J	Maximum die temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge (ESD) performance:	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS001(1)	All pins except 13, 14, 16, and 17(2)	±4000	V
			Pins 13, 14, 16, and 17(3)	±16000	
		Charged Device Model (CDM), per JESD22-C101(4)	All pins(5)	±750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Tested in accordance to JEDEC Standard 22, Test Method A114.
(3) Test method based upon JEDEC Standard 22 Test Method A114, Ethernet network pins (TD+, TD–, RD+, RD–) pins stressed with respect to GND.
(4) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(5) Tested in accordance to JEDEC Standard 22, Test Method C101.

4.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
DUAL-SUPPLY OPERATION						
	Core supply voltage (PFBIN1, PFBIN2)		1.48	1.55	1.68	V
P_D	Power dissipation(1)			200		mW
SINGLE-SUPPLY OPERATION						
	(PFBOUT connected to PFBIN1, PFBIN2, see Figure 5-1)					
P_D	Power dissipation(2)			270		mW
AVDD33	Analog 3.3-V supply		3	3.3	3.6	V
VDD_IO	3.3-V option		3	3.3	3.6	V
	2.5-V option		2.25	2.5	2.75	
	1.8-V option (MII mode only)		1.62	1.8	1.98	
T_A	Ambient temperature	TLK105L	–40		85	°C
		TLK106L	–40		105	

(1) For 100Base-TX
(2) For 100Base-TX, When internal 1.55 V is used. Device is operated from single 3.3-V supply only.

4.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC[1]		TLK105L, TLK106L RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

4.5 Thermal Information

over operating free-air temperature range (unless otherwise noted)

4.6 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC[1]		TLK105L, TLK106L RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (no airflow), JEDEC high-K model	36.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

4.7 DC Electrical Characteristics: VDD_IO

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
3.3-V VDD_IO							
V_{IH}	Input high voltage	Nominal VCC = 3.3 V	VDD_IO = 3.3 V ±10%	2			V
V_{IL}	Input low voltage		VDD_IO = 3.3 V ±10%			0.8	V
V_{OL}	Output low voltage	I_{OL} = 4 mA	VDD_IO = 3.3 V ±10%			0.4	V
V_{OH}	Output high voltage	I_{OH} = –4 mA	VDD_IO = 3.3 V ±10%	VDD_IO – 0.5			V
2.5-V VDD_IO							
V_{IH}	Input high voltage		VDD_IO = 2.5 V ±10%	1.5			V
V_{IL}	Input low voltage		VDD_IO = 2.5 V ±10%			0.5	V
V_{OL}	Output low voltage	I_{OL} = 2 mA	VDD_IO = 2.5 V ±10%			0.4	V
V_{OH}	Output high voltage	I_{OH} = –2 mA	VDD_IO = 2.5 V ±10%	VDD_IO – 0.4			V
1.8-V VDD_IO							
V_{IH}	Input high voltage		VDD_IO = 1.8 V ±10%	1.3			V
V_{IL}	Input low voltage		VDD_IO = 1.8 V ±10%			0.45	V
V_{OL}	Output low voltage	I_{OL} = 2 mA	VDD_IO = 1.8 V ±10%			0.4	V
V_{OH}	Output high voltage	I_{OH} = –2 mA	VDD_IO = 1.8 V ±10%	VDD_IO – 0.4			V

4.8 DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	Input high current	$V_{IN} = V_{CC}$			10	µA
I_{IL}	Input low current	V_{IN} = GND			10	µA
I_{OZ}	3-State leakage	$V_{OUT} = V_{CC}$, V_{OUT} = GND			±10	µA
R_{PULLUP}	Integrated pullup resistance		14.7	23.7	49.7	kΩ
$R_{PULLDOWN}$	Integrated pulldown resistance		14.5	24.9	48.1	kΩ
V_{TPTD_100}	100M transmit voltage		0.95	1	1.05	V
$V_{TPTDsym}$	100M transmit voltage symmetry				±2%	
V_{TPTD_10}	10M transmit voltage		2.2	2.5	2.8	V
C_{IN1}	CMOS input capacitance			5		pF
C_{OUT1}	CMOS output capacitance			5		pF
V_{TH1}	10Base-T Receive threshold			200		mV

4.9 Power Supply Characteristics

The data was measured using a TLK10xL evaluation board. The current from each of the power supplies is measured and the power dissipation is computed. For the single 3.3-V external supply case the power dissipation across the internal linear regulator is also included. All the power dissipation numbers are measured at the nominal power supply and typical temperature of 25°C. The power needed is given both for the device only, and including the center tap of the transformer for a total system power requirement. The center tap of the transformer is normally connected to the 3.3-V supply, thus the current needed may also be easily calculated.

4.9.1 Active Power, Single-Supply Operation

PARAMETER	TEST CONDITIONS	FROM POWER PINS	FROM TRANSFORMER CENTER TAP	UNIT
100Base-TX /W traffic (full packet 1518B rate)	Single 3.3-V external supply	203	73	mW
10Base-T /W traffic (full packet 1518B rate)		96	211	mW

4.9.2 Active Power, Dual-Supply Operation

PARAMETER	TEST CONDITIONS	FROM 3.3-V POWER	FROM 1.55-V PFBIN1, PFBIN2	FROM TRANSFORMER CENTER TAP	UNIT
100Base-TX /W traffic (full packet 1518B rate)	Dual external supplies, 3.3 V and 1.55 V	53	73	73	mW
10Base-T /W traffic (full packet 1518B rate)		23	35	212	mW

4.9.3 Power-Down Power

PARAMETER	TEST CONDITIONS(1)	FROM 3.3-V POWER	FROM 1.55-V PFBIN1, PFBIN2	FROM TRANSFORMER CENTER TAP	UNIT
IEEE PWDN	Single 3.3-V external supply	12	–	5	mW
Passive sleep mode		71	–	5	mW
Active sleep mode		71	–	5	mW
IEEE PWDN	Dual external supplies, 3.3 V and 1.55 V	12	0	5	mW
Passive sleep mode		21	23	5	mW
Active sleep mode		21	23	5	mW

(1) Measured under typical conditions.

4.10 AC Specifications

4.10.1 Power-Up Timing

See [(1)].

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Time from power up to hardware-configuration pin transition to output-driver function, using internal POR ($\overline{\text{RESET}}$ pin tied high)		100	270		ms
t_2	XI clock initialization	XI Clock must be stable for minimum of 1 µs prior to VDD ramp.	1			µs

(1) NOTE: It is important to choose pullup or pulldown resistors for each of the hardware configuration pins that provide fast RC time constants to latch in the proper value prior to the pin transitioning to an output driver.

4.10.2 Reset Timing

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	RESET pulse width	XI Clock must be stable for minimum of 1 µs during RESET pulse low time.	1			µs

4.10.3 MII Serial Management Timing

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	MDC frequency			2.5	25	MHz
t_2	MDC to MDIO (output) delay time		0		30	ns
t_3	MDIO (input) to MDC hold time		10			ns
t_4	MDIO (input) to MDC setup time		10			ns

4.10.4 100-Mbps MII Transmit Timing

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	TX_CLK high time	100-Mbps normal mode	16	20	24	ns
t_2	TX_CLK low time					
t_3	TXD[3:0], TX_EN data setup to TX_CLK	100-Mbps normal mode	10			ns
t_4	TXD[3:0], TX_EN data hold from TX_CLK	100-Mbps normal mode	0			ns

4.10.5 100-Mbps MII Receive Timing

See .

PARAMETER[(1)]		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	RX_CLK high time	100-Mbps normal mode	16	20	24	ns
t_2	RX_CLK low time					
t_3	RX_CLK to RXD[3:0], RX_DV, RX_ER delay	100-Mbps normal mode	10		30	ns

(1) RX_CLK may be held low or high for a longer period of time during transition between reference and recovered clocks. Minimum high and low times will not be violated.

4.10.6 100Base-TX Transmit Packet Latency Timing

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	TX_CLK to PMD output pair latency	100-Mbps normal mode[(1)]		4.8		bits[(2)]

(1) For normal mode, latency is determined by measuring the time from the first rising edge of TX_CLK occurring after the assertion of TX_EN to the first bit of the 'J' code group as output from the PMD Output Pair. 1 bit time = 10 ns in 100-Mbps mode.
(2) 1 bit time is equal 10 nS in 100-Mbps mode.

4.10.7 100Base-TX Transmit Packet Deassertion Timing

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	TX_CLK to PMD output pair deassertion	100-Mbps normal mode		4.6		bits

4.10.8 100Base-TX Transmit Timing ($t_{R/F}$ and Jitter)

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	100-Mbps PMD output pair t_R and t_F (1)		3	4	5	ns
	100-Mbps t_R and t_F mismatch (2)				500	ps
t_2	100-Mbps PMD output pair transmit jitter				1.4	ns

(1) Rise and fall times taken at 10% and 90% of the +1 or –1 amplitude.
(2) Normal Mismatch is the difference between the maximum and minimum of all rise and fall times.

4.10.9 100Base-TX Receive Packet Latency Timing

See .

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT(2)
t_1	Carrier sense ON delay(3)	100-Mbps normal mode		14		bits
t_2	Receive data latency	100-Mbps normal mode		19		bits
t_2	Receive data latency(4)	100-Mbps normal mode with fast RXDV detection ON		15		bits

(1) PMD Input Pair voltage amplitude is greater than the Signal Detect Turnon Threshold Value.
(2) 1 bit time = 10 ns in 100-Mbps mode
(3) Carrier Sense On Delay is determined by measuring the time from the first bit of the “J” code group to the assertion of Carrier Sense.
(4) Fast RXDV detection could be enabled by setting bit[1] of CR1 (address 0x0009).

4.10.10 100Base-TX Receive Packet Deassertion Timing

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Carrier Sense OFF Delay(1)	100-Mbps normal mode		19		bits(2)

(1) Carrier Sense Off Delay is determined by measuring the time from the first bit of the “T” code group to the deassertion of Carrier Sense.
(2) 1 bit time = 10 ns in 100-Mbps mode

4.10.11 10-Mbps MII Transmit Timing

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	TX_CLK low time	10-Mbps MII mode	190	200	210	ns
t_2	TX_CLK high time					
t_3	TXD[3:0], TX_EN data setup to TX_CLK ↑	10-Mbps MII mode	25			ns
t_4	TXD[3:0], TX_EN data hold from TX_CLK ↑	10-Mbps MII mode	0			ns

4.10.12 10-Mbps MII Receive Timing

See .

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	RX_CLK high time		160	200	240	ns
t_2	RX_CLK low time					
t_3	RX_CLK rising edge delay from RXD[3:0], RX_DV valid	10-Mbps MII mode	100			ns
t_4	RX_CLK to RXD[3:0], RX_DV delay	10-Mbps MII mode	100			ns

(1) RX_CLK may be held low for a longer period of time during transition between reference and recovered clocks. Minimum high and low times will not be violated.

4.10.13 10Base-T Transmit Timing (Start of Packet)

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT(1)
t_1	Transmit output delay from the falling edge of TX_CLK	10-Mbps MII mode		5.8		bits

(1) (1) 1 bit time = 100 ns in 10 Mbps.

4.10.14 10Base-T Transmit Timing (End of Packet)

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	End of packet high time (with 0 ending bit)		250	310		ns
t_2	End of packet high time (with 1 ending bit)		250	310		ns

4.10.15 10Base-T Receive Timing (Start of Packet)

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Carrier sense turnon delay (PMD input pair to CRS)			550	1000	ns
t_2	RX_DV latency(1)			14		bits
t_3	Receive data latency	Measurement shown from SFD		14		bits

(1) 10Base-T RX_DV Latency is measured from first bit of decoded SFD on the wire to the assertion of RX_DV

4.10.16 10Base-T Receive Timing (End of Packet)

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Carrier sense turnoff delay			1.8		µs

4.10.17 10-Mbps Jabber Timing

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Jabber activation time	10-Mbps MII mode		100		ms
t_2	Jabber deactivation time			500		ms

4.10.18 10Base-T Normal Link Pulse Timing

See .

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Pulse period	10-Mbps MII mode		16		ms
t_2	Pulse width			100		ns

(1) Transmit timing

4.10.19 Auto-Negotiation Fast Link Pulse (FLP) Timing

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Clock pulse to clock pulse period			125		µs
t_2	Clock pulse to data pulse period	Data = 1		62		µs
t_3	Clock, data pulse width			114		ns
t_4	FLP burst to FLP burst period			16		ms
t_5	Burst width			2		ms

4.10.20 100Base-TX Signal Detect Timing

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	SD internal turnon time				100	µs
t_2	Internal turnoff time				200	µs

4.10.21 100-Mbps Loopback Timing

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	TX_EN to RX_DV loopback	100-Mbps external loopback	241	242	243	ns
		100-Mbps external loopback – fast RX_DV mode	201	202	203	
		100-Mbps analog loopback	232	233	234	
		100-Mbps PCS Input loopback	120	121	122	
		100-Mbps MII loopback	8	9	10	

4.10.22 10-Mbps Internal Loopback Timing

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	TX_EN to RX_DV loopback	10-Mbps internal loopback mode		1.7		µs

4.10.23 RMII Transmit Timing

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	XI clock period	50-MHz Reference Clock		20		ns
t_2	TXD[1:0] and TX_EN data setup to X1 rising		1.4			ns
t_3	TXD[1:0] and TX_EN data hold to X1 rising	VDD_IO = 3.3 V	2			ns
		VDD_IO = 2.5 V	4.9			
t_4	XI Clock to PMD output pair latency			12		bits

4.10.24 RMII Receive Timing

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	XI clock period	50-MHz Reference Clock		20		ns
t_2	RXD[1:0], CRS_DV, RX_DV and RX_ER output delay from XI rising		4	10.8	14	ns
t_3	CRS ON delay	From JK symbol on PMD receive pair to initial assertion of CRS_DV		17.6		bits
t_4	CRS OFF delay	From TR symbol on PMD receive pair to initial assertion of CRS_DV		26.2		bits
t_5	RXD[1:0] and RX_ER latency	From symbol on receive pair. * Elasticity buffer set to default value (01)		29.7		bits
t_6	RX_CLK clock period	50-MHz *recovered clock* while working in *RMII receive clock* mode		20		ns
t_7	RXD[1:0], CRS_DV, RX_DV and RX_ER output delay from RX_CLK rising	While working in *RMII receive clock* mode		3.8		ns

NOTE

1. Per the RMII Specification, output delays assume a 25-pF load.
2. CRS_DV is asserted asynchronously in order to minimize latency of control signals through the PHY. CRS_DV may toggle synchronously at the end of the packet to indicate CRS de-assertion.
3. RX_DV is synchronous to XI. While not part of the RMII specification, this signal is provided to simplify recovery of receive data.
4. *RMII receive clock* mode is not part of the RMII specification that allows synchronization of the MAC-PHY RX interface in RMII mode. Setting register 0x000A bit [0] is required to activate this mode.

4.10.25 Isolation Timing

See .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	From deassertion of S/W or H/W reset to transition from isolate to normal mode			71		ns

5 Detailed Description

5.1 Hardware Configuration

This section includes information on the various configuration options available with the TLK10xL. The configuration options described below include:

- Bootstrap Configuration
- Power Supply Configuration
- IO Pins Hi-Z State During Reset
- Auto-Negotiation
- Auto-MDIX
- MII Isolate mode
- PHY Address
- LED Interface
- Loopback Functionality
- BIST
- Cable Diagnostics

5.1.1 Bootstrap Configuration

Bootstrap configuration is a convenient way to configure the TLK10xL into specific modes of operation. Some of the functional pins are used as configuration inputs. The logic states of these pins are sampled during reset and are used to configure the device into specific modes of operation. Table 5-1 describes bootstrap configuration.

A 2.2-kΩ resistor is used for pulldown or pullup to change the default configuration. If the default option is desired, then there is no need for external pullup or pulldown resistors. Because these pins may have alternate functions after reset is deasserted, they must not be connected directly to VCC or GND.

Table 5-1. Strap Options

PIN		TYPE	
NAME	NO.		DESCRIPTION
PHYAD0 (COL) PHYAD1 (RXD_0) PHYAD2 (RXD_1) PHYAD3 (RXD_2) PHYAD4 (RXD_3)	29 30 31 32 1	S, O, PD / PU	**PHY Address [4:0]:** The TLK10xL provides five PHY address pins, the states of which are latched into an internal register at system hardware reset. The TLK10xL supports PHY Address values 0 (<00000>) through 31 (<11111>). PHYAD[4:1] pins have weak internal pull-down resistors, and PHYAD[0] has weak internal pull-up resistor, setting the default PHYAD if no external resistors are connected.
AN_0 (LED_LINK)	17	S, O, PU	**AN_0:** FD-HD config. FD = pull up. The default wake-up is auto negotiation enable 100BT.
LED_CFG (CRS)	27	S, O, PU	**LED Configuration:** This option selects the operation mode of the LED LINK pin. Default is Mode 1. All modes are also configurable via register access. See *PHY Control Register (PHYCR), Address 0x0019*.
AMDIX_EN (RX_ER)	28	S, O, PU	**Auto-MDIX Enable:** This option sets the Auto-MDIX mode. By default, it enables Auto-MDIX. An external pull-down resistor disables Auto-MDIX mode.
MII_MODE (RX_DV)	26	S, O, PD	**MII Mode Select:** This option selects the operating mode of the MAC data interface. This pin has a weak internal pull-down, and it defaults to normal MII operation mode. An external pull-up causes the device to operate in RMII mode.

5.1.2 Power Supply Configuration

The TLK10xL provides best-in-class flexibility of power supplies.

5.1.2.1 Single-Supply Operation

If a single 3.3-V power supply is desired, the TLK10xL internal regulator provides the necessary core supply voltages. Ceramic capacitors of 10 µf and 0.1 µf must be placed close to the PFBOUT (pin 15) which is the output of the internal regulator. The PFBOUT pin must be connected to the PFBIN1 and PFBIN2 on the board. A small capacitor of 0.1 µF must be placed close to the PFBIN1 (pin 13) and PFBIN2 (pin 24). To operate in this mode, connect the TLK10xL supply pins as shown in Figure 5-1.

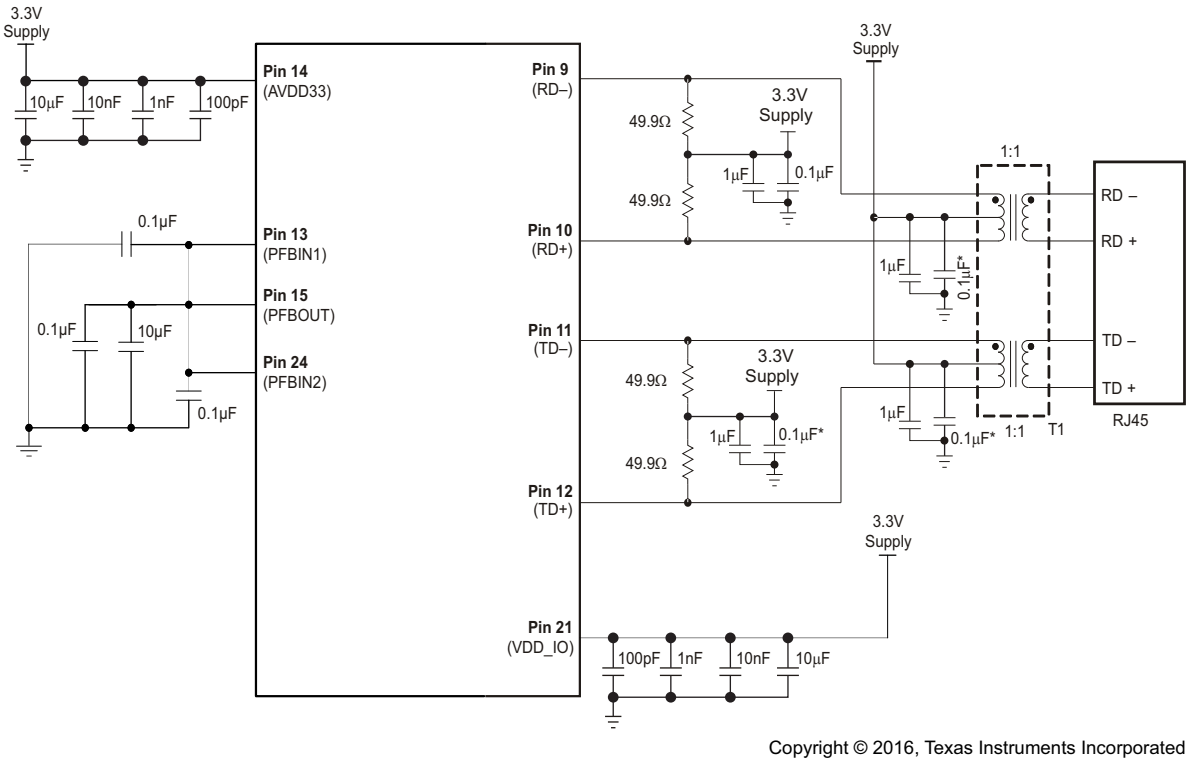


Figure 5-1. Power Connections for Single-Supply Operation

5.1.2.2 Dual-Supply Operation

When a 1.55-V external power rail is available, the TLK10xL can be configured as shown in Figure 5-2. PFBOUT (pin 15) is left floating. The 1.55-V external supply is connected to PFBIN1 (pin 13) and PFBIN2 (pin 24). Furthermore, to lower the power consumption, the internal regulator should be powered down by writing 1 to bit 15 of the VRCR register (0x00d0h).

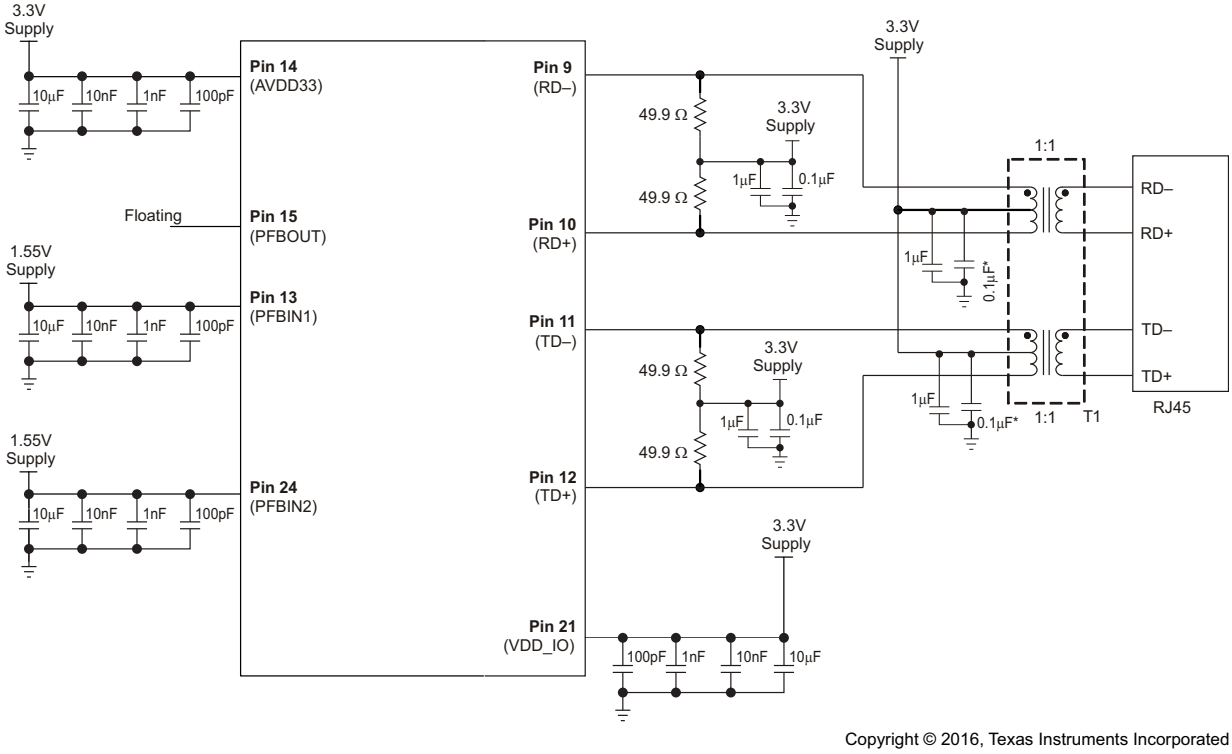


Figure 5-2. Power Connections for Dual-Supply Operation

When operating with dual supplies, follow these guidelines:

- When powering up, ramp up the 3.3-V supply before the 1.55-V supply.
- When powering down, turn off the 1.55-V supply before turning off the 3.3-V supply.
- Use the external $\overline{\text{RESET}}$ pin after power up to reset the PHY.
- To use the internal power-on-reset, PFBIN1 and PFBIN2 must be operational less than 100 ms after 3.3 V rises to detect the internal RESET.

5.1.2.3 Variable IO Voltage

The TLK10xL digital IO pins can operate with a variable supply voltage. While the primary applications use 3.3 V, VDD_IO can also operate on 2.5 V, and for MII mode only, VDD_IO of 1.8 V can be used as well. For more details, see Section 4.7.

5.1.3 IO Pins Hi-Z State During Reset

The following IO or output pins are in Hi-Z state when $\overline{\text{RESET}}$ is active (Low).

PIN NAME	TYPE	INTERNAL PU/PD	PIN NAME	TYPE	INTERNAL PU/PD
TXD_3	IO	PD	COL (MLED(1))	IO	PU
TX_EN	IO	PD	RXD_0	IO	PD
$\overline{\text{INT}}$/$\overline{\text{PWDN}}$	IO	PU	RXD_1	IO	PD
LED_LINK (MLED(1))	IO	PU	RXD_2	IO	PD
MDIO	IO		RXD_3	IO	PD
RX_DV	IO	PD	TX_CLK	O	
CRS	IO	PU	RX_CLK	O	
RX_ER	IO	PU			

(1) * MLED can be routed via REG 0x0025 (MLEDCR Register), for further details see Section 5.1.8.

5.1.4 Auto-Negotiation

The TLK10xL device auto-negotiates to operate in 10Base-T or 100Base-TX. With Auto-Negotiation enabled, the TLK10xL negotiates with the link partner to determine the speed and duplex mode. If the link partner cannot Auto-Negotiate, the TLK10xL device enters parallel-detect mode to determine the speed of the link partner. Parallel-detect mode uses fixed half-duplex mode.

The TLK10xL supports four different Ethernet protocols (10Mbs Half-Duplex, 10Mbs Full-Duplex, 100Mbs Half-Duplex, and 100Mbs Full-Duplex). Auto-Negotiation selects the highest performance protocol based on the advertised ability of the Link Partner. Control the Auto-Negotiation function within the TLK10xL by internal register access according to the IEEE specification.

Alternatively, control the HD-FD functionality by configuring the AN_0 pins. The state of AN_0 selects full or half duplex mode, both in Auto-Negotiation or force 100/10 mode as given in Table 5-2. The state of AN_0 upon power-up/reset, determines the state of bits [8:5] of the ANAR register (0x04h).

Auto-Negotiation advertises ANEN, 100BT by default. Full-Duplex or Half-Duplex configuration is available through the AN_0 bit. Internal register access configures the device for a specific mode.

Table 5-2. Auto-Negotiation Modes

AN_0	FORCED MODE
0	10Base-T, Half-Duplex 100Base-TX, Half-Duplex
1	10Base-T, Half or Full-Duplex 100Base-TX, Half or Full-Duplex

Internal register access controls the Auto-Negotiation function, as defined by the IEEE 802.3u specification. For further detail regarding Auto-Negotiation, see Clause 28 of the IEEE 802.3u specification.

5.1.5 Auto-MDIX

The TLK10xL device automatically determines whether or not it needs to cross over between pairs, eliminating the requirement for an external crossover cable. If the TLK10xL interoperates with a device that implements MDI/MDIX crossover, a random algorithm as described in IEEE 802.3 determines which device performs the crossover.

Auto-MDIX is enabled by default and can be configured through pin strap, control register CR1 (0x09h), bit 14 or via register PHYCR (0x19h), bit 15.

The crossover can be manually forced through bit 14 of the PHYCR (0x19h) register. Neither Auto-Negotiation nor Auto-MDIX is required to be enabled in forcing crossover of the MDI pairs.

Auto-MDIX can be used in the forced 100Base-TX mode. Because in modern networks all the nodes are 100Base-TX, having the Auto-MDIX working in the forced 100Base-TX mode resolves the link faster without the need for the long Auto-Negotiation period.

5.1.6 MII Isolate Mode

The TLK10xL can be put into MII-Isolate mode by writing bit 10 of the BMCR register.

When in the MII-Isolate mode, the TLK10xL ignores packet data present at the TXD[3:0], TX_EN inputs, and presents a high impedance on the TX_CLK, RX_CLK, RX_DV, RX_ER, RXD[3:0], COL, and CRS outputs. When in isolate mode, the TLK10xL continues to respond to all management transactions.

When in isolate mode, the PMD output pair does not transmit packet data, but continues to source 100Base-TX scrambled idles or 10Base-T normal link pulses. The TLK10xL can auto-negotiate or parallel detect on the receive signal at the PMD input pair. A valid link can be established for the receiver even when the TLK10xL is in Isolate mode.

5.1.7 PHY Address

The 5 PHY address inputs pins are shared with the RXD[3:0] pins and COL pin as shown in Table 5-3.

Table 5-3. PHY Address Mapping

PIN NUMBER	PHYAD FUNCTION	RXD FUNCTION
29	PHYAD0	COL
30	PHYAD1	RXD_0
31	PHYAD2	RXD_1
32	PHYAD3	RXD_2
1	PHYAD4	RXD_3

Each TLK10xL or port sharing an MDIO bus in a system must have a unique physical address. With 5 address input pins, the TLK10xL can support PHY Address values 0 (<00000>) through 31 (<11111>). The address-pin states are latched into an internal register at device power up and hardware reset. Because all the PHYAD[4:0] pins have weak internal pulldown or pullup resistors, the default setting for the PHY address is 00001 (0x01h).

See Figure 5-3 for an example of a PHYAD connection to external components. In this example, the PHYAD configuration results in address 00011 (0x03h).

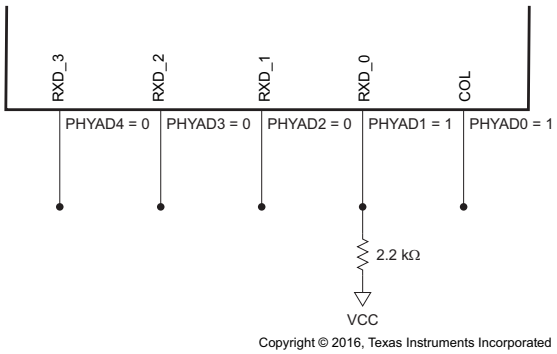


Figure 5-3. Illustrative PHYAD Configuration Example

5.1.8 LED Interface

By default, the TLK10xL supports one light emitting diode (LED) - LINK_LED, pin 17. In addition, the TLK10xL supports by register access a multi-configurable LED (MLED). The MLED is not activated by default, but by register access it can be routed through either pin 17 (allowing more configuration options for pin 17), or pin 29 supporting two simultaneous LEDs (LED_LINK on pin 17 & MLED on pin 29). When MLED is routed to the COL pin (pin 29) the COL functionality is disabled. REG 0x0025 (MLEDCR Register) controls the MLED routing and configurations. The different MLED modes are configured by bits [6:3] as described in Table 5-4.

Table 5-4. MLED Mode Select

(BIT 6:3)	MODE		(BIT 6:3)	MODE
0x0	Link OK		0x6	LED Speed: High for 10 Base TX
0x1	RX/TX Activity		0x7	Full Duplex
0x2	TX Activity		0x8	Link OK / Blink on TX/RX Activity
0x3	RX Activity		0x9	Active stretch signal
0x4	Collision		0xA	MI_LINK (100BT+FD)
0x5	LED Speed: High for 100 Base TX			

As mentioned before, by default the TLK10xL is pin compatible to the TLK105, and the default LED output is LED_LINk on pin 17. The LED can be controlled by configuration pin and internal register bits. Bit 5 of the PHY Control register (PHYCR) selects the LED mode as described in Table 5-5.

Table 5-5. LED Mode Select

MODE	LED_CFG[0] (BIT 5) or (PIN 27)	LED_LINK
1	1	ON for Good Link OFF for No Link
2	0	ON for Good Link BLINK for Activity

The LED_LINK pin in Mode 1 indicates the link status of the port. The LED is OFF when no link is present. In Mode 2 it is ON to indicate that the link is good; BLINK indicates that activity is present on either transmit or receive channel. Bits 10:9 of the LEDCR register (0x18) control the blink rate. The default blink rate is 5Hz. Enabling Enhanced LED Link via the CR2 register (0x0A) bit 4 overrides the LED blinking functionality of the PHYCR register (0x0019) bit 5. The Link LED will not blink for activity when Enhanced LED Link is enabled.

See Figure 5-4 for an example of AN0 connections to external components. In this example, the AN0 configuration results in Full-Duplex advertised.

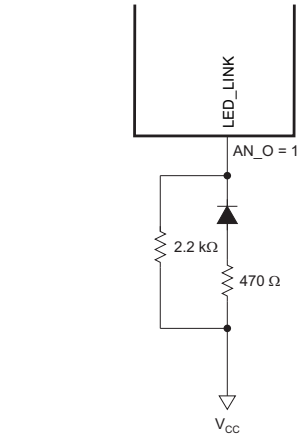


Figure 5-4. AN Pin Configuration and LED Loading Example

5.1.9 Loopback Functionality

The TLK10xL provides several options for Loopback that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the TLK10xL digital and analog data path. Generally, the TLK10xL may be configured to one of the Near-end loopback modes or to the Far-end (reverse) loopback.

5.1.9.1 Near-End Loopback

Near-end loopback provides the ability to loop the transmitted data back to the receiver through the digital or analog circuitry. The point at which the signal is looped back is selected using loopback control bits with several options being provided. Figure 5-5 shows the PHY Near-end loopback functionality.

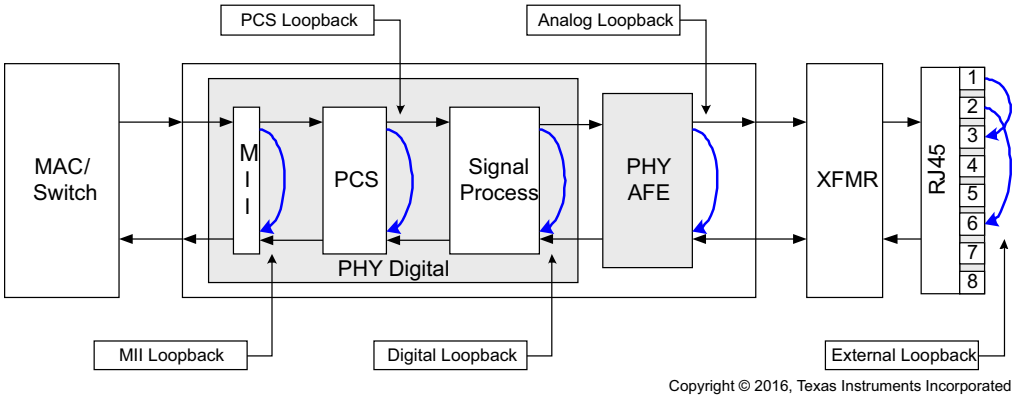


Figure 5-5. Block Diagram, Near-End Loopback Mode

The Near-end loopback mode is selected by setting the respective bit in the BIST Control Register (BISCR), MII register address 0x0016. MII loopback can be selected by using the BMCR register at address 0x0000, bit [14].

The Near-end Loopback can be selected according to the following:

- Reg 0x0000, Bit [14]: MII loopback
- Reg 0x0016, Bit [0]: PCS input loopback
- Reg 0x0016, Bit [1]: PCS output loopback
- Reg 0x0016, Bit [2]: Digital loopback
- Reg 0x0016, Bit [3]: Analog loopback

Table 5-6 describes the available operational modes for each loop mode:

Table 5-6. Loop Modes

LOOP MODE	MII	PCS INPUT	PCS OUTPUT	DIGITAL	ANALOG (1)	EXTERNAL
Operational Setting	Force/ANEG 100/10	Force 100/10	Force 100	Force 100	Force 10/100 ANEG 10	Force/ANEG 100/10
Operational MAC int.	MII Only	MII or RMII	MII or RMII	MII or RMII	MII or RMII	MII or RMII

(1) Requires 100-Ω termination

While in MII Loopback mode, there is no link indication, but packets propagate back to the MAC. While in MII Loopback mode the data is looped back, and can also be transmitted onto the media. For transmitting data during MII loopback in 100BT only please use bit [6] in the BISCR Register address 0x0016. For proper operation in analog loopback mode, attach 100-Ω terminations to the RJ45 connector. External loopback can be performed while working in normal mode (Bits 3:0 of the BISCR register are asserted to 0, and on the RJ45 connector, pin 1 is connected to pin 3 and pin 2 is connected to pin 6). To maintain the desired operating mode, Auto-Negotiation should be disabled before selecting loopback mode. This constraint does not apply for external-loopback mode. For selected loopback delay propagation timing, see Section 4.10.21.

5.1.9.2 Far-End Loopback

Far-end (Reverse) loopback is a special test mode to allow testing the PHY from the link-partner side. In this mode, data that is received from the link partner passes through the PHY's receiver, looped back on the MII and transmitted back to the link partner. Figure 5-6 shows Far-end loopback functionality.

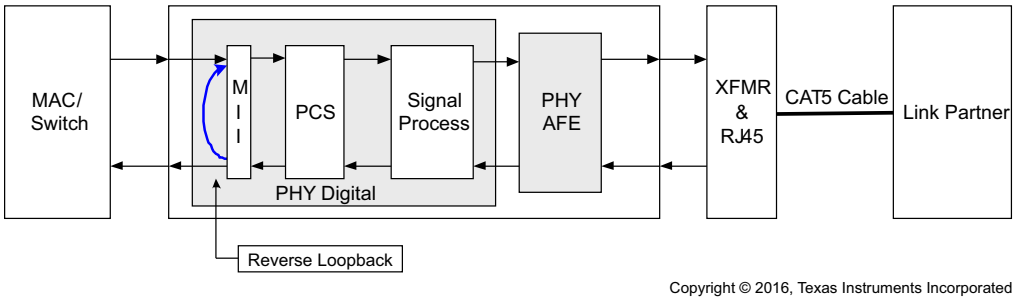


Figure 5-6. Block Diagram, Far-End Loopback Mode

The Reverse loopback mode is selected by setting bit 4 in the BIST Control Register (BISCR), MII register address 0x0016.

While in Reverse loopback mode the data is looped back and also transmitted onto the MAC Interface and all data signals that come from the MAC are ignored.

Table 5-7 describes the operating modes for Far-End loopback.

Table 5-7. Far-End Loopback Modes

OPERATIONAL MAC INT.	MII MODE	RMII MODE
Operational Setting	Force/ANEG 10/100	Force/ANEG 10

5.1.10 BIST

The device incorporates an internal PRBS Built-in Self Test (BIST) circuit to accommodate in-circuit testing or diagnostics. The BIST circuit can be used to test the integrity of the transmit and receive data paths. The BIST can be performed using both internal loopback (digital or analog) or external loopback using a cable fixture. The BIST simulates pseudo-random data transfer scenarios in format of real packets and Inter-Packet Gap (IPG) on the lines. The BIST allows full control of the packet lengths and of the IPG.

The BIST is implemented with independent transmit and receive paths, with the transmit block generating a continuous stream of a pseudo-random sequence. The device generates a 15-bit pseudo-random sequence for the BIST. The received data is compared to the generated pseudo-random data by the BIST Linear Feedback Shift Register (LFSR) to determine the BIST pass or fail status. The number of error bytes that the PRBS checker received is stored in the BICSR1 register (0x001Bh). The status of whether the PRBS checker is locked to the incoming receive bit stream, whether the PRBS has lost sync, and whether the packet generator is busy, can be read from the BISCR register (0x0016h). While the lock and sync indications are required to identify the beginning of proper data reception, for any link failures or data corruption, the best indication is the contents of the the error counter in the BICSR1 register (0x001Bh).

The PRBS test can be put in a continuous mode or single mode by using bit 14 of the BISCR register (0x0016h). In continuous mode, when one of the PRBS counters reaches the maximum value, the counter starts counting from zero again. In single mode, when the PRBS counter reaches its maximum value, the PRBS checker stops counting.

The device allows the user to control the length of the PRBS packet. By programming the BICSR2 register (0x001Ch), one can set the length of the PRBS packet. There is also an option to generate a single-packet transmission of two types, 64 and 1518 bytes, through register bit 13 of the BISCR register (0x0016h). The single generated packet is composed of a constant data.

5.1.11 Cable Diagnostics

With the vast deployment of Ethernet devices, the need for reliable, comprehensive, and user-friendly cable diagnostic tool is more important than ever. The wide variety of cables, topologies, and connectors deployed results in the need to non-intrusively identify and report cable faults. The TI cable-diagnostic unit provides extensive information about cable integrity.

The TLK10xL offers the following capabilities in its Cable Diagnostic tools kit:

1. Time Domain Reflectometry (TDR)
2. Active Link Cable Diagnostic (ALCD)

5.1.11.1 TDR

The TLK10xL uses Time Domain Reflectometry (TDR) to determine the quality of the cables, connectors, and terminations, in addition to estimating the cable length. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatches, cross faults, cross shorts, and any other discontinuities along the cable.

The TLK10xL transmits a test pulse of known amplitude (1 V or 2.5 V) down each of the two pairs of an attached cable. The transmitted signal continues down the cable and reflects from each cable imperfection, fault, bad connector, and from the end of the cable itself. After the pulse transmission the TLK10xL measures the return time and amplitude of all these reflected pulses. This technique enables measuring the distance and magnitude (impedance) of non-terminated cables (open or short), discontinuities (bad connectors), and improperly-terminated cables with ±1-m accuracy.

The TLK10xL also uses data averaging to reduce noise and improve accuracy. The TLK10xL can record up to five reflections within the tested pair. If more than 5 reflections are recorded, the TLK10xL saves the first 5 of them. If a cross fault is detected, the TDR saves the first location of the cross fault and up to 4 reflections in the tested channel. The TLK10xL TDR can measure cables up to 200 m in length.

For all TDR measurements, the transformation between time of arrival and physical distance is done by the external host using minor computations (such as multiplication, addition, and lookup tables). The host must know the expected propagation delay of the cable, which depends, among other things, on the cable category (for example, CAT5, CAT5e, or CAT6).

TDR measurement is allowed in the TLK10xL in the following scenarios:

- While Link partner is disconnected – cable is unplugged at the other side
- Link partner is connected but remains *quiet* (for example, in power-down mode)

- TDR could be automatically activated when the link fails or is dropped by setting bit 8 of register 0x0009 (CR1). The results of the TDR run after the link fails are saved in the TDR registers. The SW could read these registers at any time to apply post processing on the TDR results. This mode is designed for cases in which the link dropped due to cable disconnections, in which after link failure, the line is quiet to allow a proper function of the TDR.

5.1.11.2 ALCD

The TLK10xL also supports Active Link Cable Diagnostic (ALCD). The ALCD offers a passive method to estimate the cable length during active link. The ALCD uses passive digital signal processing based on adapted data, thus enabling measurement of cable length with an active link partner.

The ALCD Cable length measurement accuracy is ±5 m for the pair used in the Rx path (due to the passive nature of the test, only the receive path is measured).

5.2 Architecture

The TLK10xL Fast Ethernet transceiver is a physical layer core for Ethernet 100Base-TX and 10Base-T applications. The TLK10xL contains all the active circuitry required to implement the physical layer functions to transmit and receive data on standard CAT 3 and 5 unshielded twisted pair. The core supports the IEEE 802.3 Standard Fast Media Independent Interface (MII), as well as the Reduced Media Independent Interface (RMII), for direct connection to a MAC/Switch port.

The TLK10xL uses mixed signal processing to perform equalization, data recovery, and error correction to achieve robust and low power operation over the existing CAT 5 twisted pair wiring. The TLK10xL architecture not only meets the requirements of IEEE802.3, but maintains a high level of margin over the IEEE requirements for NEXT, Alien and External noise.

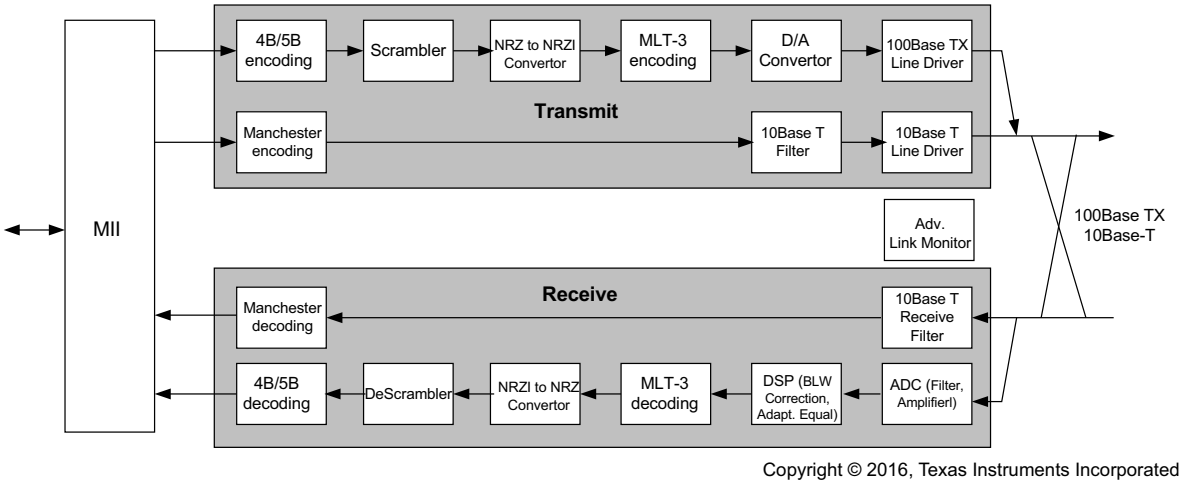


Figure 5-7. PHY Architecture

5.2.1 100Base-TX Transmit Path

In 100Base-TX, the MAC feeds the 100-Mbps transmit data in 4-bit wide nibbles through the MII interface. The data is encoded into 5-bit code groups, encapsulated with control code symbols and serialized. The control-code symbols indicate the start and end of the frame and code other information such as transmit errors. When no data is available from the MAC, IDLE symbols are constantly transmitted. The serialized bit stream is fed into a scrambler. The scrambled data stream passes through an NRZI encoder and then through an MLT3 encoder. Finally, it is fed to the DAC and transmitted through one of the twisted pairs of the cable.

5.2.1.1 MII Transmit Error Code Forwarding

According to IEEE 802.3:

> "If TX_EN is de-asserted on an odd nibble boundary, PHY should extend TX_EN by one TX_CLK cycle and behave as if TX_ER were asserted during that cycle".

The TLK10xL supports Error Forwarding in MII transmission from the MAC to the PHY. Error forwarding allows adding information to the frame to be used as an error code between the 2 MACs. The error code informs the receiving MAC on the link partner side of the reason for the error from the transmitting side. If the MAC transmits an odd number of nibbles, an additional error nibble is added to the transmitted frame just before the end of the transmission.

To turn off Transmit Error Forwarding, write to bit 1 of register CR2 (0x000A). If Error Forwarding is disabled, delivered packets contain either odd or even numbers of nibbles.

In Figure 5-8, Error Code Forwarding functionality is illustrated. The wave diagram demonstrates MAC's transmitted signals in one side and MAC's reception signals on link partner side.

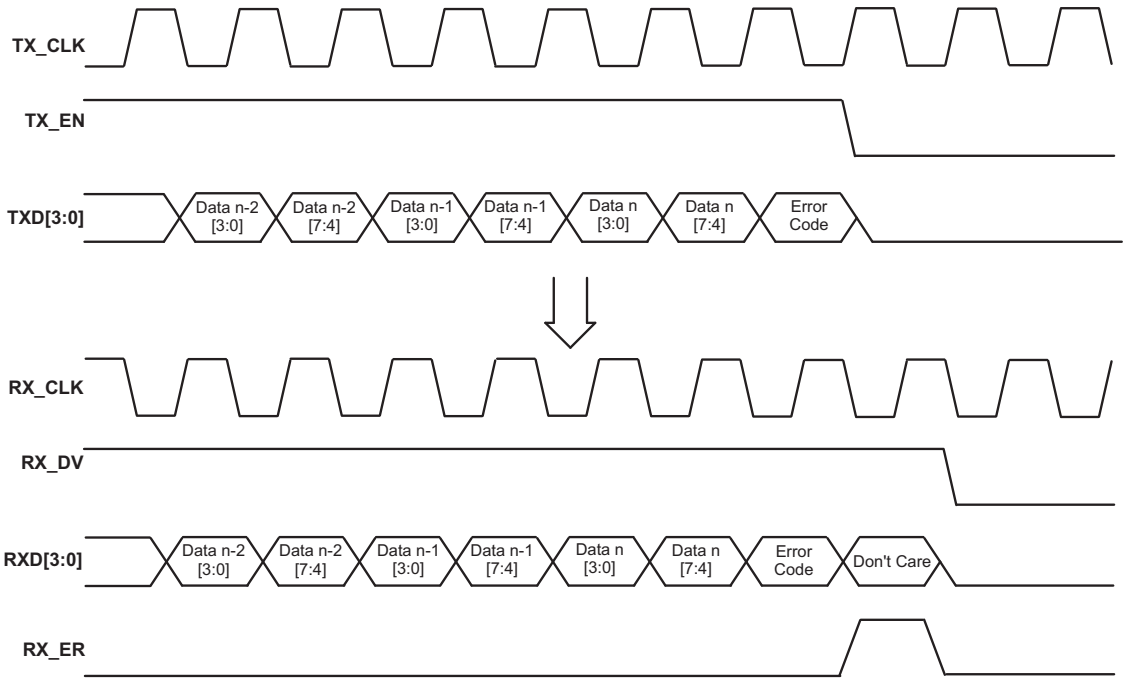


Figure 5-8. Transmit Code Error Forwarding Diagram

5.2.1.2 4-Bit to 5-Bit Encoding

The transmit data that is received from the MAC first passes through the 4-bit to 5-bit encoder. This block encodes 4-bit nibble into 5-bit code-groups according to the Table 5-8. Each 4-bit data nibble is mapped to 16 of the 32 possible code-groups. The remaining 16 code-groups are either used for control information or they are considered as not valid.

The code-group encoder substitutes the first 8 bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmission. The code-group encoder continues to replace subsequent 4-bit preamble and data nibbles with corresponding 5-bit code-groups. At the end of the transmit packet, upon the de-assertion of Transmit Enable signal from the MAC, the code-group encoder adds the T/R code-group pair (01101 00111) indicating the end of the frame.

After the T/R code-group pair, the code-group encoder continuously adds IDLEs into the transmit data stream until the next transmit packet is detected.

Table 5-8. 4-Bit to 5-Bit Code Table

4-BIT CODE	SYMBOL	5-BIT CODE	RECEIVER INTERPRETATION
0000	0	11110	Data
0001	1	01001	
0010	2	10100	
0011	3	10101	
0100	4	01010	
0101	5	01011	
0110	6	01110	
0111	7	01111	
1000	8	10010	
1001	9	10011	
1010	A	10110	
1011	B	10111	
1100	C	11010	
1101	D	11011	
1110	E	11100	
1111	F	11101	
IDLE AND CONTROL CODES			
DESCRIPTION	**SYMBOL (1)**	**5-BIT CODE**	
Inter-Packet IDLE	I	11111	IDLE
First nibble of SSD	J	11000	First nibble of SSD, translated to "0101" following /I/ (IDLE), else RX_ER asserted high
Second nibble of SSD	K	10001	Second nibble of SSD, translated to "0101" following /J/, else RX_ER asserted high
First nibble of ESD	T	01101	First nibble of ESD, causes de-assertion of CRS if followed by /R/, else assertion of RX_ER
Second nibble of ESD	R	00111	Second nibble of ESD, causes de-assertion of CRS if following /T/, else assertion of RX_ER
Transmit Error Symbol	H	00100	RX_ER
Invalid Symbol	V	00000	**INVALID** RX_ER asserted high If during RX_DV
	V	00001	
	V	00010	
	V	00011	
	V	00101	
	V	00110	
	V	01000	
	V	01100	

(1) Control code-groups I, J, K, T and R in data fields will be mapped as invalid codes, together with RX_ER asserted.

5.2.1.3 Scrambler

The purpose of the scrambler is to flatten the power spectrum of the transmitted signal, thus reducing EMI. The scrambler seed is generated with reference to the PHY address so that multiple PHYs that reside within the system will not use the same scrambler sequence.

5.2.1.4 NRZI and MLT-3 Encoding

To comply with the TP-PMD standard for 100Base-TX transmission over CAT-5 unshielded twisted pair cable, the scrambled data must be NRZI encoded. The serial binary data stream output from the NRZI encoder is further encoded to MLT-3. MLT-3 is a tri-level code where a change in the logic level represents a code bit 1 and the logic output remaining at the same level represents a code bit 0.

5.2.1.5 Digital-to-Analog Converter

The multipurpose programmable transmit Digital-to-Analog Converter (DAC) receives digital coded symbols and generates filtered analog symbols to be transmitted on the line. In 100B-TX the DAC applies a low-pass shaping filter to minimize EMI. The DAC is designed to improve the return loss requirements and enable the use of low-cost transformers.

Digital pulse-shape filtering is also applied to conform to the pulse masks defined by standard and to reduce EMI and high-frequency signal harmonics.

5.2.2 100Base-TX Receive Path

In 100B-TX, the ADC sampled data is passed to an adaptive equalizer. The adaptive equalizer drives the received symbols to the MLT3 decoder. The decoded NRZ symbols are transferred to the descrambler block for descrambling and deserialization.

5.2.2.1 Analog Front End

The Receiver Analog Front End (AFE) resides in front of the 100B-TX receiver. The AFE consists of an Analog-to-Digital Converter (ADC) and receives filters along with a Programmable Gain Amplifier (PGA).

The ADC samples the input signal at the 125-MHz clock recovered by the timing loop and feeds the data into the adaptive equalizer. The ADC is designed to optimize the SNR performance at the receiver input while maintaining high power-supply rejection ratio and low power consumption. There is only one ADC in the TLK10xL that receives the analog input data from the relevant cable pair, according to MDI-MDIX resolution.

The PGA, digitally controlled by the adaptive equalizer, fully uses the dynamic range of the ADC by adjusting the incoming-signal amplitude. Generally, the PGA attenuates short-cable strong signals and amplifies long-cable weak signals.

5.2.2.2 Adaptive Equalizer

The adaptive equalizer removes Inter-Symbol Interference (ISI) from the received signal introduced by the channel and analog Tx/Rx filters. The TLK10xL includes both Feedforward Equalization (FFE) and Decision Feedback Equalization (DFE). The combination of both adaptive modules with the adaptive gain control results in a powerful equalizer that can eliminate ISI and compensate for cable attenuation for longer-reach cables. In addition, the Equalizer includes a Shift Gear Step mechanism to provide fast convergence on the one hand and small residual-adaptive noise in steady-state on the other hand.

5.2.2.3 Baseline Wander Correction

The DC offset of the transmitted signal is shifted down or up based on the polarity of the transmitted data because the MLT-3 data is coupled onto the CAT 5 cable through a transformer that is high-pass in nature. This phenomenon is called Baseline wander. To prevent corruption of the received data because of this phenomenon, the receiver corrects the baseline wander and can receive the ANSI TP-PMD-defined *killer packet* with no bit errors.

5.2.2.4 NRZI and MLT-3 Decoding

The TLK10xL decodes the MLT-3 information from the Digital Adaptive Equalizer block to binary NRZI data. The NRZI-to-NRZ decoder is used to present NRZ-formatted data to the descrambler.

5.2.2.5 Descrambler

The descrambler is used to descramble the received NRZ data. The data is further deserialized and the parallelized data is aligned to 5-bit code-groups and mapped into 4-bit nibbles. At initialization, the 100B-TX descrambler uses the IDLE-symbols sequence to lock on the Far-end scrambler state. During that time, neither data transmission nor reception is enabled. After the Far-end scrambler state is recovered, the descrambler constantly monitors the data and checks whether it still synchronized. If, for any reason, synchronization is lost, the descrambler tries to reacquire synchronization using the IDLE symbols.

5.2.2.6 5B/4B Decoder and Nibble Alignment

The code-group decoder functions as a look-up table that translates incoming 5-bit code-groups into 4-bit nibbles. The code-group decoder first detects the Start of Stream Delimiter (SSD) /J/K/ code-group pair preceded by IDLE code-groups at the start of a packet. Once the code group alignment is determined, it is stored and used until the next start-of-frame. The decoder replaces the /J/K/ with the MAC preamble. Specifically, the /J/K/ 10-bit code-group pair is replaced by the nibble pair (0101 0101). All subsequent 5-bit code-groups are converted to the corresponding 4-bit nibbles for the duration of the entire packet. This conversion ceases upon the detection of the /T/R/ code-group pair denoting the End-of-Stream Delimiter (ESD) or with the reception of a minimum of two IDLE code-groups.

5.2.2.7 Timing Loop and Clock Recovery

The receiver must lock on the Far-end transmitter clock to sample the data at the optimum timing. The timing loop recovers the Far-end clock frequency and offset from the received data samples and tracks instantaneous phase drifts caused by timing jitter.

The TLK10xL has a robust adaptive-timing loop (Tloop) mechanism that is responsible for tracking the Far-end TX clock and adjusting the AFE sampling point to the incoming signal. The Tloop implements an advanced tracking mechanism that when combined with different available phases, always keeps track of the optimized sampling point for the data, and thus offers a robust RX path tolerant to both PPM and Jitter. The TLK10xL is capable of dealing with PPM and jitter at levels far higher than those defined by the standard.

5.2.2.8 Phase-Locked Loops (PLL)

In 10B-T the digital phase lock loop (DPLL) function recovers the Far-end link-partner clock from the received Manchester signal. The DPLL is able to combat clock jitter of up to ±18 ns and frequency drifts of ±500 ppm between the local PHY clock and the Far-end clock. The DPLL feeds the decoder with a decoded serial bit stream.

The integrated analog Phase-Locked Loop (PLL) provides the clocks to the analog and digital sections of the PHY. The PLL is driven by an external reference clock (sourced at the XI,XO pins with a crystal oscillator, or at XI with an external reference clock).

5.2.2.9 Link Monitor

The TLK10xL implements the link monitor State Machine (SM) as defined by the IEEE 802.3 100Base-TX Standard. In addition, the TLK10xL enables several add-ons to the link monitor SM activated by configuration bits. The new add-ons include the recovery state which enables the PHY to attempt recovery in the event of a temporary energy-loss situation before entering the LINK_FAIL state, thus restarting the whole link establishment procedure. This sequence allows significant reduction of the recovery time in scenarios where the link loss is temporal.

In addition, the link monitor SM enables moving to the LINK_DOWN state based on descrambler synchronization failure and not only on Signal_Status indication, which shortens the drop-link down time. These add-ons are supplementary to the IEEE standard and are bypassed by default.

5.2.2.10 Signal Detect

The signal detect function of the TLK10xL is incorporated to meet the specifications mandated by the ANSIFDDI TP-PMD Standard as well as the IEEE 802.3 100Base-TX Standard for both voltage thresholds and timing parameters.

The energy-detector module provides signal-strength indication in various scenarios. Because it is based on an IIR filter, this robust energy detector has excellent reaction time and reliability. The filter output is compared to predefined thresholds to decide the presence or absence of an incoming signal.

The energy detector also implements hysteresis to avoid jittering in signal-detect indication. In addition, it has fully-programmable thresholds and listening-time periods, enabling shortening of the reaction time if required.

5.2.2.11 Bad SSD Detection

A Bad Start of Stream Delimiter (Bad SSD) is any transition from consecutive idle code-groups to non-idle code-groups which is not prefixed by the code-group pair /J/K. If this condition is detected, the TLK10xL asserts RX_ER, and presents RXD[3:0] = 1110 to the MII for the cycles that correspond to received 5B code-groups until at least two IDLE code groups are detected. In addition, the FCSCR register (0x14h) is incremented by one for every error in the nibble.

When at least two IDLE code groups are detected, RX_ER and CRS are deasserted.

5.2.3 10Base-T Receive Path

In 10B-T, after the far-end clock is recovered, the received Manchester symbols pass to the Manchester decoder. The serial decoded bit stream is aligned to the start of the frame, deserialized to 4-bit wide nibbles and sent to the MAC through the MII.

5.2.3.1 10M Receive Input and Squelch

The squelch feature determines when valid data is present on the differential receive inputs. The TLK10xL implements a squelch to prevent impulse noise on the receive inputs from being mistaken for a valid signal. Squelch operation is independent of the 10Base-T operating mode. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10Base-T standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of a packet is checked by the squelch, and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) are rejected. When this first squelch level is exceeded correctly, the opposite squelch level must then be exceeded no earlier than 50 ns. Finally, the signal must again exceed the original squelch level no earlier than 50 ns to qualify as a valid input waveform, and not be rejected. This checking procedure results in the typical loss of three preamble bits at the beginning of each packet. When the transmitter is operating, five consecutive transitions are checked before indicating that valid data is present. At this time, the squelch circuitry is reset.

5.2.3.2 Collision Detection

When in Half-Duplex mode, a 10Base-T collision is detected when receive and transmit channels are active simultaneously. Collisions are reported by the COL signal on the MII.

The COL signal remains set for the duration of the collision. If the PHY is receiving when a collision is detected, it is reported immediately (through the COL pin).

5.2.3.3 Carrier Sense

Carrier Sense (CRS) may be asserted due to receive activity after valid data is detected through the squelch function. For 10-Mbps Half Duplex operation, CRS is asserted during either packet transmission or reception. For 10-Mbps Full Duplex operation, CRS is asserted only during receive activity.

CRS is deasserted following an end-of-packet.

5.2.3.4 Jabber Function

Jabber is a condition in which a station transmits for a period of time longer than the maximum permissible packet length, usually due to a fault condition. The jabber function monitors the TLK10xL output and disables the transmitter if it attempts to transmit a packet of longer than legal size. A jabber timer monitors the transmitter and disables the transmission if the transmitter is active for approximately 100 ms.

When disabled by the Jabber function, the transmitter stays disabled for the entire time that the ENDEC module's internal transmit enable is asserted. This signal must be de-asserted for approximately 500 ms (the *unjab* time) before the Jabber function re-enables the transmit outputs.

The Jabber function is only available and active in 10Base-T mode.

5.2.3.5 Automatic Link Polarity Detection and Correction

Swapping the wires within the twisted pair causes polarity errors. Wrong polarity affects the 10B-T PHYs. The 100B-TX is immune to polarity problems because it uses MLT3 encoding. The 10B-T automatically detects reversed polarity according to the received link pulses or data. Note that the default transmit link pulse polarity for the TLK10xL is reversed.

5.2.3.6 10Base-T Transmit and Receive Filtering

External 10Base-T filters are not required when using the TLK10xL, because the required signal conditioning is integrated into the device. Only isolation transformers and impedance matching resistors are required for the 10Base-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmit signal are attenuated by at least 30 dB.

5.2.3.7 10Base-T Operational Modes

The TLK10xL has two basic 10Base-T operational modes:

- Half Duplex mode – In Half Duplex mode, the TLK10xL functions as a standard IEEE 802.3 10Base-T transceiver supporting the CSMA/CD protocol.
- Full Duplex mode – In Full Duplex mode, the TLK10xL is capable of simultaneously transmitting and receiving without asserting the collision signal. The TLK10xL 10Mbs ENDEC is designed to encode and decode simultaneously.

5.2.4 Auto-Negotiation

The auto-negotiation function, described in detail in IEEE802.3 chapter 28, provides the means to exchange information between two devices and automatically configure both of them to take maximum advantage of their abilities.

5.2.4.1 Operation

Auto negotiation uses the 10B-T link pulses to encapsulate the transmitted data in a sequence of pulses, also referred to as a Fast Link Pulses (FLP) burst. The FLP burst consists of a series of closely spaced 10B-T link integrity test pulses that form an alternating clock or data sequence. Extraction of the data bits from the FLP Burst yields a Link Code Word that identifies the operational modes supported by the remote device, as well as some information used for the auto negotiation function's handshake mechanism.

The information exchanged between the devices during the auto-negotiation process consists of the devices' abilities, such as duplex support and speed. This information allows higher levels of the network (MAC) to send to the other link partner vendor-specific data (through the Next Page mechanism, see below), and provides the mechanism for both parties to agree on the highest performance mode of operation.

When auto negotiation has started, the TLK10xL transmits FLP on one twisted pair and listens on the other, thus trying to find out whether the other link partner supports the auto negotiation function as well. The decision on which pair to transmit and listen depends on the MDI/MDI-X state. If the other link partner activates auto negotiation, then the two parties begin to exchange their information. If the other link partner is a legacy PHY or does not activate the auto negotiation, then the TLK10xL uses the parallel detection function, as described in IEEE802.3 chapters 40 and 28, to determine 10B-T or 100B-TX operation modes.

5.2.4.2 Initialization and Restart

The TLK10xL initiates the auto negotiation function if one of the following events have happened:

1. Hardware reset deassertion
2. Software reset (through register)
3. Auto negotiation restart (through register BMCR (0x0000h) bit 9)
4. Power-up sequence (through register BMCR (0x0000h) bit 11)

The auto-negotiation function is also initiated when the auto-negotiation enable bit is set in register BMCR (0x0000h) bit 12 and one of the following events has happened:

1. Software restart
2. Transitioning to *link_fail* state, as described in IEEE802.3

To disable the auto-negotiation function during operation, clear register BMCR (0x0000h) bit 12. During operation, setting or resetting this register does not affect the TLK10xL operation. For the changes to take place, issue a restart command through register BMCR (0x0000h) bit 9.

5.2.4.3 Next Page Support

The TLK10xL supports the optional feature of the transmission and reception of auto-negotiation additional (vendor specific) next pages.

If next pages are needed, the user must set register ANAR(0x0004h) bit 15 to 1. The next pages are then sent and received through registers ANNPTR(0x0007h) and ANLNPTR(0x0008h), respectively. The user must poll register ANER(0x0006h) bit 1 to check whether a new page has been received, and then read register ANLNPTR for the received next page's content. Only after register ANLNPTR is read may the user write to register ANNPTR the next page to be transmitted. After register ANNPTR is written, new next pages overwrite the contents of register ANLNPTR.

If register ANAR(0x0004h) bit 15 is set, then the next page sequence is controlled by the user, meaning that the auto-negotiation function always waits for register ANNPTR to be written before transmitting the next page.

If additional user-defined next pages are transmitted and the link partner has more next pages to send, it is the user's responsibility to keep writing null pages (of value 0x2001) to register ANNPTR until the link partner notifies that it has sent its last page (by setting bit 15 of its transmitted next page to zero).

5.2.5 Link Down Functionality

The TLK10xL includes advanced link-down capabilities that support various real-time applications. The link-down mechanism of the TLK10xL is configurable and includes enhanced modes that allow extremely fast reaction times to link-drops.

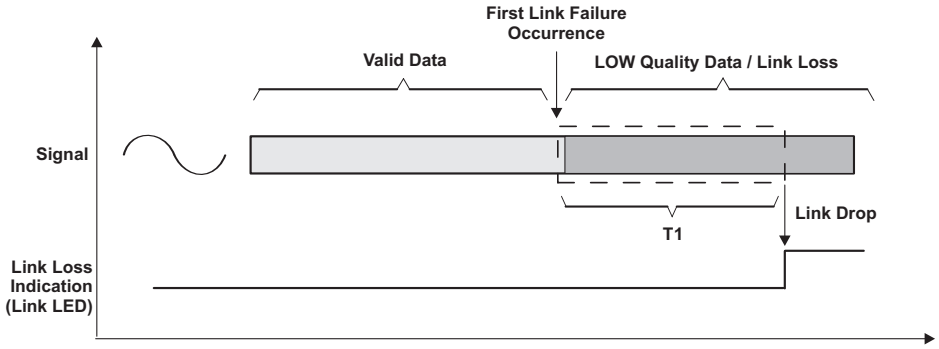


Figure 5-9. TLK10xL Link Loss Mechanism

As described in Figure 5-9, the TLK10xL link loss mechanism is based on a time window search period, in which the signal behavior is monitored. The T1 window is set by default to reduce typical link-drops to less than 1 ms.

The TLK10xL supports enhanced modes that shorten the window called Fast Link Down mode. In this mode, which can be configured in Control Register 3 (CR3), address 0x000B, bits 3:0, the T1 window is shortened significantly, in most cases less than 10 µs. In this period of time, there are several criteria allowed to generate link loss event and drop the link:

1. Count RX Error in the MII interface: When a predefined number of 32 RX Error occurrences in time window of 10 µs is reached the link drops.
2. Count MLT3 Errors at the signal processing output (100BT uses MLT3 coding, and when a violation of this coding is detected, an MLT3 error is declared). When a predefined number of 20 errors occurrences in 10µs is reached, the link drops.
3. Count Low Signal Quality Threshold crossing (When the signal quality is under a certain threshold that allows proper link conditions). When a predefined number of 20 occurrences in 10 µs is reached, the link drops.
4. Signal or Energy Loss Indications. When the energy detector indicates energy loss, the link is dropped. Typical reaction time is 10 µs.

The Fast Link Down functionality allows the use of each of these options separately or in any combination.

NOTE

Because this mode enables extremely quick reaction time, it is more exposed to temporary bad link-quality scenarios.

5.2.6 IEEE 1588 Precision Timing Protocol Support

The TLK10xLsupports an IEEE 1588 indication pulse at the SFD (start frame delimiter) for the RX and TX paths in 100BT mode. The pulse can be delivered to various pins as configured by register 0x3e. The pulse indicates the actual time the symbol is presented on the lines (for TX), or the first bit where the /J/ symbol is received (RX). Exact timing of the pulse can be adjusted using register 0x3f. Each increment of phase value is an 8-ns step.

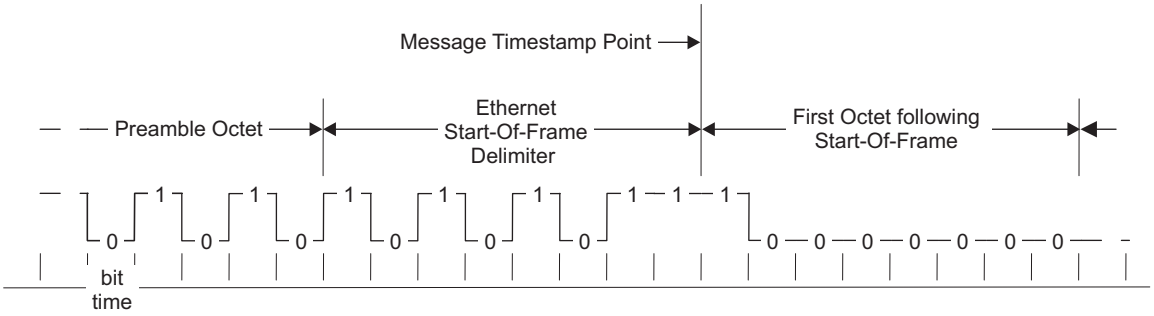


Figure 5-10. IEEE 1588 Message Timestamp Point

5.3 Register Maps

Table 5-9. Register Map

OFFSET HEX	ACCESS	TAG	DESCRIPTION
00h	RW	BMCR	Basic Mode Control Register
01h	RO	BMSR	Basic Mode Status Register
02h	RO	PHYIDR1	PHY Identifier Register 1
03h	RO	PHYIDR2	PHY Identifier Register 2
04h	RW	ANAR	Auto-Negotiation Advertisement Register
05h	RO	ANLPAR	Auto-Negotiation Link Partner Ability Register
06h	RO	ANER	Auto-Negotiation Expansion Register
07h	RW	ANNPTR	Auto-Negotiation Next Page TX
08h	RO	ANLNPTR	Auto-Negotiation Link Partner Ability Next Page Register
09h	RW	CR1	Control Register 1
0Ah	RW	CR2	Control Register 2
0Bh	RW	CR3	Control Register 3
0Ch	RW	RESERVED	RESERVED
0Dh	RW	REGCR	Register control register
0Eh	RW	ADDAR	Address or Data register
0Fh	RW	FLDS	Fast Link Down Status
0x0010	RO	PHYSTS	PHY Status Register
0x0011	RW	PHYSCR	PHY Specific Control Register
0x0012	RW	MISR1	MII Interrupt Status Register 1
0x0013	RW	MISR2	MII Interrupt Status Register 2
0x0014	RO	FCSCR	False Carrier Sense Counter Register
0x0015	RO	RECR	Receive Error Count Register
0x0016	RW	BISCR	BIST Control Register
0x0017	RO	RBR	RMII and Status Register
0x0018	RW	LEDCR	LED Control Register
0x0019	RW	PHYCR	PHY Control Register
0x001A	RW	10BTSCR	10Base-T Status/Control Register

Table 5-9. Register Map (continued)

OFFSET HEX	ACCESS	TAG	DESCRIPTION
0x001B	RW	BICSR1	BIST Control and Status Register 1
0x001C	RO	BICSR2	BIST Control and Status Register 2
0x001D	RW	RESERVED	RESERVED
0x001E	RW	CDCR	Cable Diagnostic Control Register
0x001F	RW	PHYRCR	PHY Reset Control Register
EXTENDED REGISTERS			
0x0020- 0x0024	RW	RESERVED	RESERVED
0x0025	RW	MLEDCR	Multi LED Control register
0x0026	RW	RESERVED	RESERVED
0x0027	RW	COMPTR	Compliance Test register
0x0028- 0x003CD	RW	RESERVED	RESERVED
0x003E	RW	PTPPSEL	IEEE1588 Precision Timing Pin Select
0x003F	RW	PTPCFG	IEEE1588 Precision Timing Configuration
0x0040	RW	RESERVED	RESERVED
0x0041	RW	RESERVED	RESERVED
0x0042	RO	TXCPSR	TX_CLK Phase Shift Register
0x0043- 0x00AD	RW	RESERVED	RESERVED
0x00AE	RW	PWRBOCR	Power Back Off Control Register
0x00AF- 0x00CF	RW	RESERVED	RESERVED
0x00D0	RW	VRCR	Voltage Regulator Control Register
0x00D1-0x0154	RW	RESERVED	RESERVED
0x0155	RW	ALCDRR1	ALCD Control and Results 1
0x0156- 0x016F	RW	RESERVED	RESERVED
0x0170	RW	CDSCR1	Cable Diagnostic Specific Control Register 1
0x0171	RW	CDSCR2	Cable Diagnostic Specific Control Register 2
0x0172	RW	RESERVED	RESERVED
0x0173	RW	CDSCR3	Cable Diagnostic Specific Control Register 3
0x0174-0x0176	RW	RESERVED	RESERVED
0x0177	RW	CDSCR4	Cable Diagnostic Specific Control Register 4
0x0178- 0x017F	RW	RESERVED	RESERVED
0x0180	RO	CDLRR1	Cable Diagnostic Location Result Register 1
0x0181	RO	CDLRR2	Cable Diagnostic Location Result Register 2
0x0182	RO	CDLRR3	Cable Diagnostic Location Result Register 3
0x0183	RO	CDLRR4	Cable Diagnostic Location Result Register 4
0x0184	RO	CDLRR5	Cable Diagnostic Location Result Register 5
0x0185	RO	CDLAR1	Cable Diagnostic Amplitude Result Register 1
0x0186	RO	CDLAR2	Cable Diagnostic Amplitude Result Register 2
0x0187	RO	CDLAR3	Cable Diagnostic Amplitude Result Register 3
0x0188	RO	CDLAR4	Cable Diagnostic Amplitude Result Register 4
0x0189	RO	CDLAR5	Cable Diagnostic Amplitude Result Register 5
0x018A	RW	CDGRR	Cable Diagnostic General Result Register
0x018B-0x0214	RW	RESERVED	RESERVED
0x0215	RW	ALCDRR2	ALCD Control and Results 2 Register
0x021D	RW	ALCDRR3	ALCD Control and Results 3 Register

Table 5-10. Register Table

REGISTER NAME	ADDR	TAG	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Basic Mode Control Register	00h	BMCR	Reset	Loopback	Speed Selection	Auto-Neg Enable	IEEE Power Down	Isolate	Restart Auto-Neg	Duplex Mode	Collision Test	Reserved						
Basic Mode Status Register	01h	BMSR	100Base - T4	100Base - TX FDX	100Base - TX HDX	10Base-T FDX	10Base-T HDX	Reserved				MF Preamble Suppress	Auto-Neg Complete	Remote Fault	Auto-Neg Ability	Link Status	Jabber Detect	Extended Capability
PHY Identifier Register 1	02h	PHYIDR 1	OUI MSB															
PHY Identifier Register 2	03h	PHYIDR 2	OUI LSB						VNDR_ MDL						MDL_ REV			
Auto-Negotiation Advertisement Register	04h	ANAR	Next Page Ind	Reserved	Remote Fault	Reserved	ASM_DI R	PAUSE	100B-T4	100B-TX_FD	100B-TX	10B-T_FD	10B-T	Protocol Selection[4:0]				
Auto-Negotiation Link Partner Ability Register (Base Page)	05h	ANLPAR	Next Page Ind	ACK	Remote Fault	Reserved	ASM_DI R	PAUSE	100B-T4	100B-TX_FD	100B-TX	10B-T_FD	10B-T	Protocol Selection[4:0]				
Auto-Negotiation Expansion Register	06h	ANER	Reserved											PDF	LP_NP_ ABLE	NP_ ABLE	PAGE_ RX	LP_AN_AB LE
Auto-Negotiation Next Page TX Register	07h	ANNPTR	Next Page Ind	Reserved	Message Page	ACK2	TOG_TX	CODE										
Auto-Negotiate Link Partner Ability Page Register	08h	ANLNPTR	Next Page Ind	Reserved	Message Page	ACK2	Toggle	CODE										
Control Register 1	09h	CR1	Reserved						RMII Enhance Mode	TDR Auto Run	Link Loss Recovery	Fast Auto MDI/X	Robust Auto MDI/X	Fast AN Enable	Fast AN Select		Fast RXDV Detect	Reserved
Control Register 2	0Ah	CR2	100BT Force Far-End Link drop	Reserved								Fast Link-Up in PD	Extended FD Ability	Enhance LED Link	Isolate MII in 100BT HD	RXERR During IDLE	Odd Nibble Detect Disable	RMII Receive Clock
Control Register 3	0Bh	CR3	Reserved					Fast Link Down Mode	Reserved			Polarity Swap	MDI/X Swap	Reserved	Fast Link Down Sel			
Register Control Register	0Dh	REGCR	Function		Reserved									DEVICE ADDRESS				
Address or Data Register	0Eh	ADDAR	Addr/ Data															
Fast Link Down Status	0Fh	FLDS	Reserved							Fast Link Down Status[4:0]					Reserved			
PHY Status Register	10h	PHYSTS	Reserved	MDI-X Mode	Receive Err Latch	Polarity Status	False Carrier Sen Latch	Signal Detect	Descramb Lock	Page Receive	MII Interrupt	Remote Fault	Jabber Detect	Auto-Neg Status	Loopback Status	Duplex Status	Speed Status	Link Status
PHY Specific Control Register	11h	PHYSCR	Disable PLL	Power Save Enable	Power Save Mode		Scrambler Bypass	Reserved	Loopback Fifo Depth		Reserved			COL FD Enable	INT POL	TINT	INT_EN	INT_OE
MII Interrupt Status Register 1	12h	MISR1	Reserved		Link Status INT	Speed INT	Duplex Mode INT	Auto-Neg Comp INT	FC HF INT	RE HF INT	Reserved		Link Status En	Speed EN	Duplex Mode En	Auto-Neg Comp En	FC HF En	RE HF En
MII Interrupt Status Register 2	13h	MISR2	Reserved	Auto-Neg Error INT	Page Received INT	Loopback FIFO O/U INT	MDI Crossover INT	Sleep Mode INT	Polarity INT	Jabber INT	Reserved	Auto-Neg Error EN	Page Received EN	Loopback FIFO O/U EN	MDI Crossover EN	Sleep Mode EN	Polarity EN	Jabber EN

Table 5-10. Register Table (continued)

REGISTER NAME	ADDR	TAG	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MII Interrupt Control Register	14h	FCSCR	Reserved								FCS Count							
Receive Error Counter Register	15h	RECR	RX Err Count															
BIST Control Register	16h	BISCR	Reserved	PRBS Count Mode	Generate PRBS Packets	Packet Gen Enable	PRBS Checker Lock	PRBS Checker SyncLoss	Packet Gen Status	Power Mode	Reserved	Transmit in MII Loopback	Reserved	Loopback Mode				
RMII Control, Status Register	17h	RCSR	Reserved										RMII Mode	RMII Revision	RMII OVF Status	RMII UNF Status	ELAST BUF	
LED Control Register	18h	LEDCR	Reserved					Blink Rate		LED Speed Polarity	LED Link Polarity	LED Activity Polarity	Drive LED Speed	Drive LED Link	Drive LED Activity	Speed LED ON/OFF	Link LED ON/OFF	Activity LED ON/OFF
PHY Control Register	19h	PHYCR	Auto MDI/X Enable	Force MDI/X	Pause RX Status	Pause TX Status	MI Link Status	Reserved			Bypass LED Stretching	LED CFG		PHY ADDR				
BIST Packet Length register	1Ah	10BTSCR	Reserved		Receiver TH	Squelch				Reserved	NLP Disable	Reserved		Polarity Status	Reserved			Jabber Disable
BIST Control, Status Register 1	1Bh	BICSR1	BIST Err Count								BIST IPG Length							
BIST Control, Status Register 2	1Ch	BICSR2	Reserved					Packet Length										
Cable Diagnostic Control Register	1Eh	CDCR	Diagnostic Start	Reserved					Link Quality	Link Quality	Reserved						Diagnostic Done	Diagnostic Fail
Power Down Register	1Fh	PDR	Software Reset	Software Restart	Reserved													

Table 5-11. Register Table, Extended Registers

Register Name	Addr	Tag	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Multi LED Control	25h	MLED	Reserved					MLED pin 29 Route, Enable (COL Disable)	MLED Polarity	Reserved		MLED Configuration				Reserved	MLED pin 17 Routing Cnfig.	"MLED pin Routing enable"
Compliance Test Register	27h	COMPTR	Reserved										Test Mode Select	Test Configuration				
1588 PTP Pin Select	3Eh	PTPPSEL	Reserved									cfg_1588_TX_pin_sel			Reserved	cfg_1588_RX_pin_sel		
1588 PTP Config	3Fh	PTPCFG	cfg_1588_TX_set_phase			cfg_1588_RX_set_phase			cfg_TX_ERR_sel	Reserved								
TX_CLK	42h	TXCPSR	Reserved											Phase Shift En	Phase Shift Value			
Voltage Regulator Control Register	D0h	VRCR	VRPD	Reserved														
PowerBack Off Control Register	AEh	PWRBOCR	Reserved							PowerBack Off		Reserved						
ALCD Control and Results 1	155h	ALCDRR1	alcd_start	Reserved		alcd_done	alcd_out1								Reserved	alcd_ctrl		
Cable Diagnostic Specific Control Register 1	170h	CDSCR1	Reserved	Cross Disable	TPTD Bypass	TPRD Bypass	Reserved	Average Cycles			Reserved							
Cable Diagnostic Specific Control Register 2	171h	CDSCR2	Reserved												TDR pulse control			
Cable Diagnostic Specific Control Register 3	173h	CDSCR3	Cable length								Reserved							
Cable Diagnostic Specific Control Register 4	177h	CDSCR4				Short cables TH					Reserved							
Cable Diagnostic Location Results Register 1-5	180h	CDLRR1	TPTD/RD Peak Location															
	181h	CDLRR2																
	182h	CDLRR3																
	183h	CDLRR4																
	184h	CDLRR5																
Cable Diagnostic Amplitude Results Register 1-5	185h	CDLAR1	Reserved	TPTD/RD Peak Amplitude							Reserved	TPTD/RD Peak Amplitude						
	186h	CDLAR2																
	187h	CDLAR3																
	188h	CDLAR4																
	189h	CDLAR5																
Cable Diagnostic General Results	18Ah	CDGRR	TPTD Peak Polarity 5	TPTD Peak Polarity 4	TPTD Peak Polarity 3	TPTD Peak Polarity 2	TPTD Peak Polarity 1	TPRD Peak Polarity 5	TPRD Peak Polarity 4	TPRD Peak Polarity 3	TPRD Peak Polarity 2	TPRD Peak Polarity 1	Cross Detect on TPTD	Cross Detect on TPRD	Above 5 TPTD Peaks	Above 5 TPTD Peaks	Reserved	Reserved
ALCD Control and Results 2	215h	ALCDRR2	Reserved												alcd_out2			
ALCD Control and Results 3	21Dh	ALCDRR3	Reserved				FAGC Accumulator											

5.3.1 Register Definition

In the register definitions under the *Default* heading, the following definitions hold true:

- COR = Clear on Read
- Pin_Strap = Default value loads from strapping pin after reset
- LH = Latched High and held until read, based upon the occurrence of the corresponding event
- LL = Latched Low and held until read, based upon the occurrence of the corresponding event
- RO = Read Only access
- RO/COR = Read Only, Clear on Read
- RO/P = Read Only, Permanently set to a default value
- RW = Read Write access
- RW/SC = Read Write Access or Self Clearing bit
- SC = Register sets on event occurrence and Self-Clears when event ends

5.3.1.1 Basic Mode Control Register (BMCR)

Table 5-12. Basic Mode Control Register (BMCR), Address 0x0000

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	Reset	0, RW/SC	**PHY Software Reset:** 1 = Initiate software Reset / Reset in Process 0 = Normal operation Writing a 1 to this bit resets the PHY. When the reset operation is done, this bit is cleared to 0 automatically. The configuration is relatched.
14	MII Loopback	0, RW	**MII Loopback:** 1 = MII Loopback enabled 0 = Normal operation When MII loopback mode is activated, the transmitter data presented on MII TXD is looped back to MII RXD internally.
13	Speed Selection	1, RW	**Speed Select:** When auto-negotiation is disabled writing to this bit allows the port speed to be selected. 1 = 100Mbs 0 = 10Mbs
12	Auto-Negotiation Enable	1, RW	**Auto-Negotiation Enable:** 1 = Auto-Negotiation Enabled – bits 8 and 13 of this register are ignored when this bit is set. 0 = Auto-Negotiation Disabled – bits 8 and 13 determine the port speed and duplex mode.
11	IEEE Power Down	0, RW	**Power Down:** 1 = Enables IEEE power-down mode 0 = Normal operation Setting this bit powers down the PHY. Only minimal register functionality is enabled during the power-down condition. To control the power-down mechanism, this bit is ORed with the input from the $\overline{\text{INT}}$/PWDN pin. When the active low $\overline{\text{INT}}$/PWDN is asserted, this bit is set.
10	Isolate	0, RW	**Isolate:** 1 = Isolates the Port from the MII with the exception of the serial management 0 = Normal operation

Table 5-12. Basic Mode Control Register (BMCR), Address 0x0000 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
9	Restart Auto-Negotiation	0, RW/SC	**Restart Auto-Negotiation:** 1 = Restart Auto-Negotiation. Re-initiates the Auto-Negotiation process. If Auto-Negotiation is disabled (bit 12 = 0), this bit is ignored. This bit is self-clearing and returns a value of 1 until Auto-Negotiation is initiated, whereupon it self-clears. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit. 0 = Normal operation Reinitiates the Auto-Negotiation process. If Auto-Negotiation is disabled (bit 12 = 0), this bit is ignored. This bit is self-clearing and returns a value of 1 until Auto-Negotiation is initiated, whereupon it self-clears. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit.
8	Duplex Mode	1, Pin_Strap led control	**Duplex Mode:** When auto-negotiation is disabled writing to this bit allows the port Duplex capability to be selected. 1 = Full Duplex operation 0 = Half Duplex operation
7	Collision Test	0, RW	**Collision Test:** 1 = Collision test enabled 0 = Normal operation When set, this bit causes the COL signal to be asserted in response to the assertion of TX_EN within 512 bit times. The COL signal is de-asserted within 4 bit times in response to the deassertion of TX_EN.
6:0	RESERVED	0, RO	**RESERVED:** Write ignored, read as 0.

5.3.1.2 Basic Mode Status Register (BMSR)

Table 5-13. Basic Mode Status Register (BMSR), Address 0x0001

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	100Base-T4	0, RO/P	**100Base-T4 Capable:** This protocol is not available. Always 0 = Device does not perform 100Base-T4 mode.
14	100Base-TX Full Duplex	1, RO/P	**100Base-TX Full Duplex Capable:** 1 = Device able to perform 100Base-TX in full duplex mode 0 = Device not able to perform 100Base-TX in full duplex mode
13	100Base-TX Half Duplex	1, RO/P	**100Base-TX Half Duplex Capable:** 1 = Device able to perform 100Base-TX in half duplex mode 0 = Device not able to perform 100Base-TX in half duplex mode
12	10Base-T Full Duplex	1, RO/P	**10Base-T Full Duplex Capable:** 1 = Device able to perform 10Base-T in full duplex mode 0 = Device not able to perform 10Base-T in full duplex mode
11	10Base-T Half Duplex	1, RO/P	**10Base-T Half Duplex Capable:** 1 = Device able to perform 10Base-T in half duplex mode 0 = Device not able to perform 10Base-T in half duplex mode
10:7	RESERVED	0, RO	**RESERVED:** Write as 0, read as 0
6	MF Preamble Suppression	1, RO/P	**Preamble Suppression Capable:** 1 = Device able to perform management transaction with preamble suppressed, 32-bits of preamble needed only once after reset, invalid opcode, or invalid turnaround. 0 = Device will not perform management transaction with preambles suppressed
5	Auto-Negotiation Complete	0, RO	**Auto-Negotiation Complete:** 1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete (either still in process, disabled, or reset)
4	Remote Fault	0, RO/LH	**Remote Fault:** 1 = Remote Fault condition detected (cleared on read or by reset). Fault criteria: Far-End Fault Indication or notification from Link Partner of Remote Fault. 0 = No remote fault condition detected
3	Auto-Negotiation Ability	1, RO/P	**Auto Negotiation Ability:** 1 = Device is able to perform Auto-Negotiation 0 = Device is not able to perform Auto-Negotiation
2	Link Status	0, RO/LL	**Link Status:** 1 = Valid link established (for either 10- or 100-Mbps operation) 0 = Link not established
1	Jabber Detect	0, RO/LH	**Jabber Detect:** This bit only has meaning in 10-Mbps mode. 1 = Jabber condition detected 0 = No Jabber. condition detected This bit is implemented with a latching function, such that the occurrence of a jabber condition causes it to set until it is cleared by a read to this register by the management interface or by a reset.
0	Extended Capability	1, RO/P	**Extended Capability**: 1 = Extended register capabilities 0 = Basic register set capabilities only

5.3.1.3 PHY Identifier Register 1 (PHYIDR1)

The PHY Identifier Registers 1 and 2 together form a unique identifier for the TLK10xL. The identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number and the model revision number. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier if desired. The PHY Identifier is intended to support network management. The Texas Instruments IEEE-assigned OUI is 080028h, implemented as Reg 0x2 [15:0] = OUI[21:6] = 2000(h) and Reg 0x3 [15:10] = OUI[5:0] = A(h).

Table 5-14. PHY Identifier Register 1 (PHYIDR1), Address 0x0002

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	OUI_MSB	0010 0000 0000 0000, RO/P	**OUI[21:6] = 2000(h):** The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bits 1 and 2).

5.3.1.4 PHY Identifier Register 2 (PHYIDR2)

Table 5-15. PHY Identifier Register 2 (PHYIDR2), Address 0x0003

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:10	OUI_LSB	1010 00, RO/P	**OUI[5:0] = 28(h)**
9:4	VNDR_MDL	10 0001, RO/P	**Vendor Model Number:** The six bits of vendor model number are mapped from bits 9 to 4 (most significant bit to bit 9).
3:0	MDL_REV	0010, RO/P	**Model Revision Number:** Four bits of the vendor model revision number are mapped from bits 3 to 0 (most significant bit to bit 3). This field is incremented for all major device changes.

5.3.1.5 Auto-Negotiation Advertisement Register (ANAR)

This register contains the advertised abilities of this device as they are transmitted to its link partner during Auto-Negotiation.

Table 5-16. Auto-Negotiation Advertisement Register (ANAR), Address 0x0004

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RW	**Next Page Indication:** 0 = Next Page Transfer not desired 1 = Next Page Transfer desired
14	RESERVED	0, RO/P	**RESERVED by IEEE:** Writes ignored, Read as 0
13	RF	0, RW	**Remote Fault:** 1 = Advertises that this device has detected a Remote Fault 0 = No Remote Fault detected
12	RESERVED	0, RW	**RESERVED for Future IEEE use:** Write as 0, Read as 0
11	ASM_DIR	0, RW	**Asymmetric PAUSE Support for Full Duplex Links:** The ASM_DIR bit indicates that asymmetric PAUSE is supported. 1 = Asymmetric PAUSE implemented. Advertise that the DTE/MAC has implemented both the optional MAC control sublayer and the pause function as specified in clause 31 and annex 31B of IEEE802.3u. 0 = Asymmetric PAUSE not implemented Encoding and resolution of PAUSE bits is defined in IEEE 802.3 Annex 28B, Tables 28B-2 and 28B-3, respectively. Pause resolution status is reported in PHYCR[13:12].
10	PAUSE	0, RW	**PAUSE Support for Full Duplex Links:** The PAUSE bit indicates that the device is capable of providing the symmetric PAUSE functions as defined in Annex 31B. 1 = MAC PAUSE implemented. Advertise that the DTE (MAC) has implemented both the optional MAC control sub-layer and the pause function as specified in clause 31 and annex 31B of 802.3u. 0 = MAC PAUSE not implemented Encoding and resolution of PAUSE bits is defined in IEEE 802.3 Annex 28B, Tables 28B-2 and 28B-3, respectively. Pause resolution status is reported in PHYCR[13:12].
9	100B-T4	0, RO/P	**100Base-T4 Support:** 1 = 100Base-T4 is supported by the local device 0 = 100Base-T4 not supported
8	100B-TX_FD	1, RW	**100Base-TX Full Duplex Support:** 1 = 100Base-TX Full Duplex is supported by the local device 0 = 100Base-TX Full Duplex not supported
7	100B-TX	1, RW	**100Base-TX Support:** 1 = 100Base-TX is supported by the local device 0 = 100Base-TX not supported
6	10B-T_FD	1, RW	**10Base-T Full Duplex Support:** 1 = 10Base-T Full Duplex is supported by the local device 0 = 10Base-T Full Duplex not supported
5	10B-T	1, RW	**10Base-T Support:** 1 = 10Base-T is supported by the local device 0 = 10Base-T not supported
4:0	Selector	0 0001, RW	**Protocol Selection Bits:** These bits contain the binary encoded protocol selector supported by this port. <00001> indicates that this device supports IEEE 802.3u.

5.3.1.6 Auto-Negotiation Link Partner Ability Register (ANLPAR) (BASE Page)

This register contains the advertised abilities of the Link Partner as received during Auto-Negotiation. The content changes after the successful auto-negotiation if Next-pages are supported.

Table 5-17. Auto-Negotiation Link Partner Ability Register (ANLPAR) (BASE Page), Address 0x0005

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RO	**Next Page Indication:** 0 = Link Partner does not desire Next Page Transfer 1 = Link Partner desires Next Page Transfer
14	ACK	0, RO	**Acknowledge:** 1 = Link Partner acknowledges reception of the ability data word 0 = Not acknowledged. The Auto-Negotiation state machine will automatically control the this bit based on the incoming FLP bursts.
13	RF	0, RO	**Remote Fault:** 1 = Remote Fault indicated by Link Partner 0 = No Remote Fault indicated by Link Partner
12	RESERVED	0, RO	**RESERVED for Future IEEE use:** Write as 0, read as 0
11	ASM_DIR	0, RO	**ASYMMETRIC PAUSE:** 1 = Asymmetric pause is supported by the Link Partner 0 = Asymmetric pause is not supported by the Link Partner
10	PAUSE	0, RO	**PAUSE:** 1 = Pause function is supported by the Link Partner 0 = Pause function is not supported by the Link Partner
9	100B-T4	0, RO	**100Base-T4 Support:** 1 = 100Base-T4 is supported by the Link Partner 0 = 100Base-T4 is not supported by the Link Partner
8	100B-TX_FD	0, RO	**100Base-TX Full Duplex Support:** 1 = 100Base-TX Full Duplex is supported by the Link Partner 0 = 100Base-TX Full Duplex is not supported by the Link Partner
7	100B-TX	0, RO	**100Base-TX Support:** 1 = 100Base-TX is supported by the Link Partner 0 = 100Base-TX is not supported by the Link Partner
6	10B-T_FD	0, RO	**10Base-T Full Duplex Support:** 1 = 10Base-T Full Duplex is supported by the Link Partner 0 = 10Base-T Full Duplex is not supported by the Link Partner
5	10B-T	0, RO	**10Base-T Support:** 1 = 10Base-T is supported by the Link Partner 0 = 10Base-T is not supported by the Link Partner
4:0	Selector	0 0000, RO	**Protocol Selection Bits:** Link Partner's binary encoded protocol selector.

5.3.1.7 Auto-Negotiate Expansion Register (ANER)

This register contains additional Local Device and Link Partner status information.

Table 5-18. Auto-Negotiate Expansion Register (ANER), Address 0x0006

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:5	RESERVED	0, RO	**RESERVED:** Writes ignored, Read as 0.
4	PDF	0, RO	**Parallel Detection Fault:** 1 = Fault detected via the Parallel Detection function 0 = No fault detected
3	LP_NP_ABLE	0, RO	**Link Partner Next Page Able:** 1 = Link Partner does support Next Page 0 = Link Partner does not support Next Page
2	NP_ABLE	1, RO/P	**Next Page Able:** 1 = Indicates local device is able to send additional *Next Pages* 0 = Indicates local device is not able to send additional *Next Pages*
1	PAGE_RX	0, RO/COR	**Link Code Word Page Received:** 1 = Link Code Word has been received, cleared on a read 0 = Link Code Word has not been received
0	LP_AN_ABLE	0, RO	**Link Partner Auto-Negotiation Able:** 1 = indicates that the Link Partner supports Auto-Negotiation 0 = indicates that the Link Partner does not support Auto-Negotiation

5.3.1.8 Auto-Negotiate Next Page Transmit Register (ANNPTR)

This register contains the next page information sent by this device to its Link Partner during Auto-Negotiation.

Table 5-19. Auto-Negotiation Next Page Transmit Register (ANNPTR), Address 0x0007

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RW	**Next Page Indication:** 0 = No other Next Page Transfer desired 1 = Another Next Page desired
14	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0
13	MP	1, RW	**Message Page:** 1 = Message Page 0 = Unformatted Page
12	ACK2	0, RW	**Acknowledge2:** 1 = Will comply with message 0 = Cannot comply with message Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received.
11	TOG_TX	0, RO	**Toggle:** 1 = Value of toggle bit in previously transmitted Link Code Word was 0 0 = Value of toggle bit in previously transmitted Link Code Word was 1 Toggle is used by the Arbitration function within Auto-Negotiation to synchronize with the Link Partner during Next Page exchange. This bit always takes the opposite value of the Toggle bit in the previously exchanged Link Code Word.
10:0	CODE	000 0000 0001, RW	This field represents the code field of the next page transmission. If the MP bit is set (bit 13 of this register), then the code is interpreted as a *Message Page*, as defined in annex 28C of IEEE 802.3u. Otherwise, the code is interpreted as an *Unformatted Page*, and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

5.3.1.9 Auto-Negotiation Link Partner Ability Next Page Register (ANLNPTR)

This register contains the next page information sent by this device to its Link Partner during Auto-Negotiation.

Table 5-20. Auto-Negotiation Link Partner Ability Register Next Page (ANLNPTR), Address 0x0008

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	NP	0, RO	**Next Page Indication:** 1 = No other Next Page Transfer desired 0 = Another Next Page desired
14	ACK	0, RO	**Acknowledge:** 1 = Link Partner acknowledges reception of the ability data word 0 = Not acknowledged The Auto-Negotiation state machine automatically controls this bit based on the incoming FLP bursts. Software should not attempt to write to this bit.
13	MP	1, RO	**Message Page:** 1 = Message Page 0 = Unformatted Page
12	ACK2	0, RO	**Acknowledge2:** 1 = Link Partner has the ability to comply to next-page message 0 = Link Partner cannot comply to next-page message Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received.
11	Toggle	0, RO	**Toggle:** 1 = Value of toggle bit in previously transmitted Link Code Word was 0 0 = Value of toggle bit in previously transmitted Link Code Word was 1 Toggle is used by the Arbitration function within Auto-Negotiation to synchronize with the Link Partner during Next Page exchange. This bit always takes the opposite value of the Toggle bit in the previously exchanged Link Code Word.
10:0	CODE	000 0000 0001, RO	**Code:** This field represents the code field of the next page transmission. If the MP bit is set (bit 13 of this register), then the code is interpreted as a Message Page, as defined in annex 28C of IEEE 802.3u. Otherwise, the code is interpreted as an Unformatted Page, and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

5.3.1.10 Control register 1 (CR1)

Table 5-21. Control Register 1 (CR1), Address 0x0009

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:10	RESERVED	1, RW	**RESERVED**
9	RMII Enhanced Mode	0, RW	**RMII Enhanced Mode:** 1 = Enable RMII Enhanced Mode 0 = RMII operates in normal mode In normal mode, If the line is not idle CRS_DV goes high. As soon as the False Carrier is detected, RX_ER is asserted and RXD is set to “2”. This situation remains for the duration of the receive event. While in enhanced mode, CRS_DV is disqualified and de-asserted when the False Carrier detected. This status also remains for the duration of the receive event. In addition in normal mode, the start of the packet is intact. Each symbol error is indicated by setting RX_ER high. The data on RXD is replaced with “1” starting with the first symbol error. While in enhanced mode, the CRS_DV is de-asserted with the first symbol error.
8	TDR AUTORUN	0, RW	**TDR Auto Run at link down:** 1 = Enable execution of TDR procedure after link down event 0 = Disable automatic execution of TDR
7	Link Loss Recovery	0, RW	**Link Loss Recovery:** 1 = Enable Link Loss Recovery mechanism. This mode allow recovery from short interference and continue to hold the link up for period of additional few mSec till the short interference will gone and the signal is OK. 0 = Normal Link Loss operation. Link status will go down approximately 250µs from signal loss.
6	Fast Auto MDI-X	0, RW	**Fast Auto MDI/MDIX:** 1 = Enable Fast Auto MDI/MDIX mode 0 = Normal Auto MDI/MDIX mode. If both link partners are configured to work in Force 100Base-TX mode (Auto-Negotiation is disabled), this mode enables Automatic MDI/MDIX resolution in a short time.
5	Robust Auto MDI-X	0, RW	**Robust Auto MDI-X :** 1 = Enable Robust Auto MDI/MDIX resolution 0 = Normal Auto MDI/MDIX mode If link partners are configured to operational modes that are not supported by normal Auto MDI/MDIX mode (like Auto-Neg versus Force 100Base-TX or Force 100Base-TX versus Force 100Base-TX), this Robust Auto MDI/MDIX mode allows MDI/MDIX resolution and prevents deadlock.
4	Fast AN En	0, RW	**Fast AN En:** 1 = Enable Fast Auto-Negotiation mode – The PHY auto-negotiates using Timer setting according to Fast AN Sel bits (bits 3:2 this register) 0 = Disable Fast Auto-Negotiation mode – The PHY auto-negotiates using normal Timer setting Adjusting these bits reduces the time it takes to Auto-negotiate between two PHYs. **Note:** When using this option care must be taken to maintain proper operation of the system. While shortening these timer intervals may not cause problems in normal operation, there are certain situations where this may lead to problems.

Table 5-21. Control Register 1 (CR1), Address 0x0009 (continued)

<table>
<tr><th>BIT</th><th>BIT NAME</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td>3:2</td><td>Fast AN Sel</td><td>0, RW</td><td>Fast Auto-Negotiation Select bits:
<table>
<tr><th>Fast AN Select</th><th>Break Link Timer</th><th>Link Fail Inhibit Timer</th><th>Auto-Neg Wait Timer</th></tr>
<tr><td><00></td><td>80</td><td>50</td><td>35</td></tr>
<tr><td><01></td><td>120</td><td>75</td><td>50</td></tr>
<tr><td><10></td><td>240</td><td>150</td><td>100</td></tr>
<tr><td><11></td><td>NA</td><td>NA</td><td>NA</td></tr>
</table>
Adjusting these bits reduces the time it takes to Auto-negotiate between two PHYs. In Fast AN mode, both PHYs should be configured to the same configuration. These 2 bits define the duration for each state of the Auto Negotiation process according to the table above. The new duration time must be enabled by setting “Fast AN En” - bit 4 of this register. Note: Using this mode in cases where both link partners are not configured to the same Fast Auto-negotiation configuration might produce scenarios with unexpected behavior.</td></tr>
<tr><td>1</td><td>Fast RXDV Detection</td><td>0, RW</td><td>Fast RXDV Detection:
1 = Enable assertion high of RX_DV on receive packet due to detection of /J/ symbol only. If a consecutive /K/ does not appear, RX_ER is generated.
0 = Disable Fast RX_DV detection. The PHY operates in normal mode - RX_DV assertion after detection of /J/K/.</td></tr>
<tr><td>0</td><td>RESERVED</td><td>1, RW</td><td>RESERVED</td></tr>
</table>

5.3.1.11 Control Register 2 (CR2)

Table 5-22. Control Register 2 (CR2), Address 0x000A

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	100BT Force Far-End Link drop	0, RW	**100BT Force Far-End Link drop:** Writing a 1 asserts the 100BT Force Far-End link drop mode. In this mode (only valid in force 100BT), the PHY disables the TX upon link drop to allow the far-end peer to drop its link as well, thus allowing both link partners be aware of the system link failure. This mode exceeds the standard definition of force 100BT.
15	RESERVED	0, RW	**RESERVED**
14	RESERVED	0, RW	**RESERVED**
13:7	RESERVED	000 0010, RW	**RESERVED**
6	Fast Link-Up in Parallel Detect	0, RW	**Fast Link-Up in Parallel Detect Mode:** 1 = Enable Fast Link-Up time During Parallel Detection 0 = Normal Parallel Detection link establishment In Fast Auto MDI-X and in Robust Auto MDI-X modes (bits 6 and 5 in register CR1), this bit is automatically set.
5	Extended FD Ability	0, RW	**Extended Full-Duplex Ability:** 1 = Force Full-Duplex while working with link partner in forced 100B-TX. When the PHY is set to Auto-Negotiation or Force 100B-TX and the link partner is operated in Force 100B-TX, the link is always Full Duplex 0 = Disable Extended Full Duplex Ability. Decision to work in Full Duplex or Half Duplex mode follows IEEE specification.
4	Enhanced LED Link	0, RW	**Enhanced LED Link Functionality:** 1 = LED Link is ON only when link is established in 100B-TX Full Duplex mode. 0 = LED Link is ON when link is established. Enabling Enhanced LED Link overrides the LED blinking functionality of the PHYCR register (0x0019) bit 5. The Link LED will not blink for activity when Enhanced LED Link is enabled.
3	Isolate MII in 100BT HD	0, RW	**Isolate MII outputs when FD Link @ 100BT is not achievable:** 1 = When HD link established in 100B-TX MII outputs are isolated 0 = Normal MII outputs operation
2	RXERR During IDLE	1, RW	**Detection of Receive Symbol Error During IDLE State:** 1 = Enable detection of Receive symbol error during IDLE state 0 = Disable detection of Receive symbol error during IDLE state.
1	Odd-Nibble Detection Disable	0, RW	**Detection of Transmit Error:** 1 = Disable detection of transmit error in odd-nibble boundary 0 = Enable detection of de-assertion of TX_EN on an odd-nibble boundary. In this case TX_EN is extended by one additional TX_CLK cycle and behaves as if TX_ER were asserted during that additional cycle.
0	RMII Receive Clock	0, RW	**RMII Receive Clock:** 1 = RMII Data (RXD [1:0]) is sampled and referenced to RX_CLK 0 = RMII Data (RXD [1:0]) is sampled and referenced to XI

5.3.1.12 Control Register 3 (CR3)

Table 5-23. Control Register 3 (CR3), Address 0x000B

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:11	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
10	Fast Link Down Mode	0, RW	**Drop the link based on descrambler link loss**, This option can be enabled in parallel to the other fast link down modes in bit [3:0] 1= Drop the link on descrambler link loss 0= Do not drop the link on descrambler link loss
9:7	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
6	Polarity Swap	0, RW	**Polarity Swap:** 1 = Normal polarity 0 = Inverted polarity on both pairs: TPTD+ ↔ TPTD-, TPRD+ ↔ TPRD- **Port Mirror function:** To Enable port mirroring, set bit 5 and this bit high.
5	MDI/MDIX Swap	0, RW	MDI/MDIX Swap: 1 = Swap MDI pairs (Receive on TPTD pair, Transmit on TPRD pair) 0 = MDI pairs normal (Receive on TPRD pair, Transmit on TPTD pair) **Port Mirror function:** To Enable port mirroring, set this bit and bit 6 high.
4	RESERVED	0, RW	**RESERVED**
3:0	Fast Link Down Mode	0, RW	**Fast Link Down Modes:** Bit 3 Drop the link based on **RX Error count** of the MII interface – When a predefined number of 32 RX Error occurrences in a 10µs interval is reached, the link will be dropped. Bit 2 Drop the link based on **MLT3 Errors count** (Violation of the MLT3 coding in the DSP output) – When a predefined number of 20 MLT3 Error occurrences in a 10µs interval is reached, the link will be dropped. Bit 1 Drop the link based on **Low SNR Threshold** – When a predefined number of 20 Threshold crossing occurrences in a 10µs interval is reached, the link will be dropped. Bit 0 Drop the link based on **Signal/Energy loss** indication – When the Energy detector indicates Energy Loss, the link will be dropped. Typical reaction time is 10µs. The Fast Link Down function is an OR of all these 5 options (bits 10, 3:0), so the designer can enable combinations of these conditions.

5.3.1.13 Extended Register Addressing

REGCR (0x000D) and ADDAR (0x000E) allow read/write access to the extended register set (addresses above 0x001F) using indirect addressing.

- **REGCR [15:14] = 00:** A write to ADDAR modifies the extended register set address register. This address register must be initialized in order to access any of the registers within the extended register set.
- **REGCR [15:14] = 01:** A read/write to ADDAR operates on the register within the extended register set selected (pointed to) by the value in the address register. The address register contents (pointer) remain unchanged.
- **REGCR [15:14] = 10:** A read/write to ADDAR operates on the register within the extended register set selected (pointed to) by the value in the address register. After that access is complete, for both reads and writes, the value in the address register is incremented.
- **REGCR [15:14] = 11:** A read/write to ADDAR operates on the register within the extended register set selected (pointed to) by the value in the address register. After that access is complete, for write accesses only, the value in the address register is incremented. For read accesses, the value of the address register remains unchanged.

5.3.1.13.1 Register Control Register (REGCR)

This register is the MDIO Manageable MMD access control. In general, register REGCR (4:0) is the device address DEVAD that directs any accesses of the ADDAR (0x000E) register to the appropriate MMD. REGCR also contains selection bits for auto increment of the data register. This register contains the device address to be written to access the extended registers. Write 0x1F into bits 4:0 of this register. REGCR also contains selection bits (15:14) for the address auto-increment mode of ADDAR.

Table 5-24. Register Control Register (REGCR), address 0x000D

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:14	Function	0, RW	00 = Address 01 = Data, no post increment 10 = Data, post increment on read and write 11 = Data, post increment on write only
13:5	RESERVED	0, RO	**RESERVED: Writes ignored, read as 0**.
4:0	DEVAD	0, RW	Device Address: In general, these bits [4:0] are the device address DEVAD that directs any accesses of ADDAR register (0x000E) to the appropriate MMD. Specifically, the TLK10xL uses the vendor specific DEVAD [4:0] = “11111” for accesses. All accesses through registers REGCR and ADDAR should use this DEVAD. Transactions with other DEVAD are ignored.

5.3.1.13.2 Address or Data Register (ADDAR)

This register is the address/data MMD register. ADDAR is used in conjunction with REGCR register (0x000D) to provide the access by indirect read/write mechanism to the extended register set.

Table 5-25. Data Register (ADDAR), address 0x000E

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	Addr/data	0, RW	If REGCR register 15:14 = 00, holds the MMD DEVAD's address register, otherwise holds the MMD DEVAD's data register

5.3.1.14 Fast Link Down Status Register

Table 5-26. Fast Link Down Status (FLDS), Address 0x000F

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:9	RESERVED	0, RO	**RESERVED**
8:4	Fast Link Down Status[4:0]	0, RO, LH	**Status Registers** that latch high each time a given Fast Link Down mode is activated and causes a link drop (assuming this criterion was enabled): Bit 4 Descrambler Loss Sync Bit 3 RX Errors Bit 2 MLT3 Errors Bit 1 SNR level Bit 0 Signal/Energy Lost
3:0	RESERVED	0, RO	**RESERVED**

5.3.1.15 PHY Status Register (PHYSTS)

This register provides quick access to commonly accessed PHY control status and general information.

Table 5-27. PHY Status Register (PHYSTS), Address 0x0010

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
14	MDI-X Mode	0,RO	**MDI-X mode as reported by the Auto-Negotiation state machine:** 1 = MDI pairs swapped (Receive on TPTD pair, Transmit on TPRD pair) 0 = MDI pairs normal (Receive on TRD pair, Transmit on TPTD pair) This bit will be affected by the settings of the AMDIX_EN and FORCE_MDIX bits in the PHYCR register. When MDIX is enabled, but not forced, this bit will update dynamically as the Auto-MDIX algorithm swaps between MDI and MDI-X configurations.
13	Receive Error Latch	0,RO/LH	**Receive Error Latch:** 1 = Receive error event has occurred since last read of RXERCNT register (0x0015) 0 = No receive error event has occurred This bit will be cleared upon a read of the RECR register
12	Polarity Status	0,RO	**Polarity Status:** 1 = Inverted Polarity detected 0 = Correct Polarity detected This bit is a duplication of bit 4 in the 10BTSCR register (0x001A). This bit will be cleared upon a read of the 10BTSCR register, but not upon a read of the PHYSTS register.
11	False Carrier Sense Latch	0,RO/LH	**False Carrier Sense Latch:** 1 = False Carrier event has occurred since last read of FCSCR register (0x0014) 0 = No False Carrier event has occurred This bit will be cleared upon a read of the FCSR register.
10	Signal Detect	0,RO/LL	**Signal Detect:** Active high 100Base-TX unconditional Signal Detect indication from PMD
9	Descrambler Lock	0,RO/LL	**Descrambler Lock:** Active high 100Base-TX Descrambler Lock indication from PMD

Table 5-27. PHY Status Register (PHYSTS), Address 0x0010 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
8	Page Received	0,RO	**Link Code Word Page Received:** 1 = A new Link Code Word Page has been received. This bit is a duplicate of Page Received (bit 1) in the ANER register and it is cleared on read of the ANER register (0x0006). 0 = Link Code Word Page has not been received. This bit will not be cleared upon a read of the PHYSTS register.
7	MII Interrupt	0,RO	**MII Interrupt Pending:** 1 = Indicates that an internal interrupt is pending. Interrupt source can be determined by reading the MISR Register (0x0012). Reading the MISR will clear this Interrupt bit indication. 0 = No interrupt pending
6	Remote Fault	0,RO	**Remote Fault:** 1 = Remote Fault condition detected. Fault criteria: notification from Link Partner of Remote Fault via Auto-Negotiation. Cleared on read of BMSR register (0x0001) or by reset. 0 = No remote fault condition detected
5	Jabber Detect	0,RO	**Jabber Detect:** 1 = Jabber condition detected. This bit has meaning only in 10 Mb/s mode. This bit is a duplicate of the Jabber Detect bit in the BMSR register (0x0001). 0 = No Jabber This bit will not be cleared upon a read of the PHYSTS register.
4	Auto-Neg Status	0,RO	**Auto-Negotiation Status:** 1 = Auto-Negotiation complete 0 = Auto-Negotiation not complete
3	MII Loopback Status	0,RO	**MII Loopback:** 1 = Loopback active (enabled) 0 = Normal operation
2	Duplex Status	0,RO	**Duplex Status:** 1 = Full duplex mode 0 = Half duplex mode This bit indicates duplex status and is determined from Auto-Negotiation or Forced Modes. Therefore, it is only valid if Auto-Negotiation is enabled and complete and there is a valid link or if Auto-Negotiation is disabled and there is a valid link.
1	Speed Status	0,RO	**Speed Status:** 1 = 10 Mb/s mode 0 = 100 Mb/s mode This bit indicates the status of the speed and is determined from Auto-Negotiation or Forced Modes. Speed Status is only valid if Auto-Negotiation is enabled and complete and there is a valid link or if Auto-Negotiation is disabled and there is a valid link.
0	Link Status	0,RO	**Link Status:** 1 = Valid link established (for either 10 or 100 Mb/s operation). This bit is a duplicate of the Link Status bit in the BMSR register (0x0001). 0 = Link not established This bit will not be cleared upon a read of the PHYSTS register.

5.3.1.16 PHY Specific Control Register (PHYSCR)

This register implements the PHY Specific Control register. This register allows access to general functionality inside the PHY to enable operation in reduced power modes and control interrupt mechanism.

Table 5-28. PHY Specific Control Register (PHYSCR), Address 0x0011

<table>
<tr><th>BIT</th><th>BIT NAME</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td>15</td><td>Disable PLL</td><td>0,RW</td><td>Disable PLL:
1 = Disable internal clocks Circuitries
0 = Normal mode of operation
Note: Clock Circuitry can be disabled only in IEEE power-down mode</td></tr>
<tr><td>14</td><td>PS Enable</td><td>0,RW</td><td>Power Save Modes Enable:
1 = Enable power save modes
0 = Normal mode of operation</td></tr>
<tr><td>13:12</td><td>PS Modes</td><td>00,RW</td><td>Power Save Modes:
<table>
<tr><th>Power Mode</th><th>Name</th><th>Description</th></tr>
<tr><td><00></td><td>Normal</td><td>Normal operation mode. PHY is fully functional</td></tr>
<tr><td><01></td><td>IEEE power down</td><td>Low Power mode that shut down all internal circuitry beside SMI functionality.</td></tr>
<tr><td><10></td><td>Active Sleep</td><td>Low Power Active Energy Saving mode
that shut down all internal circuitry beside SMI and energy detect functionalities. In this mode the PHY sends NLP every 1.4 Sec to wake up link-partner. Automatic power-up is done when link partner is detected.</td></tr>
<tr><td><11></td><td>Passive Sleep</td><td>Low Power Energy Saving mode
that shut down all internal circuitry beside SMI and energy detect functionalities. Automatic power-up is done when link partner is detected.</td></tr>
</table></td></tr>
<tr><td>11</td><td>Scrambler Bypass</td><td>0,RW</td><td>Scrambler Bypass:
1 = Scrambler bypass enabled
0 = Scrambler bypass disabled</td></tr>
<tr><td>10</td><td>RESERVED</td><td>0, RO</td><td>RESERVED: Writes ignored, read as 0.</td></tr>
<tr><td>9:8</td><td>Loopback FIFO Depth</td><td>01,RW</td><td>Far-End Loopback FIFO Depth:
00 = 4 nibbles FIFO
01 = 5 nibbles FIFO
10 = 6 nibbles FIFO
11 = 8 nibbles FIFO
This FIFO is used to adjust RX (recovered) clock rate to TX clock rate. FIFO depth need to be set based on expected maximum packet size and clock accuracy. Default value sets to 5 nibbles.</td></tr>
<tr><td>7:5</td><td>RESERVED</td><td>000, RO</td><td>RESERVED: Writes ignored, read as 0.</td></tr>
<tr><td>4</td><td>COL FD Enable</td><td>0, RW</td><td>Collision in Full-Duplex Mode:
1 = Enable generating Collision signaling in Full Duplex
0 = Disable Collision indication in Full Duplex mode. Collision will be active in Half Duplex only.</td></tr>
<tr><td>3</td><td>INT POL</td><td>1,RW</td><td>Interrupt Polarity:
1 = Steady state (normal operation) is 1 logic and during interrupt is 0 logic.
0 = Steady state (normal operation) is 0 logic and during interrupt is 1 logic.</td></tr>
<tr><td>2</td><td>tint</td><td>0,RW</td><td>Test Interrupt:
1 = Generate an interrupt
0 = Do not generate interrupt
Forces the PHY to generate an interrupt to facilitate interrupt testing. Interrupts will continue to be generated as long as this bit remains set.</td></tr>
</table>

Table 5-28. PHY Specific Control Register (PHYSCR), Address 0x0011 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
1	INT_EN	0,RW	**Interrupt Enable:** 1 = Enable event based interrupts 0 = Disable event based interrupts Enable interrupt dependent on the event enables in the MISR register (0x0012).
0	INT_OE	0,RW	**Interrupt Output Enable:** 1 = $\overline{\text{INT}}$ / $\overline{\text{PWDN}}$ is an Interrupt Output 0 = $\overline{\text{INT}}$ / $\overline{\text{PWDN}}$ is a Power Down Enable active low interrupt events via the $\overline{\text{INT}}$ / $\overline{\text{PWDN}}$ pin by configuring the $\overline{\text{INT}}$ / $\overline{\text{PWDN}}$ pin as an output.

5.3.1.17 MII Interrupt Status Register 1 (MISR1)

This register contains events status and enables for the interrupt function. If an event has occurred since the last read of this register, the corresponding status bit will be set. If the corresponding enable bit in the register is set, an interrupt will be generated if the event occurs. The PHYSCR register (0x0011) bits 1 and 0 must also be set to allow interrupts. The status indications in this register will be set even if the interrupt is not enabled.

Table 5-29. MII Interrupt Status Register 1 (MISR1), Address 0x0012

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:14	RESERVED	00, RO	**RESERVED:** Writes ignored, read as 0.
13	Link Status Changed INT	0,RO, COR	**Change of Link Status interrupt:** 1 = Change of link status interrupt is pending 0 = No change of link status
12	Speed Changed INT	0,RO, COR	**Change of Speed Status interrupt:** 1 = Change of speed status interrupt is pending 0 = No change of speed status
11	Duplex Mode Changed INT	0,RO, COR	**Change of duplex status interrupt:** 1 = Duplex status change interrupt is pending 0 = No change of duplex status
10	Auto-Negotiation Completed INT	0,RO, COR	**Auto-Negotiation Complete interrupt:** 1 = Auto-negotiation complete interrupt is pending. 0 = No Auto-negotiation complete event is pending
9	FC HF INT	0,RO, COR	**False Carrier Counter half-full interrupt:** 1 = False carrier counter (Register FCSCR, address 0x0014) exceeds half-full interrupt is pending 0 = False carrier counter half-full event is not pending
8	RE HF INT	0,RO, COR	**Receive Error Counter half-full interrupt:** 1 = Receive error counter (Register RECR, address 0x0015) exceeds half full interrupt is pending 0 = No Receive error counter half full event pending
7:6	RESERVED	00, RO	**RESERVED:** Writes ignored, read as 0.
5	Link Status Changed EN	0, RW	**Enable** Interrupt on change of link status
4	Speed Changed EN	0, RW	**Enable** Interrupt on change of speed status
3	Duplex Mode Changed EN	0, RW	**Enable** Interrupt on change of duplex status
2	Auto-Negotiation Completed EN	0, RW	**Enable** Interrupt on Auto-negotiation complete event
1	FC HF EN	0, RW	**Enable** Interrupt on False Carrier Counter Register half-full event
0	RE HF EN	0, RW	**Enable** Interrupt on Receive Error Counter Register half-full event

5.3.1.18 MII Interrupt Status Register 2 (MISR2)

This register contains events status and enables for the interrupt function. If an event has occurred since the last read of this register, the corresponding status bit will be set. If the corresponding enable bit in the register is set, an interrupt will be generated if the event occurs. The PHYSCR register (0x0011) bits 1 and 0 must also be set to allow interrupts. The status indications in this register will be set even if the interrupt is not enabled.

Table 5-30. MII Interrupt Status Register 2 (MISR2), Address 0x0013

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
14	AN Error INT	0,RO, COR	**Auto-Negotiation Error Interrupt:** 1 = Auto-negotiation error interrupt is pending 0 = No Auto-negotiation error event pending
13	Page Rec INT	0,RO, COR	**Page Receive Interrupt:** 1 = Page has been received 0 = Page has not been received
12	Loopback FIFO OF/UF INT	0,RO, COR	**Loopback FIFO Overflow/Underflow Event Interrupt:** 1 = FIFO Overflow/Underflow event interrupt pending 0 = No FIFO Overflow/Underflow event pending
11	MDI Crossover Changed INT	0,RO, COR	**MDI/MDIX Crossover Status Changed Interrupt:** 1 = MDI crossover status changed interrupt is pending 0 = MDI crossover status has not changed
10	Sleep Mode INT	0,RO, COR	**Sleep Mode Event Interrupt:** 1 = Sleep Mode event interrupt is pending 0 = No sleep mode event pending
9	Polarity Changed INT	0,RO, COR	**Polarity Changed Interrupt:** 1 = Data polarity changed interrupt pending 0 = No Data polarity event pending
8	Jabber Detect INT	0,RO	**Jabber Detect Event Interrupt:** 1 = Jabber detect event interrupt pending 0 = No Jabber detect event pending
7	RESERVED	0,RW	**RESERVED:** Writes ignored, read as 0
6	AN Error EN	0,RW	**Enable** Interrupt on Auto-Negotiation error event
5	Page Rec EN	0,RW	**Enable** Interrupt on page receive event
4	Loopback FIFO OF/UF EN	0,RW	**Enable** Interrupt on loopback FIFO overflow/underflow event
3	MDI Crossover Changed EN	0,RW	**Enable** Interrupt on change of MDI/X status
2	Sleep Mode Event EN	0,RW	**Enable** Interrupt sleep mode event
1	Polarity Changed EN	0,RW	**Enable** Interrupt on change of polarity status
0	Jabber Detect EN	0,RW	**Enable** Interrupt on Jabber detection event

5.3.1.19 False Carrier Sense Counter Register (FCSCR)

This counter provides information required to implement the "False Carriers" attribute within the MAU managed object class of Clause 30 of the IEEE 802.3u specification.

Table 5-31. False Carrier Sense Counter Register (FCSCR), Address 0x0014

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	RESERVED	0000 0000, RO	**RESERVED:** Writes ignored, read as 0
7:0	FCSCNT	0,RO / COR	**False Carrier Event Counter:** This 8-bit counter increments on every false carrier event. This counter stops when it reaches its maximum count (FFh). When the counter exceeds half full (7Fh), an interrupt event is generated. This register is cleared on read.

5.3.1.20 Receiver Error Counter Register (RECR)

This counter provides information required to implement the "Symbol Error During Carrier" attribute within the PHY managed object class of Clause 30 of the IEEE 802.3u specification.

Table 5-32. Receiver Error Counter Register (RECR), Address 0x0015

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	RX Error Count	0, RO, / COR	**RX_ER Counter:** When a valid carrier is present (only while RXDV is set), and there is at least one occurrence of an invalid data symbol, this 16-bit counter increments for each receive error detected. The RX_ER counter does not count in MII loopback mode. The counter stops when it reaches its maximum count of FFFFh. When the counter exceeds half-full (7FFFh), an interrupt is generated. This register is cleared on read.

5.3.1.21 BIST Control Register (BISCR)

This register is used for Build-In Self Test (BIST) configuration. The BIST functionality provides Pseudo Random Bit Stream (PRBS) mechanism including packet generation generator and checker. Selection of the exact loopback point in the signal chain is also done in this register.

Table 5-33. BIST Control Register (BISCR), Address 0x0016

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0
14	PRBS Count Mode	0, RW	**PRBS Single/Continues Mode:** 1 = Continuous mode, the PRBS counters reaches max count value, pulse is generated and counter starts counting from zero again. 0 = Single mode, When BIST Error Counter reaches its max value, PRBS checker stops counting.
13	Generate PRBS Packets	0, RW	**Generated PRBS Packets:** 1 = When packet generator is enabled, generate continuous packets with PRBS data. When packet generator is disabled, PRBS checker is still enabled. 0 = When packet generator is enabled, generate single packet with constant data. PRBS gen/check is disabled.
12	Packet Generation Enable	0, RW	**Packet Generation Enable:** 1 = Enable packet generation with PRBS data 0 = Disable packet generator
11	PRBS Checker Lock	0,RO	**PRBS Checker Lock Indication:** 1 = PRBS checker is locked and synced on received bit stream 0 = PRBS checker is not locked
10	PRBS Checker Sync Loss	0,RO,LH	**PRBS Checker Sync Loss Indication:** 1 = PRBS checker lose sync on received bit stream – This is an error indication 0 = PRBS checker is not locked
9	Packet Gen Status	0,RO	**Packet Generator Status Indication:** 1 = Packet Generator is active and generate packets 0 = Packet Generator is off
8	Power Mode	0,RO	**Sleep Mode Indication:** 1 = Indicate that the PHY is in normal power mode 0 = Indicate that the PHY is in one of the sleep modes, either active or passive
7	RESERVED	0, RO	RESERVED: Writes ignored, read as 0.
6	Transmit in MII Loopback	0, RW	**Transmit Data in MII Loop-back Mode (valid only at 100BT):** 1 = Enable transmission of the data from the MAC received on the TX pins to the line in parallel to the MII loopback to RX pins. This bit may be set only in MII Loopback mode – setting bit 14 in BMCR register (0x0000). 0 = Data is not transmitted to the line in MII loopback
5	RESERVED	0, RO	**RESERVED:** Must be 0

Table 5-33. BIST Control Register (BISCR), Address 0x0016 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
4:0	Loopback Mode	0, RW	**Loop-back Mode Select:** The PHY provides several options for Loopback that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the TLK10xL digital and analog data path Near-end Loopback 00001 = PCS Input Loopback 00010 = PCS Output Loopback 00100 = Digital Loopback 01000 = Analog Loopback (requires 100Ω termination) Far-end Loopback: 10000 = Reverse Loopback

5.3.1.22 RMII Control and Status Register (RCSR)

This register configures the RMII Mode of operation. When RMII mode is disabled, the RMII functionality is bypassed.

Table 5-34. RMII Control and Status Register (RCSR), Address 0x0017

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:6	RESERVED	0000 0000 00, RO	**RESERVED:** Writes ignored, read as 0.
5	RMII Mode	0, RW, Pin_Strap	**RMII Mode Enable:** RMII Mode is operational if device powered up in RMII mode (pin_strap) and 50Mhz clock present. *Please note*, that in order to switch from RMII to MII and vise versa, the PHY must initialize after power up in RMII mode (Strap is '1' and REF_CLK is 50MHz). If the PHY initializes in MII mode, this bit has no effect. 1 = Enable RMII (Reduced MII) mode of operation 0 = Enable MII mode of operation
4	RMII Revision Select	0, RW	**RMII Revision Select:** 1 = (RMII revision 1.0) CRS_DV will remain asserted until final data is transferred. CRS_DV will not toggle at the end of a packet. 0 = (RMII revision 1.2) CRS_DV will toggle at the end of a packet to indicate de-assertion of CRS.
3	RMII OVFL Status	0, COR	**RX FIFO Over Flow Status:** 1 = Normal 0 = Overflow detected
2	RMII OVFL Status	0, COR	**RX FIFO Under Flow Status:** 1 = Normal 0 = Underflow detected
1:0	ELAST_BUF	01, RW	**Receive Elasticity Buffer Size:** This field controls the Receive Elasticity Buffer which allows for frequency variation tolerance between the 50MHz RMII clock and the recovered data. The following values indicate the tolerance in bits for a single packet. The minimum setting allows for standard Ethernet frame sizes at ±50ppm accuracy for both RMII and Receive clocks. For greater frequency tolerance the packet lengths may be scaled (for ±100ppm, divide the packet lengths by 2). 00 = 14 bit tolerance (up to 16800 byte packets) 01 = 2 bit tolerance (up to 2400 byte packets) 10 = 6 bit tolerance (up to 7200 byte packets) 11 = 10 bit tolerance (up to 12000 byte packets)

5.3.1.23 LED Control Register (LEDCR)

This register provides the ability to directly manually control the Link LED output.

Table 5-35. LED Control Register (LEDCR), Address 0x0018

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:11	RESERVED	0000 0, ro	**RESERVED:** Writes ignored, read as 0.
10:9	Blink Rate	10, RW	**LED Blinking Rate (ON/OFF duration):** 00 = 20Hz (50mSec) 01 = 10Hz (100mSec) 10 = 5Hz (200mSec) 11 = 2Hz (500mSec)
8	RESERVED	RO	RESERVED
7	LED Link Polarity	0, RW, Pin_Strap	**LED Link Polarity Setting:** 1 = Active High polarity setting 0 = Active Low polarity setting The Link LED polarity is defined by the strap value of this pin. If the pin is strapped high via a pull-up resistor, the LED will be active low. If the pin is strapped low via a pull-down resistor, the LED will be active high. This register allows override of the strapping value.
6	RESERVED	RO	RESERVED
5	RESERVED	RO	RESERVED
4	Drive Link LED	0, RW	**Drive LED Link to the forced On/Off setting defined in bit 1:** 1 = Drive value of On/Off bit onto LED_LINK output pin 0 = Normal operation
3	RESERVED	RO	RESERVED
2	RESERVED	RO	RESERVED
1	Link LED On/Off Setting	0, RW	Value to force on Link LED output
0	RESERVED	RO	RESERVED

5.3.1.24 PHY Control Register (PHYCR)

This register provides the ability to control and set general functionality inside the PHY.

Table 5-36. PHY Control Register (PHYCR), Address 0x0019

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	Auto MDI/X Enable	1, RW, Pin_Strap	**Auto-MDIX Enable:** 1 = Enable Auto-negotiation Auto-MDIX capability 0 = Disable Auto- negotiation Auto-MDIX capability
14	Force MDI/X	0, RW	**Force MDIX:** 1 = Force MDI pairs to cross. (Receive on TPTD pair, Transmit on TPRD pair) 0 = Normal operation. (Transmit on TPTD pair, Receive on TPRD pair)
13	Pause RX Status	0, RO	**Pause Receive Negotiated Status:** Indicates that pause receive should be enabled in the MAC. Based on bits [11:10] in ANAR register and bits [11:10] in ANLPAR register settings. This function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, “Pause Resolution”, only if the Auto-Negotiated Highest Common Denominator is a full duplex technology.
12	Pause TX Status	0,RO	**Pause Transmit Negotiated Status:** Indicates that pause transmit should be enabled in the MAC. Based on bits [11:10] in ANAR register and bits [11:10] in ANLPAR register settings. This function shall be enabled according to IEEE 802.3 Annex 28B Table 28B-3, “Pause Resolution”, only if the Auto-Negotiated Highest Common Denominator is a full duplex technology.
11	MI Link Status	0, RO	**MII Link Status:** 1 = 100BT Full-duplex Link is active and it was established using Auto-Negotiation 0 = No active link of 100BT Full-duplex, established using Auto-Negotiation
10:8	RESERVED	000, RO	**RESERVED:** Writes ignored, read as 0.
7	Bypass LED Stretching	0, RW	**Bypass LED Stretching:** 1 = Bypass LED stretching 0 = Normal LED operation Set this bit to 1 to bypass the LED stretching; the LED reflects the internal value.
6	RESERVED	RO	RESERVED
5	LED CFG	0, RW, Pin_Strap	**LED Configuration Modes:**

Mode	LED_CFG	LED_LINK
1	1	ON for Good Link
		OFF for No Link
2	0	ON for Good Link
		BLINK for Activity

4:0	PHY ADDR	0000 1, RO	**PHY Address:** Strapping configuration for PHY Address.

5.3.1.25 10Base-T Status/Control Register (10BTSCR)

This register provides the ability to control and read status of the PHY's internal 10Base-T functionality.

Table 5-37. 10Base-T Status/Control Register (10BTSCR), Address 0x001A

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:14	RESERVED	000, RO	**RESERVED:** Writes ignored, read as 0.
13	Receiver TH	0, RW	**Lower Receiver Threshold Enable:** 1 = Enable 10Base-T lower receiver threshold to allow operation with longer cables 0 = Normal 10Base-T operation
12:9	Squelch	0000, RW	**Squelch Configuration:** Used to set the Peak Squelch 'ON' threshold for the 10Base-T receiver. Every step is equal to 50mV and allow raising/lowering the Squelch threshold from 200mV to 600mV. The default Squelch threshold is set to 200mV.
8	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
7	NLP Disable	0, RW	**NLP Transmission Control:** 1 = Disable transmission of NLPs 0 = Enable transmission of NLPs
6:5	RESERVED	00, RO	**RESERVED:** Writes ignored, read as 0.
4	Polarity Status	0, RO	**10Mb Polarity Status:** 1 = Inverted Polarity detected 0 = Correct Polarity detected This bit is a duplication of bit 12 in the PHYSTS register (0x0010). Both bits will be cleared upon a read of 10BTSCR register, but not upon a read of the PHYSTS register.
3:1	RESERVED	000, RO	**RESERVED:** Writes ignored, read as 0.
0	Jabber Disable	0, RW	**Jabber Disable:** 1 = Jabber function disabled 0 = Jabber function enabled **Note:** This function is applicable only in 10Base-T

5.3.1.26 BIST Control and Status Register 1 (BICSR1)

This register provides the total number of error bytes that was received by the PRBS checker and defines the Inter packet Gap (IPG) for the packet generator.

Table 5-38. BIST Control and Status Register 1 (BICSR1), Address 0x001B

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	BIST Error Count	0, RO	**BIST Error Count:** Holds number of erroneous bytes that were received by the PRBS checker. Value in this register is locked when write is done to bit[0] or bit[1] (see below). When PRBS Count Mode set to zero, count stops on 0xFF. See BISCR register (0x0016) for further details **Note:** Writing "1" to bit 15 will **lock** counter's value for successive read operation and **clear** the BIST Error Counter.
7:0	BIST IPG Length	0111 1101, RW	**BIST IPG Length:** Inter Packet Gap (IPG) Length defines the size of the gap (in bytes) between any 2 successive packets generated by the BIST. Default value is 0x7D which is equal to 125 bytes

5.3.1.27 BIST Control and Status Register2 (BICSR2)

This register allows programming the length of the generated packets in bytes for the BIST mechanism.

Table 5-39. BIST Control and Status Register 2 (BICSR2), Address 0x001C

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:11	RESERVED	0000 0, RO	**RESERVED:** Writes ignored, read as 0.
10:0	BIST Packet Length	101 1101 1100, RW	**BIST Packet Length:** Length of the generated BIST packets. The value of this register defines the size (in bytes) of every packet that generated by the BIST. Default value is 0x5DC which is equal to 1500 bytes

5.3.2 Cable Diagnostic Control Register (CDCR)

Table 5-40. Cable Diagnostic Control Register (CDCR), Address 0x001E

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	Diagnostic Start	0, RW	**Cable Diagnostic Process Start:** 1 = Start execute cable measurement 0 = Cable Diagnostic is disabled Diagnostic Start bit is cleared with raise of Diagnostic Done indication.
14:10	RESERVED	000 00, RO	**RESERVED:** Writes ignored, read as 0.
9:8	Link Quality	00, RO	**Link Quality Indication** 00 = Reserved 01 = Good Quality Link Indication 10 = Mid Quality Link Indication 11 = Poor Quality Link Indication The value of these bits are valid **only** when link is active – While reading "1" from "Link Status" bit 0 on PHYSTS register (0x0010).
7:4	RESERVED	0000, RO	**RESERVED:** Writes ignored, read as 0.
3:2	RESERVED	00, RO	**RESERVED:** Writes ignored, read as 0.
1	Diagnostic Done	0, RO	**Cable Diagnostic Process Done:** 1 = Indication that cable measurement process completed 0 = Diagnostic has not completed
0	Diagnostic Fail	0, RO	**Cable Diagnostic Process Fail:** 1 = Indication that cable measurement process failed 0 = Diagnostic has not failed

5.3.3 PHY Reset Control Register (PHYRCR)

Table 5-41. PHY Reset Control Register (PHYRCR), Address 0x001F

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	Software Reset	0, RW,SC	**Software Reset:** 1 = Reset PHY. This bit is self cleared and has same effect as Hardware reset pin. 0 = Normal Operation
14	Software Restart	0, RW,SC	**Software Restart:** 1 = Reset PHY. This bit is self cleared and resets all PHY circuitry except the registers. 0 = Normal Operation
13:0	RESERVED	00 0000 0000 0000, RO	Writes ignored, read as 0

5.3.4 Multi LED Control register (MLEDCR)

Table 5-42. Multi LED Control Register (MLEDCR), Address 0x0025

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:11	RESERVED	0000 0, RO	Writes ignored, read as 0
10	MLED pin 29 Route & Enable (COL Disable)	0, RW	Disable collision pin, and enable and route MLED (Multi LED) output to pin 29 Default - LINK advertise, LED_CFG strap can change to LINK+ACT
9	MLED Polarity RW Strap	RW, Strap	The polarity of MLED depends on the routing configuration and the strap being used on the selected pin. If the pin is strapped high via a pull-up resistor, the LED will be active low. If the pin is strapped low via a pull-down resistor, the LED will be active high.
8:7	RESERVED	0 0, RW, SC	RESERVED
6:3	MLED Configuration	000 0, RW	0000 = Link OK 0001 = RX/TX Activity 0010 = TX Activity 0011 = RX Activity 0100 = Collision 0101 = Speed: High for 100 Base TX 0110 = Speed: High for 10 Base TX 0111 = Full Duplex 1000 = Link OK / Blink on TX/RX Activity 1001 = Active Stretch Signal 1010 = MII LINK (100BT+FD)
2	RESERVED	0, RW	Writes ignored, read as 0.
1	MLED pin 17 Routing Cnfig.	0, RW	Route MLED to pin 17 (requires bit[0] to be enabled)
0	MLED pin Routing enable	0, RW	Enable routing for MLED according to MLED pin routing config

5.3.5 Compliance Test register (COMPTR)

This register allows generation of test patterns for compliance testing.

Table 5-43. Compliance Test Register (COMPTR), Address 0x0027

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:6	RESERVED	0000 0000 00, RO	Writes ignored, read as 0
5	Test Mode Select	0, RW	MSB bit for 100Base-TX test mode. Note: bit 4 must be '0' for 100Base-TX test modes.
4:0	Test Configuration	0 0000, RW	Bit 4 enables 10Base-T test modes. 1 = 10Base-T test modes 0 = 100Base-TX test modes
			For 10Base-T testing, bits [3:0] select the 10Base-T pattern as follows: 0000 = Single NLP 0000 = Single NLP 0001 = Single Pulse 1 0010 = Single Pulse 0 0011 = Repetitive 1 0100 = Repetitive 0 0101 = Preamble (repetitive '10') 0110 = Single 1 followed by TP_IDLE 0111 = Single 0 followed by TP_IDLE 1000 = Repetitive '1001' sequence 1001 = Random 10Base-T data 1010 = TP_IDLE_00 1011 = TP_IDLE_01 1100 = TP_IDLE_10 1101 = TP_IDLE_11 1001 = Random 10Base-T data
			For 100Base-TX testing, bits {5,[3:0]} select the transmit sequence. The test mode transmits a repetitive sequence consisting of a '1' followed by a configurable number of '0' bits. Bits {5,[3:0]} define the number of '0' bits that follow the '1'. 1 to 31 '1' bits may be selected. 0,0001 - 1,1111: single '0' to 31 zeroes 0,0000: Clear the register
			Note 1: Bit 4 must be '0' for 100Base-TX test modes. Note 2: 100Base-T test modes must be cleared before applying a new value. Bits {5,[3:0]} must be written to 0x0 before configuring a new value. Note 3: When performing 100Base-TX or 10Base-T tests, the speed must be forced using the Basic Mode Control Register (BMCR), address 0x0000.

5.3.6 IEEE1588 Precision Timing Pin Select (PTPPSEL)

This register configures the .

Table 5-44. IEEE1588 Precision Timing Pin Select (PTPPSEL), Address 0x003E

BIT	BIT NAME	DEFAULT	DESCRIPTION	
15:7	RESERVED	<0000 0>, RO	**RESERVED:** Writes ignored, read as 0.	
6:4	cfg_1588_TX_pin_sel	0, RW	**IEEE 1588 TX Pin Select:** Assigns transmit SFD pulse indication to pin selected by value in column at right.	001 - LED_ACT Pin 010 - LED_SPEED Pin 011 - LED_LINK Pin 100- CRS Pin 101 - COL Pin 110 - PWDNN/INT Pin 111 - No pulse output
3	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.	
2:0	cfg_1588_RX_pin_sel	0, RW	**IEEE 1588 RX Pin Select:** Assigns receive SFD pulse indication to pin selected by value in column at right.	

5.3.7 IEEE1588 Precision Timing Configuration (PTPCFG)

This register allows programming the length of the generated packets in bytes for the BIST mechanism.

Table 5-45. IEEE1588 Precision Timing Configuration (PTPCFG), Address 0x003F

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:13	cfg_1588_TX_set_phase	<101>, RW	**PTP Transmit Timing:** Set 1588 indication for TX path (8ns step)
12:10	cfg_1588_RX_set_phase	<101>, RW	**PTP Receive TIming:** Set 1588 indication for RX path (8ns step)
9:8	cfg_TX_ERR_sel	0, (TRIM)	**Configure TX ERR Input Pin:** 00 - No TX ERR 01 - Use LED ACT as TX_ERR 10 - Use PWRDN as TX_ERR 11 - USe COL as TX_ERR
7:0	RESERVED	<0100 0100>, RW	**RESERVED**

5.3.8 TX_CLK Phase Shift Register (TXCPSR)

This register allows programming the phase of the MII transmit clock (TX_CLK pin). The TX_CLK has a fixed phase to the XI pin. However the default phase, while fixed, may not be ideal for all systems, therefore this register may be used by the system to align the reference clock (XI pin) to the TX_CLK. The phase shift value is in 4ns units. The phase shift value should be between 0 and 10 (0ns to 40ns). If value greater than 10 is written, the update value will be the written value modulo 10.

Table 5-46. TX_CLK Phase Shift Register (TXCPSR), Address 0x0042

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:5	RESERVED	0000 0000 000, RO	**RESERVED:** Writes ignored, read as 0
4	Phase Shift Enable	0,RW,SC	**TX Clock Phase Shift Enable:** 1 = Perform Phase Shift to the TX_CLK according to the value written to Phase Shift Value in bits [4:0]. 0 = No change in TX Clock phase
3:0	Phase Shift Value	0000,RW	**TX Clock Phase Shift Value:** The value of this register represents the current phase shift between Reference clock at XI and MII Transmit Clock at TX_CLK. Any different value that will be written to these bits will shift TX_CLK by 4 times the difference (in nSec). For example, if the value of this register is 0x2, Writing 0x9 to this register shifts TX_CLK by 28nS (4 times 7).However, since the maximum difference between XI and TX_CLK could be 40nSec (value of 10) in case of writing value bigger than 10, the updated value is the written value modulo 10.

5.3.9 Power Back Off Control Register (PWRBOCR)

Table 5-47. Power Back Off Control Register (PWRBOCR), Address 0x00AE

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	1, RO	**RESERVED**
14	RESERVED	0, RO	**RESERVED**
13:9	RESERVED	00 000, RO	**RESERVED**
8:6	Power Back Off	0, RW	**Power Back Off Level:** See *TLK110 Power Back Off for Short Cables* application note (SLLA328) 000 = Normal Operation 001 = Level 1 (up to 140m cable between TLK link partners) 010 = Level 2 (up to 100m cable between TLK link partners) 011 = Level 3 (up to 80m cable between TLK link partners) Others = Reserved
5:0	RESERVED	10 0000, RO	**RESERVED**

5.3.10 Voltage Regulator Control Register (VRCR)

This register gives the host processor the ability to power down the voltage-regulator block of the PHY via register access. This power-down operation is available in systems operating with an external power supply.

Table 5-48. Voltage Regulator Control Register (VRCR), Address 0x00D0

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	VRPD	0, RW, SC	**Voltage Regulator Power Down:** 1 = Power Down. Allow the system to power down the voltage regulator block of the PHY using register access. 0 = Normal Operation. Voltage Regulator is powered and outputs voltage on the PFBOUT pin.
14:0	RESERVED	000 0000 0000, RW	**RESERVED:** Must be written as 0.

5.3.11 Cable Diagnostic Configuration/Result Registers

5.3.11.1 ALCD Control and Results 1 (ALCDRR1)

Table 5-49. ALCD Control and Results 1 (ALCDRR1), Address 0x0155

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	alcd_start	0, SC	1 = Start ALCD
14:13		00, RO	**RESERVED:** Writes ignored, read as 0.
12	alcd_done	0, RO	**TPTD Diagnostic Bypass** 1 = Bypass TPTD diagnostic. TDR on TPTD pair is not executed. 0 = TDR is executed on TPTD pair
11:4	alcd_out1	0000 0000, RO	**alcd_out1**
3	RESERVED	0, RO	**RESERVED**: Writes ignored, read as 0
2:0	alcd_ctrl	001,RW	**Control of ALCD Average factor**

5.3.11.2 Cable Diagnostic Specific Control Registers (CDSCR1 - CDSCR4)

Use CDSCR1 to select the channel for the cable diagnostics test. CDSCR1 contains the enable and bypass bits for the diagnostic tests, and defines the number of executed and averaged TDR sequences. CDSCR2 - CDSCR4 configure other parameters for cable diagnostics.

Table 5-50. Cable Diagnostic Specific Control Register (CDSCR), Address 0x0170

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
14	Diagnostic Cross Disable	0, RW	**Cross TDR Diagnostic mode** 1 = Disable TDR Cross mode – TDR will be executed in regular mode only 0 = Diagnostic of crossing pairs is enabled In Cross Diagnostic mode, the TDR mechanism is looking for reflection on the other pair to check short between pairs.
13	Diagnostic TPTD Bypass	0, RW	**TPTD Diagnostic Bypass** 1 = Bypass TPTD diagnostic. TDR on TPTD pair will not be executed. 0 = TDR is executed on TPTD pair In bypass TPTD, results are available in TPRD slots.
12	Diagnostic TPRD Bypass	0, RO	**TPRD Diagnostic Bypass** 1 = Bypass TPRD diagnostic. TDR on TPRD pair will not be executed. 0 = TDR is executed on TPRD pair
11	RESERVED	1, RW	**RESERVED:** Must be Set to 1.

Table 5-50. Cable Diagnostic Specific Control Register (CDSCR), Address 0x0170 (continued)

BIT	BIT NAME	DEFAULT	DESCRIPTION
10:8	Diagnostics Average Cycles	110, RW	**Number Of TDR Cycles to Average:** <000>: 1 TDR cycle <001>: 2 TDR cycles <010>: 4 TDR cycles <011>: 8 TDR cycles <100>: 16 TDR cycles <101>: 32 TDR cycles <110>: 64 TDR cycles (default) <111>: Reserved
7:0	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.

Table 5-51. Cable Diagnostic Specific Control Register 2 (CDSCR2), Address 0x0171

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:4	RESERVED	1100 1000 0101, RW	**RESERVED:** Ignore on read
3:0	TDR pulse control	1100, RW	Configure expected self reflection in TDR

Table 5-52. Cable Diagnostic Specific Control Register 3 (CDSCR3), Address 0x0173

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	Cable length cfg	1111 1111, RW	Configure duration of listening to detect long cable reflections
7:0	RESERVED	1111 1111, RW	**RESERVED:** Ignore on read

Table 5-53. Cable Diagnostic Specific Control Register 4 (CDSCR4), Address 0x0177

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:13	RESERVED	000, RW	**RESERVED:** Ignore on read
12:8	Short cables TH	1 1000, RW	TH to compensate for strong reflections in short cables
7:0	RESERVED	1001 0110, RW	**RESERVED:** Ignore on read

5.3.11.3 Cable Diagnostic Location Results Register 1 (CDLRR1)

This register provides the peaks locations after execution of the TDR. The values of this register are valid after reading 1 in Diagnostic Done bit 1 in register CDCR (0x1E).

Table 5-54. Cable Diagnostic Location Results Register 1 (CDLRR1), Address 0x0180

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	TPTD Peak Location 2	0000 0000, RO	Location of the **Second** peak discovered by the TDR mechanism on Transmit Channel (TPTD). The value of these bits is translated into distance from the PHY
7:0	TPTD Peak Location 1	0000 0000, RO	Location of the **First** peak discovered by the TDR mechanism on Transmit Channel (TPTD). The value of these bits is translated into distance from the PHY

5.3.11.4 Cable Diagnostic Location Results Register 2 (CDLRR2)

This register provides the peaks locations after execution of the TDR. The values of this register are valid after reading 1 in Diagnostic Done bit 1 in register CDCR (0x1E).

Table 5-55. Cable Diagnostic Location Results Register 2 (CDLRR2), Address 0x0181

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	TPTD Peak Location 4	0000 0000, RO	Location of the **Fourth** peak discovered by the TDR mechanism on Transmit Channel (TPTD). The value of these bits is translated into distance from the PHY.
7:0	TPTD Peak Location 3	0000 0000, RO	Location of the **Third** peak discovered by the TDR mechanism on Transmit Channel (TPTD). The value of these bits is translated into distance from the PHY.

5.3.11.5 Cable Diagnostic Location Results Register 3 (DDLRR3)

This register provides the peaks locations after execution of the TDR. The values of this register are valid after reading 1 in Diagnostic Done bit 1 in register CDCR (0x1E).

Table 5-56. Cable Diagnostic Location Results Register 3 (DDLRR3), Address 0x0182

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	TPRD Peak Location 1	0000 0000, RO	Location of the **First** peak discovered by the TDR mechanism on Receive Channel (TPRD). The value of these bits is translated into distance from the PHY.
7:0	TPTD Peak Location 5	0000 0000, RO	Location of the **Fifth** peak discovered by the TDR mechanism on Transmit Channel (TPTD). The value of these bits is translated into distance from the PHY.

5.3.11.6 Cable Diagnostic Location Results Register 4 (CDLRR4)

This register provides the peaks locations after execution of the TDR. The values of this register are valid after reading 1 in Diagnostic Done bit 1 in register CDCR (0x1E).

Table 5-57. Cable Diagnostic Location Results Register 4 (CDLRR4), Address 0x0183

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	TPRD Peak Location 3	0000 0000, RO	Location of the **Third** peak discovered by the TDR mechanism on Receive Channel (TPRD). The value of these bits is translated into distance from the PHY.
7:0	TPRD Peak Location 2	0000 0000, RO	Location of the **Second** peak discovered by the TDR mechanism on Receive Channel (TPRD). The value of these bits is translated into distance from the PHY.

5.3.11.7 Cable Diagnostic Location Results Register 5 (CDLRR5)

This register provides the peaks locations after execution of the TDR. The values of this register are valid after reading 1 in Diagnostic Done bit 1 in register CDCR (0x1E).

Table 5-58. Cable Diagnostic Location Results Register 5 (CDLRR5), Address 0x0184

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:8	TPRD Peak Location 5	0000 0000, RO	Location of the **Fifth** peak discovered by the TDR mechanism on Receive Channel (TPRD). The value of these bits is translated into distance from the PHY.
7:0	TPRD Peak Location 4	0000 0000, RO	Location of the **Fourth** peak discovered by the TDR mechanism on Receive Channel (TPRD). The value of these bits is translated into distance from the PHY.

5.3.11.8 Cable Diagnostic Amplitude Results Register 1 (CDARR1)

This register provides the peaks amplitude measurement after the execution of the TDR. The values of this register are valid after reading 1 in Diagnostic Done bit 1 in register CDCR (0x1E).

Table 5-59. Cable Diagnostic Amplitude Results Register 1 (CDARR1), Address 0x0185

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0,RO	**RESERVED:** Writes ignored, read as 0.
14:8	TPTD Peak Amplitude 2	000 0000, RO	Amplitude of the **Second** peak discovered by the TDR mechanism on Transmit Channel (TPTD). The value of these bits is translated into type of cable fault, interference, or both. This amplitude value refers to peak location stored in bits [15:8] in register CDLRR1 (0x180)
7	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
6:0	TPTD Peak Amplitude 1	000 0000, RO	Amplitude of the **First** peak discovered by the TDR mechanism on Transmit Channel (TPTD). The value of these bits is translated into type of cable fault, interference, or both. This amplitude value refers to peak location stored in bits [7:0] in register CDLRR1 (0x180)

5.3.11.9 Cable Diagnostic Amplitude Results Register 2 (CDARR2)

This register provides the peaks amplitude measurement after the execution of the TDR. The values of this register are valid after reading 1 in Diagnostic Done bit 1 in register CDCR (0x1E).

Table 5-60. Cable Diagnostic Amplitude Results Register 2 (CDARR2), Address 0x0186

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0,RO	**RESERVED:** Writes ignored, read as 0.
14:8	TPTD Peak Amplitude 4	000 0000, RO	Amplitude of the **Fourth** peak discovered by the TDR mechanism on Transmit Channel (TPTD). The value of these bits is translated into type of cable fault, interference, or both. This amplitude value refers to peak location stored in bits [15:8] in register CDLRR2 (0x181)
7	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
6:0	TPTD Peak Amplitude 3	000 0000, RO	Amplitude of the **Third** peak discovered by the TDR mechanism on Transmit Channel (TPTD). The value of these bits is translated into type of cable fault, interference, or both. This amplitude value refers to peak location stored in bits [7:0] in register CDLRR2 (0x181)

5.3.11.10 Cable Diagnostic Amplitude Results Register 3 (CDARR3)

This register provides the peaks amplitude measurement after the execution of the TDR. The values of this register are valid after reading 1 in Diagnostic Done bit 1 in register CDCR (0x1E).

Table 5-61. Cable Diagnostic Amplitude Results Register 3 (CDARR3), Address 0x0187

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
14:8	TPRD Peak Amplitude 1	000 0000, RO	Amplitude of the **First** peak discovered by the TDR mechanism on Receive Channel (TPRD). The value of these bits is translated into type of cable fault, interference, or both. This amplitude value refers to peak location stored in bits [15:8] in register CDLRR3 (0x182)
7	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
6:0	TPTD Peak Amplitude 5	000 0000, RO	Amplitude of the **Fifth** peak discovered by the TDR mechanism on Transmit Channel (TPTD). The value of these bits is translated into type of cable fault, interference, or both. This amplitude value refers to peak location stored in bits [7:0] in register CDLRR3 (0x182)

5.3.11.11 Cable Diagnostic Amplitude Results Register 4 (CDARR4)

This register provides the peaks amplitude measurement after the execution of the TDR. The values of this register are valid after reading 1 in Diagnostic Done bit 1 in register CDCR (0x1E).

Table 5-62. Cable Diagnostic Amplitude Results Register 4 (CDARR4), Address 0x0188

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
14:8	TPRD Peak Amplitude 3	000 0000, RO	Amplitude of the **Third** peak discovered by the TDR mechanism on Receive Channel (TPRD). The value of these bits is translated into type of cable fault, interference, or both. This amplitude value refers to peak location stored in bits [15:8] in register CDLRR4 (0x183)
7	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
6:0	TPRD Peak Amplitude 2	000 0000, RO	Amplitude of the **Second** peak discovered by the TDR mechanism on Receive Channel (TPRD). The value of these bits is translated into type of cable fault, interference, or both. This amplitude value refers to peak location stored in bits [7:0] in register CDLRR4 (0x183)

5.3.11.12 Cable Diagnostic Amplitude Results Register 5 (CDARR5)

This register provides the peaks amplitude measurement after the execution of the TDR. The values of this register are valid after reading 1 in Diagnostic Done bit 1 in register CDCR (0x1E).

Table 5-63. Cable Diagnostic Amplitude Results Register 5 (CDARR5), Address 0x0189

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
14:8	TPRD Peak Amplitude 5	000 0000, RO	Amplitude of the **Fifth** peak discovered by the TDR mechanism on Receive Channel (TPRD). The value of these bits is translated into type of cable fault, interference, or both. This amplitude value refers to peak location stored in bits [15:8] in register CDLRR4 (0x184)
7	RESERVED	0, RO	**RESERVED:** Writes ignored, read as 0.
6:0	TPRD Peak Amplitude 4	000 0000, RO	Amplitude of the **Fourth** peak discovered by the TDR mechanism on Receive Channel (TPRD). The value of these bits is translated into type of cable fault, interference, or both. This amplitude value refers to peak location stored in bits [7:0] in register CDLRR4 (0x184)

5.3.11.13 Cable Diagnostic General Results Register (CDGRR)

This register provides general measurement results after the execution of the TDR. The Cable Diagnostic software should post process this result together with other Peaks' location and amplitude results.

Table 5-64. Cable Diagnostic General Results Register (CDGRR), Address 0x018A

BIT	BIT NAME	DEFAULT	DESCRIPTION
15	TPTD Peak Polarity 5	0, RO	Polarity of the **Fifth** peak discovered by the TDR mechanism on Transmit Channel (TPTD)
14	TPTD Peak Polarity 4	0, RO	Polarity of the **Fourth** peak discovered by the TDR mechanism on Transmit Channel (TPTD)
13	TPTD Peak Polarity 3	0, RO	Polarity of the **Third** peak discovered by the TDR mechanism on Transmit Channel (TPTD)
12	TPTD Peak Polarity 2	0, RO	Polarity of the **Second** peak discovered by the TDR mechanism on Transmit Channel (TPTD)
11	TPTD Peak Polarity 1	0, RO	Polarity of the **First** peak discovered by the TDR mechanism on Transmit Channel (TPTD)
10	TPRD Peak Polarity 5	0, RO	Polarity of the **Fifth** peak discovered by the TDR mechanism on Receive Channel (TPRD)
9	TPRD Peak Polarity 4	0, RO	Polarity of the **Fourth** peak discovered by the TDR mechanism on Receive Channel (TPRD)
8	TPRD Peak Polarity 3	0, RO	Polarity of the **Third** peak discovered by the TDR mechanism on Receive Channel (TPRD)
7	TPRD Peak Polarity 2	0, RO	Polarity of the **Second** peak discovered by the TDR mechanism on Receive Channel (TPRD)
6	TPRD Peak Polarity 1	0, RO	Polarity of the **First** peak discovered by the TDR mechanism on Receive Channel (TPRD)
5	Cross Detect on TPTD	0, RO	Cross Reflection were detected on TPTD. Indicate on Short between TPTD and TPRD
4	Cross Detect on TPRD	0, RO	Cross Reflection were detected on TPRD. Indicate on Short between TPTD and TPRD
3	Above 5 TPTD Peaks	0, RO	More than 5 reflections were detected on TPTD
2	Above 5 TPRD Peaks	0, RO	More than 5 reflections were detected on TPRD
1:0	RESERVED	00, RO	**RESERVED:** Writes ignored, read as 0

5.3.11.14 ALCD Control and Results 2 (ALCDRR2)

Table 5-65. ALCD Control and Results 2 (ALCDRR2), Address 0x0215

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:4	RESERVED	RO	
3:0	alcd_out2	<0011>, RW	Control word to analog PGA

5.3.11.15 ALCD Control and Results 3 (ALCDRR3)

Table 5-66. ALCD Control and Results 3 (ALCDRR3), Address 0x021D

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:12	RESERVED	0000, RO	**RESERVED**
11:0	FAGC Accumulator	0110 0000 0000, RW	**FAGC Accumulator:**

6 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Interfaces

6.1.1 Media Independent Interface (MII)

The Media Independent Interface (MII) is a synchronous 4-bit wide nibble data interface that connects the PHY to the MAC in 100B-TX and 10B-T modes. The MII is fully compliant with IEEE802.3-2002 clause 22.

The MII signals are summarized below.

Data signals	TXD [3:0]
	RXD [3:0]
Transmit and receive-valid signals	TX_EN
	RX_DV
Line-status signals	CRS (carrier sense)
	COL (collision) (By default, the COL pin is disabled, and can be configured to be enabled instead of LED_LINK using bit [10] in register 0x0025).

Figure 6-1 shows the MII-mode signals.

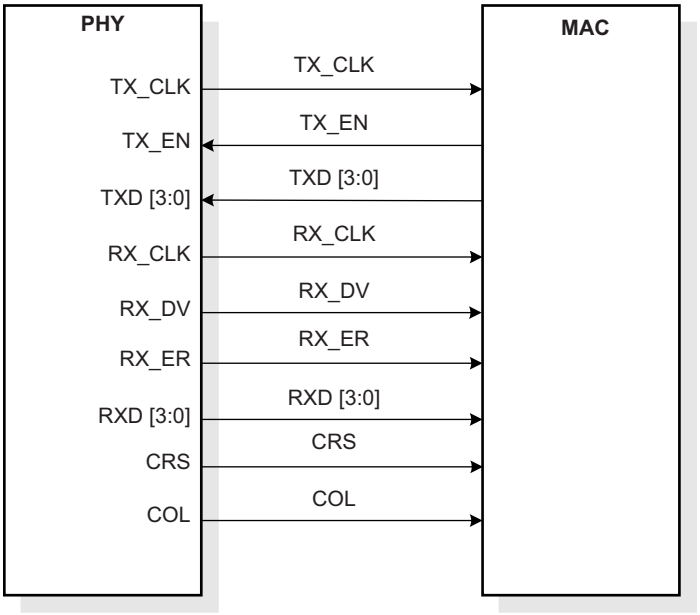


Figure 6-1. MII Signaling

The Isolate bit (BMCR register bit 10), defined in IEEE802.3-2002, electrically isolates the PHY from the MII (if set, all transactions on the MII interface are ignored by the PHY).

Additionally, the MII interface includes the carrier sense signal CRS, as well as a collision detect signal COL. The CRS signal asserts to indicate the reception of data from the network or as a function of transmit data in Half Duplex mode. The COL signal asserts as an indication of a collision which can occur during half-duplex operation when both transmit and receive operation occur simultaneously.

6.1.2 Reduced Media Independent Interface (RMII)

TLK10xL incorporates the Reduced Media Independent Interface (RMII) as specified in the RMII specification (rev1.2) from the RMII consortium. The purpose of this interface is to provide a low-cost alternative to the IEEE 802.3u MII as specified in Clause 22. Architecturally, the RMII specification provides an additional reconciliation layer on either side of the MII, but can be implemented in the absence of an MII.

The RMII specification has the following characteristics:

- Supports 10-Mbps and 100-Mbps data rates
- Single clock reference sourced from the MAC to PHY (or from an external source)
- Provides independent 2 bit wide (di-bit) transmit and receive data paths
- Uses CMOS signal levels, operates at 3.3-V or 2.5-V VDD_IO levels

In this mode, data transfers two bits at a time using the 50-MHz RMII reference clock for both transmit and receive. RMII mode uses the following pins:

SIGNAL	PIN
XI (RMII reference clock is 50 MHz)	23
TXD_0	4
TXD_1	5
TX_EN	3
CRS_DV	27

RX_ER	28
RXD_0	30
RXD_1	31

Data on TXD [1:0] are latched at the PHY with reference to the reference-clock edges on the XI pin. Data on RXD [1:0] are latched at the MAC with reference to the same reference clock edges on the XI pin. The RMII operates at the same speed (50 MHz) in both 10B-T and 100B-TX. In 10B-T the data is 10 times slower than the reference clock, so transmit data is sampled every 10 clocks. Likewise, receive data is generated on every 10th clock so that an attached MAC device can sample the data every 10 clocks.

In addition, RMII mode supplies an RX_DV signal which allows a simpler method of recovering receive data without the need to separate RX_DV from the CRS_DV indication. RX_ER is also supported even though not required by RMII spec (the TLK10xL supports optional use of RX_ER and RX_DV in RMII as an extra feature). RMII mode requires a 50-MHz oscillator connected to the device XI pin.

The TLK10xL supports a special mode called *RMII receive clock* mode. This mode, which is not part of the RMII specification, allows synchronization of the MAC-PHY RX interface. In this mode, the PHY generates a recovered 50-MHz clock through the RX_CLK pin and synchronizes the RXD[1:0], CRS_DV, RX_DV and RX_ER signals to this clock. Setting register 0x000A bit [0] is required to activate this mode.

Figure 6-2 describes the RMII signals connectivity between the TLK10xL and any MAC device.

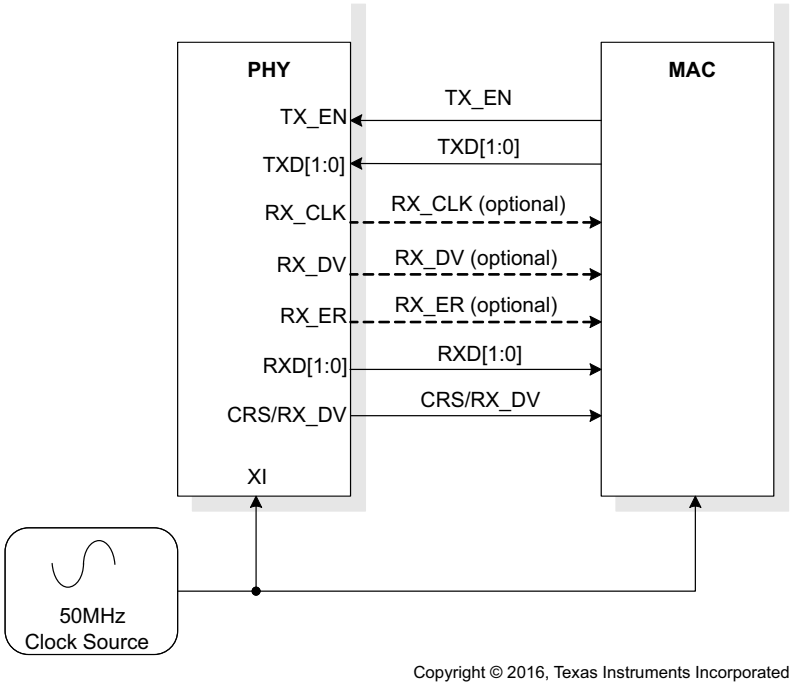


Figure 6-2. TLK10xL RMII/MAC Connection

RMII function includes a programmable elastic buffer to adjust for the frequency differences between the reference clock and the recovered receive clock. The programmable elastic buffer minimizes internal propagation delay based on expected maximum packet size and clock accuracy.

Table 6-1 indicates how to program the buffer FIFO based on the expected maximum packet size and clock accuracy. It assumes that the RMII reference clock and the Far-end transmitter clock have the same accuracy.

Table 6-1. Recommended RMII Packet Sizes

START THRESHOLD RBR[1:0]	LATENCY TOLERANCE	RECOMMENDED PACKET SIZE AT ±50 PPM	RECOMMENDED PACKET SIZE AT ±100 PPM
1(4-bits)	2 bits	2400 bytes	1200 bytes
2(8-bits)	6 bits	7200 bytes	3600 bytes
3(12-bits)	10 bits	12000 bytes	6000 bytes
0(16-bits)	14 bits	16800 bytes	8400 bytes

6.1.3 Serial Management Interface

The Serial Management Interface (SMI), provides access to the TLK10xL internal register space for status information and configuration. The SMI is compatible with IEEE802.3-2002 clause 22. The implemented register set consists of all the registers required by the IEEE802.3-2002, plus several others to provide additional visibility and controllability of the TLK10xL device.

The SMI includes the MDC management clock input and the management MDIO data pin. The MDC clock is sourced by the external management entity, also called Station (STA), and can run at a maximum clock rate of 25 MHz. MDC is not expected to be continuous because it can be turned off by the external management entity when the bus is idle.

The MDIO is sourced by the external management entity and by the PHY. The data on the MDIO pin is latched on the rising edge of the MDC clock. The MDIO pin requires a pullup resistor (2.2 kΩ) which, during IDLE and turnaround, pulls MDIO high.

Up to 32 PHYs can share a common SMI bus. To distinguish between the PHYs, a 5-bit address is used. During power-up reset, the TLK10xL latches the PHYAD[4:0] configuration pins (Pin 29 to Pin 32) to determine its address.

The management entity must not start an SMI transaction in the first cycle after power-up reset. To maintain valid operation, the SMI bus must remain inactive at least one MDC cycle after hard reset is deasserted.

In normal MDIO transactions, the register address is taken directly from the management-frame **reg_addr** field, thus allowing direct access to 32 16-bit registers (including those defined in IEEE802.3 and vendor specific). The data field is used for both reading and writing. The Start code is indicated by a <01> pattern. This pattern makes sure that the MDIO line transitions from the default idle line state. Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device may actively drive the MDIO signal during the first bit of Turnaround. The addressed TLK10xL drives the MDIO with a zero for the second bit of turnaround and follows this with the required data. Figure 6-3 shows the timing relationship between MDC and the MDIO as driven or received by the Station (STA) and the TLK10xL (PHY) for a typical register read access.

For write transactions, the station-management entity writes data to the addressed TLK10xL, thus eliminating the requirement for MDIO Turnaround. The Turnaround time is filled by the management entity by inserting <10>. Figure 6-4 shows the timing relationship for a typical MII register write access. The frame structure and general read or write transactions are shown in Table 6-2, Figure 6-3, and Figure 6-4.

Table 6-2. Typical MDIO Frame Format

MII MANAGEMENT SERIAL PROTOCOL	<IDLE><START><OP CODE><DEVICE ADDR><REG ADDR><TURNAROUND><DATA><IDLE>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><xxxx xxxx xxxx xxxx><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><xxxx xxxx xxxx xxxx><idle>

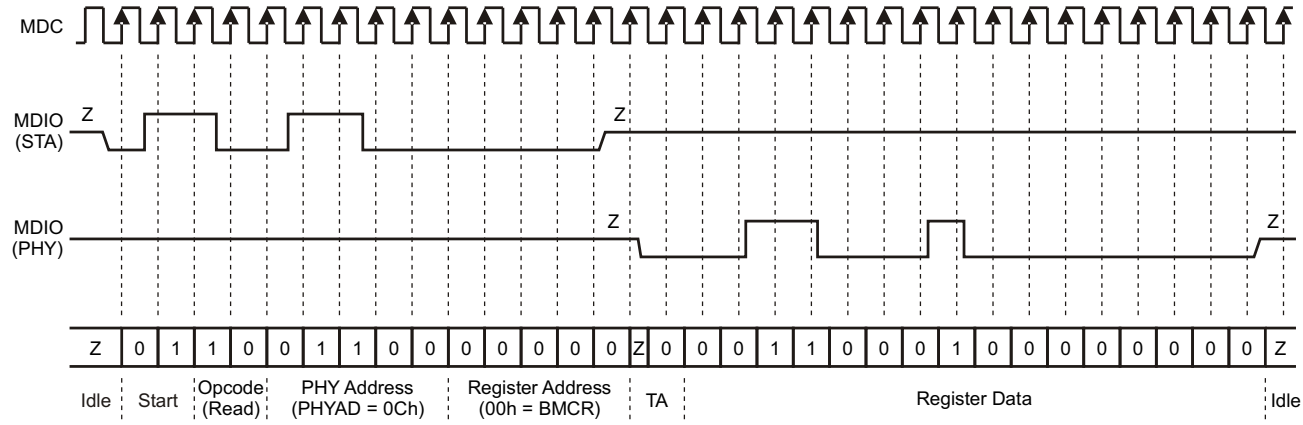


Figure 6-3. Typical MDC/MDIO Read Operation

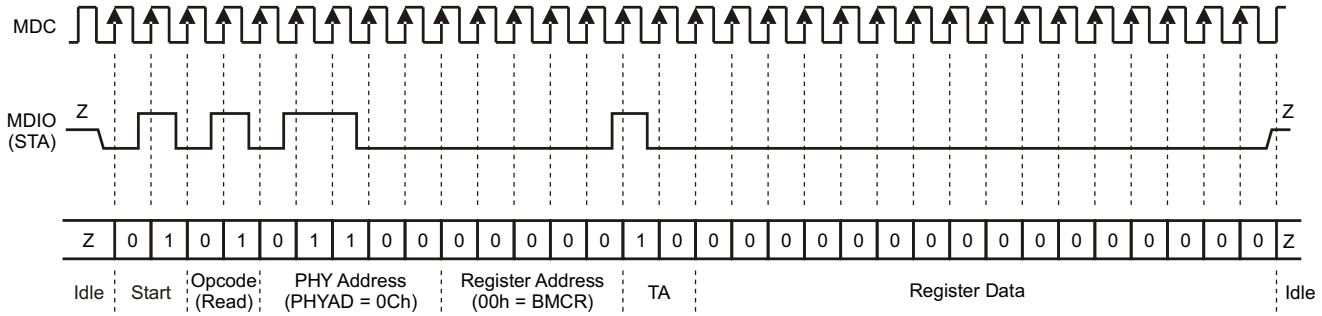


Figure 6-4. Typical MDC/MDIO Write Operation

6.1.3.1 Extended Address Space Access

The TLK10xL SMI function supports read/write access to the extended register set using registers REGCR(0x000Dh) and ADDAR(0x000Eh) and the MDIO Manageable Device (MMD) indirect method defined in IEEE802.3ah Draft for clause 22 for accessing the clause 45 extended register set.

The standard register set, MDIO registers 0 to 31, is accessed using the normal direct-MDIO access or the indirect method, except for register REGCR(0x000Dh) and ADDAR(0x000Eh) which is accessed only using the normal MDIO transaction. The SMI function ignores indirect accesses to these registers.

REGCR(0x000Dh) is the MDIO Manageable MMD access control. In general, register REGCR(4:0) is the device address DEVAD that directs any accesses of ADDAR(0x000Eh) register to the appropriate MMD. Specifically, the TLK10xL uses the vendor-specific **DEVAD[4:0] = "11111"** for accesses. All accesses through registers REGCR and ADDAR must use this DEVAD. Transactions with other DEVAD are ignored. REGCR[15:14] holds the access function: address (00), data with no post increment (01), data with post increment on read and writes (10) and data with post increment on writes only (11).

- ADDAR is the address/data MMD register. ADDAR is used in conjunction with REGCR to provide the access to the extended register set. If register REGCR[15:1] is 00, then ADDAR holds the address of the extended address space register. Otherwise, ADDAR holds the data as indicated by the contents of its address register. When REGCR[15:14] is set to 00, accesses to register ADDAR modify the extended register set address register. This address register must always be initialized to access any of the registers within the extended register set.
- When REGCR[15:14] is set to 01, accesses to register ADDAR access the register within the extended register set selected by the value in the address register.
- When REGCR[15:14] is set to 10, access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for both reads and writes, the value in the address register is incremented.

- When REGCR[15:14] is set to 11, access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for write accesses only, the value in the address register is incremented. For read accesses, the value of the address register remains unchanged.

The following sections describe how to perform operations on the extended register set using register REGCR and ADDAR.

6.1.3.1.1 Write Address Operation

To set the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.

Subsequent writes to register ADDAR (step 2) continue to write the address register.

6.1.3.1.2 Read Address Operation

To read the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Read the register address from register ADDAR.

Subsequent reads to register ADDAR (step 2) continue to read the address register.

6.1.3.1.3 Write (No Post Increment) Operation

To write a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Write the content of the desired extended register set register to register ADDAR.

Subsequent writes to register ADDAR (step 4) continue to rewrite the register selected by the value in the address register.

NOTE

Steps (1) and (2) can be skipped if the address register was previously configured.

6.1.3.1.4 Read (No Post Increment) Operation

To read a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Read the content of the desired extended register set register to register ADDAR.

Subsequent reads from register ADDAR (step 4) continue reading the register selected by the value in the address register.

NOTE

Steps (1) and (2) can be skipped if the address register was previously configured.

6.1.3.1.5 Write (Post Increment) Operation

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the register address from register ADDAR.
3. Write the value 0x801F (data, post increment on reads and writes function field = 10, DEVAD = 31) or the value 0xC01F (data, post increment on writes function field = 11. DEVAD = 31) to register REGCR.
4. Write the content of the desired extended register set register to register ADDAR.

Subsequent writes to register ADDAR (step 4) write the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

6.1.3.1.6 Read (Post Increment) Operation

To read a register in the extended register set and automatically increment the address register to the next higher value following the write operation:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment on reads and writes function field = 10, DEVAD = 31) to register REGCR.
4. Read the content of the desired extended register set register to register ADDAR.

Subsequent reads to register ADDAR (step 4) read the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

6.2 Reset and Power-Down Operation

The TLK10xL includes an internal power-on-reset (POR) function, and therefore does not need an explicit reset for normal operation after power up.

At power up, if required by the system, the RESET pin (active low) should be deasserted 200 µs after the power is ramped up to allow the internal circuits to settle and for the internal regulators to stabilize. If required during normal operation, the device can be reset by a hardware or software reset.

6.2.1 Hardware Reset

A hardware reset is accomplished by applying a low pulse (TTL level), with a duration of at least 1 µs, to RESET. This pulse resets the device such that all registers are reinitialized to default values, and the hardware configuration values are relatched into the device (similar to the power-up or reset operation). The time from the point when the reset pin is deasserted to the point when the reset has concluded internally is approximately 200 µs.

6.2.2 Software Reset

An **IEEE registers software reset** is accomplished by setting the reset bit (bit 15) of the BMCR register (0x0000h). This bit only resets the IEEE-defined standard registers in the address space 0x00h to 0x07h.

A **global software reset** is accomplished by setting bit 15 of register PHYRCR (0x001F) to 1. This bit resets all the internal circuits in the PHY including IEEE-defined registers (0x00h to 0x07h) and all the extended registers. The global software reset resets the device such that all registers are reset to default values and the hardware configuration values are maintained.

A **global software *restart*** is accomplished by setting bit 14 of register PHYRCR (0x001F) to 1. This action resets all the PHY circuits except the registers in the Register File.

The time from the point when the resets or restart bits are set to the point when the software resets or the restart concludes is approximately 200 µs. TI recommends that the software driver code must wait 500 µs following a software reset before allowing further serial MII operations with the TLK10xL.

6.2.3 Power Down and Interrupt

The power-down and interrupt functions are multiplexed on pin 8 of the device. By default, this pin functions as a power-down input and the interrupt function is disabled. This pin can be configured as an interrupt output pin by setting bit 0 (INT_OE) to 1 in the PHYSCR (0x0011h) register. The PHYSCR register is also used to enable and set the polarity of the interrupt.

6.2.3.1 Power-Down Control Mode

The INT/PWDN pin can be asserted low to put the device in a power-down mode. An external control signal can be used to drive the pin low, overcoming the weak internal pullup resistor. Alternatively, the device can be configured to initialize into a power-down state by use of an external pulldown resistor on the INT/PWDN pin.

6.2.3.2 Interrupt Mechanisms

The interrupt function is controlled through register access. All interrupt sources are disabled by default. The MISR1 (0x0012) and MISR2 (0x0013) registers provide independent interrupt enable bits for the various interrupts supported by the TLK10xL. The INT/PWDN pin is asynchronously asserted low when an interrupt condition occurs. The source of the interrupt can be determined by reading the interrupt status registers MISR1 (0x0012h) and MISR2 (0x0013). One or more bits in the MISR registers will be set, indicating all currently-pending interrupts. Reading the MISR registers clears ALL pending interrupts.

6.2.4 Power Save Modes

The TLK10xL supports three types of power-save modes. The lowest power consumption is achieved in IEEE power down mode. To enter IEEE power down mode, pull the INT/PWDN pin to LOW or program bit 11 in the Basic Mode Control Register (BMCR), address 0x0000. In this mode, all internal circuitry except SMI functionality is shut down (Register access is still available).

To enable and activate all other power save modes through register access, use register PHYSCR (0x0011h). Setting bit 14 enables all power-save modes; bits [13:12] select between them.

Setting bits [13:12] to 01 powers down the PHY, forcing it into IEEE power down mode (Similar to BMCR bit 11 functionality).

Setting bits [13:12] to 10 puts the PHY in Low Power Active Energy Saving mode.

Setting bits [13:12] to 11 puts the PHY in Low Power Passive Energy Saving mode.

When these bits are cleared, the PHY powers up and returns to the last state it was in before it was powered down.

6.3 Design Guidelines

6.3.1 TPI Network Circuit

Figure 6-5 shows the recommended circuit for a 10/100-Mbps twisted pair interface. Common mode chokes on the device side of the transformer are required. Variations with PCB and component characteristics require that the application be tested to verify that the circuit meets the requirements of the intended application.

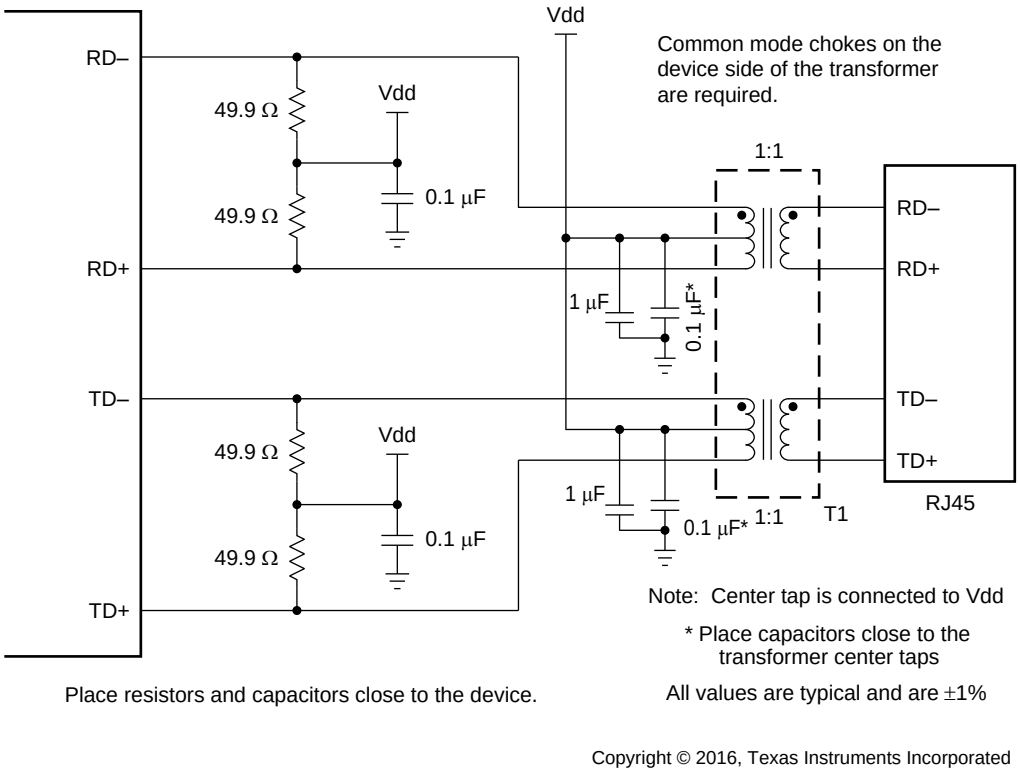


Figure 6-5. 10/100-Mbps Twisted Pair Interface

6.3.2 Clock In (XI) Requirements

The TLK10xL supports an external CMOS-level oscillator source or an internal oscillator with an external crystal.

6.3.2.1 Oscillator

If an external clock source is used, XI must be tied to the clock source and XO must be left floating. The oscillator must use the same supply voltage as the VDD_IO supply. When operating in RMII, the oscillator supply voltage must be 3.3 V or 2.5 V.

6.3.2.2 Crystal

The use of a 25-MHz, parallel, 20-pF load crystal is recommended if a crystal source is desired. Figure 6-6 shows a typical connection for a crystal resonator circuit. The load capacitor values varies with the crystal vendors; check with the vendor for the recommended loads.

The oscillator circuit is designed to drive a parallel-resonance AT-cut crystal with a minimum drive level of 100 μW and a maximum of 500 μW. If a crystal is specified for a lower drive level, a current limiting resistor must be placed in series between XO and the crystal.

As a starting point for evaluating an oscillator circuit, if the requirements for the crystal are not known, set the values for C_{L1} and C_{L2} at 33 pF, and R_1 must be set at 0 Ω. Specifications for a 25-MHz crystal are listed in Table 6-5.

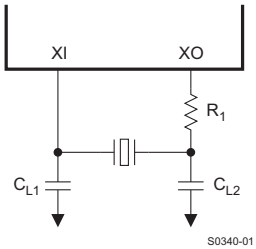


Figure 6-6. Crystal Oscillator Circuit

Table 6-3. 25-MHz Oscillator Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency tolerance	Operational temperature			±50	ppm
Frequency stability	1 year aging			±50	ppm
Rise / fall time	10%–90%			8	ns
Jitter (short term)	Cycle-to-cycle		50		ps
Jitter (long term)	Accumulative over 10 ms			1	ns
Symmetry	Duty cycle	40%		60%	
Load capacitance			15	30	pF

Table 6-4. 50-MHz Oscillator Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			50		MHz
Frequency tolerance	Operational temperature			±50	ppm
Frequency stability	1 year aging			±50	ppm
Rise / fall time	10%–90%			6	ns
Jitter (short term)	Cycle-to-cycle		50		ps
Jitter (long term)	Accumulative over 10 ms			1	ns
Symmetry	Duty cycle	40%		60%	

Table 6-5. 25-MHz Crystal Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency tolerance	Operational temperature			±50	ppm
	At 25°C			±50	ppm
Frequency stability	1 year aging			±5	ppm
Load capacitance		10		40	pF

6.3.3 Thermal Vias Recommendation

The following thermal via guidelines apply to DOWN_PAD, pin 33:

1. Thermal via size = 0.2mm
2. Recommend 4 vias
3. Vias have a center to center separation of 2mm.

Adherence to this guideline is required to achieve the intended operating temperature range of the device. Figure 6-7 illustrates an example layout.

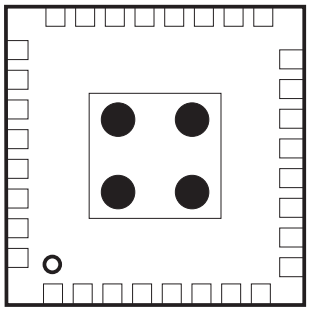


Figure 6-7. Example Layout

7 Device and Documentation Support

7.1 Documentation Support

The following documents describe the TLK10xL devices. Copies of these documents are available on the Internet at www.ti.com.

SLVA531 ***TLK1XX Design & Layout Guide.***

7.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLK105L	Click here	Click here	Click here	Click here	Click here
TLK106L	Click here	Click here	Click here	Click here	Click here

7.3 Community Resources

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

7.4 Trademarks

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7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical Packaging and Orderable Information

8.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLK105LRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLK105L	Samples
TLK105LRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLK105L	Samples
TLK106LRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	TLK106L	Samples
TLK106LRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	TLK106L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

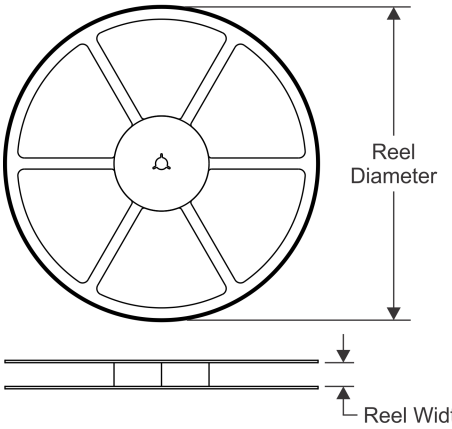
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

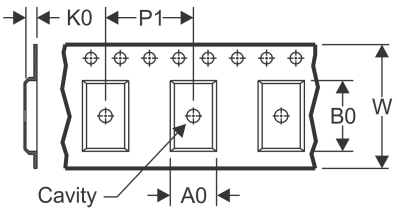
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

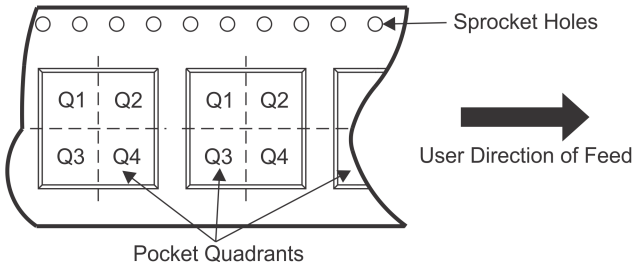


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

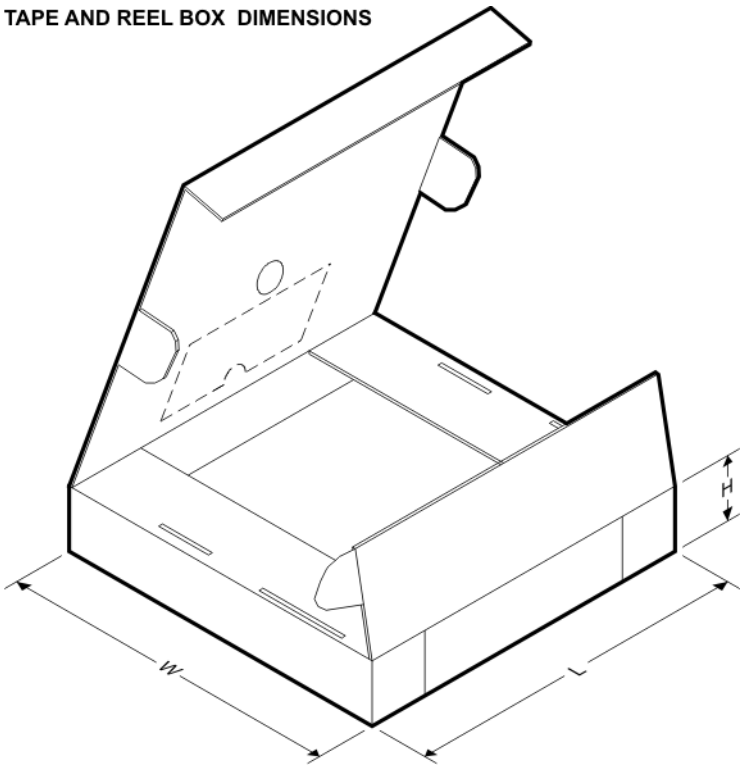
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLK105LRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TLK105LRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TLK106LRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TLK106LRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLK105LRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
TLK105LRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
TLK106LRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
TLK106LRHBT	VQFN	RHB	32	250	210.0	185.0	35.0

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