FemtoClock™ Crystal/LVCMOS-to-3.3V, 2.5V LVPECL Frequency Synthesizer

ICS843001I-22

DATA SHEET

General Description

The ICS843001I-22 is a a highly versatile, low phase noise LVPECL/LVCMOS Synthesizer which can generate low jitter reference clocks for a variety of communications applications and is a member of the HiPerClocks™ family of high performance clock solutions from IDT. The dual crystal interface allows the synthesizer to support up to two communication standards in a given application (i.e. 1GB Ethernet with a 25MHz crystal and 1Gb Fibre Channel using a 26.5625MHz crystal). The rms phase jitter performance is typically less than 1ps, thus making the device acceptable for use in demanding applications such as OC48 SONET and 10Gb Ethernet. The ICS843001I-22 is packaged in a small 24-pin TSSOP package.

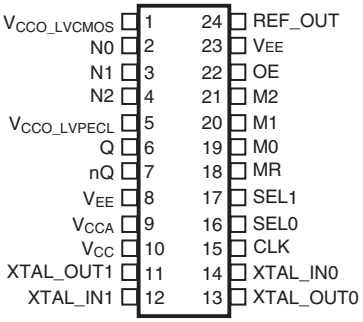
Control Input Function Table

Input	Outputs	
OE	**Q/nQ**	**REF_OUT**
0	High-Impedance	High-Impedance
1	High-Impedance	Active
FLOAT	Active	High-Impedance

Features

- One 3.3Vdifferential LVPECL output pair and one LVCMOS/LVTTL single-ended reference clock output
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- VCO range: 490MHz – 640MHz
- Output frequency range: 49MHz – 640MHz
- Supports the following applications: SONET, Ethernet, Fibre Channel, Serial ATA, and HDTV
- RMS phase jitter @ 125MHz (1.875MHz - 20MHz): 0.50ps (typical)
- Full 3.3V or 2.5V supply mode
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) package

Pin Assignment



ICS843001I-22

24-Lead TSSOP
4.4mm x 7.8mm x 0.925mm
package body
G Package
Top View

Block Diagram

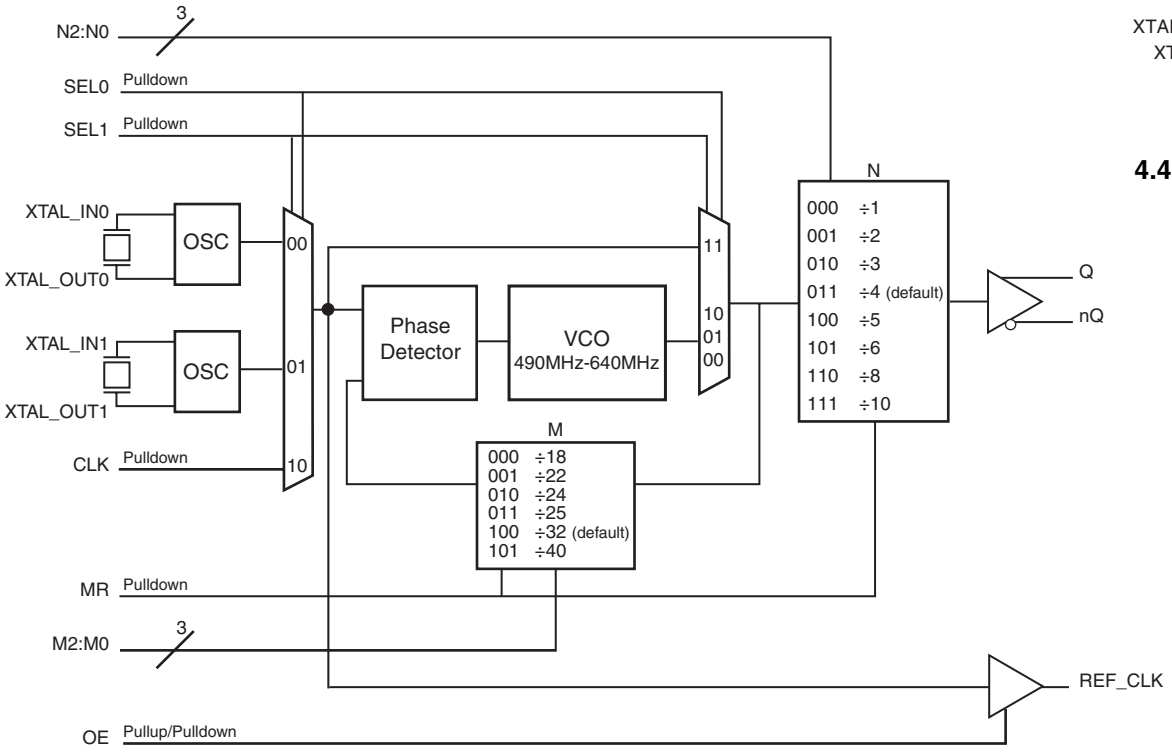


Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{CCO_LVCMOS}	Power		Output supply pin for REF_CLK output.
2, 3	N0, N1	Input	Pullup	Output divider select pins. Default ÷4. LVCMOS/LVTTL interface levels. See Table 3C.
4	N2	Input	Pulldown	
5	V_{CCO_LVPECL}	Power		Output supply pin for LVPECL output.
6, 7	Q, nQ	Output		Differential output pair. LVPECL interface levels.
8, 23	V_{EE}	Power		Negative supply pins.
9	V_{CCA}	Power		Analog supply pin.
10	V_{CC}	Power		Core supply pin.
11, 12	XTAL_OUT1, XTAL_IN1	Input		Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input.
13, 14	XTAL_OUT0, XTAL_IN0	Input		Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input.
15	CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
16, 17	SEL0, SEL1	Input	Pulldown	Input MUX select pins. LVCMOS/LVTTL interface levels. See Table 3D.
18	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true output Q to go low and the inverted output nQ to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
19, 20	M0, M1	Input	Pulldown	Feedback divider select pins. Default value = ÷32. See Table 3B. LVCMOS/LVTTL interface levels.
21	M2	Input	Pullup	
22	OE	Input		3-State clock output enable, (High/Low/Float). See page 1, *Control Input Function Table.*
24	REF_OUT	Output		Reference clock output. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	REF_OUT			15		Ω

Function Tables

Table 3A. Common Configuration Table

Input Reference Clock (MHz)	M Divider Value	N Divider Value	VCO (MHz)	Output Frequency (MHz)	Application
27	22	8	594	74.25	HDTV
22.4	25	8	560	70	
24.75	24	8	594	74.25	HDTV
25	24	3	600	200	Processor
14.8351649	40	8	593.4066	74.1758245	HDTV
19.44	32	4	622.08	155.52	SONET
19.44	32	8	622.08	77.76	SONET
19.44	32	1	622.08	622.08	SONET
19.44	32	2	622.08	311.04	SONET
19.53125	32	4	625	156.25	10 GigE
20	25	2	500	250	Ethernet
25	25	5	625	125	1 GigE
25	25	10	625	62.5	1 GigE
25	24	6	600	100	PCI Express
25	24	4	600	150	SATA
25	24	8	600	75	SATA
26.5625	24	6	637.5	106.25	Fibre Channel 1
26.5625	24	3	637.5	212.5	4 Gig Fibre Channel
26.5625	24	4	637.5	159.375	10 Gig Fibre Channel
31.25	18	3	562.5	187.5	12 GigE

Table 3B. Programmable M Output Divider Function Table

Inputs			M Divider Value	Input Frequency (MHz)	
M2	M1	M0		Minimum	Maximum
0	0	0	18	27.22	35.56
0	0	1	22	22.27	29.09
0	1	0	24	20.41	26.67
0	1	1	25	19.6	25.6
1	0	0	32	15.31	20
1	0	1	40	12.25	16

Table 3C. Programmable N Output DividerFunction Table

Inputs			M Divider Value
N2	N1	N0	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4 (default)
1	0	0	5
1	0	1	6
1	1	0	8
1	1	1	10

Table 3D. Bypass Mode Function Table

Inputs			
SEL1	SEL0	Reference	PLL Mode
0	0	XTAL0	Active
0	1	XTAL1	Active
1	0	CLK	Active
1	1	CLK	Bypass

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current Outputs, V_O (LVCMOS)	 50mA 100mA -0.5V to V_{CCO_LVCMOS} + 0.5V
Package Thermal Impedance, θ_{JA}	70°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCO\_LVCMOS} = V_{CCO\_LVPECL} = 3.3V \pm 10\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.97	3.3	3.63	V
V_{CCA}	Analog Supply Voltage		2.97	3.3	3.63	V
V_{CCO_PECL}, V_{CCO_CMOS}	Output Supply Voltage		2.97	3.3	3.63	V
I_{EE}	Power Supply Current				160	mA
I_{CCO_LVPECL} + I_{CCO_LVCMOS}	Output Supply Current				8	mA

Table 4B. Power Supply DC Characteristics, $V_{CC} = V_{CCO\_LVCMOS} = V_{CCO\_LVPECL} = 2.5V \pm 5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
V_{CCA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{CCO_PECL}, V_{CCO_CMOS}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				155	mA
I_{CCO_LVPECL} + I_{CCO_LVCMOS}	Output Supply Current				8	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO\_LVCMOS} = 3.3V \pm 10\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		$V_{CC} = 3.63V$	2		$V_{CC} + 0.3$	V
			$V_{CC} = 2.625V$	1.7		$V_{CC} + 0.3$	V
V_{IM}	Input Medium Voltage		$V_{CC} = 3.63V$				V
			$V_{CC} = 2.625V$				V
V_{IL}	Input Low Voltage		$V_{CC} = 3.63V$	-0.3		0.8	V
			$V_{CC} = 2.625V$	-0.3		0.7	V
I_{IH}	Input High Current	CLK, M0, M1, N2, MR, OE, SEL0, SEL1	$V_{CC} = V_{IN} = 3.63V$ or $2.625V$			150	µA
		M2, N0, N1	$V_{CC} = V_{IN} = 3.63V$ or $2.625V$			5	µA
I_{IM}	Input Medium Current						µA
I_{IL}	Input Low Current	CLK, M0, M1, N2, MR, OE, SEL0, SEL1	$V_{CC} = 3.63V$ or $2.625V$, $V_{IN} = 0V$	-5			µA
		M2, N0, N1, OE	$V_{CC} = 3.63V$ or $2.625V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage: NOTE 1	REF_OUT	$V_{CCO\_LVCMOS} = 3.63V$	2.6			V
			$V_{CCO\_LVCMOS} = 2.625V$	1.8			V
V_{OL}	Output Low Voltage: NOTE 1	REF_OUT	$V_{CCO\_LVCMOS} = 3.63V$ or $2.625V$			0.5	V

NOTE 1: Output terminated with 50Ω to $V_{CCO\_LVCMOS}/2$. See Parameter Measurement Information Section, "3.3V LVCMOS Output Load Test Circuit Diagram".

Table 4D. LVPECL DC Characteristics, $V_{CC} = V_{CCO\_LVPECL} = 3.3V \pm 10\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Current; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 0.9$	µA
V_{OL}	Output Low Current; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	µA
V_{SWING}	Peak-toPeak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to $V_{CCO\_LVPECL} - 2V$.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		14		35.55	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

Table 6. Input Frequency Characteristics, $V_{CC} = V_{CCO\_LVCMOS} = V_{CCO\_LVPECL}$ 3.3V ± 10%, V_{EE} = 0V,T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	CLK	SEL1 = 1, SEL0 = 0	14		35.55	MHz
		CLK	SEL1 = 1, SEL0 = 0	DC		250	MHz

AC Electrical Characteristics

Table 7A. AC Characteristics, $V_{CC} = V_{CCO\_LVCMOS} = V_{CCO\_LVPECL}$ = 3.3V ± 10%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			49		640	MHz
t_{jit}(Ø)	RMS Phase Jitter, (Random); NOTE 1		125MHz, (1.875MHz – 20MHz)		0.50		ps
f_{VCO}	PLL VCO Lock Range			490		640	MHz
t_R / t_F	Output Rise/Fall Time	Q/nQ	20% to 80%	200		500	ps
		REF_OUT	20% to 80%	200		700	ps
odc	Output Duty Cycle	Q/nQ		45		55	%
		REF_OUT	$f \leq$ 250MHz	44		56	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Phase jitter measured using a crystal interface.

Table 7B. AC Characteristics, $V_{CC} = V_{CCO\_LVCMOS} = V_{CCO\_LVPECL} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			49		640	MHz
$t_{jit}(Ø)$	RMS Phase Jitter, (Random); NOTE 1		125MHz, (1.875MHz – 20MHz)		0.50		ps
f_{VCO}	PLL VCO Lock Range			490		640	MHz
t_R / t_F	Output Rise/Fall Time	Q/nQ	20% to 80%	200		500	ps
		REF_OUT	20% to 80%	300		800	ps
odc	Output Duty Cycle	Q/nQ		45		55	%
		REF_OUT	$f \leq 250$MHz	44		56	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Phase jitter measured using a crystal interface.

Typical Phase Noise at 125MHz

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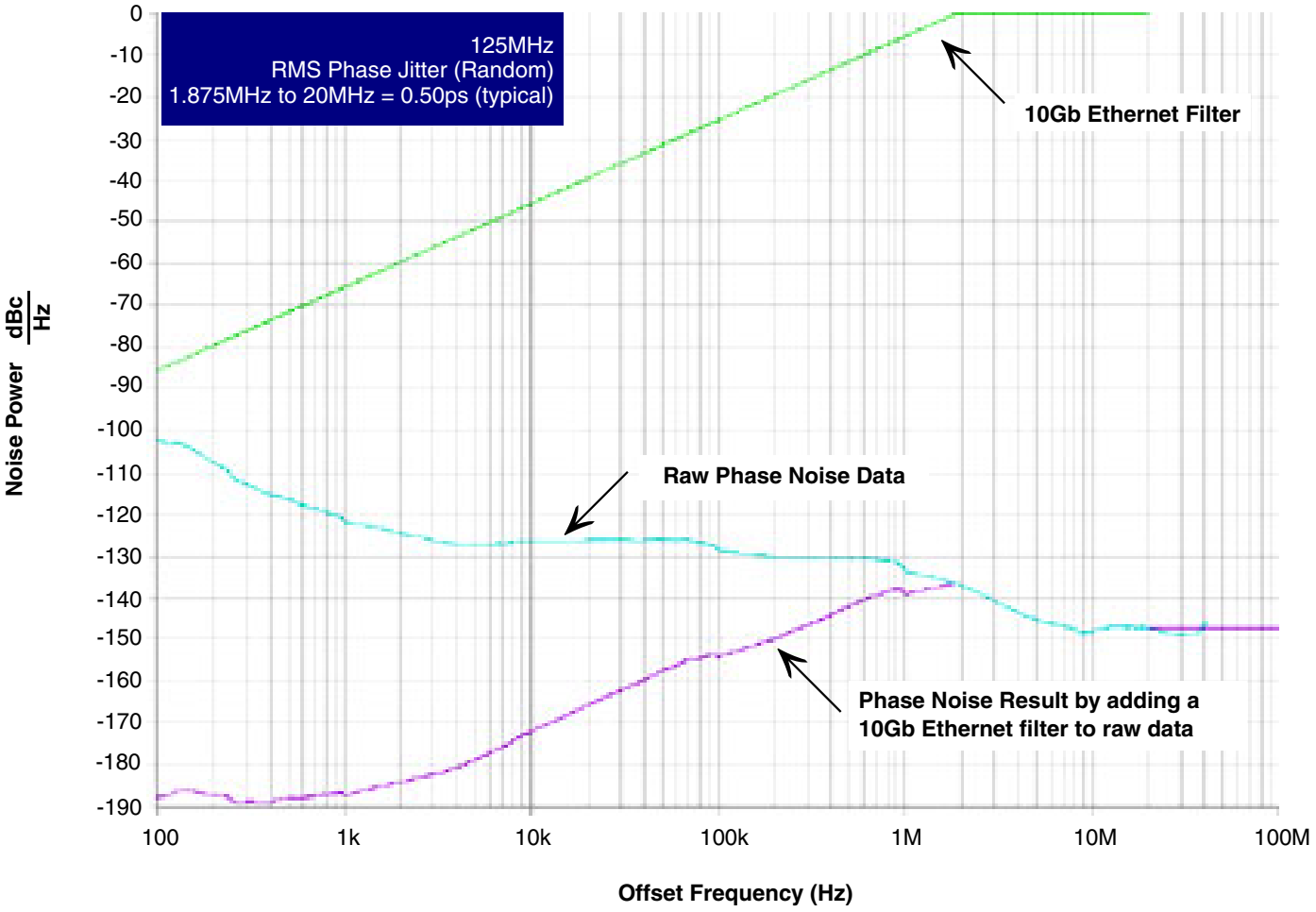
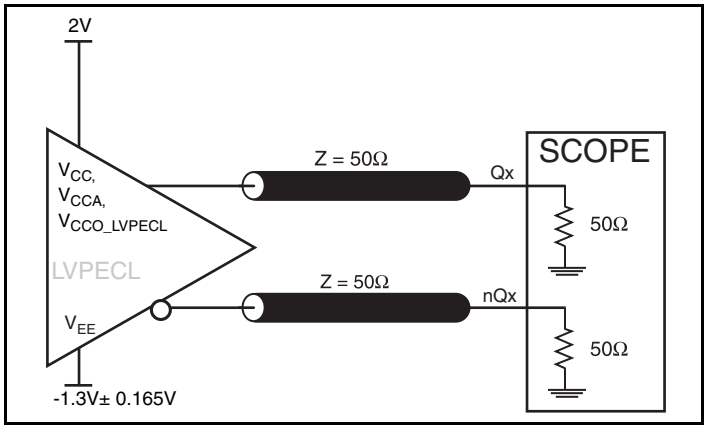
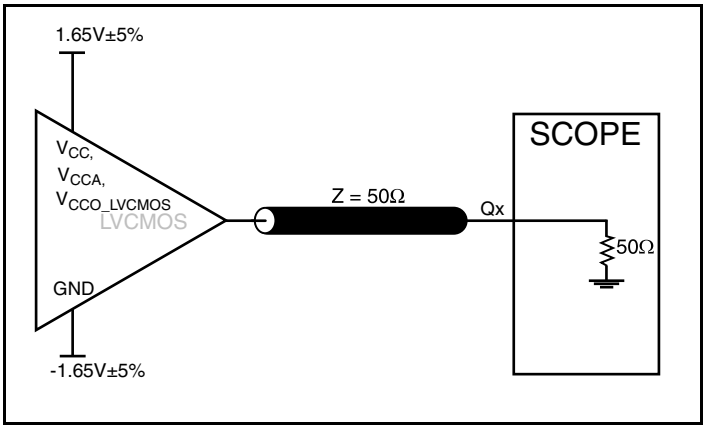


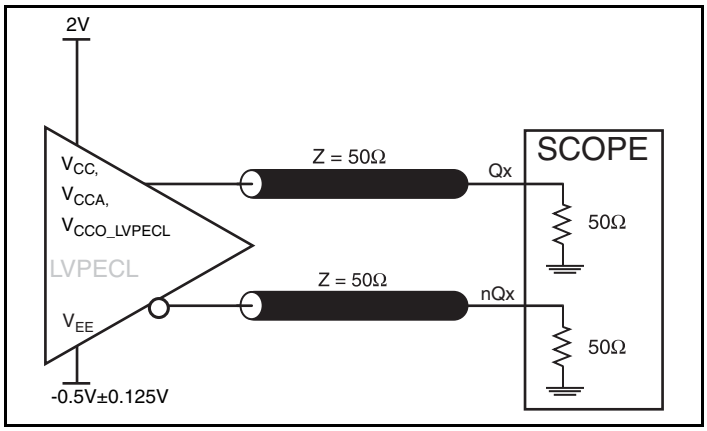
Parameter Measurement Information



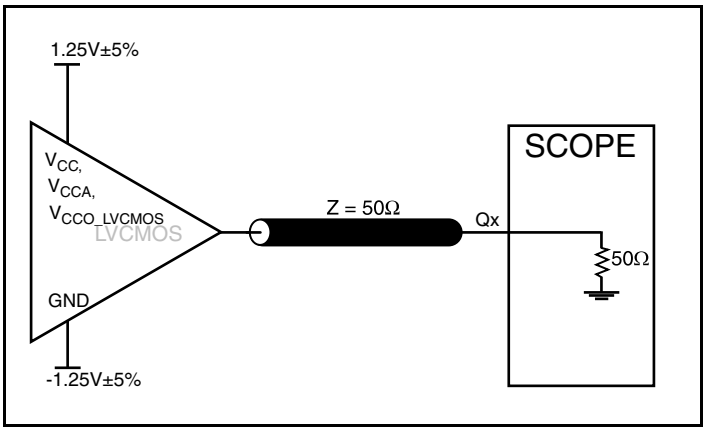
3.3V LVPECL Output Load AC Test Circuit



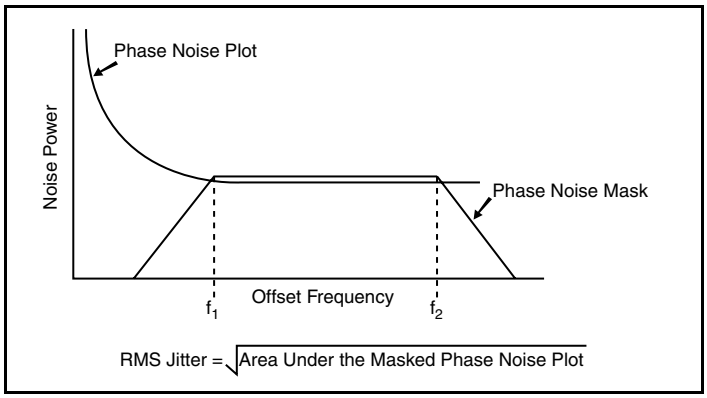
3.3V LVCMOS Output Load AC Test Circuit



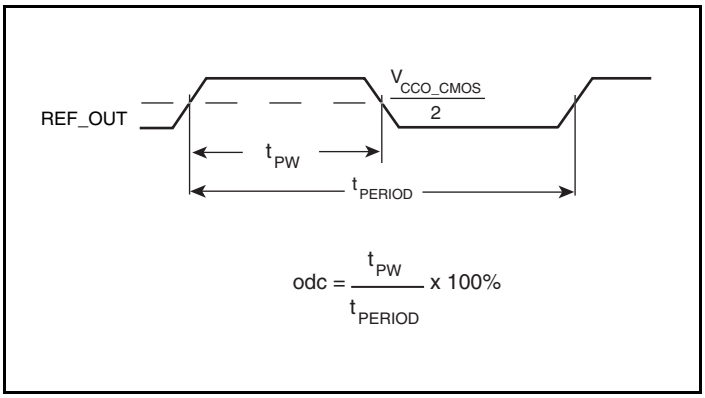
2.5V LVPECL Output Load AC Test Circuit



2.5V LVCMOS Output Load AC Test Circuit

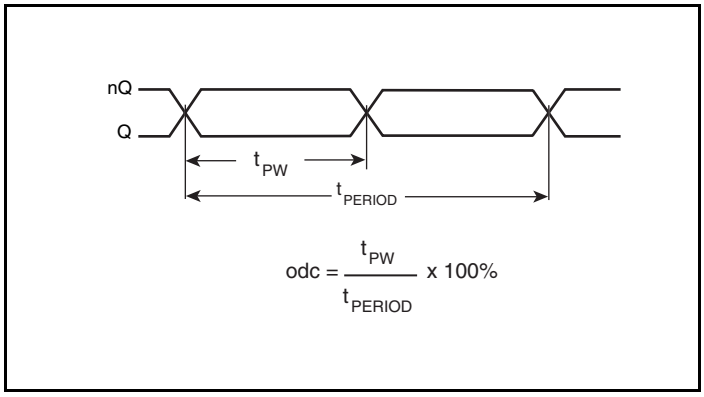


RMS Phase Jitter

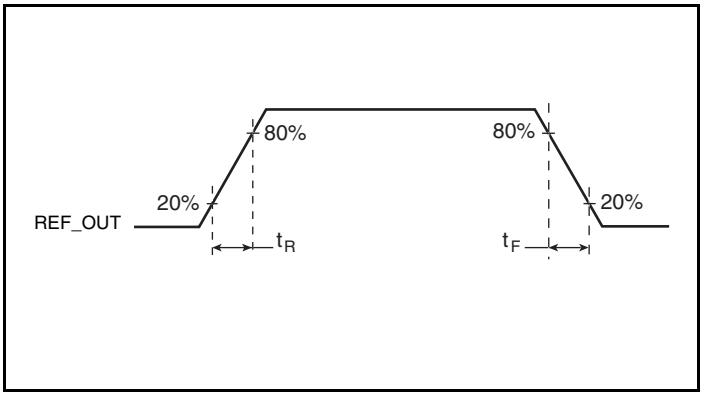


LVCMOS Output Duty Cycle/Pulse Width/Period

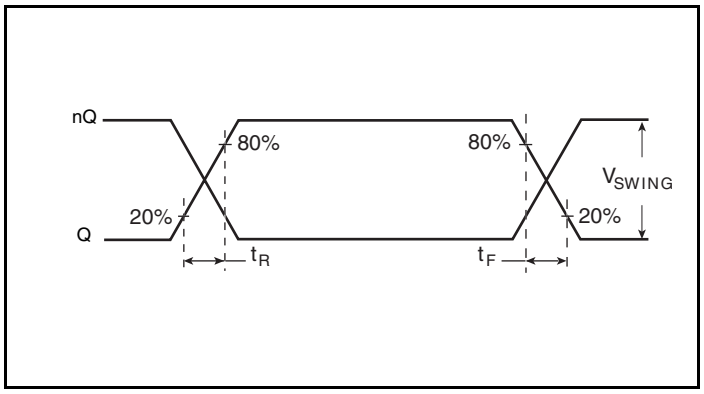
Parameter Measurement Information, continued



LVPECL Output Duty Cycle/Pulse Width/Period



LVCMOS Output Rise/Fall Time



LVPECL Output Rise/Fall Time

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843001I-22 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, V_{CCO_X} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

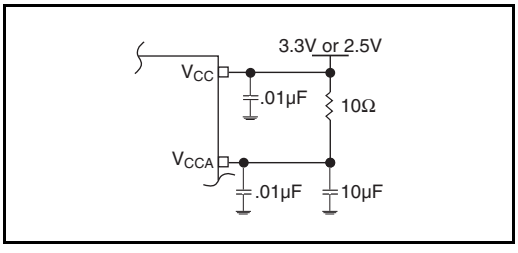


Figure 1. Power Supply Filtering

Crystal Input Interface

The ICS843001I-22 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 26.5625MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

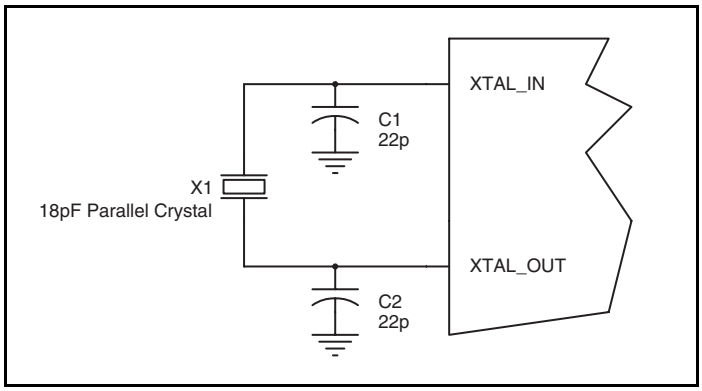


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

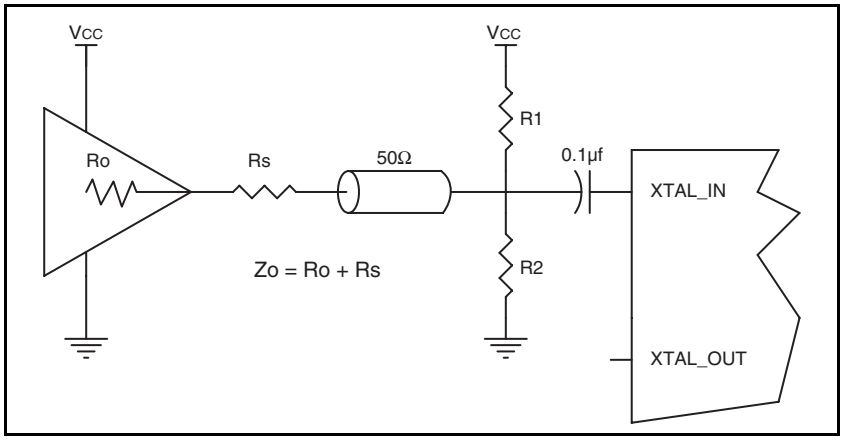


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK Input

For applications not requiring the use of the clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

The unused LVPECL output pair can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVCMOS Output

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

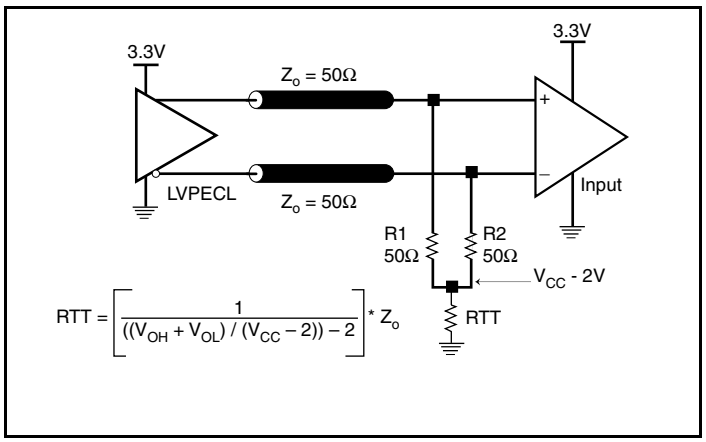


Figure 4A. 3.3V LVPECL Output Termination

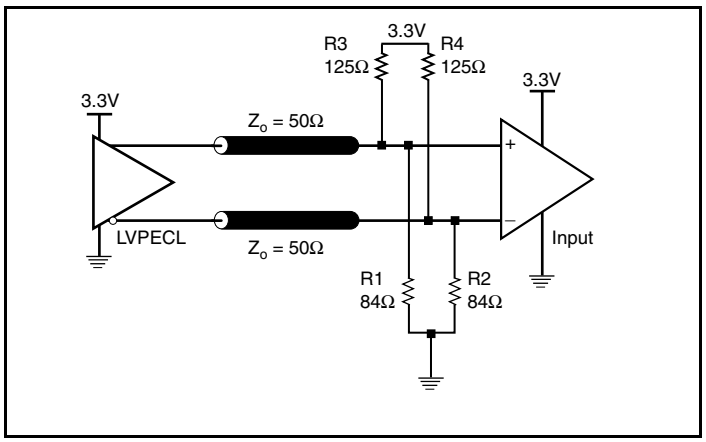


Figure 4B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

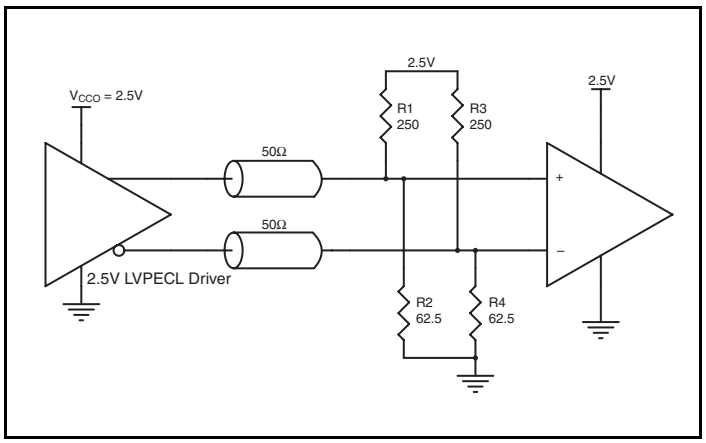


Figure 5A. 2.5V LVPECL Driver Termination Example

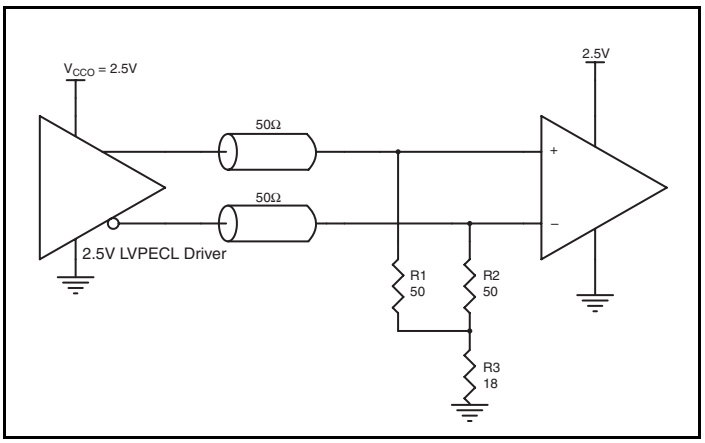


Figure 5B. 2.5V LVPECL Driver Termination Example

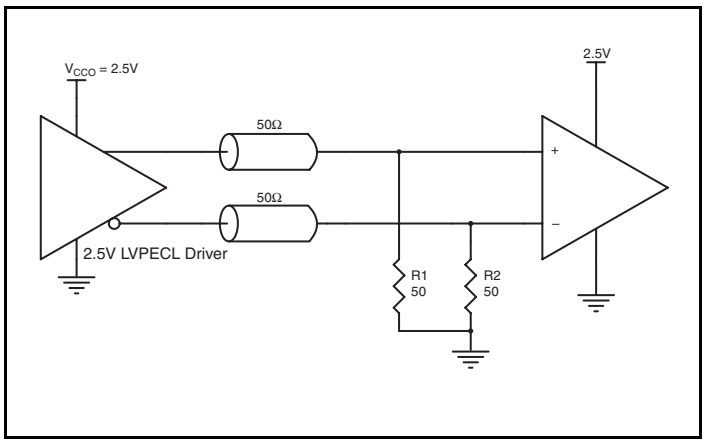
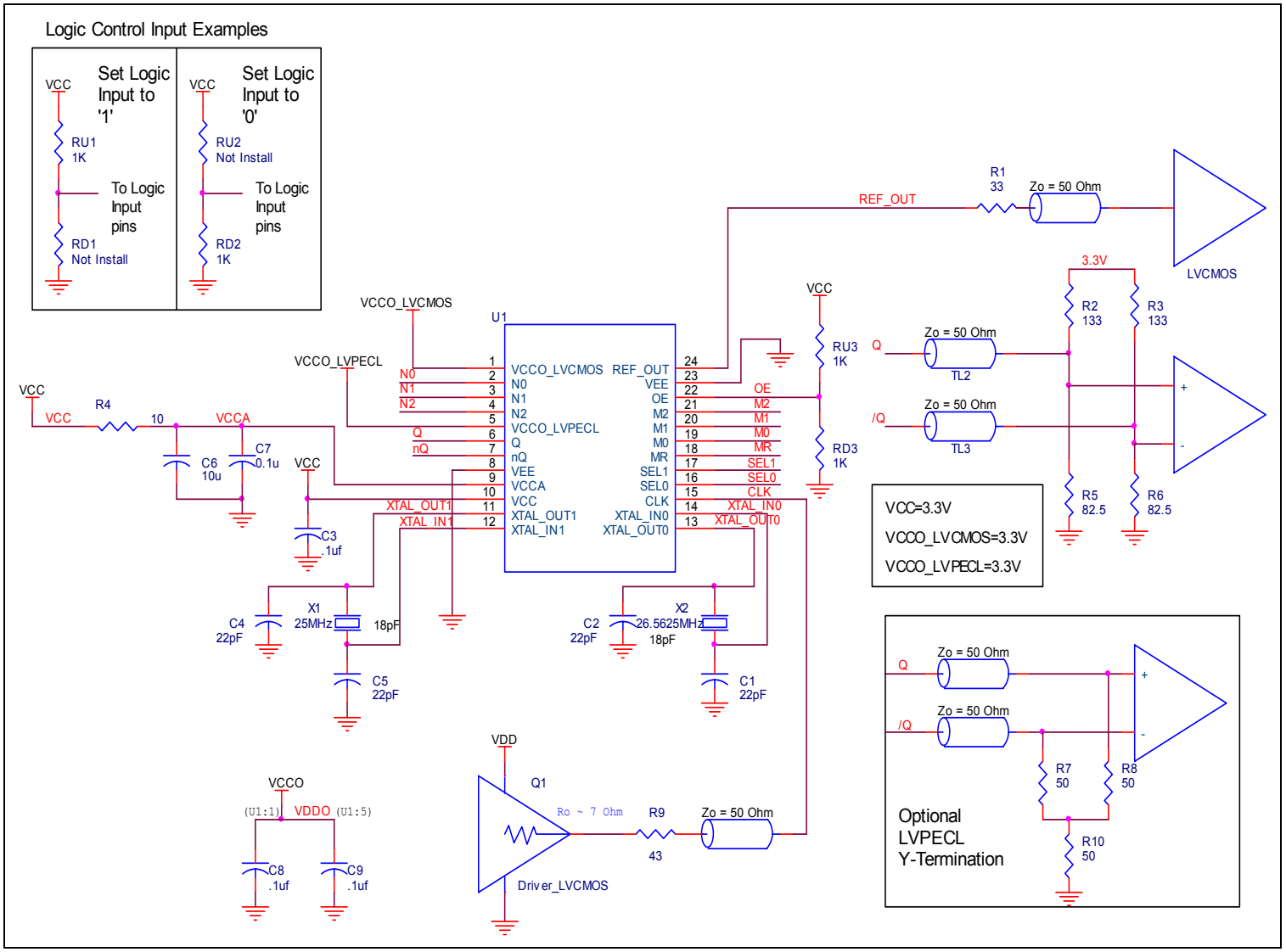


Figure 5C. 2.5V LVPECL Driver Termination Example

Schematic Layout

Figure 6 shows an example of ICS843001I-22 application schematic. In this example, the device is operated at V_{CC} = V_{CCO_LVCMOS} = V_{CCO_LVPECL} = 3.3V. The 18pF parallel resonant 25MHz crystal is used. The C1 = C2 = 22pF and C4 = C5 = 22pF are recommended for frequency accuracy. For different board layouts, the C1, C2, C4 and C5 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVPECL terminations and one example of LVCMOS are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.



ICS843001I-22 Layout Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS843001I-22.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843001I-22 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 160mA = **554.4mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**

Total Power$_{\_MAX}$ (3.3V, with all outputs switching) = 554.4mW + 30mW = **584.4mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 8 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.584W * 65°C/W = 123°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 8. Thermal Resitance θ_{JA} for 24 Lead TSSOP, Forced Convection

θ_{JA} **vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

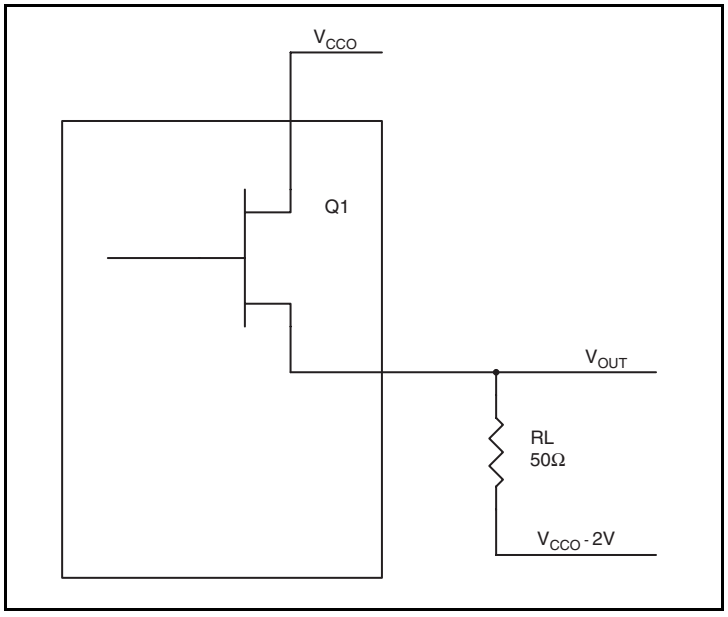


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} – 0.9V}$
  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{COO\_MAX} – 1.7V}$
  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 9. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP

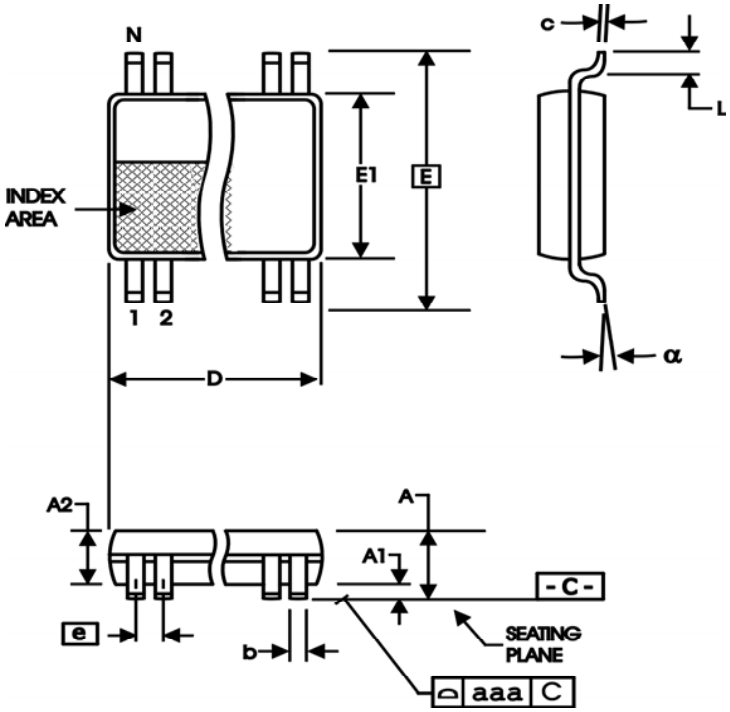
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

Transistor Count

The transistor count for ICS843001I-22 is: 3881

Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP



6.10 mm. Body, 0.65 mm. Pitch TSSOP
(240 mil)* (25.6mil)*

Table 10. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	24	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843001AGI-22	ICS843001AI22	24 Lead TSSOP	Tube	-40°C to 85°C
843001AGI-22T	ICS843001AI22	24 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C
843001AGI-22LF	ICS43001AI22L	“Lead-Free” 24 Lead TSSOP	Tube	-40°C to 85°C
843001AGI-22LFT	ICS43001AI22L	“Lead-Free” 24 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		1 12	General Description - corrected crystal frequency from 25.5625MHz crystal to 26.5625MHz crystal. Added *LVCMOS to XTAL Interface* section. Updated format throughout the datasheet.	3/23/07
A	T11	16 19	Power Considerations - Changed Ambient Temperature from 70° to 85° Ordering Information - Removed “ICS” from Part/Order Number	2/19/09
B		1 15	Corrected block diagram. When updated format on 3/23/07, block diagram was not duplicated correctly. Added Schematic layout. Updated header/footer.	6/25/09

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