RFSA3714

50MHz to 6000MHz, Digital Step Attenuator

Package: QFN, 24-pin,
4.0mm x 4.0mm x 0.85mm

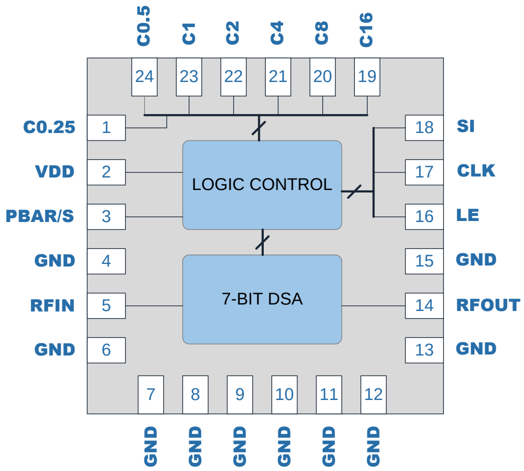
The RFMD's RFSA3714 is a 7-bit digital step attenuator (DSA) that features high linearity over the entire 31.75dB gain control range with 0.25dB steps. The RFSA3714 features three modes of control: serial, latched parallel, and direct parallel programming. The RFSA3714 has a low insertion loss of 1.5dB at 2GHz. Patent pending circuit architecture provides Overshoot-free transient switching performance. The RFSA3714 is available in a 4mm x 4mm QFN package.

Features

- 7-Bit, 31.75dB Range, 0.25dB Step
- Patent Pending Circuit Architecture
- Overshoot-free Transient Switching Performance
- Frequency Range 50MHz to 6000MHz
- High Linearity, IIP3 >55dBm
- Serial and Parallel Control Interface
- Fast Switching Speed, <120nsec
- Single Supply 3V to 5V Operation
- RF Pins Have No DC Voltage, Can be DC Grounded Externally
- Power-up Default Setting Is Maximum Attenuation

Applications

- 2G through 4G Base Stations
- Point-to-Point
- WiFi
- Test Equipment



Functional Block Diagram

Ordering Information

RFSA3714SQ	Sample bag with 25 pieces
RFSA3714SR	7" Reel with 100 pieces
RFSA3714TR13	13" Reel with 2500 pieces
RFSA3714PCK-410	50MHz to 6000MHz PCBA with 5-piece sample bag

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{DD})	-0.5 to +6.0	V
All Other DC and Logic Pins (Supply Voltage Must Be Applied Prior to Any Other Pin Voltages)	-0.5 to +6.0	V
Maximum Input Power at RFIN Pin at 85°C Case Temperature	+30	dBm
Maximum Input Power at RFOUT Pin at 85°C Case Temperature	+27	dBm
Storage Temperature Range	-40 to +150	°C
ESD Rating - Human Body Model (HBM)	1000	V
Moisture Sensitivity Level	MSL1	

Caution! ESD sensitive device.

RFMD Green: RoHS status based on EU Directive 2011/65/EU (at time of this document revision), halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Recommended Operating Condition

Parameter	Specification			Unit
	Min	Typ	Max	
Operating Temperature Range (RF Input Power Handling Derates Above 85°C)	-40		+105	°C
Operating Junction Temperature			125	°C
Supply Voltage	2.7		5.5	V

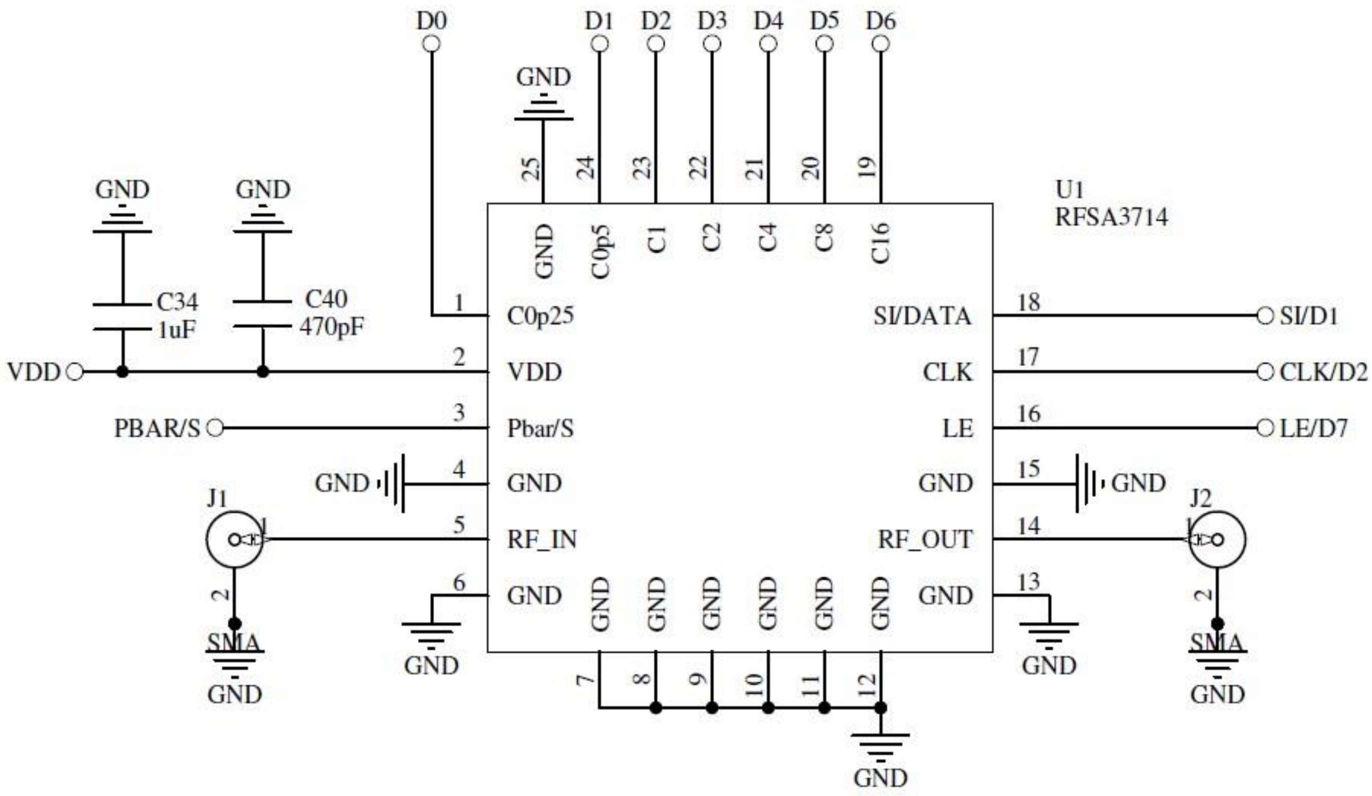
Nominal Operating Parameters

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
General Performance					
Supply Current		180		µA	Steady state operation, current draw during attenuation state transitions is higher.
Thermal Resistance		55		°C/W	At maximum attenuation state with RF power applied to the RFIN pin
RF Input Power at RFIN Pin			27	dBm	Continuous operation at +85°C case temperature
RF Input Power at RFOUT Pin			20	dBm	
RF Performance					
Frequency Range	50		6000	MHz	
Insertion Loss		1.5		dB	2000MHz, 0dB attenuation
Attenuation Range		31.75		dB	0.25dB step size
Absolute Attenuation Error		±(0.2 + 4%)		dB	
Input IP3		55		dBm	
Input P0.1dB		30		dBm	
Return Loss		15		dB	
Input and Output Impedance		50		Ω	

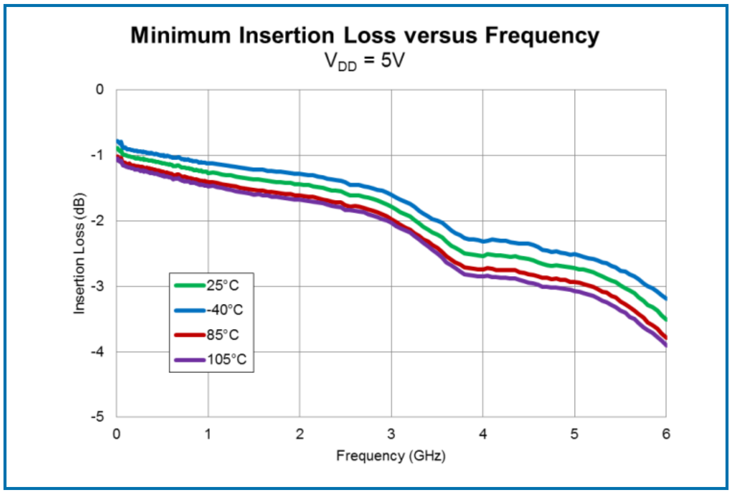
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
General Performance					
Switching Speed		120		nsec	50% control to 10%/90% RF
Successive Step Phase Delta		2		Deg	2000MHz
Control					
Digital Logic Low			0.63	V	
Digital Logic High	1.17			V	

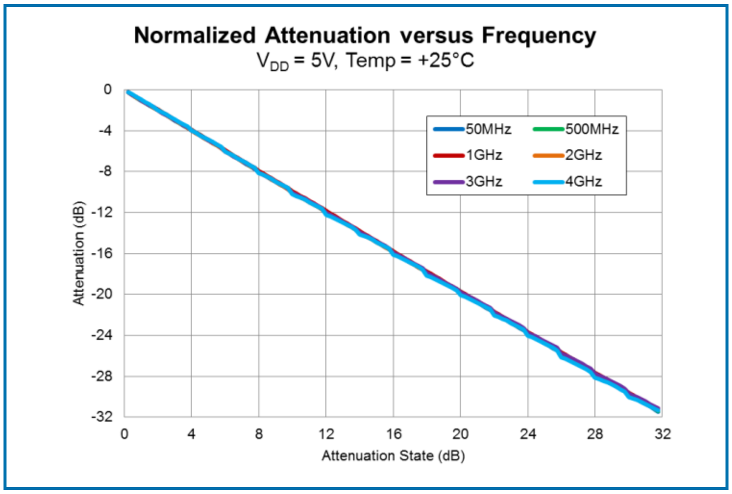
Note: Typical performance at these conditions: Temp = 25°C, 2000MHz, 5V Supply Voltage

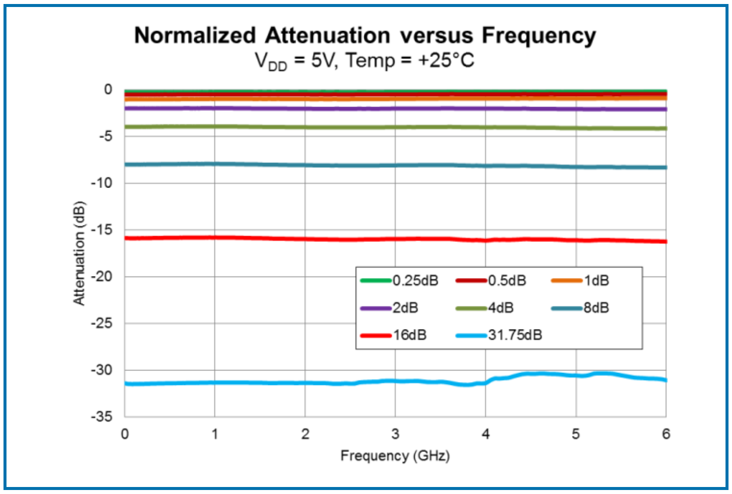
Typical Application Schematic

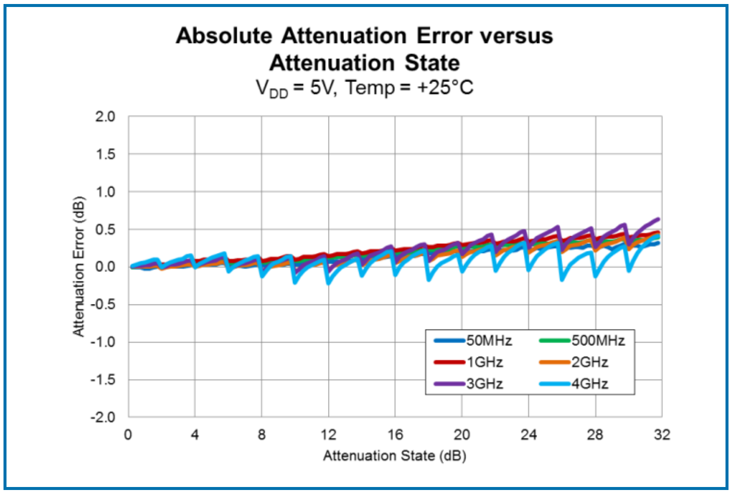


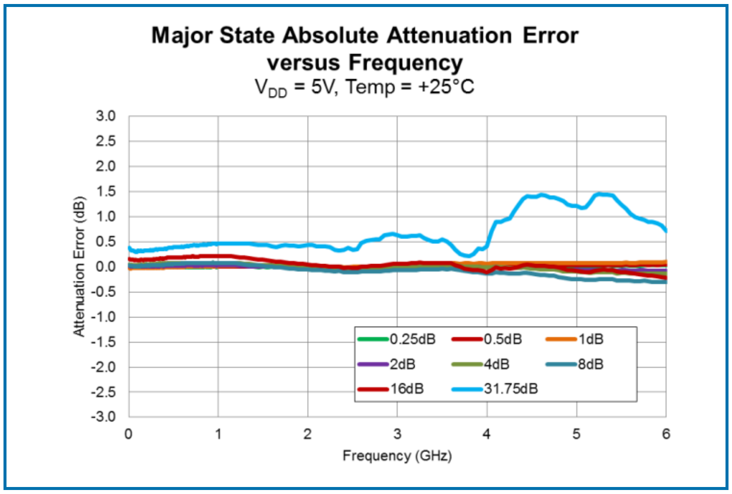
Typical Performance: 0.25dB Steps

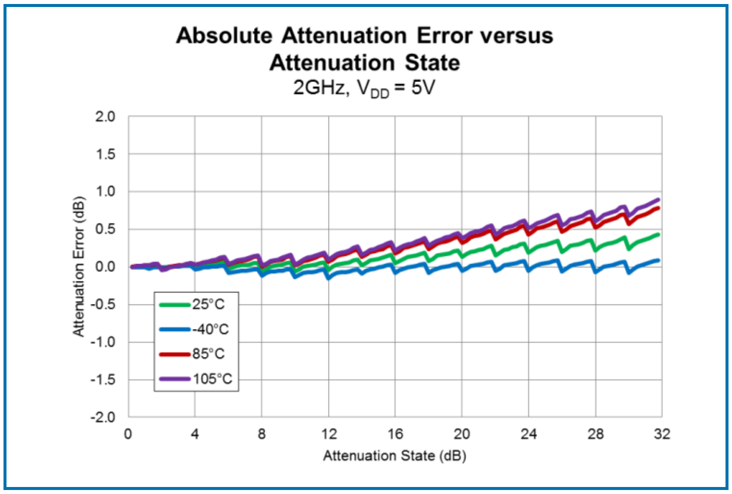




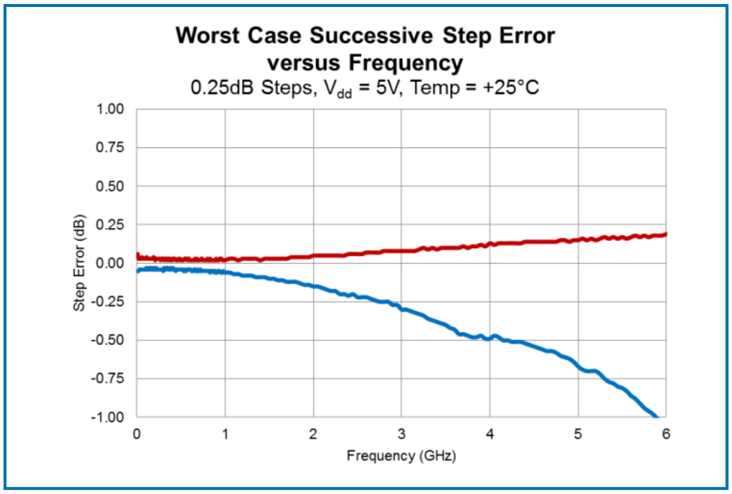


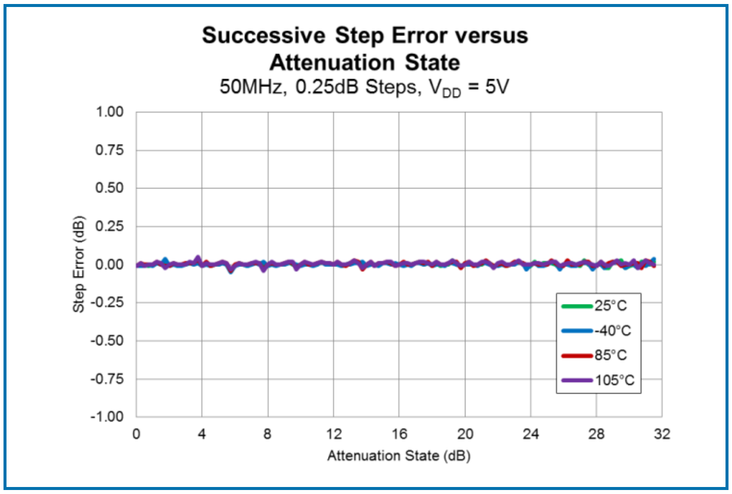


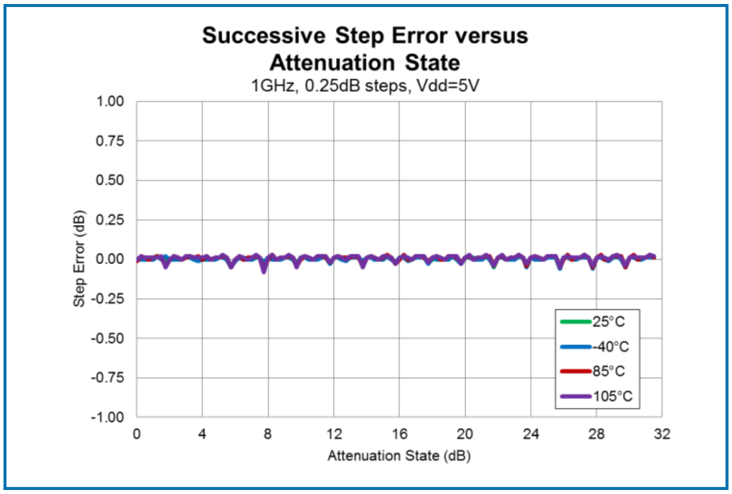


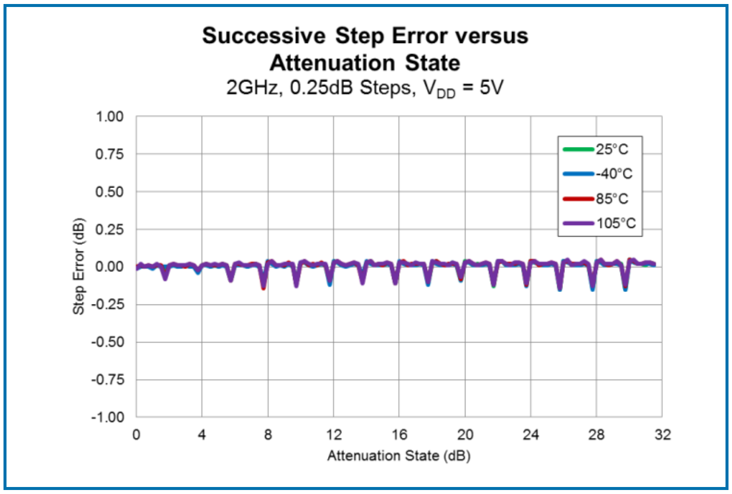


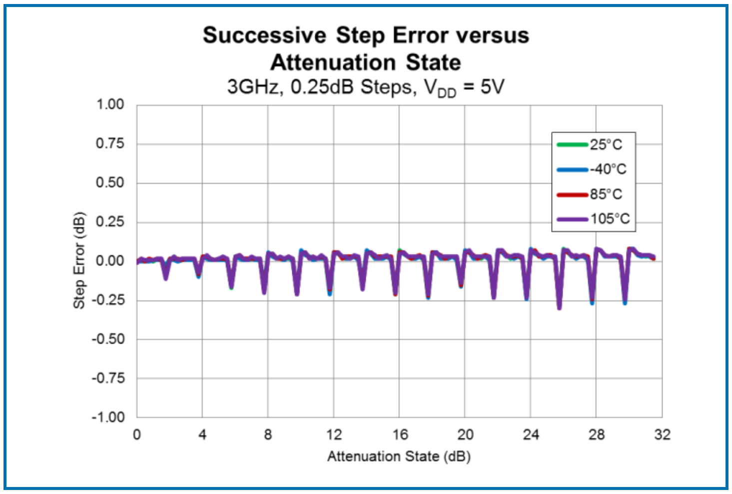
Typical Performance: 0.25dB Steps

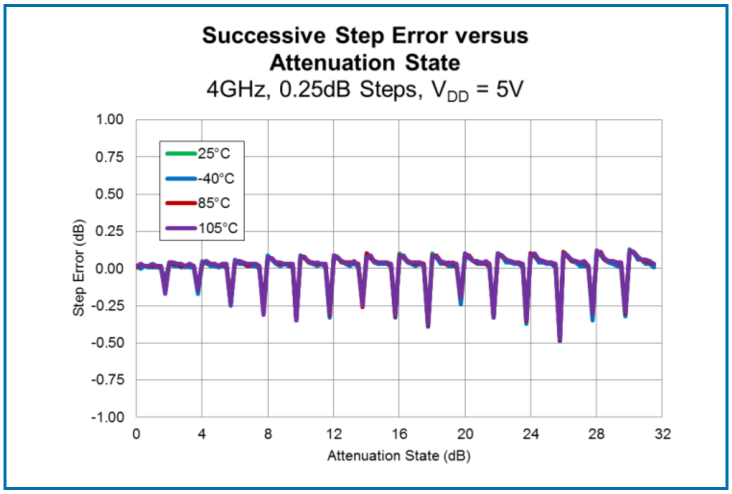






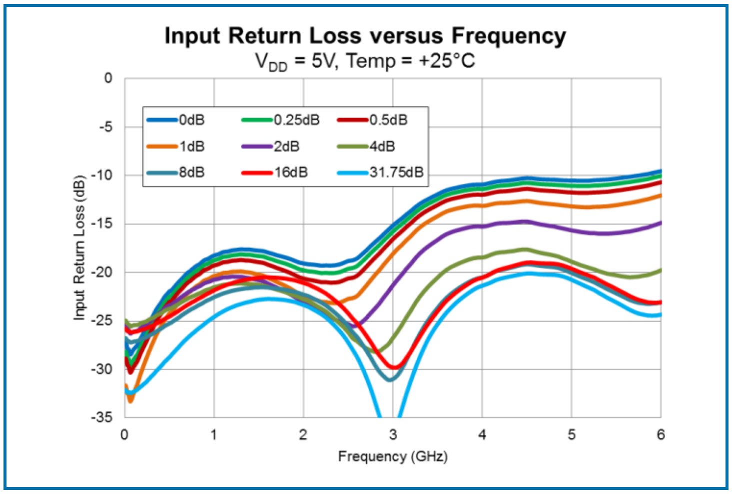


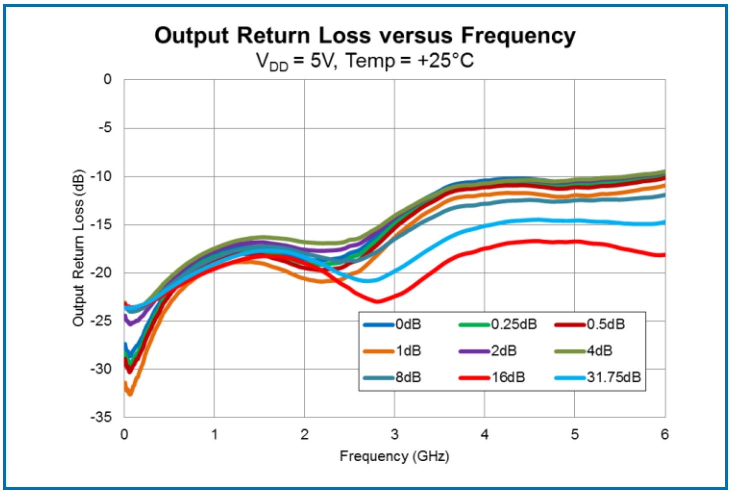


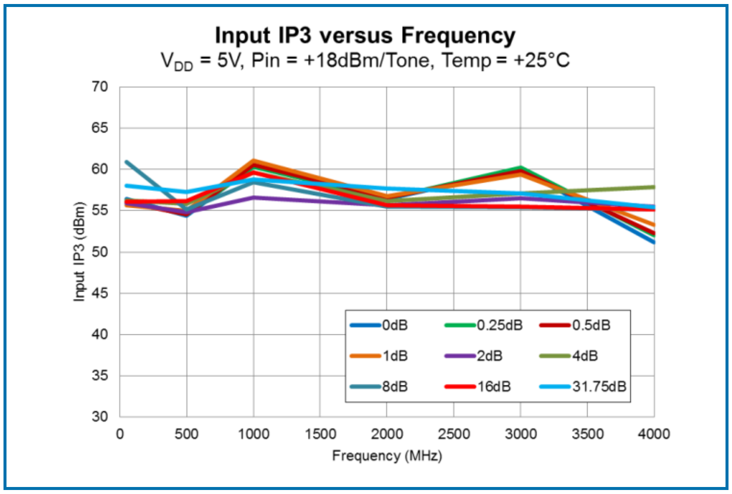


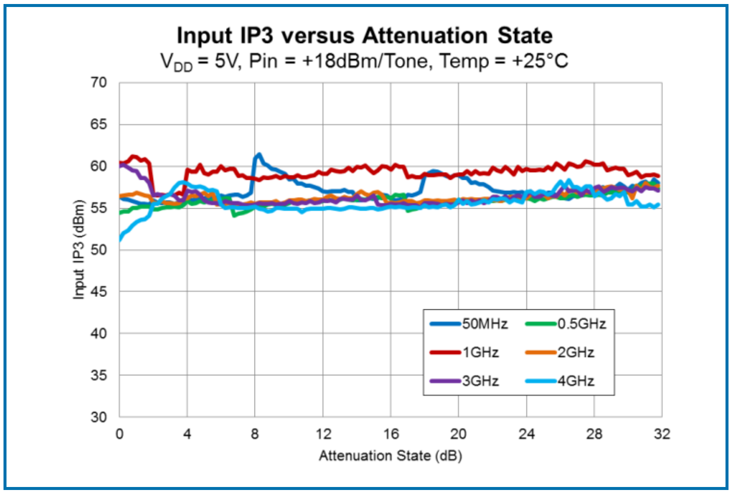
Note: Attenuator remains monotonic if step error is less than +0.25dB.

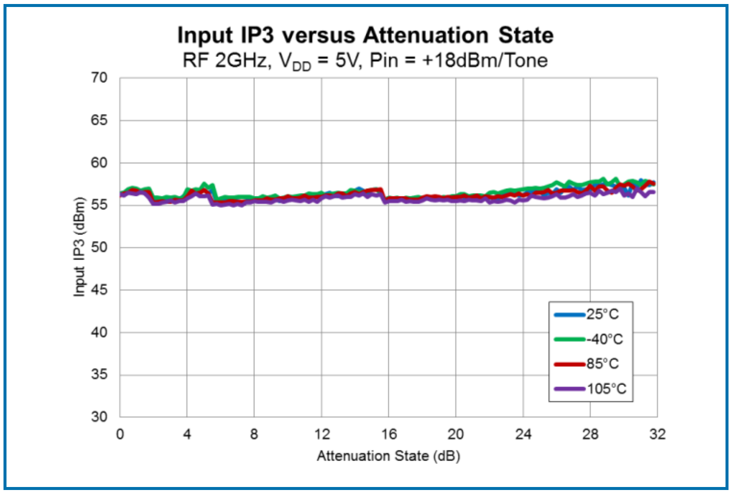
Typical Performance: 0.25dB Steps

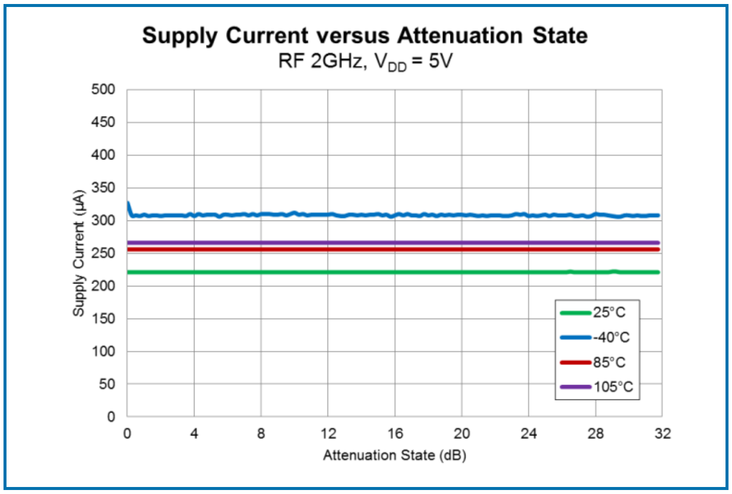




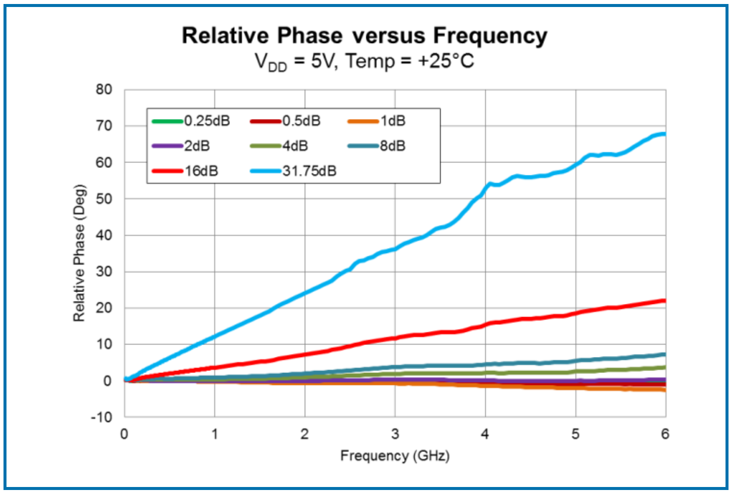


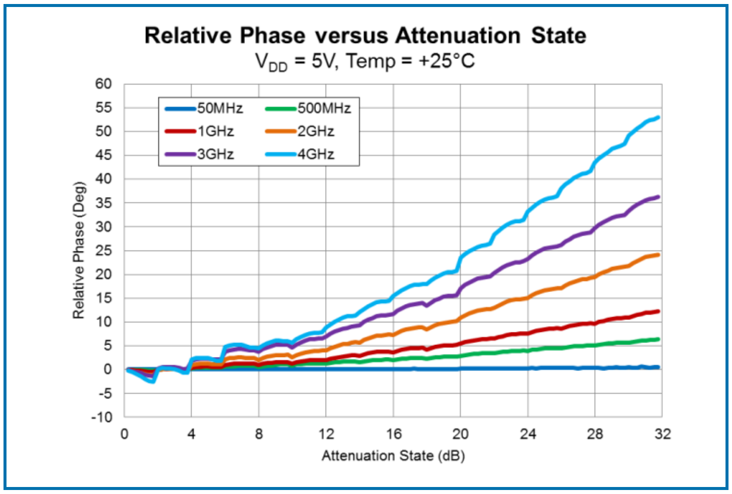


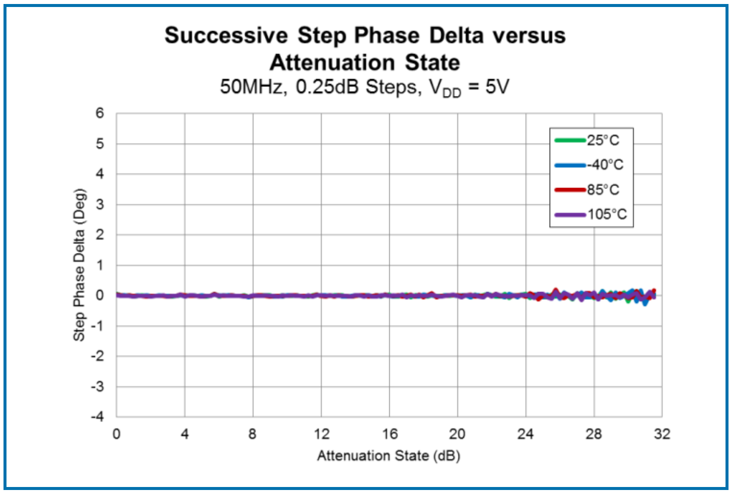


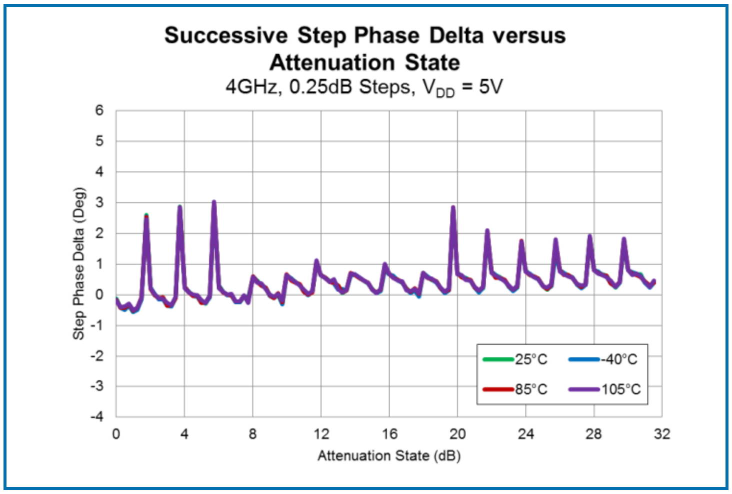


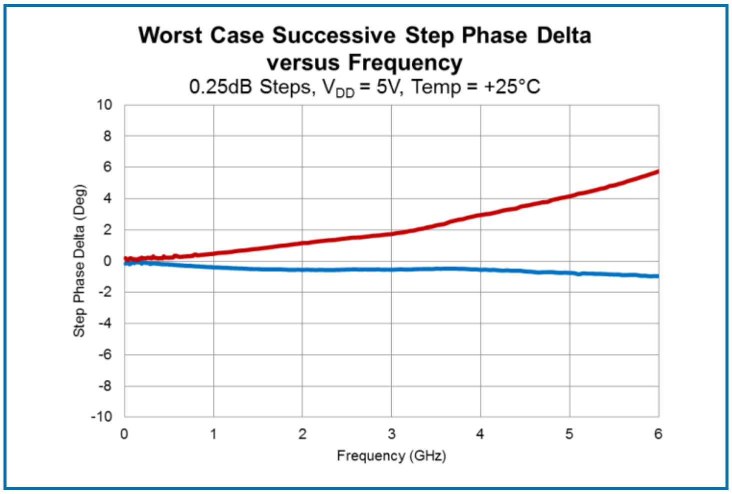
Typical Performance: 0.25dB Steps



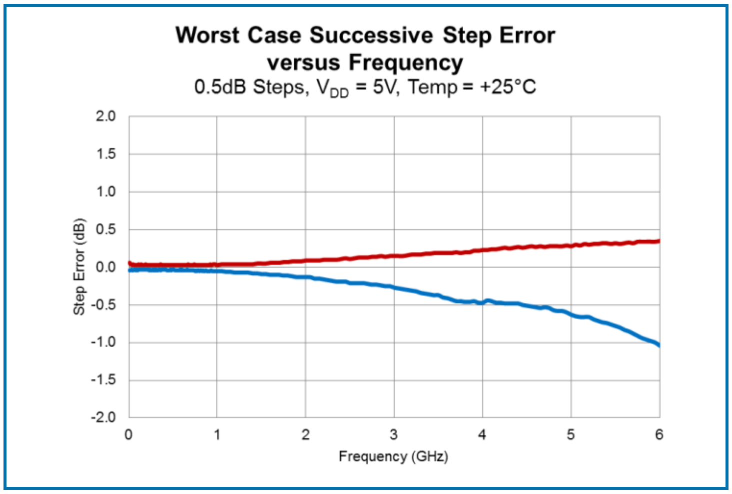


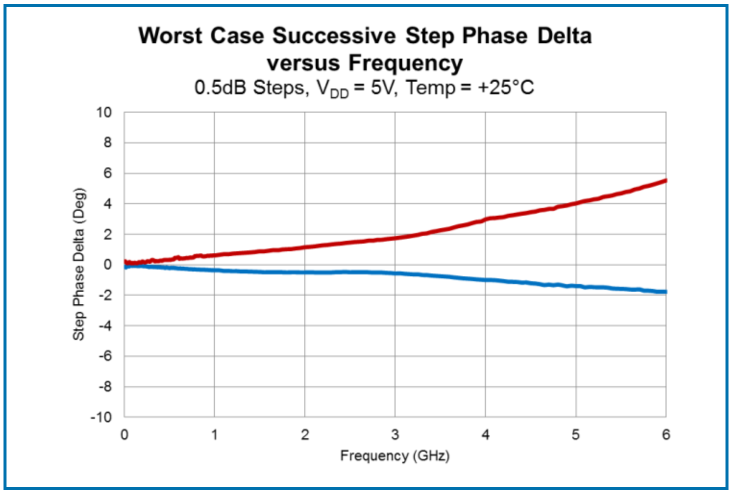




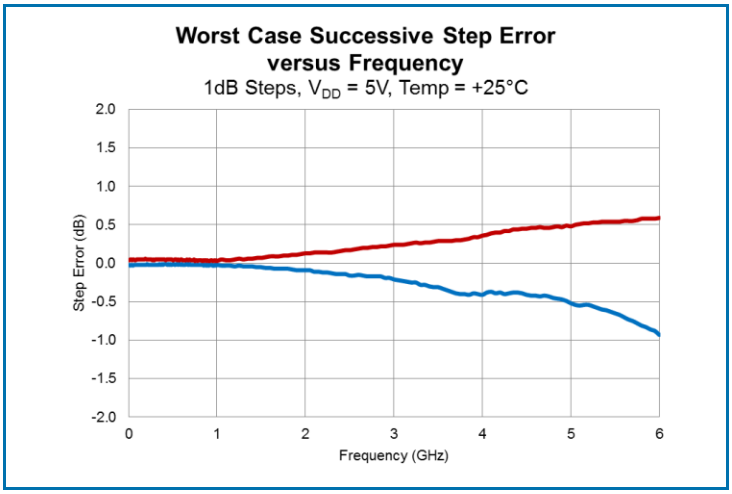


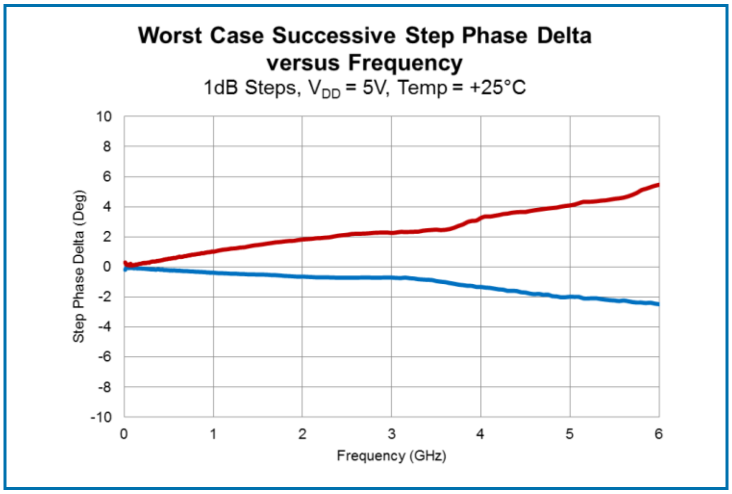
Typical Performance: 0.5dB Steps





Typical Performance: 1.0dB Steps

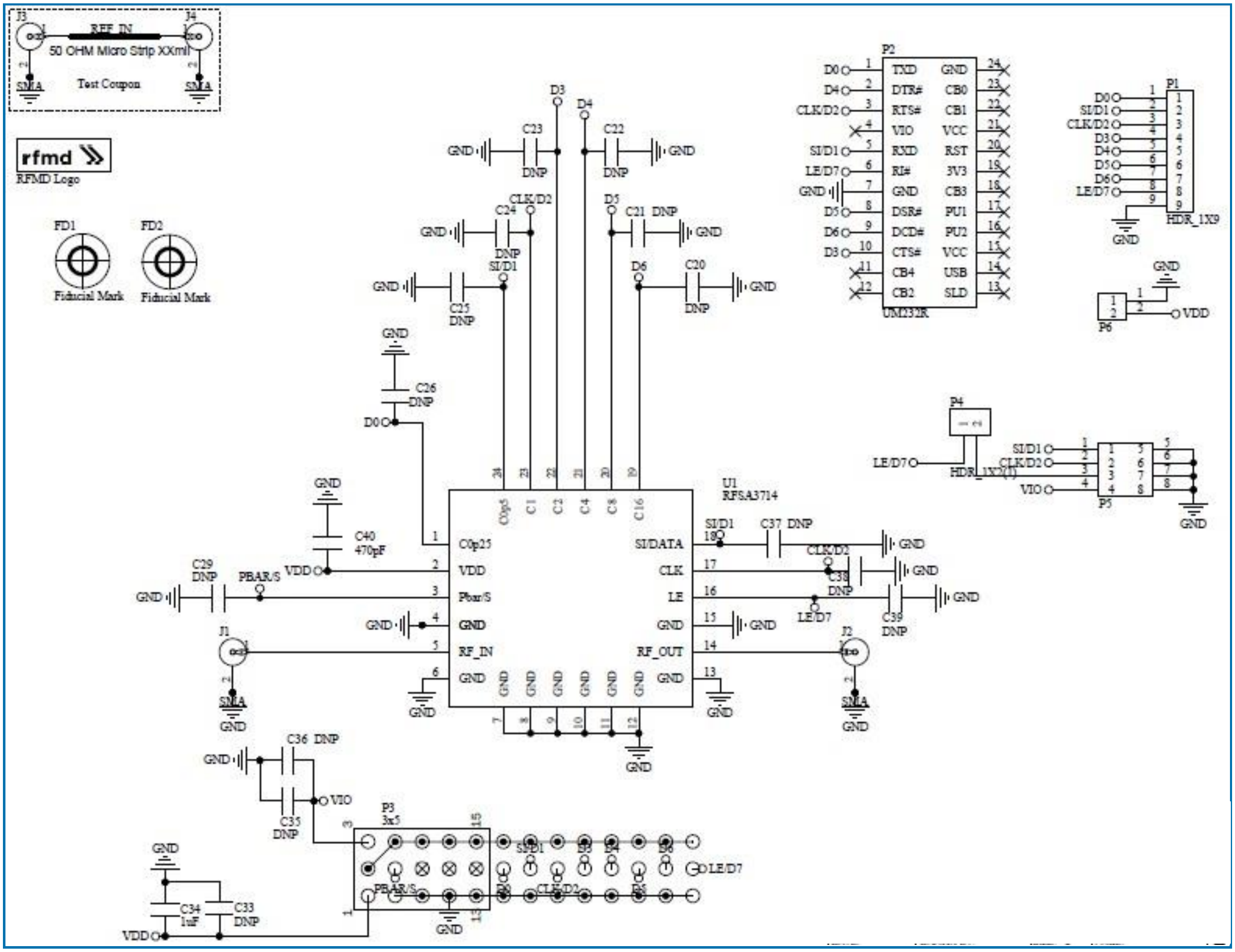




Notes:

1. Top 2 Plots: Attenuator remains monotonic if step error is less than +0.5dB.
2. Bottom 2 Plots: Attenuator remains monotonic if step error is less than +1.0dB

Evaluation Board Schematic 50MHz to 6000MHz Application Circuit

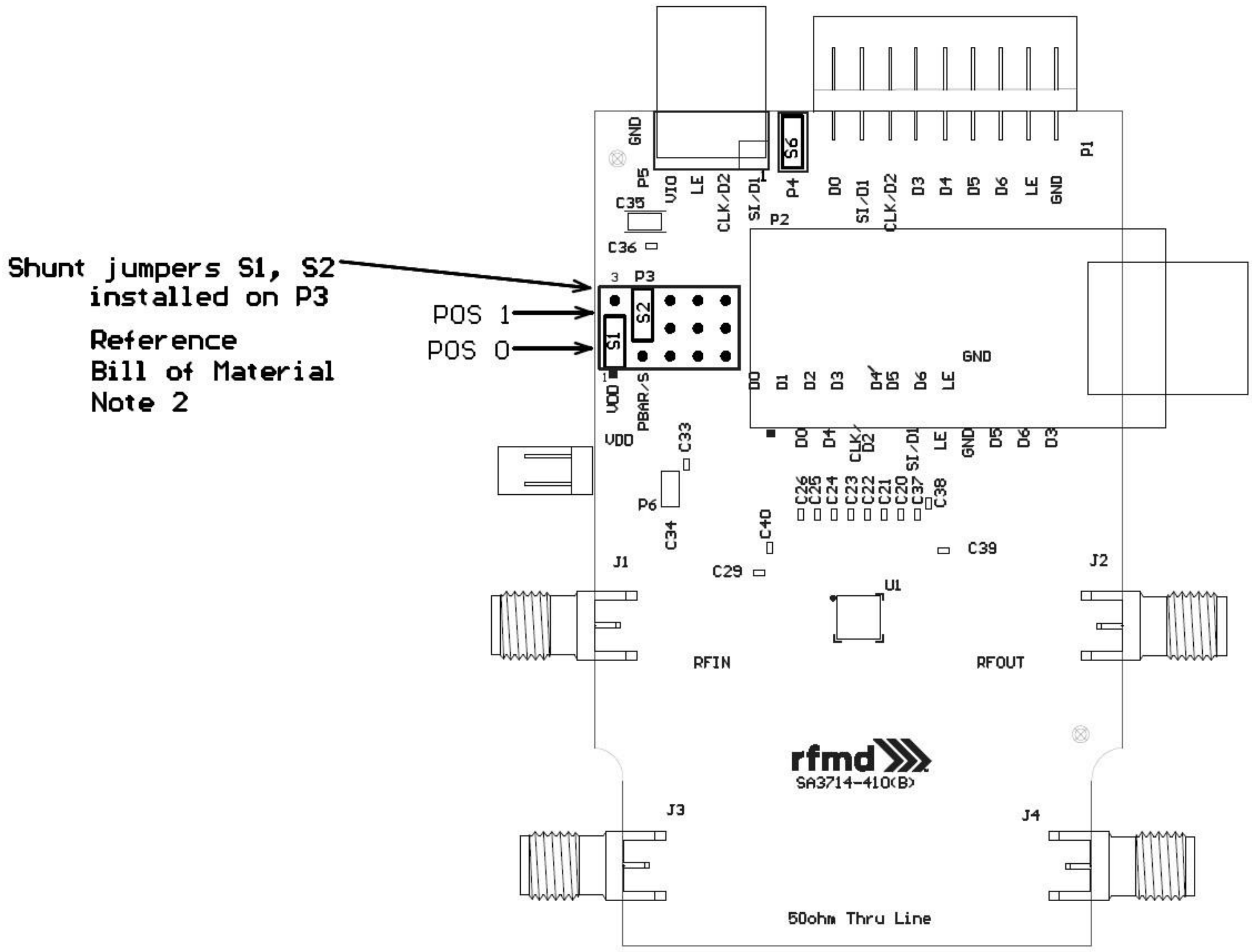


Evaluation Board Bill of Materials (BOM) 50MHz to 6000MHz Application Circuit

Description	Reference Designator	Manufacturer	Manufacturer's P/N
SA3714-410		Dynamic Details (DDI) Toronto	SA3714-410(B)
Digital Step Attenuator 50MHz to 6000MHz	U1	RFMD	RFSA3714SB
CAP, 1µF, 10%, 25V, X7R, 1206	C34	Taiyo Yuden (USA), Inc.	CE TMK316BJ105KL-T
CONN, SMA, END LNCH, UNIV, HYB MNT	J1-J4	Molex	SD-7351-4000
CONN, HDR, ST, 9-PIN, 0.100”	P1	Samtec Inc.	TSW-109-07-G-S
CONN, SKT, 24-PIN DIP, 0.600”, T/H	P2	Aries Electronics Inc.	24-6518-10
MOD, USB TO SERIAL UART, SSOP-28	M1 (See Note 1)	Future Technology Devices Int’l	UM232R
CONN, HDR, ST, 3 x 5, 0.100”, T/H	P3 (See Note 2)	Samtec Inc.	TSW-105-07-L-T
CONN, HDR, ST, 2-PIN, 0.100:	P4	Samtec Inc.	TSW-102-07-G-S
CONN, HDR, 2 x 4, RA, 0.100, T/H	P5	Samtec Inc.	TSW-104-08-G-D-RA
CONN, HDR, ST, PLRZD, 2-PIN, 0.100”	P6	ITW Pancon	MPSS100-2-C
CAP, 470pF, 5%, 50V, C0G, 0402	C40	Murata Electronics	GRM1555C1H471JA01D
Jumper, 2-Pin	S1-S2 (See Note 2)	3M Interconnect Solutions	929950-00
DNP	C20-C26, C29, C33, C35-C39, S6	N/A	N/A

Notes:
1. M1 should be mounted into P2 with respect to the Pin 1 alignment of M1 and P2.
2. Jumpers S1 and S2 should be installed on P3.

Evaluation Board Assembly Drawing



Evaluation Board Jumper Programming

Jumpers	Connector	Signal	Position	U1 Connection	Comment
S1	P3	Logic Voltage	**0**	VDD (From P6)	
			1	VIO (From P5)	
S2		PBar/S	0	GND	Parallel Mode
			1	U1_VDD	Serial Mode
S6	P4	LE	**OPEN**	LE	All Other Modes
			INSTALLED	LE (From P5 Pin 3)	Serial Mode Using P5

Note: Default jumper settings are **BOLD**.

Evaluation Board Programming Using USB Interface

Serial Mode

All programming jumpers on the evaluation board are set to the default values indicated in the table. Refer to the Control Bit Generator (CBG) Software Reference Manual for detailed instructions on how to setup the software for use. Apply the supply voltage to P6. Select 'RFSA3714' from the RFMD parts list of the CBG user interface. Set the attenuation value using the CBG user interface. The attenuator is set to the desired state and measurement can be taken.

Latched Parallel Mode

Evaluation board programming jumper S2 is set to '0'. All other programming jumpers are not required and can be set to any position. Refer to the Control Bit Generator Software Reference Manual for detailed instructions on how to set up the software for use. Apply the supply voltage to P6. Select 'RFSA3714-P' from the RFMD part list of the CBG user interface. Set the attenuation value using the CBG user interface. The attenuator is set to the desired state and measurements can be taken.

Evaluation Board Programming Using External Bus

Serial Mode

The configuration allows the user to control the attenuator through the P5 connector using an external harness. Remove the USB interface board if it is currently installed on the evaluation board. Connect a user-supplied harness to the P5 connector. Note that the top row of P5 contains the serial bus signals and the bottom row is ground. Programming jumper S1 is set to '0' and S2 is set to '1'. Jumper S6 is installed and allows the LE signal to be routed from the P5 connector to the attenuator. Apply the supply voltage P6. Send the appropriate signals onto the serial bus lines in accordance with the Serial Mode Timing Diagram. The attenuator is set to the desired state and measurements can be taken.

Latched Parallel Mode

This configuration allows the user to control the attenuator through the P1 connector using an external harness. Remove the USB interface it if is currently installed on the evaluation board. Connect a user-supplied harness to the P1 connector. The parallel bus signal names for P1 are indicated on the evaluation board. Programming jumper S2 is set to ‘0’ to select parallel mode. All other programming jumpers are not required and can be set to any position. Apply the supply voltage to P6. Send the appropriate signals onto the parallel bus lines in accordance with the Latched Parallel Mode Timing Diagram. The attenuator is set to the desired state and measurements can be taken.

Direct Parallel Mode

This configuration allows the user to control the attenuator through the P1 connector using an external harness. When using this mode the LE signal is held at logic high so that the attenuation will change immediately when there is a change in logic state for any of the parallel bus signals. Remove the USB interface if it is currently installed on the evaluation board. Connect a user-supplied harness to the P1 connector. The parallel bus signal names for P1 are indicated on the evaluation board. Programming jumper S2 is set to ‘0’ to select parallel mode. All other programming jumpers are not required and can be set to any position. Apply the supply voltage to P6. Send the appropriate signals onto the parallel bus lines. The attenuator is set to the desired state and measurements can be taken.

Default Power-up State

The default attenuation state is maximum (31.75dB) when supply voltage is applied to the attenuator in both serial and parallel modes. If a different attenuation state is desired during power up, this can be accomplished by applying signals according to the Parallel Mode Truth Table. The attenuator will power up to the state applied to the parallel bus during turn on. The LE signal must be held to logic ‘0’ during power up.

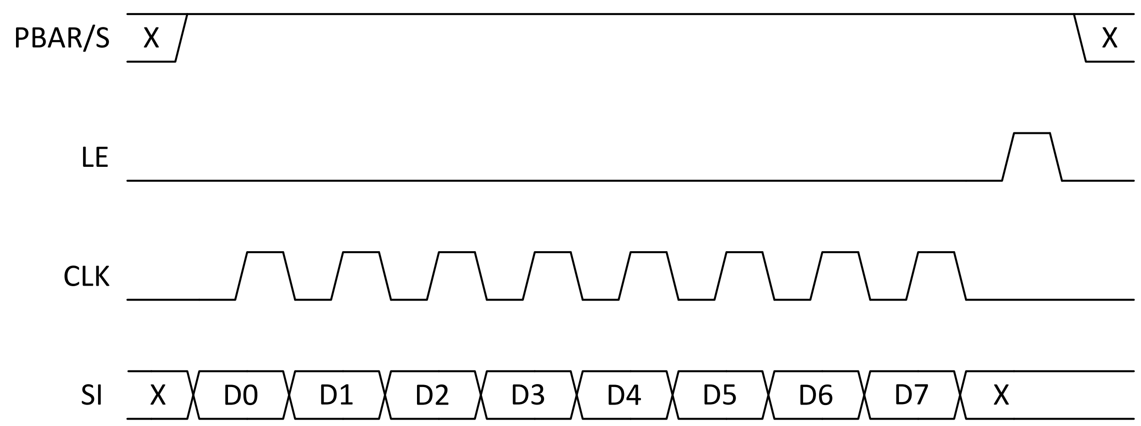
Pin Names and Descriptions

Pin	Name	Description
1	C0.25	0.25dB Parallel Control Bit
2	VDD	Supply Voltage
3	PBAR/S	Mode Select Pin Logic Low = Parallel Logic High = Serial
4	GND	Ground Pin
5	RFIN	RF Input Pin, Incident RF power must enter this pin for rated thermal performance and reliability. Do not apply DC power to this pin. Pin may be DC grounded externally and is grounded thru resistors internal to the part.
6	GND	Ground Pin
7	GND	Ground Pin
8	GND	Ground Pin
9	GND	Ground Pin
10	GND	Ground Pin
11	GND	Ground Pin
12	GND	Ground Pin
13	GND	Ground Pin
14	RFOUT	RF Output Pin; Do not apply DC power to this pin. Pin may be DC grounded externally and is grounded thru resistors internal to the part.
15	GND	Ground Pin
16	LE	Latch Enable, The leading edge of signal on LE causes the attenuator to change setting for serial and latched parallel modes. For direct parallel mode keep LE at a logic high level.
17	CLK	Serial Clock Input
18	SI	Serial Data Input
19	C16	16dB Parallel Control Bit
20	C8	8dB Parallel Control Bit
21	C4	4dB Parallel Control Bit
22	C2	2dB Parallel Control Bit
23	C1	1dB Parallel Control Bit
24	C0.5	0.5dB Parallel Control Bit

Serial Mode Attenuation Word Truth Table

Attenuation Word								Attenuation State
D7	D6	D5	D4	D3	D2	D1	D0 (LSB)	
X	L	L	L	L	L	L	L	0dB / Reference Insertion Loss
X	L	L	L	L	L	L	H	0.25dB
X	L	L	L	L	L	H	L	0.5dB
X	L	L	L	L	H	L	L	1dB
X	L	L	L	H	L	L	L	2dB
X	L	L	H	L	L	L	L	4dB
X	L	H	L	L	L	L	L	8dB
X	H	L	L	L	L	L	L	16dB
X	H	H	H	H	H	H	H	31.75dB

Serial Mode Timing Diagram

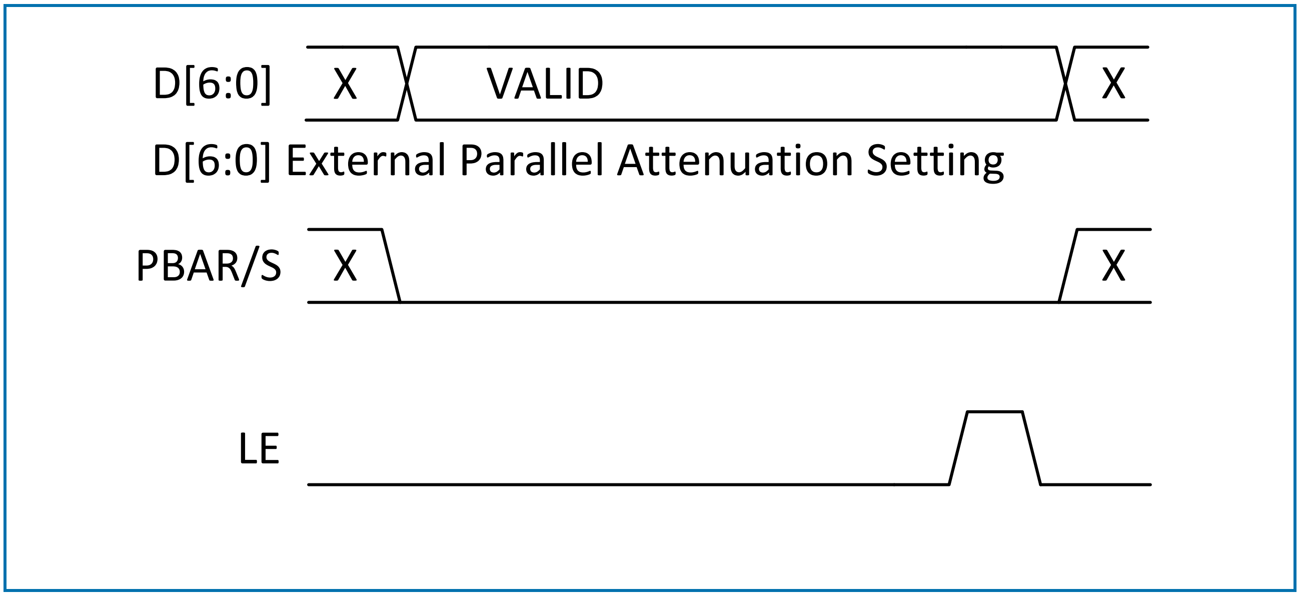


Note: Bit D7 is not used and can be set to logic high or low

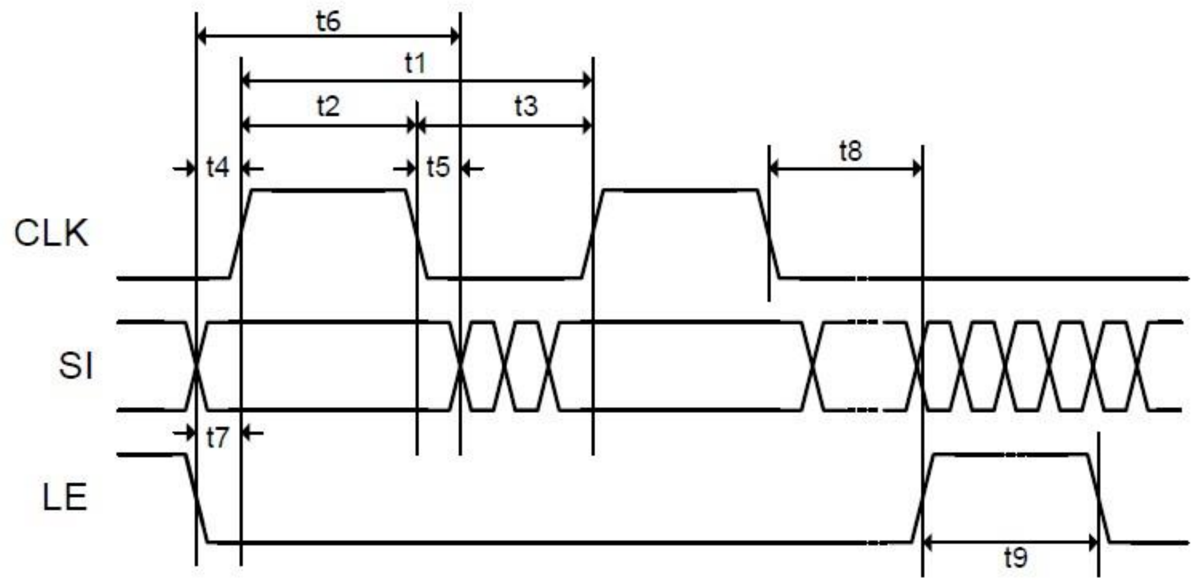
Parallel Mode Truth Table

Parallel Input Control Setting							Attenuation State
D6 (C16)	D5 (C8)	D4 (C4)	D3 (C2)	D2 (C1)	D1 (C0.5)	D0 (C0.25)	
L	L	L	L	L	L	L	0dB / Reference Insertion Loss
L	L	L	L	L	L	H	0.25dB
L	L	L	L	L	H	L	0.5dB
L	L	L	L	H	L	L	1dB
L	L	L	H	L	L	L	2dB
L	L	H	L	L	L	L	4dB
L	H	L	L	L	L	L	8dB
H	L	L	L	L	L	L	16dB
H	H	H	H	H	H	H	31.75dB

Latched Parallel Mode Timing Diagram

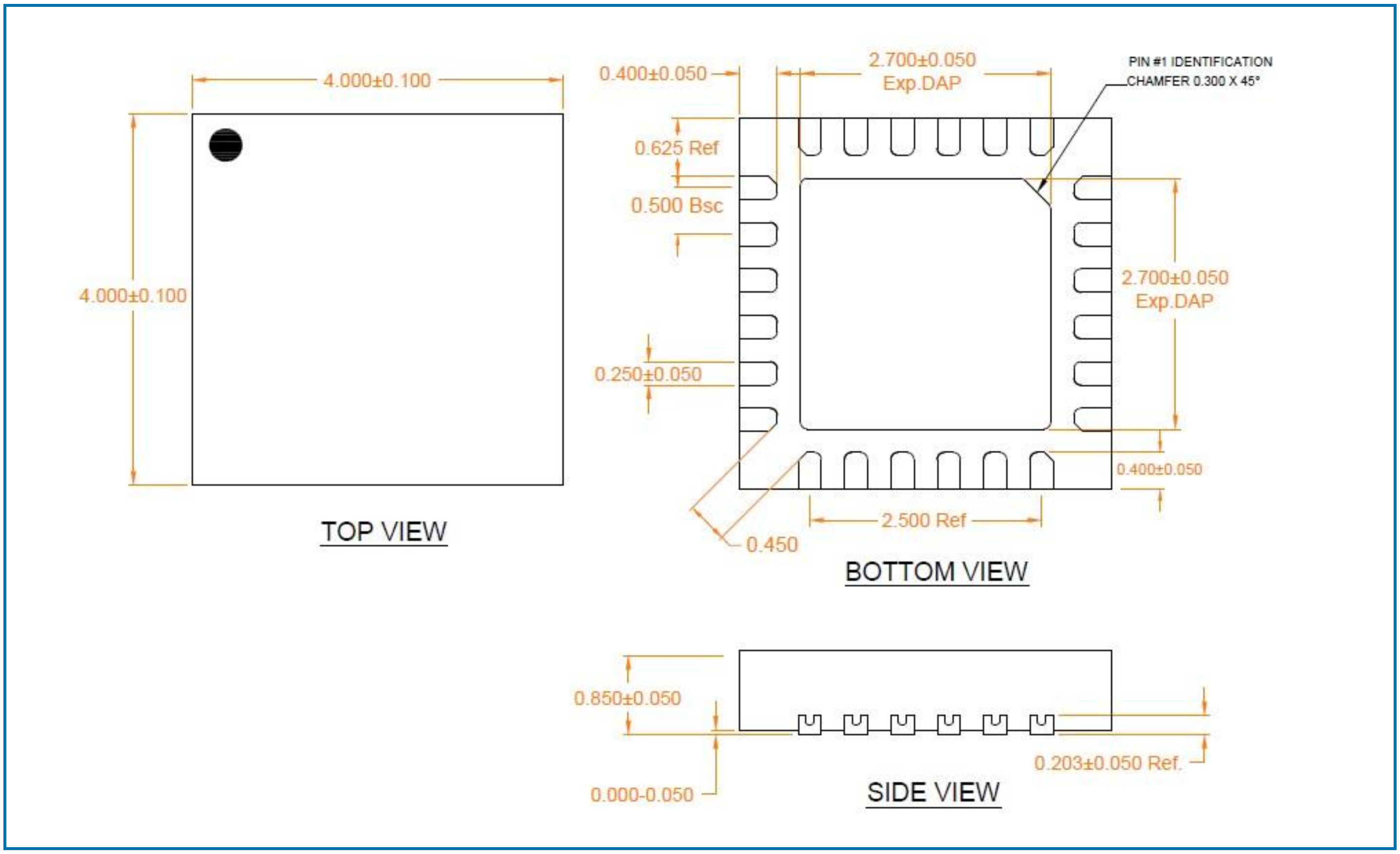


Serial Bus Timing Specifications

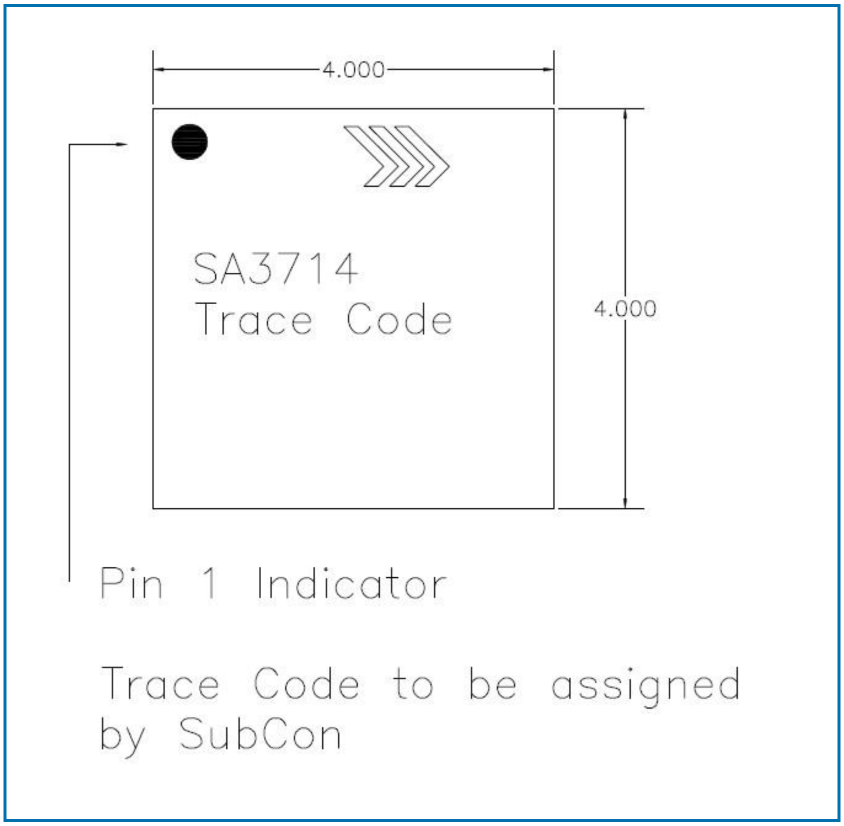


Parameter	Limit	Unit	Comment
t1	25	MHz max	CLK Frequency
t2	20	ns min	CLK High
t3	20	ns min	CLK Low
t4	5	ns min	SI to CLK Setup Time
t5	5	ns min	SI to CLK Hold Time
t6	30	ns min	SI Valid
t7	5	ns min	LE to CLK Setup Time
t8	5	ns min	CLK to LE Setup Time
t9	10	ns min	LE Pulse Width

Package Outline Drawing (Dimensions in millimeters)



Branding Diagram



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