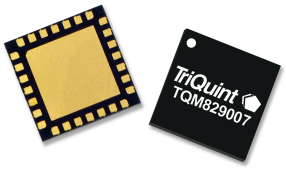
TQM829007

0.6-1.0 GHz ¼ W Digital Variable Gain Amplifier

Applications

- 3G / 4G Wireless Infrastructure
- CDMA, WCDMA, LTE
- Repeaters
- ISM Infrastructure

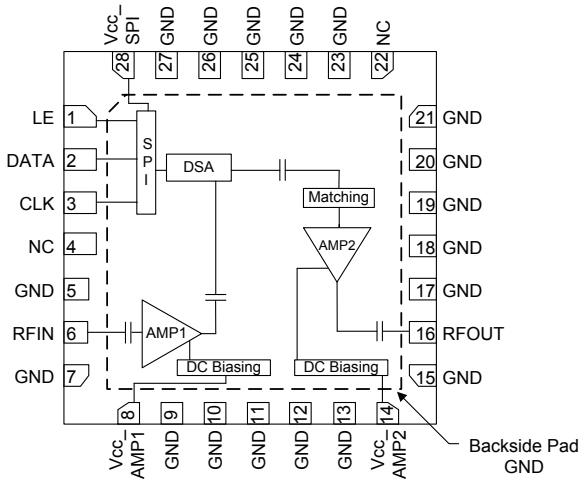


28-pin 6x6 mm leadless SMT package

Product Features

- 0.6-1.0 GHz Frequency Range
- 31.5 dB Maximum Gain at 0.9 GHz
- 31.5 dB Gain Range in 0.5 dB Steps
- +40 dBm Output IP3
- +24.3 dBm Output P1dB
- 2.1 dB Noise Figure at Max. Gain State
- Fully Internally Matched Module
- Integrated Blocking Capacitors, Bias Inductors
- 3-wire SPI Control Programming

Functional Block Diagram



General Description

The TQM829007 is a digital variable gain amplifier (DVGA) featuring high linearity performance in a fully integrated module. The amplifier module features the integration of a low noise amplifier gain block, a digital-step attenuator (DSA), along with a high linearity ¼W amplifier. The module has the added features of integrating all matching components with bias chokes and blocking capacitors. The internal DSA offers 0.5 dB step, 6-bit, and 31.5 dB range and is controlled with a serial periphery interface (SPI™).

The TQM829007 features variable gain from 0 to 31.5 dB at 0.9 GHz, has +40 dBm Output IP3, and +24.3 dBm P1dB. The amplifier also has a very low 2.1 dB Noise Figure (at maximum gain) allowing it to be an ideal DVGA for both receiver and transmitter applications. The amplifier operates from a single +5V supply and is available in a compact 28-pin 6x6 mm leadless SMT package.

The TQM829007 is pin compatible with the TQM879006 (1.4-2.7GHz, 0.25W DVGA) and TQM879008 (1.5-2.7 GHz, 0.5W DVGA). This allows one to size the right type of device for specific system level requirements as well as making the DVGA family ideal for applications where a common PCB layout is used for different frequency bands.

Pin Configuration

Pin No.	Label
1	LE
2	DATA
3	CLK
4, 22	NC
6	RFIN
8	VCC_AMP1
14	VCC_AMP2
16	RFOUT
28	VCC_SPI
5, 7, 9-13, 15,17-21, 23-27	GND
Backside Pad	GND

Ordering Information

Part No.	Description
TQM829007	0.6-1.0 GHz Digital VGA
TQM829007-PCB	Fully Assembled Evaluation Board Includes USB control board, EVH

Standard T/R size = 2500 pieces on a 13” reel.

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−55 to +150°C
RF Input Power, 50Ω,T = 25°C	+12 dBm
V_{DD}, Power Supply Voltage	+5.5 V
Digital Input Voltage	V_{CC}+0.5V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{CC} (pins 8, 14, 28)	+4.75	+5.0	+5.25	V
Case Temperature	−40		+85	°C
Tj (for>10^6 hours MTTF)			170	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions: V_{CC}=+5 V, Temp= +25°C, 50Ω system, Maximum Gain State

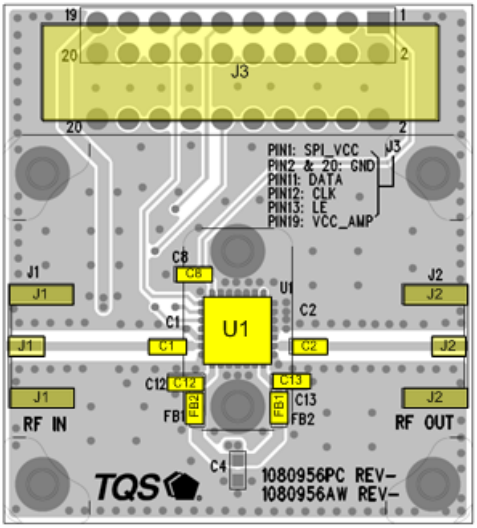
Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		600		1000	MHz
Test Frequency			900		
Gain		28.5	31.7		dB
Gain Control Range	0.5 dB Step Size		31.5		dB
Attenuation Accuracy	3 wire SPI, 6 states	± (0.5 + 3% of Atten. Setting) Max			dB
Control Interface	3-wire SPI		6		Bit
Input Return Loss			16		dB
Output Return Loss			22		dB
Output P1dB			+24.3		dBm
Output IP3	Pout =+11 dBm/tone, Δf=1MHz	+36.5	+40		dBm
Noise Figure			2.1		dB
I/O Impedance			50		Ω
Supply Voltage			+5		V
Supply Current		130	174	215	mA
Thermal Resistance, θ_{jc}	Module (junction to case)			36.7	°C/W

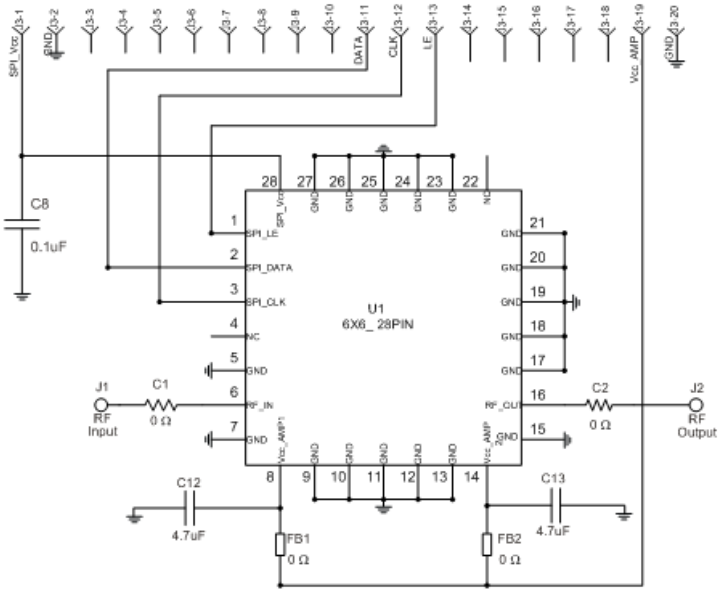
Chain Analysis Table

Test conditions: V_{CC}=+5 V, Temp= +25°C, 50Ω system, Maximum Gain State, Freq.=900 MHz

Parameter	AMP1	DSA	AMP2	Overall Performance
Gain (dB)	14.5	-1.2	18.4	31.7
NF (dB)	2.0	1.2	2.1	2.1
OIP3 (dBm)	40.6	56	39.5	39.5
P1dB (dBm)	21.4	28.8	24.3	24.3
Icc (mA)	85	2.0	87	174

TQM829007-PCB Evaluation Board





Notes:

1. For PCB Board Layout, see page 9 for more information.
2. All Components are of 0603 size unless stated otherwise.
3. For SPI Timing Diagram, see page 6.
4. 0 Ω jumpers may be replaced with copper traces in the target application layout.
5. Different ground pins are used for SPI (digital) and analog supply voltages.
6. The primary RF microstrip characteristic line impedance is 50 Ω.
7. The single power supply is used to provide supply voltage to AMP1 and AMP2

Bill of Material –TQM829007-PCB

Reference Des.	Value	Description	Manufacturer	Part Number
U1		0.6 – 1.0 GHz ¼ W DVGA	TriQuint	TQM829007
C8	0.1 uF	Cap, Chip, 0603, 16V, X7R, 10%	various	
C12, C13	4.7 uF	Cap, Chip, 0603, 6.3V, X5R, 20%	various	
C1, C2, FB1, FB2	0 Ω	Res, Chip, 0603, 1/16W, 5%	various	
C4	Do Not Place			

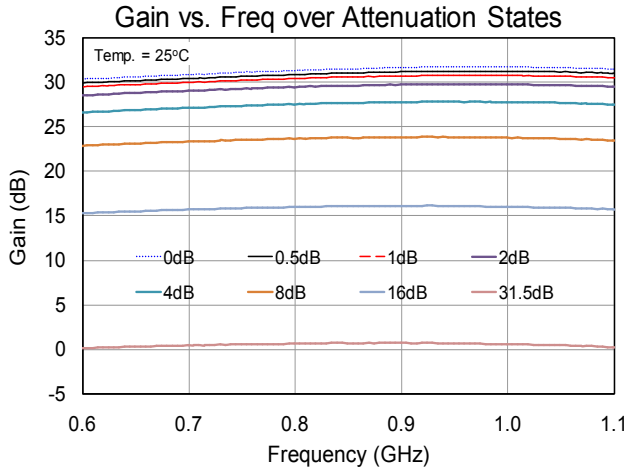
Typical Performance – TQM829007-PCB

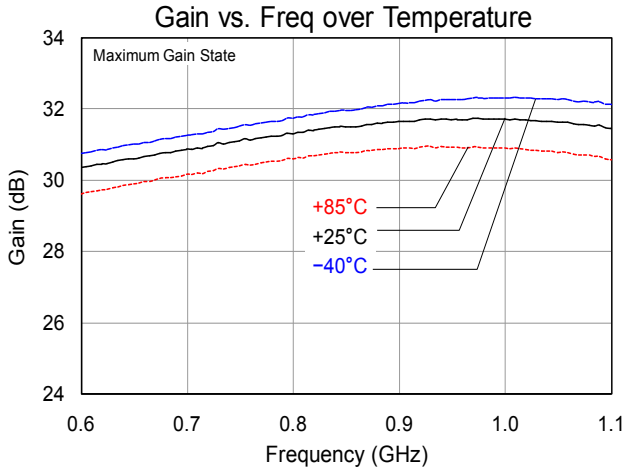
Test conditions unless otherwise noted: V_{CC}=+5 V, I_{CC}=174 mA (Typ.), Temp=25°C, 50 Ω system, Maximum Gain State

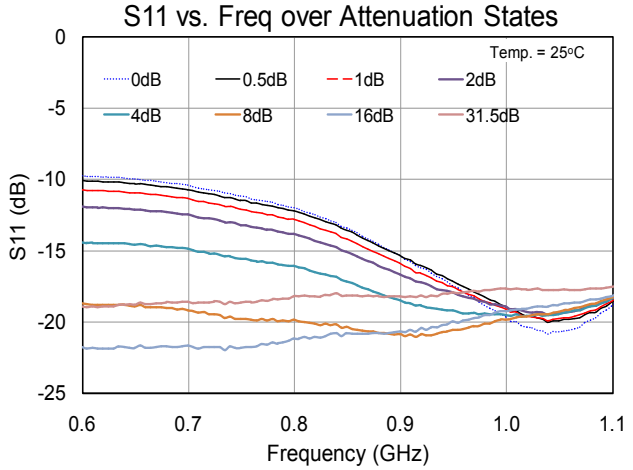
Parameter	Typical Value					Units
Frequency	0.6	0.7	0.8	0.9	1.0	GHz
Gain	30.5	31	31.5	31.7	31.6	dB
Input Return Loss	10	10.5	12	16	20	dB
Output Return Loss	8	10	14	22	18	dB
Output P1dB	+24.6	+24.5	+24.3	+24.3	+24.4	dBm
Output IP3 @ Pout=+11 dBm/tone, Δf =1 MHz	+40	+39.5	+39.3	+39.5	+38.7	dBm
Noise Figure	2.2	2.2	2.0	2.1	2.1	dB

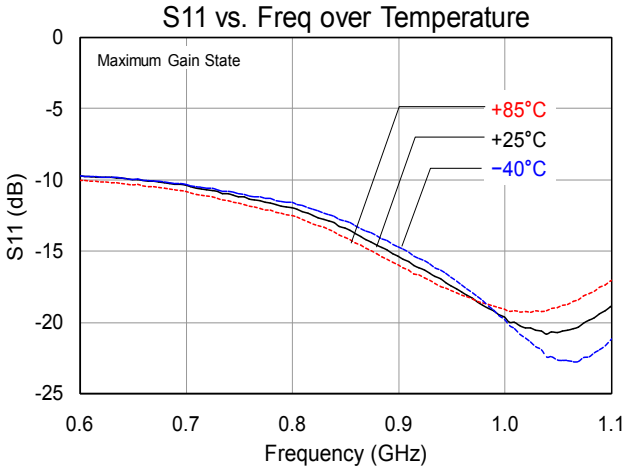
Typical Performance Plots – TQM829007-PCB

Test conditions: V_{CC}=+5 V, Temp= +25°C, 50Ω system



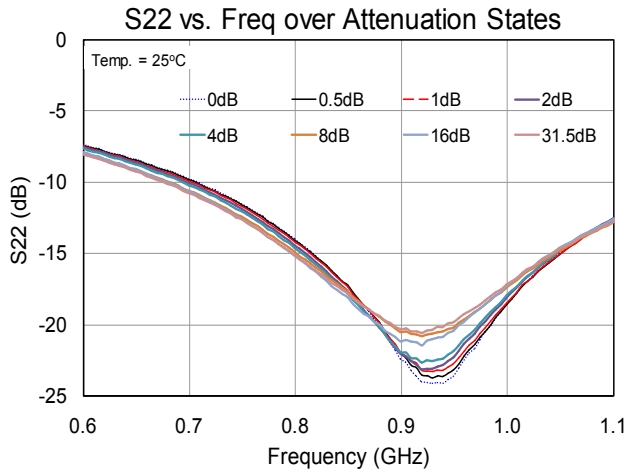


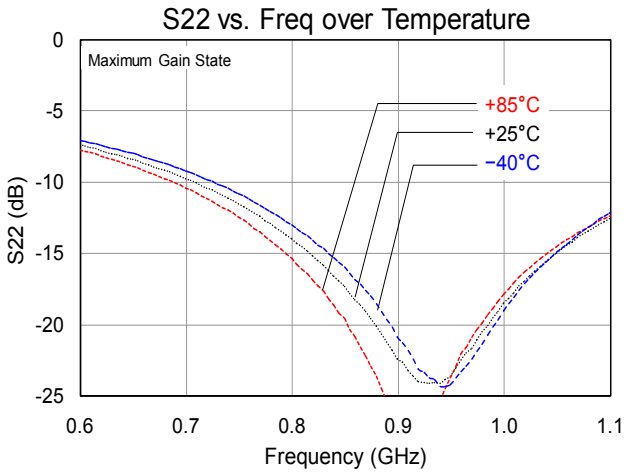


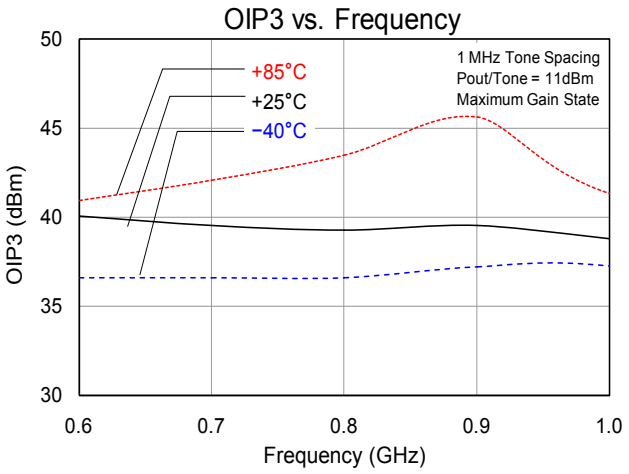


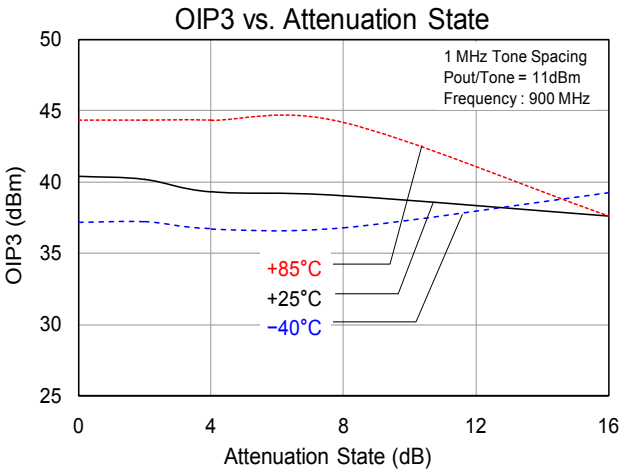
Typical Performance Plots – TQM829007-PCB

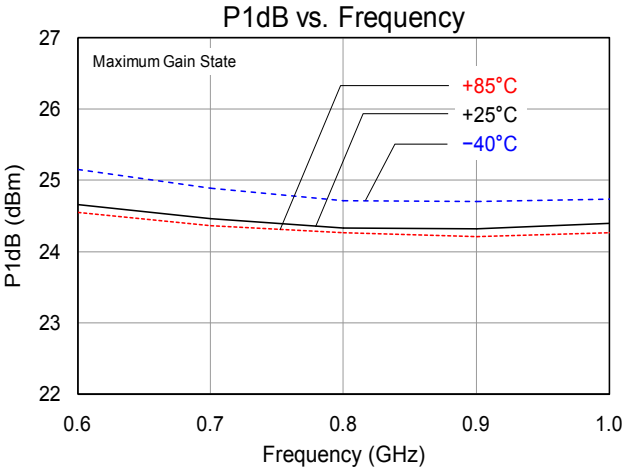
Test conditions: V_{CC}=+5 V, Temp= +25°C, 50Ω system

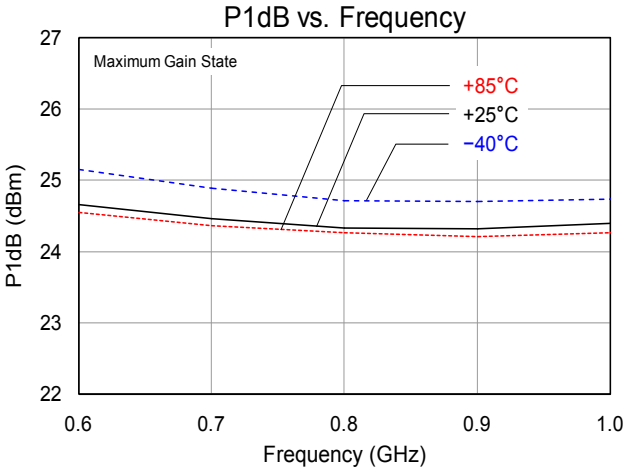












Serial Control Interface

The TQM829007 has a CMOS SPI™ input compatible serial interface. This serial control interface converts the serial data input stream to parallel output word. The input is 3-wire (CLK, LE and SID) SPI™ input compatible. At power up, the serial control interface resets the DSA to the minimum gain state. The 6-bit SID (Serial Input Data) word is loaded into the register on rising edge of the CLK, MSB first. When LE is high, CLK is internally disabled.

Serial Control Timing Characteristics (Test conditions: V_{CC} = +5 V, Temp.=25°C)

Parameter	Condition	Min	Max	Units
Clock Frequency	50% Duty Cycle		10	MHz
LE Setup Time, t_{LESUP}	after last CLK rising edge	10		ns
LE Pulse Width, t_{LEPW}		30		ns
SERIN set-up time, t_{SDSUP}	before CLK rising edge	10		ns
SERIN hold-time, t_{SDHLD}	after CLK rising edge	10		ns
LE Pulse Spacing t_{LE}	LE to LE pulse spacing	630		ns
Propagation Delay t_{PLO}	LE to Parallel output valid		30	ns

Serial Control DC Logic Characteristics (Test conditions: V_{CC} = +5 V, Temp.=25°C)

Parameter	Condition	Min	Max	Units
Input Low State Voltage, V_{IL}		0	0.8	V
Input High State Voltage, V_{IH}		2.4	V_{CC}	V
Input Current, I_{IH} / I_{IL}	On SID, LE and CLK pins	−10	+10	µA

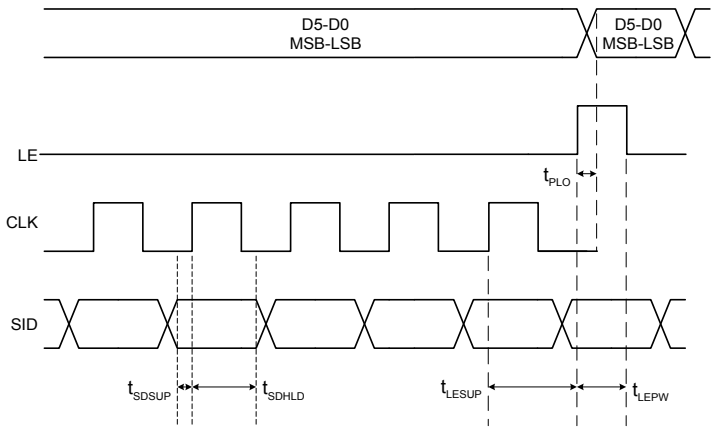
SERIN Control Logic Truth Table

6-Bit Control Word						Attenuation State
MSB					LSB	
D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	Reference : IL
1	1	1	1	1	0	0.5 dB
1	1	1	1	0	1	1 dB
1	1	1	0	1	1	2 dB
1	1	0	1	1	1	4 dB
1	0	1	1	1	1	8 dB
0	1	1	1	1	1	16 dB
0	0	0	0	0	0	31.5 dB

Any combination of the possible 64 states will provide an attenuation of approximately the sum of bits selected

Timing Diagram

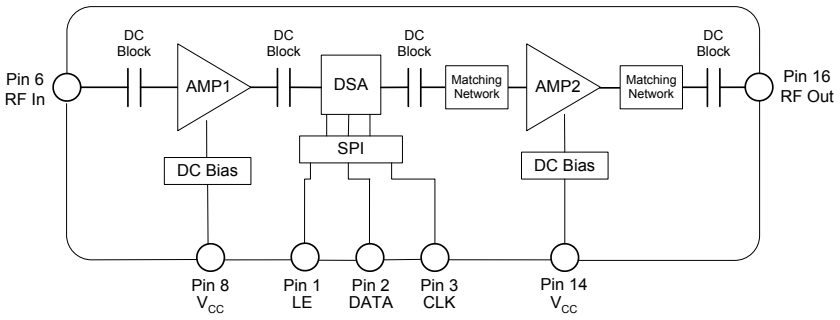
CLK is internally disabled when LE is high



Detailed Device Description

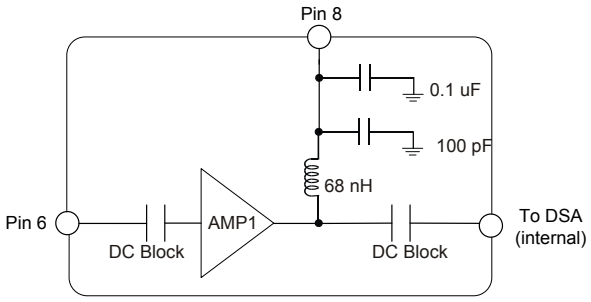
The TQM829007 is a 50 Ω internally matched digital variable gain amplifier (DVGA) featuring high linearity over the entire gain control range. The amplifier module features the integration of a low noise amplifier gain block, a digital-step attenuator, along with a high linearity ¼W amplifier as shown in the functional diagram below. The module is unconditionally stable. Internal blocking capacitors and bias structures keep external parts count to a minimum. The DVGA has an operational frequency range from 0.6 – 1.0 GHz.

Functional Block Diagram



AMP1

AMP1 is a wide band low noise amplifier gain block in DVGA module. The amplifier provides 14.5 dB gain, 2.0 dB noise figure, +40.6 dBm OIP3 at 0.9 GHz while only drawing 85 mA current. External DC blocks and biasing is not required. AMP1 is DC blocked internally and is connected internally to two bypass capacitors (100 pF, 0.1 uF) followed by 68 nH inductor inside the module as shown in the figure below.

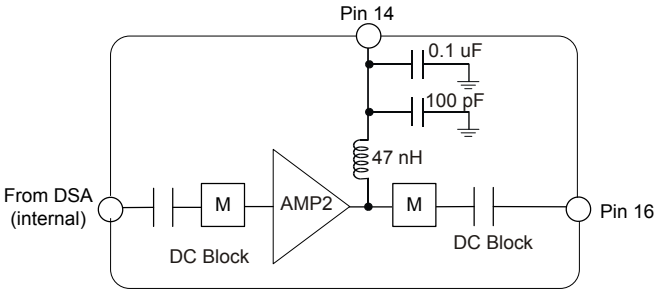


DSA (Digital Step Attenuator)

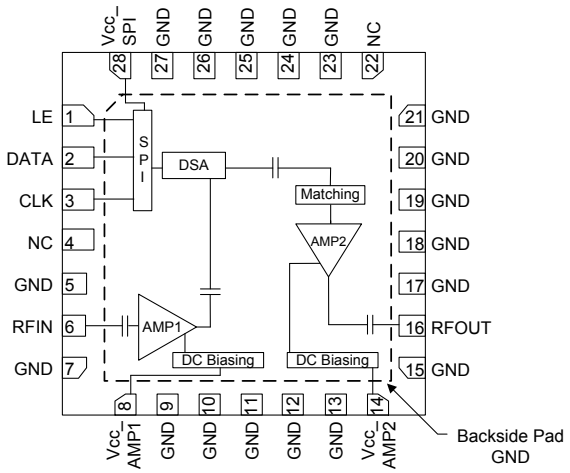
DVGA has a serial digital step attenuator that is controlled with 6-bit serial periphery interface (SPI™) and has 0.5 dB step size with 31.5 dB attenuation range. This 50-ohm RF DSA maintains high attenuation accuracy over frequency and temperature. "000000" represents maximum attenuation state. External bypass capacitors are needed to compensate the inductance effect associated with long transmission lines on the evaluation board.

AMP2

AMP2 is high linearity ¼-W amplifier in DVGA module. The amplifier provides 18.4 dB gain, +24.3 dBm P1dB, +39.5 dBm OIP3 at 0.9 GHz while only drawing 87 mA current. The amplifier is tuned over 0.6 – 1.0 GHz bandwidth using internal matching components. AMP2 is DC blocked internally and is connected internally to two bypass capacitors (100 pF, 0.1 uF) followed by a 47 nH inductor inside the module as shown in the figure below. External DC blocks and biasing are not required.



Pin Configuration and Description



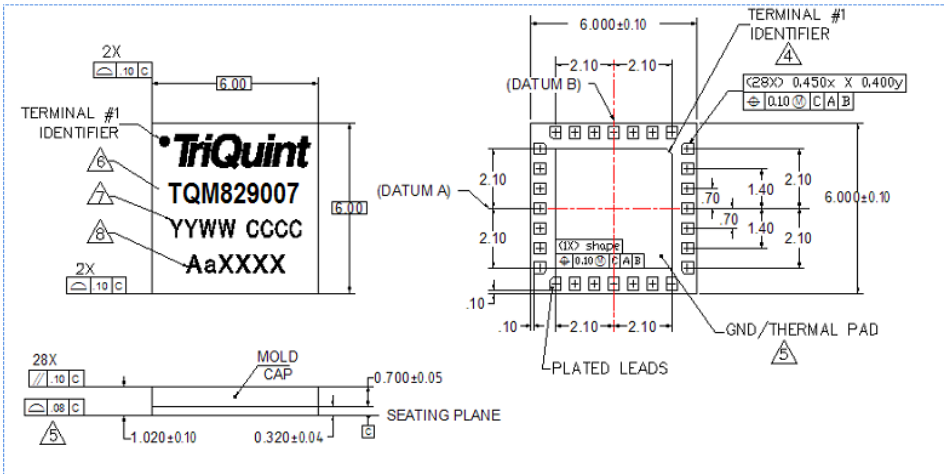
Pin No.	Label	Description
1	LE	Serial Latch Enable Input. When LE is high, latch is clear and content of SPI control the attenuator. When LE is low, data in SPI is latched.
2	DATA	Serial data input. The data and clock pins allow the data to be entered serially into SPI and is independent of Latch state.
3	CLK	Serial clock input.
4, 22	N/C	No connect or open. This pin is not connected in this module
6	RFIN	Input, matched to 50 ohms. Internally DC blocked.
8	VCC_AMP1	Supply Voltage to AMP1. This pin is connected internally to 2 bypass capacitors (100 pF, 0.1 uF) followed by a 68 nH inductor inside the module.
14	VCC_AMP2	Supply Voltage to AMP2. This pin is connected internally to 2 bypass capacitors (100 pF, 0.1 uF) followed by a 47 nH inductor inside the module.
16	RFOUT	Output matched to 50 ohms. Internally DC blocked.
28	VCC_SPI	SPI and DSA DC supply. Internal connection to 0.1 uF bypass capacitor.
5, 7, 9-13, 15,17-21, 23-27	GND	RF/DC Ground Connection
Backside Pad	GND	RF/DC Ground Connection

Evaluation Board PCB Information

TriQuint PCB 1080956 Material and Stack-up

Package Marking and Dimensions

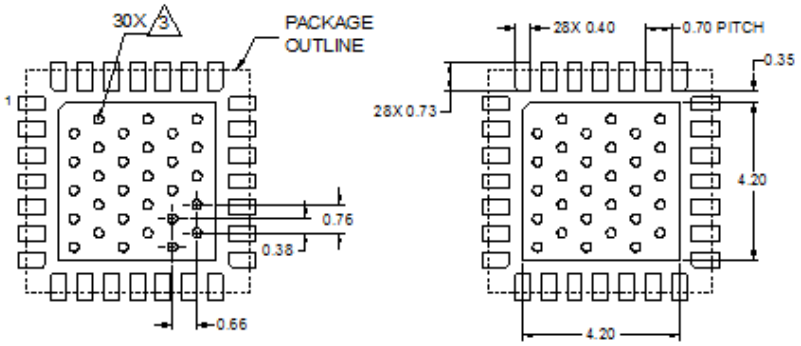
Marking: Part number – TQM829007
Year/week code – YYWW CCCC
Assembly code– AaXXXX



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
5. Co-planarity applies to the exposed ground/thermal pad as well as the contact pins.
6. Package body length/width does not include plastic flash protrusion across mold parting line.

PCB Mounting Pattern



COMPONENT SIDE

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating:	Class 1C
Value:	Passes ≥ 1000 V to < 2000 V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JS-001-2012

ESD Rating:	Class C3
Value:	Passes ≥ 1000 V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101F

MSL Rating

MSL Rating:	Level 3
Test:	+260 °C convection reflow
Standard:	JEDEC standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260 °C max. reflow temp.) and tin/lead (245 °C max. reflow temp.) soldering processes.

Package lead plating: electrolytic plated Au over Ni

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

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