RF1141A

Low Loss SPDT Switch 400MHz to 3.0GHz

The RF1141A is a low loss SPDT optimized for use in multi-band cellular antenna tuning applications. It offers low on-state resistance and high RF port-to-port isolation in a small package. RF ports 1 and 2 are left 'open' in the off-state for optimal tuning performance and circuit placement. RF1141A provides rugged power handling and simple one-bit GPIO control. The enable pin can also configure a third "all-off state" as well as low power mode.

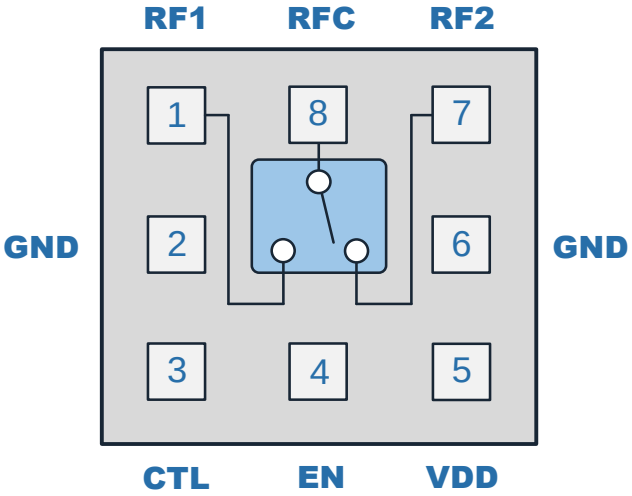

Figure 1. Functional Schematic

Package: Laminate Module, 9-pin, 1.67mm x 1.47mm x 0.59mm

Features

- 400MHz to 3.0GHz Operation
- Low On-state Insertion Loss & Resistance
- High Isolation All-off State (RF1,RF2)
- Symmetric SPDT
- Linear IIP3: > 75dBm Typ
- Rugged Power & Peak Voltage Handling
- Wide Supply Range: 2.4 – 5.8V
- HBM ESD Protection: 2kV

Applications

- Antenna Tuning
- Band Switching
- Impedance Tuning

Ordering Information

RF1141ASR	100-pc 7" Reel
RF1141ASQ	25-pc Sample Bag
RF1141ASB	5-pc Sample Bag
RF1141ATR13-5K	5000-pc, 13" Tape and Reel
RF1141APCK-410	Fully Assembled EVB

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DS150911

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage, V_{DD}	+6.0	V
Control Voltage, V_{CTL}	+3.0	V
Enable Voltage, V_{EN}	+6.0	V
RF Input Power - 50Ω	42	dBm
Max differential RF voltage between two RF ports or any RF port to ground.	40	V_P
Operating Case Temperature	-30 to +85	°C
Storage Temperature	-55 to +150	°C
ESD All Pins, HBM, JESD22-A114	2,000	V

Caution! ESD sensitive device.

RFMD Green: RoHS status based on EU Directive 2011/65/EU (at time of this document revision), halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Nominal Operating Parameters

Parameter	Specification			Unit	Conditions
	Min	Typ	Max		
					Electrical Specifications: Temp = 25°C, 50Ω, Active Mode. V_{DD} = 2.85V, V_{EN} = 0/1.8V, V_{CTL} = 0/1.8V.
Operating Frequency	400	-	3000	MHz	
Supply Voltage V_{DD}	2.4	2.85	5.8	V	
Supply Current I_{DD}	-	75	90	µA	Active Mode
	-	2.5	5	µA	Low Power Mode, V_{EN} & V_{CTL} = 0V
EN Control Voltage High V_{HIGH_EN}	1.2	1.8	V_{DD}	V	EN pin
Control Voltage High V_{HIGH_CTL}	1.2	1.8	2.8	V	CTL pin
Control Voltage Low V_{LOW}	0	0	0.45	V	
Control Current I_{CTL}	-	-	5	µA	V_{CTL} = 1.8V
Enable Control Current I_{EN}	-	-	5	µA	V_{EN} = 1.8V

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Electrical Specifications – Linear Parameters

Parameter	Specification			Unit	Conditions
	Min	Typ	Max		
					Electrical Specifications: Temp = 25°C, 50Ω, Active Mode. V_{DD} = 2.85V, V_{EN} = 0/1.8V, V_{CTL} = 0/1.8V.
Insertion Loss (RFC to RF1/RF2) Logic States 1 & 2	-	0.20	0.35	dB	700 MHz
	-	0.20	0.40	dB	915 MHz
	-	0.30	0.50	dB	1910 MHz
	-	0.45	0.75	dB	2700 MHz
Isolation (RFC to RF1/RF2) Logic States 1 & 2	21	25	-	dB	700 MHz
	20	23	-	dB	915 MHz
	14	17	-	dB	1910 MHz
	11	14	-	dB	2700 MHz
Isolation (RFC to RF1/RF2) Logic State 3	16	20	-	dB	700 MHz
	14	18	-	dB	915 MHz
	9	12	-	dB	1910 MHz
	7	10	-	dB	2700 MHz
Isolation (RF1 to RF2) Logic State 3	40	45	-	dB	700 MHz
	35	40	-	dB	915 MHz
	25	29	-	dB	1910 MHz
	20	24	-	dB	2700 MHz
Return Loss (RFC) Logic States 1 & 2	25	30	-	dB	915 MHz
	15	20	-	dB	1910 MHz
R_{ON} (RFC to RF1/RF2) Logic States 1 & 2	-	1.05	1.4	Ω	
C_{OFF} (RFC to RF1/RF2) Logic State 1 & 2	-	0.240	0.290	pF	
Start-up time	-	8	10	µs	50% VDD to large signal fully compliant
ON and OFF Switching speed Between Logic States 1 and 2 Between Logic States 1 and 3 Between Logic States 2 and 1	-	3	5	µs	50% control to 90% RF ON
ON and OFF Switching speed Between Logic States 3 and 2	-	5	10	µs	50% control to 90% RF OFF

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Electrical Specifications – Nonlinear Parameters

Parameter	Specification			Unit	Conditions
	Min	Typ	Max		
					Electrical Specifications: Temp = 25°C, 50Ω, Active Mode. V_{DD} = 2.85V, V_{EN} = 0/1.8V, V_{CTL} = 0/1.8V.
Second Harmonics	-	-90	-80	dBm	704 MHz, Pin = 23 dBm
Third Harmonics	-	-100	-90	dBm	
Second Harmonics	-	-73	-60	dBm	915 MHz, Pin = 35 dBm
Third Harmonics	-	-67	-55	dBm	
Second Harmonics	-	-77	-65	dBm	1910 MHz, Pin = 33 dBm
Third Harmonics	-	-73	-60	dBm	
Second Harmonics	-	-93	-80	dBm	2570 MHz, Pin = 23 dBm
Third Harmonics	-	-100	-90	dBm	
IIP2, Low	110	120	-	dBm	Refer to IIP2 conditions table
IIP2, High	120	130	-	dBm	Refer to IIP2 conditions table
IIP3, Band I & Band II	-	81	-	dBm	Refer to IIP3 conditions table
IIP3, Band V and Band VIII	-	81	-	dBm	Refer to IIP3 conditions table
Receive Spurious 700 – 2700 MHz	-	-118	-113	dBm	No RF Signal
	-	-113	-108	dBm	RF – 915 MHz at 35dBm
	-	-113	-108	dBm	RF – 1910 MHz at 33dBm

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Control Logic

Logic State	MODE	EN	CTL	RFC-RF1	RFC-RF2
1	Active	V_{HIGH_EN}	V_{LOW}	ON	OFF
2	Active	V_{HIGH_EN}	V_{HIGH_CTL}	OFF	ON
3	Active	V_{LOW}	V_{HIGH_CTL}	OFF	OFF
4	Low Power	V_{LOW}	V_{LOW}	Low Power Mode, No RF Applied	

IIP2 Test Conditions

Band	In-band freq	CW tone 1		CW tone 2	
	[MHz]	[MHz]	[dBm]	[MHz]	[dBm]
Band I Low (IMT)	2140	1950	+20	190	-15
Band I High (IMT)	2140	1950	+26	4090	-20
Band II Low (PCS)	1960	1880	+20	80	-15
Band II High (PCS)	1960	1880	+26	3840	-20
Band V Low (Cell)	881.5	836.5	+20	45	-15
Band V High (Cell)	881.5	836.5	+26	1718	-20
Band VIII Low	942.5	897.5	+20	45	-15
Band VIII High	942.5	897.5	+26	1840	-20

IIP3 Test Conditions

Band	In-band freq	CW tone 1		CW tone 2	
	[MHz]	[MHz]	[dBm]	[MHz]	[dBm]
Band I High (IMT)	2140	1950	+20	1760	-15
Band II High (PCS)	1960	1880	+20	1800	-15
Band V High (Cell)	881.5	836.5	+20	791.5	-15
Band VIII High	942.5	897.5	+20	852.5	-15

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Pin Out

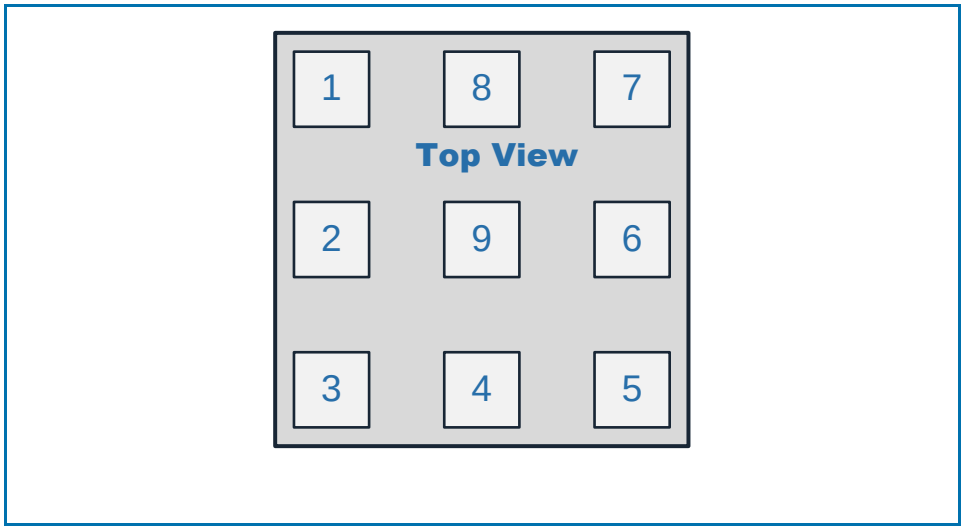

Figure 2. Pin Out Diagram

Pin Names and Descriptions

Pin	Name	Details
1	RF1	RF Port 1
2	GND	Ground
3	CTL	Control
4	EN	Enable
5	V_{DD}	Supply Voltage
6	GND	Ground
7	RF2	RF Port 2
8	RFC	RF Common Port
9	GND	Ground

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Evaluation Board Schematic

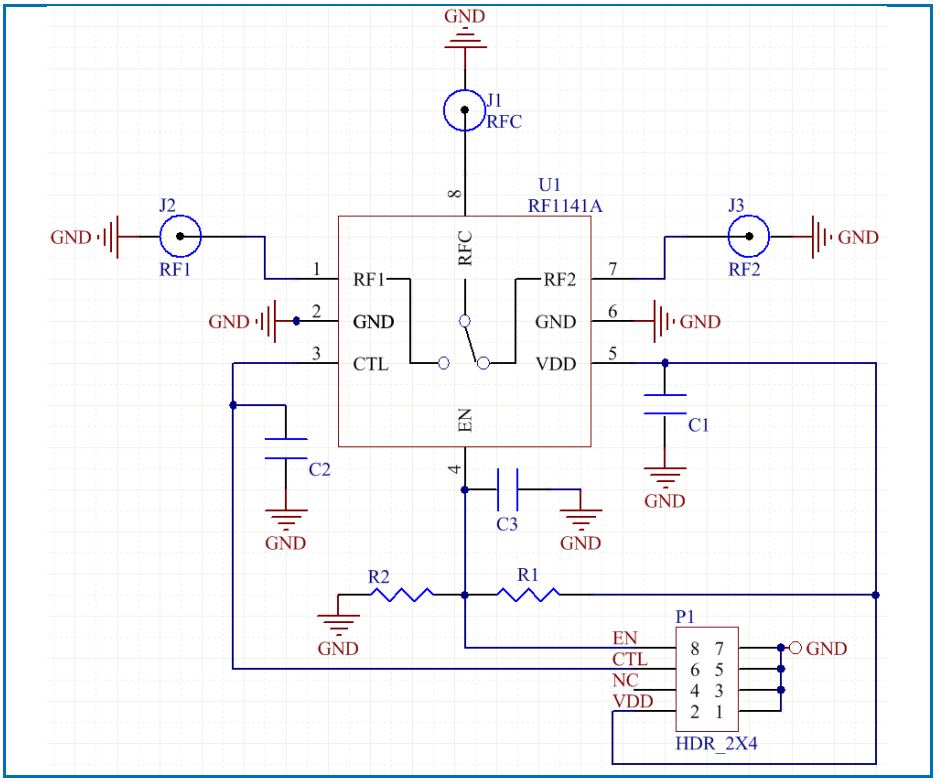

Figure 3. Evaluation Board Schematic

Parts List

Part Number	Part	Part Description
U1	RF1141A	RF1141A, SPDT Switch
J1, J2 & J3	SMA connector	Edge mount 0.068” SMA connector
C1	100 pF capacitor	(0402) 100 pF de-coupling capacitor
C2 & C3	NC	Do not populate (0402)
R1 & R2	NC	Do not populate (0402)
P1	2X4 RA header	2X4 right angled header with 0.1” spacing

Application Guidelines

Decoupling Capacitors = The decoupling capacitor on V_{DD} may be used for noise reduction. The value of the de-coupling capacitor should be selected based on the application.

DC Blocking Capacitors = DC blocking capacitor is not required on an RF port if no DC voltage exists on that port.

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Package Outline and Branding Drawing (Dimensions in millimeters)

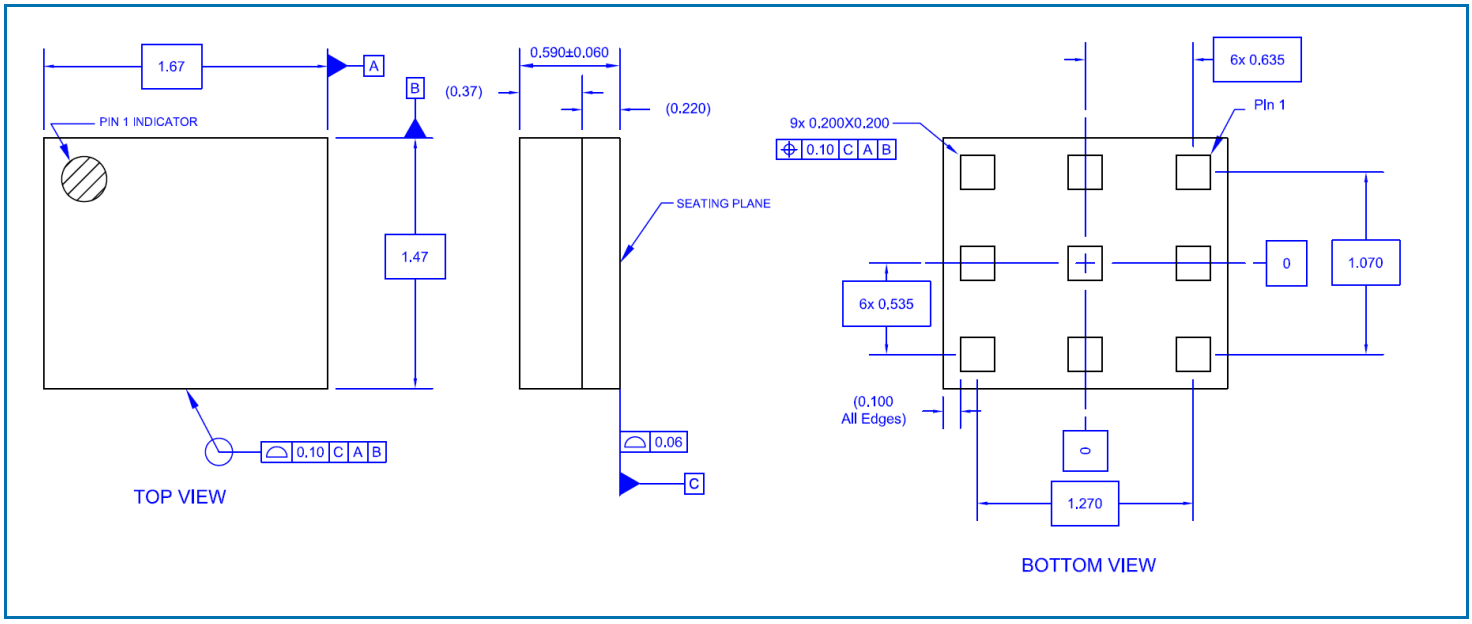

Figure 4. Package Outline and Branding Drawing

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Evaluation Board Layout

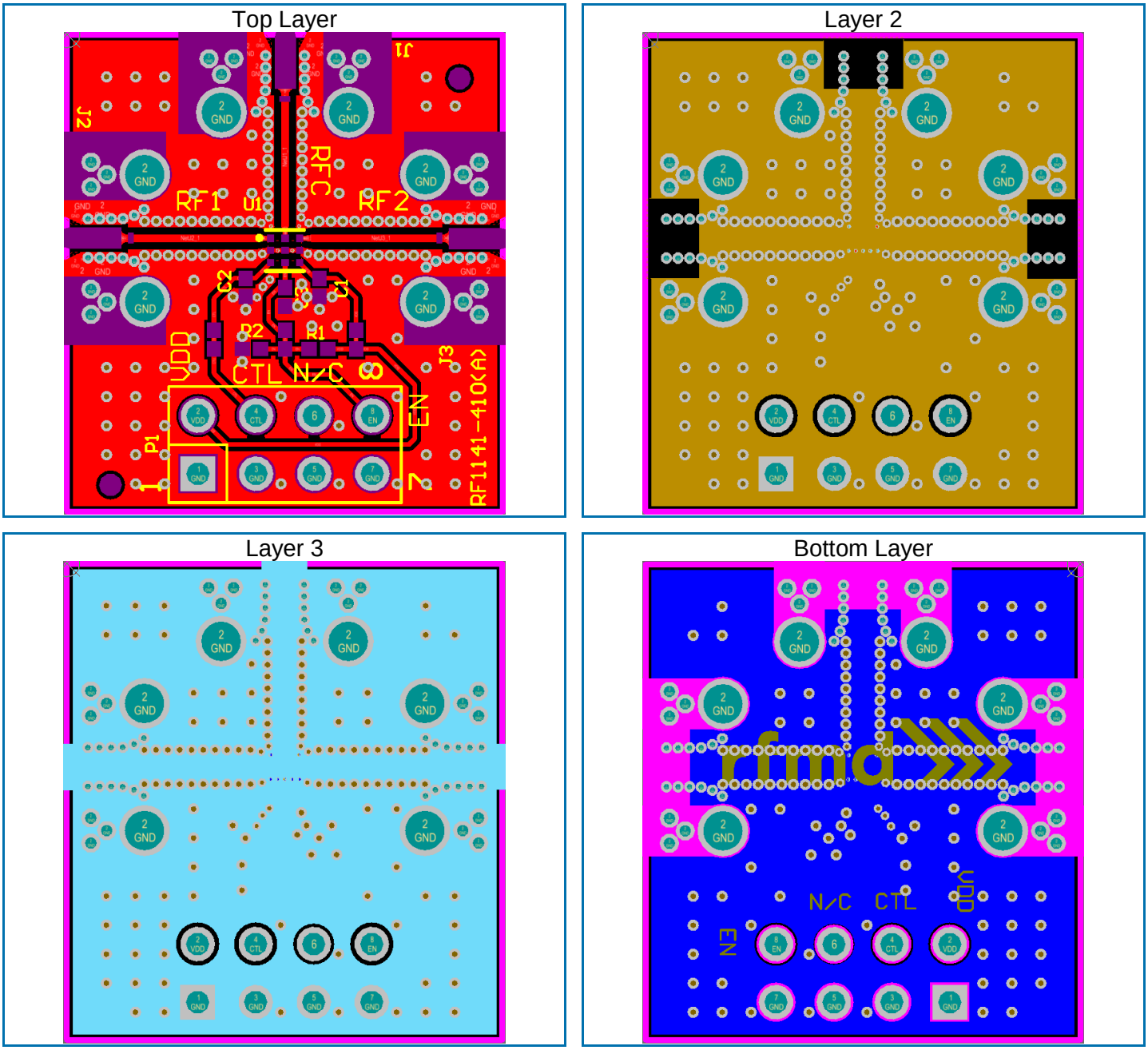

Figure 5. EVB layout layer by layer

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EVB Layer Information

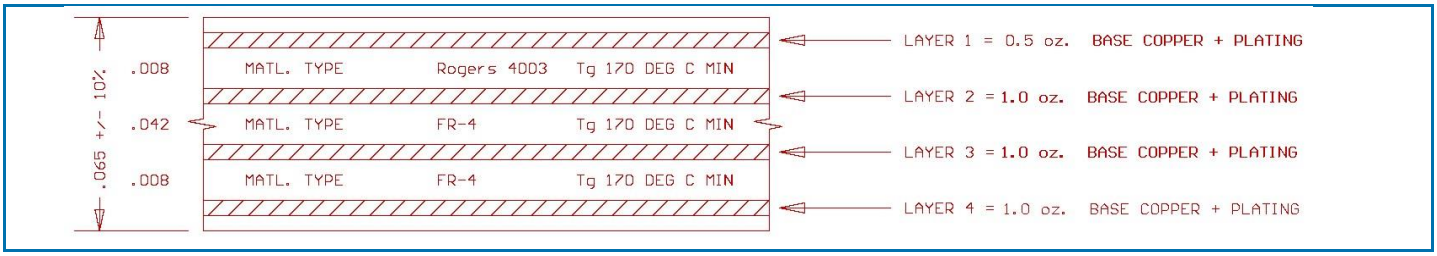

Figure 6. PCB Stack-up

PCB Design Requirements

PCB Metal Land Pattern

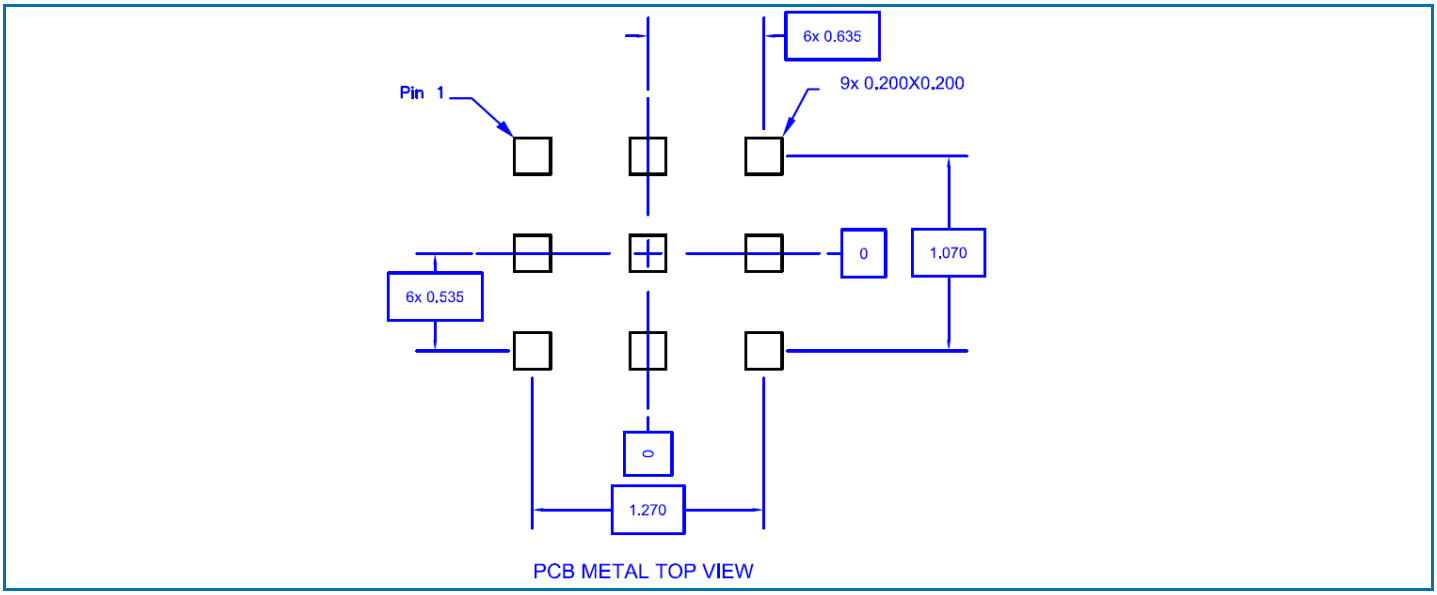

Figure 7. PCB Metal Land Pattern

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PCB Soldermask Pattern

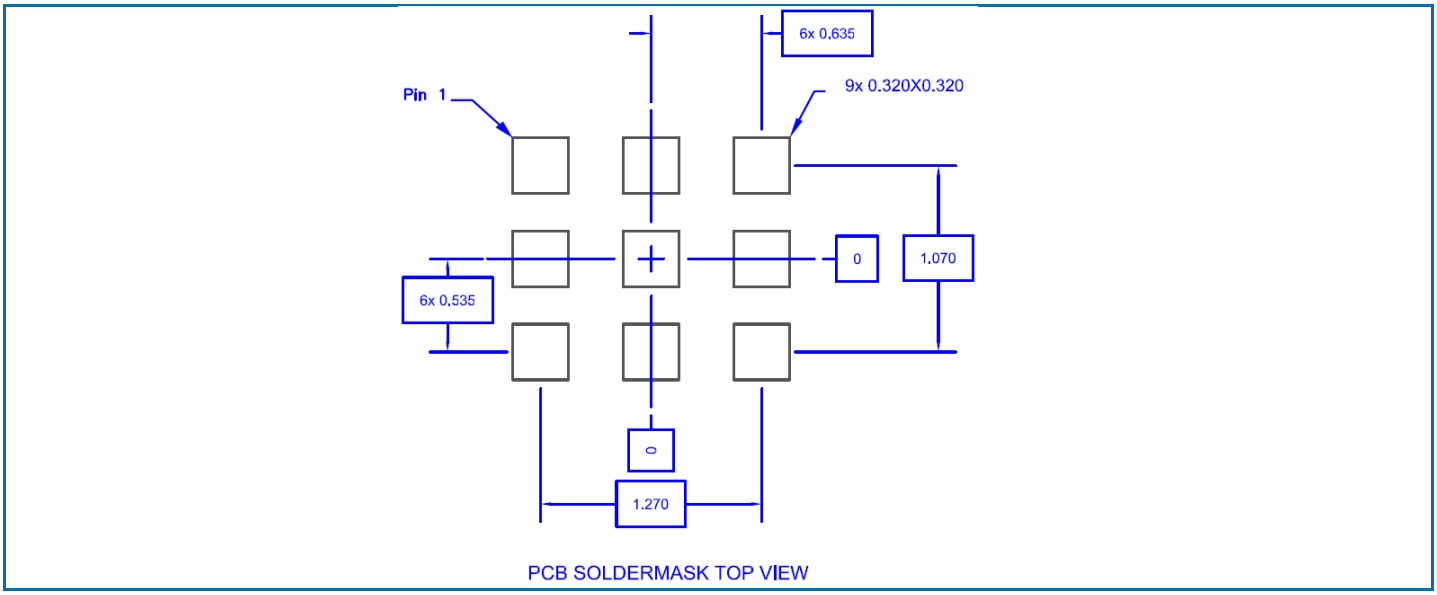

Figure 8. PCB Soldermask Pattern

PCB Stencil Pattern

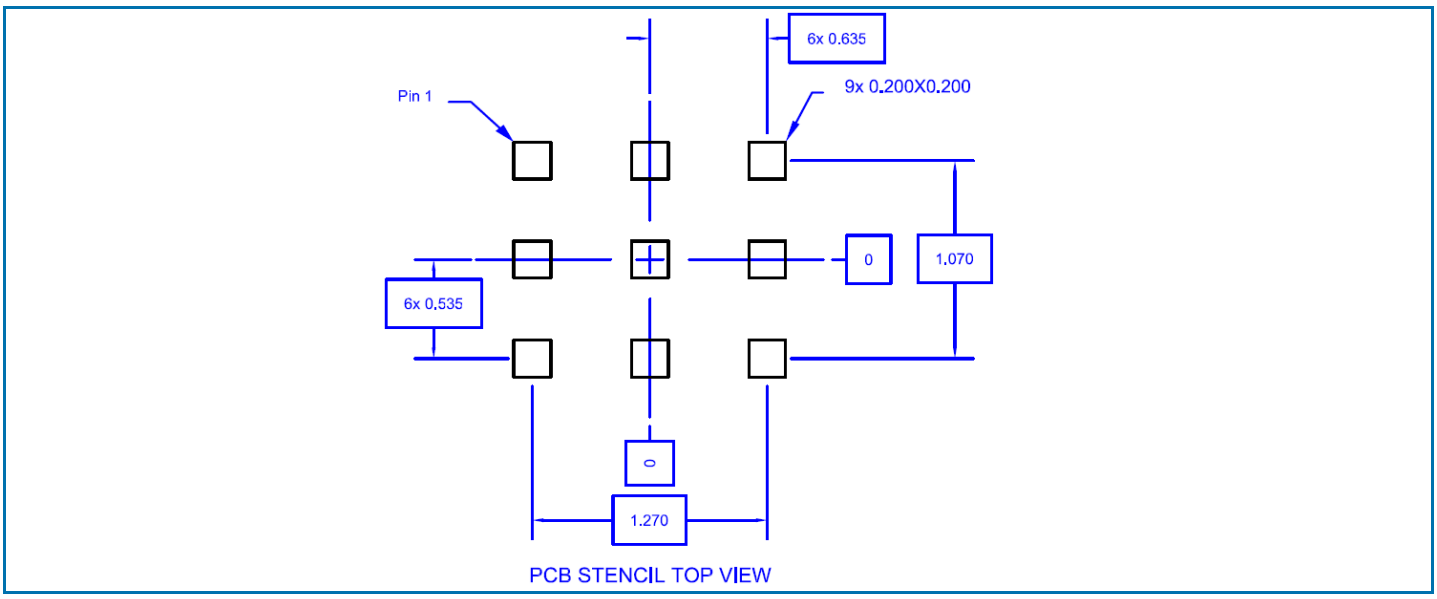

Figure 9. PCB Stencil Pattern

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Timing Diagram

Power ON and OFF sequence

It is very important that the user adheres to the correct power-on/off sequence in order to avoid damaging the device. The control signal V_{CTL} should be set to 0V unless V_{DD} is set in the operating voltage range.

RF signal should not be applied on any of the RF ports when the V_{DD} is below 2.4V.

Note - V_{EN} can be connected to V_{DD} such that they can be applied and removed at the same time, but logic states 3 and 4 cannot be set in this configuration.

Power ON –

1) Apply voltage supply - V_{DD}
2) Apply Enable and Control - V_{EN} and V_{CTL}
3) Wait 20µs or greater and then apply RF

Change logic state –

1) Remove RF
2) Change Enable V_{EN} and Control V_{CTL} to set the switch to desired logic state
4) Wait 5µs or greater and then apply RF

Power OFF –

1) Remove RF
2) Remove Enable and Control - V_{EN} and V_{CTL}
3) Remove V_{DD}

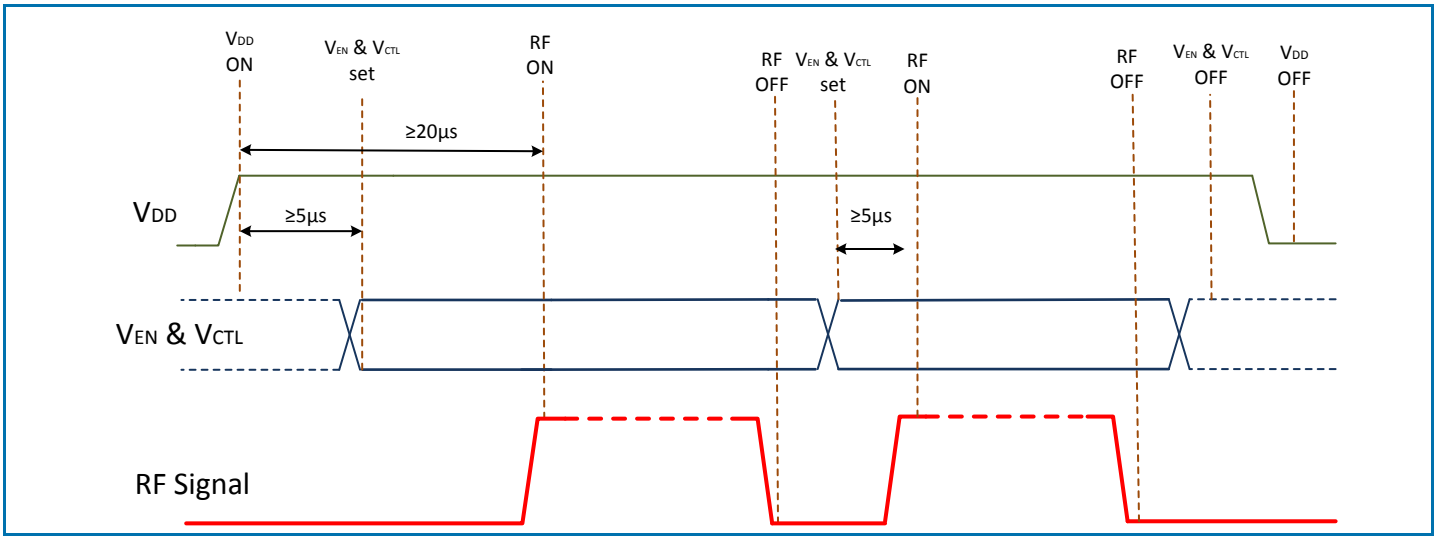

Figure 10. Timing sequence

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Revision History

Revision	Release Date	Description
DS140513	May 13, 2014	Production released.
DS140609	June 9, 2014	Update IIP3 specifications
DS150911	September 11, 2015	Update to Abs Max Table for Power Handling

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