Stepping Motor Driver Series

Constant Current 2ch
36V Simple Series

BD63922EFV/BD63942EFV/BD63962EFV ver.1

●Outline

BD63922EFV,BD63942EFV,BD63962EFV are the ultra simple type that provides the minimum function for driving stepping motor and various protection circuits.

As for its basic function, it is a low power consumption bipolar PWM constant current-drive driver with power supply's rated voltage of 36V and rated output current of 0.8A, 1.2A, 1.5A, and each driver is pin-compatible so that replacement can be done easily. Also it makes μ-STEP drive possible by inputting external DAC signal so that it provides wider application area. There are excitation modes of FULL STEP & HALF STEP mode. This series contributes to reduction of mounting area, cost down, safety design.

●Feature

1) Power supply: one system drive (rated voltage of 36V)
2) Rated output current: 0.8A, 1.2A, 1.5A
3) Low ON resistance DMOS output
4) Parallel IN drive mode
5) 2ch drive DC motor
6) PWM constant current control (self oscillation)
7) Built-in spike noise cancel function (external noise filter is unnecessary)
8) FULL STEP applicable to HALF STEP
9) Applicable to μstep drive
10) Forward/reverse break mode for DC motor
11) Power save function
12) Built-in logic input pull-down resistor
13) Power-on reset function
14) Thermal shutdown circuit (TSD)
15) Over current protection circuit (OCP)
16) Under voltage lock out circuit (UVLO)
17) Over voltage lock out circuit (OVLO)
18) Malfunction prevention at the time of no applied power supply (Ghost Supply Prevention)
19) Electrostatic discharge: 4kV (HBM specification)
20) Microminiature, ultra-thin and high heat-radiation (exposed metal type) HTSSOP package
21) Pin-compatible line-up

●Application

Laser beam printer, Scanner, Photo printer, FAX, Ink jet printer, Mini printer, Sewing machine, Toy, and Robot etc.

DEC. 2008

●Absolute maximum ratings(Ta=25°C)

Item	Symbol	BD63922EFV	BD63942EFV	BD63962EFV	Unit
Supply voltage	$V_{CC1,2}$	-0.2～+36.0			V
Power dissipation	Pd	1.1 ※1			W
		4.0 ※2			
Input voltage for control pin	V_{IN}	-0.2～+5.5			V
RNF maximum voltage	V_{RNF}	0.5			V
Maximum output current	I_{OUT}	0.8 ※3	1.2 ※3	1.5 ※3	A/phase
Maximum output current(peak) ※4	$I_{OUTpeak}$	1.0 ※3	1.5 ※3	2.0 ※3	A/phase
Operating temperature range	T_{opr}	-25～+85			°C
Storage temperature range	T_{stg}	-55～+150			°C
Junction temperature	T_{jmax}	+150			°C

※1 70mm×70mm×1.6mm glass epoxy board. Derating in done at 8.8mW/°C for operating above Ta=25°C.

※2 4-layer recommended board. Derating in done at 32.0mW/°C for operating above Ta=25°C.

※3 Do not, however exceed Pd, ASO and T_{jmax}=150°C.

※4 Pulse width tw≦1ms, duty 20%.

●Operating conditions(Ta= -25～+85°C)

Item	Symbol	BD63922EFV	BD63942EFV	BD63962EFV	Unit
Supply voltage	$V_{CC1,2}$	19～28			V
Output current (DC)	I_{OUT}	0.5 ※5	0.9 ※5	1.2 ※5	A/phase

※5 Do not however exceed Pd, ASO.

●Electrical characteristics

Applicable to all the series (Unless otherwise specified Ta=25°C, $V_{cc1,2}$=24V)

Item	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Whole						
Circuit current at standby	I_{CCST}	-	0.6	2.0	mA	PS=L
Circuit current	I_{CC}	-	2.7	7.0	mA	PS=H, VREF=0.4V
Control input (IN1A, IN1B, IN2A, IN2B, PS)						
H level input voltage	V_{INH}	2.0	-	-	V	
L level input voltage	V_{INL}	-	-	0.8	V	
Output (OUT1A, OUT1B, OUT2A, OUT2B)						
Output ON resistance (BD63920EFV)	R_{ON}	-	2.8	3.6	Ω	I_{OUT} =0.3A Sum of upper and lower
Output ON resistance (BD63940EFV)	R_{ON}	-	1.4	1.8	Ω	I_{OUT} =0.7A Sum of upper and lower
Output ON resistance (BD63960EFV)	R_{ON}	-	1.1	1.4	Ω	I_{OUT} =1.0A Sum of upper and lower
Output leak current	I_{LEAK}	-	-	10	μA	
Current control						
RNFX input current	I_{RNFX}	-40	-20	-	μA	RNFX=0V
VREFX input current	I_{VREF}	-2.0	-0.1	-	μA	VREFX=0V
VREFX input voltage range	V_{REF}	0	-	0.4	V	
Comparator offset	V_{COFS}	-20	0	20	mV	VREFX=0.4V
Minimum on time	T_{ONMIN}	0.3	0.7	1.2	μs	R=39kΩ, C=1000pF

●Characteristics reference data (Unless otherwise specified $V_{cc1,2}$=24V)

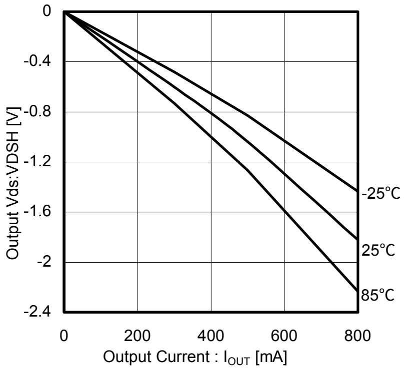


Fig.1 Output H voltage (BD63922EFV)

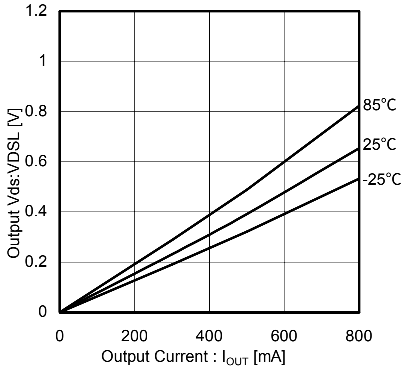


Fig.2 Output L voltage (BD63922EFV)

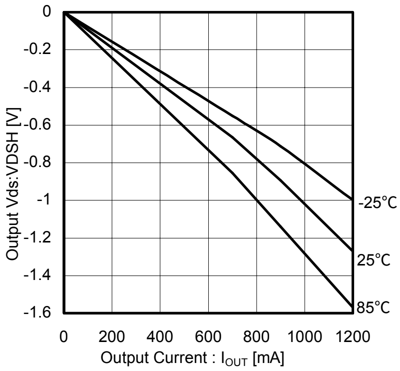


Fig.3 Output H voltage (BD63942EFV)

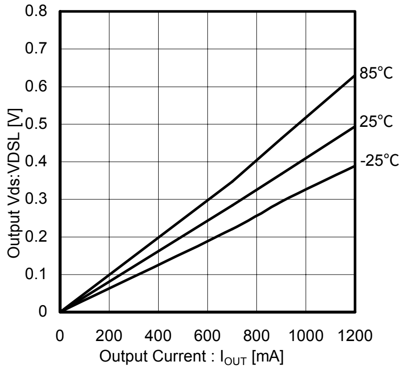


Fig.4 Output L voltage (BD63942EFV)

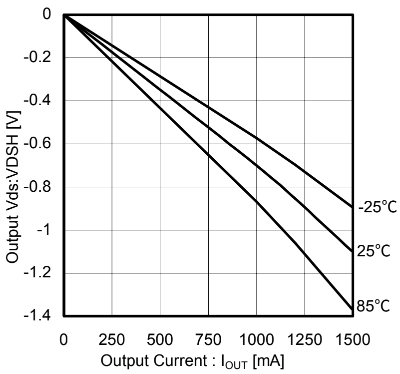


Fig.5 Output H voltage (BD63962EFV)

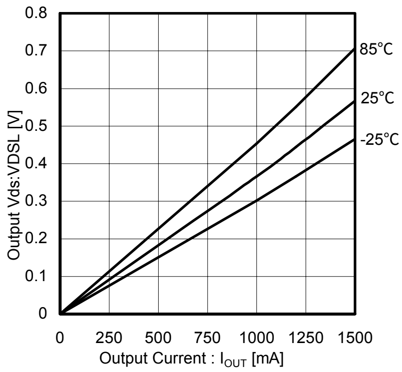


Fig.6 Output L voltage (BD63962EFV)

●Terminal function

1) BD63922EFV/BD63942EFV/BD63962EFV

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	PGND	Ground terminal	13	IN1A	Logic input terminal
2	IN2B	Logic input terminal	14	PGND	Ground terminal
3	VREF2	Output current value setting terminal	15	VCC1	Power supply terminal
4	CR2	Connection terminal of CR for setting PWM frequency	16	OUT1A	H bridge output terminal
5	NC	Non connection	17	RNF1	Connection terminal of resistor for output current detection
6	TEST	Terminal for testing (used by connecting with GND)	18	OUT1B	H bridge output terminal
7	GND	Ground terminal	19	OUT2B	H bridge output terminal
8	PS	Power save terminal	20	RNF2	Connection terminal of resistor for output current detection
9	CR1	Connection terminal of CR for setting PWM frequency	21	OUT2A	H bridge output terminal
10	VREF1	Output current value setting terminal	22	VCC2	Power supply terminal
11	IN1B	Logic input terminal	23	NC	Non connection
12	NC	Non connection	24	IN2A	Logic input terminal

●Block diagram・Application circuit diagram・Input output equivalent circuit diagram

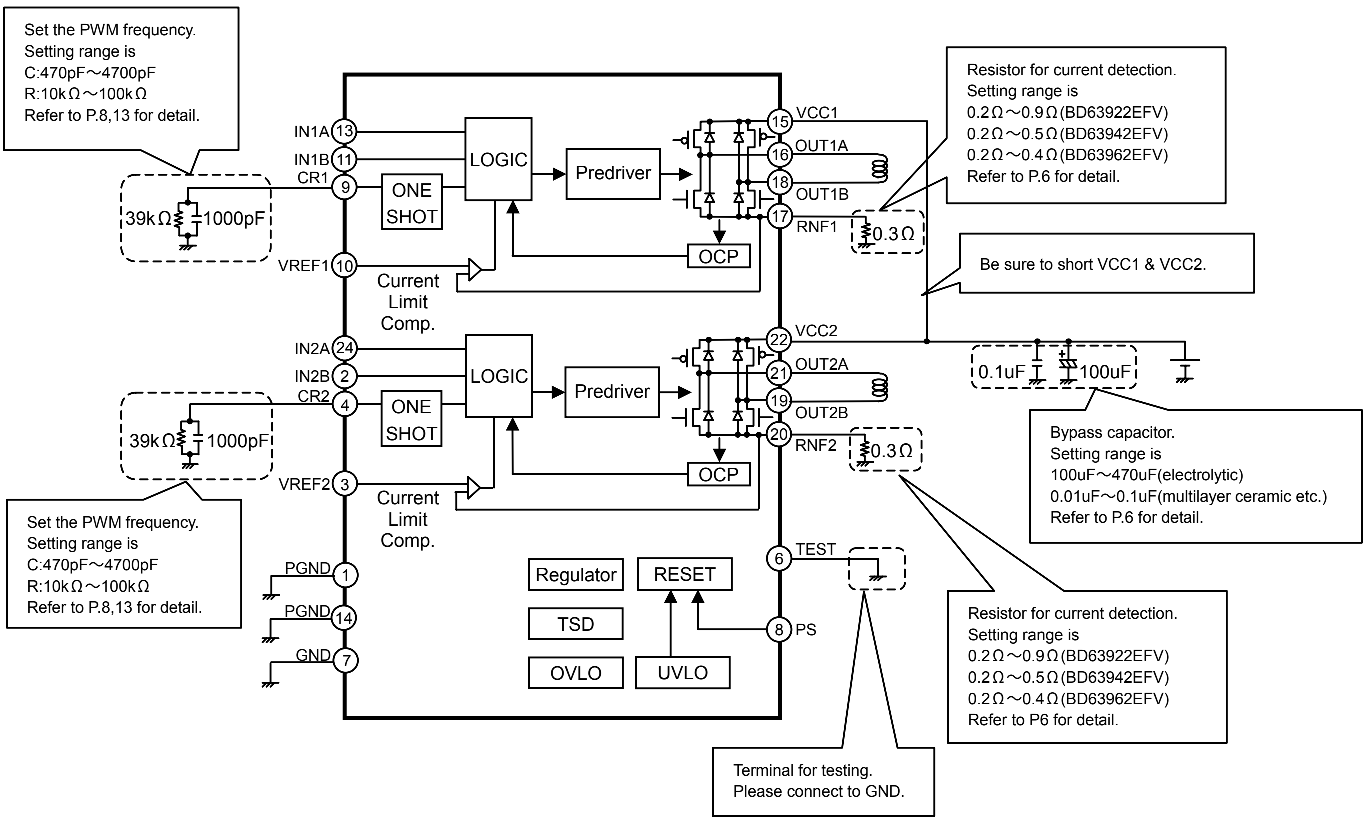


Fig.7 Block diagram & Application circuit diagram

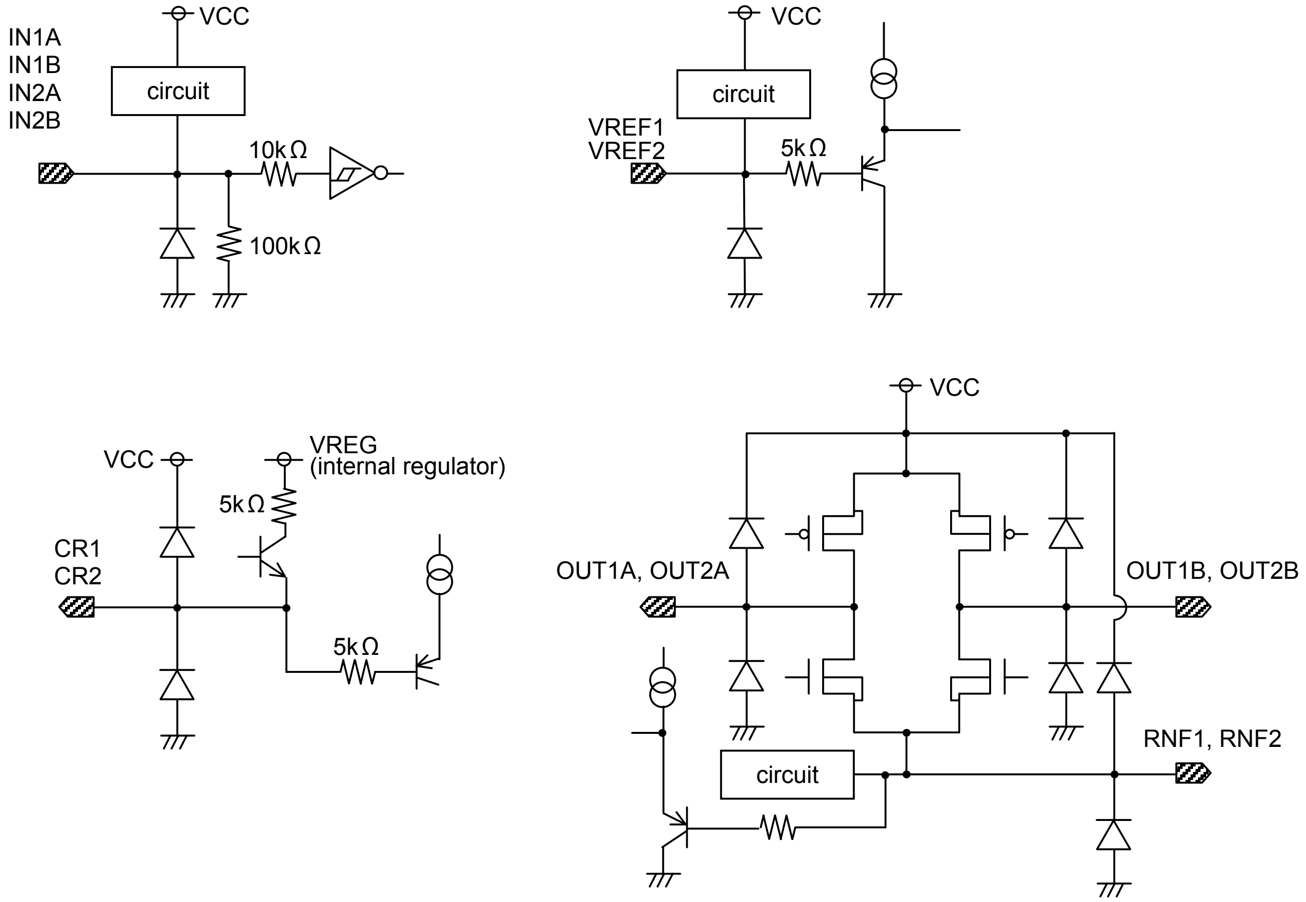


Fig.8 Input output equivalent circuit diagram

●Points to notice for terminal description and PCB layout

○PS／Power save terminal

PS can make circuit standby state and make motor output OPEN. Please be careful because there is a delay of 40μs(max.) before it is returned from standby state to normal state and the motor output becomes ACTIVE.

PS	State
L	Standby state (RESET)
H	ACTIVE

○IN1A, IN1B, IN2A, IN2B／Control logic input terminal

These terminals decide output state.

	Input		Output		
PS	IN1A IN2A	IN1B IN2B	OUT1A OUT2A	OUT1B OUT2B	
L	X	X	OPEN	OPEN	Stand by (All circuits)
H	L	L	OPEN	OPEN	Stand by
H	H	L	H	L	Forward
H	L	H	L	H	Reverse
H	H	H	L	L	Brake

X: H or L

○TEST Terminal／Terminal for testing

This is the terminal used at the time of shipping test. Please connect to GND. Be aware that there is a possibility of malfunction depending on conditions when GND is unconnected.

○VCC1,VCC2／Power supply terminal

Motor's drive current is flowing in it, so please wire in such a way that the wire is thick & short and has low impedance. Voltage VCC may have great fluctuation, so please arrange the bypass capacitor of about 100μF～470μF as close to the terminal as possible and adjust in such a way that the voltage VCC is stable. Please increase the capacity if needed especially when a large current is used or those motors that have great back electromotive force are used. In addition, for the purpose of reducing of power supply's impedance in wide frequency bandwidth, parallel connection of multi-layered ceramic capacitor of 0.01μF～0.1μF etc is recommended. Extreme care must be used to make sure that the voltage VCC does not exceed the rating even for a moment. VCC1 & VCC2 are shorted inside IC, so please be sure to short externally VCC1 & VCC2 when using. If used without shorting, malfunction or destruction may occur because of concentration of current routes etc., so please make sure that they are shorted when in use. Still more, in the power supply terminal, there is built-in clamp component for preventing of electrostatic destruction. If steep pulse or voltage of surge more that maximum absolute rating is applied, this clamp component operates, as a result there is the danger of destruction, so please be sure that the maximum absolute rating must not be exceeded. It is effective to mount a Zener diode of about the maximum absolute rating. Moreover, the diode for preventing of electrostatic destruction is inserted between Vcc terminal and GND terminal, as a result there is the danger of IC destruction if reverse voltage is applied between Vcc terminal and GND terminal, so please be careful.

○GND,PGND／Ground terminal

In order to reduce the noise caused by switching current and to stabilize the internal reference voltage of IC, please wire in such a way that the wiring impedance from this terminal is made as low as possible to achieve the lowest electrical potential no matter what operating state it may be.

○OUT1A,OUT1B,OUT2A,OUT2B／H Bridge output terminal

Motor's drive current is flowing in it, so please wire in such a way that the wire is thick & short and has low impedance. It is also effective to add a Schottky diode if output has positive or negative great fluctuation when large current is used etc, for example, if counter electromotive voltage etc. is great. Moreover, in the output terminal, there is built-in clamp component for preventing of electrostatic destruction. If surge or voltage more that maximum absolute voltage is applied, this clamp component operates, as a result there is the danger of even destruction, so please be sure that the maximum absolute rating must not be exceeded.

○RNF1,RNF2／Connection terminal of resistor for detecting of output current

Connect the current detection resistors of the values that correspond to each product (IC) between the terminal and GND. (see page 4) In view of the power consumption of the current-detecting resistor, please determine the resistor in such a way that $W=I_{OUT}^2 \cdot R$[W] does not exceed the power dissipation of the resistor. In addition, please wire in such a way that it has a low impedance and does not have a impedance in common with other GND patterns because motor's drive current flows in the pattern through RNF terminal～current-detecting resistor～GND. Please do not exceed the rating because there is the possibility of circuits' malfunction etc. if RNF voltage has exceeded the maximum rating (0.5V). Moreover, please be careful because if RNF terminal is shorted to GND, large current flows without normal PWM constant current control, then there is the danger that OCP or TSD will operate. If RNF terminal is open, then there is the possibility of such malfunction as output current does not flow either, so please do not let it open.

○VREF／Output current value-setting terminal

This is the terminal to set the output current value. The output current value can be set by VREF voltage and current-detecting resistor (RNF resistor).

BD63922EFV: Output current I_{OUT} [A] = VREF [V] / {RNF [Ω] + 0.046}
BD63942EFV: Output current I_{OUT} [A] = VREF [V] / {RNF [Ω] + 0.043}
BD63962EFV: Output current I_{OUT} [A] = VREF [V] / {RNF [Ω] + 0.035}

Please avoid using it with VREF terminal open because if VREF terminal is open, the input is unsettled, and the VREF voltage increases, and then there is the possibility of such malfunctions as the setting current increases and a large current flows etc. Please keep to the input voltage range because if the voltage of over 0.5V is applied on VREF terminal, then there is also the danger that a large current flows in the output and so OCP or TSD will operate. Besides, please take into consideration the outflow current (max.2μA) if inputted by resistance division when selecting the resistance value. The minimum current, which can be controlled by VREF voltage, is determined by motor coil's L & R values and minimum ON time because there is a minimum ON time in PWM drive. It is also effective to bias from exterior at the condition of VREF1 and VREF2 are shorted except when μSTEP drive that is described on page 10 is performed.

○CR1,CR2／Connection terminal of CR for setting PWM frequency

This is the terminal to set the minimum ON time and OFF time. Please connect the external C(470pF～4700pF) and R(10kΩ～100kΩ) between this terminal and GND.

The OFF time is determined by Toff[s]　C・R・0.81. Please interconnect from external components to GND in such a way that the interconnection does not have impedance in common with other GND patterns. In addition, please carry out the pattern design in such ways as keeps such steep pulses as square wave etc. away and that there is no noise plunging. Please mount the two components of C and R if being used by PWM constant current control because normal PWM constant current control becomes impossible if CR terminal is open or it is biased externally. If the PWM frequency is low, there is a possibility that it will cause noise by being in the human auditory range, therefore pay attention to OFF time not to become longer than 50μsec.

○NC terminal

This terminal is unconnected electrically with IC internal circuit. Have this terminal open or GND connected.

○IC back side metal／Metal for heat-radiation

For HTSSOP-B24 package, the heat-radiating metal is mounted on IC's back side, and on the metal the heat-radiating treatment is performed when in use, which becomes the precondition to use, so please secure sufficiently the heat-radiating area by surely connecting by solder with the GND plane on the board and getting as wide GND pattern as possible. Please be careful because the allowable loss as shown in page 12 can not be secured if not connected by solder. Moreover, the back side metal is shorted with IC chip's back side and becomes the GND potential, so there is the danger of malfunction and destruction if shorted with potentials other than GND, therefore please absolutely do not design patterns other than GND through the IC's back side.

●PWM Constant current control

1) Current control operation

Output transistor is turned on and so the output current increases, and when the RNF voltage (the voltage is converted into by output current due to external resistor of RNF terminal) reaches the voltage value, which is VREF input voltage, the current limit comparator operates and enters the current decay mode. After that, the OFF time, which is caused by CR timer, has passed before the output is again turned on. The above-mentioned process is repeated.

2) Noise cancel function

In order to avoid the incorrect detection of current-detecting comparator's caused by RNF spike noise that occurs at the time of output ON, the noise cancel time Tn is set up, so the current detection within the noise cancel time immediately after the output transistor is turned on is invalid. Therefore, the constant current drive is possible without external filter. And the noise cancel time becomes the minimum ON time of the motor output transistor.

3) CR Timer

CR voltage is clamped at 0.9V (Typ.) during output ON, and as soon as the output current reaches the current limit value and enters the current decay mode, the discharge begins and goes on till 0.4V(Typ.), then the output is turned on again and the charge begins simultaneously. The time taken to discharge from 0.9V (Typ.) to 0.4V (Typ.) is the OFF time Toff. In addition, CR terminal starts charging, and the time taken to charge from 0.4V (Typ.) to 0.8V (Typ.) is the noise cancel time Tn. Then, Toff and Tn can be set by CR terminal's external constant according to the following formula (Typ.).

T_{off}[s] C・R・0.81

T_n[s] C・R'・ln[(VCR-0.4)/(VCR-0.8)] In the formula: VCR=V・R/(R'+R)

V : internal regulator voltage 5V(Typ.)

R': CR terminal's internal impedance of 5kΩ(Typ.)

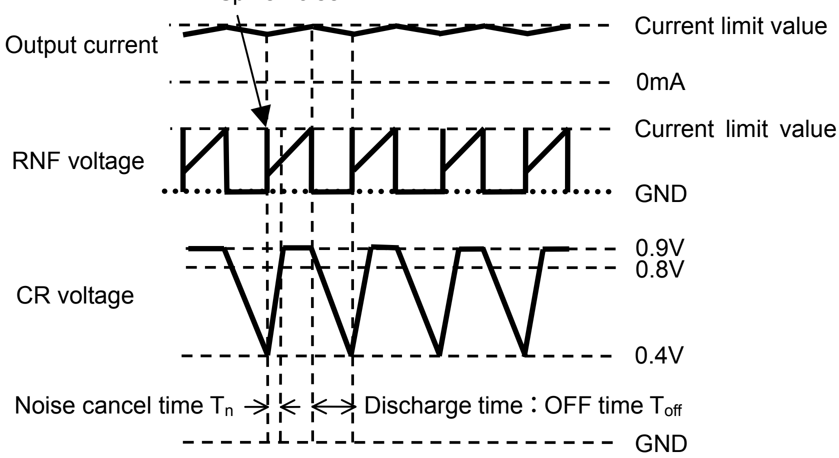


Fig.9 Timing chart of CR voltage, RNF voltage, and output current

Please use the resistor of over 10kΩ(10kΩ～100kΩ recommended) because if the resistance value is low, the clamp voltage 0.9V(Typ.) can not be reached. If a capacitor with a value of a few thousand pico farad is used (470pF～4700pF recommended), the noise cancel time Tn becomes longer, and there is the danger that the output current, which is flowing, is greater than the current limit value because of L and R values of motor coil. Moreover, it is necessary to be careful because if the OFF time Toff is set longer than normal, the output current's ripple becomes larger, the average current is decreased, and then the rotating efficiency may be reduced. Please choose the optimal value in order to reduce the motor drive noise and the distortion of output current's waveform etc. to a minimum.

●Current decay mode

For the PWM constant current drive of this IC, the current decay mode is SLOW DECAY mode. Moreover, in order to reduce the power consumption of IC to a minimum, SLOW DECAY adopts the current decay based on the synchronous rectification mode, so low-power-consumption and high-efficiency drive is realized. The state of output transistor and the route of motor's regenerative current during current attenuating for SLOW DECAY mode are as follows.

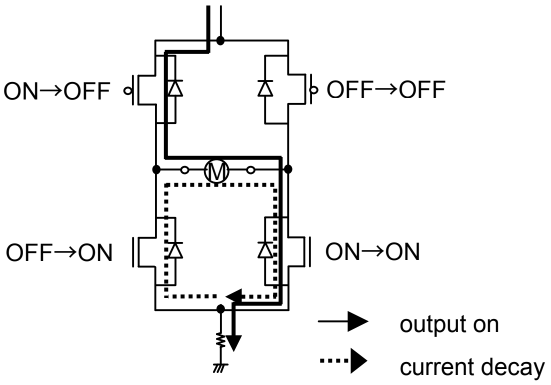


Fig.10 Route of regenerative current during current decay

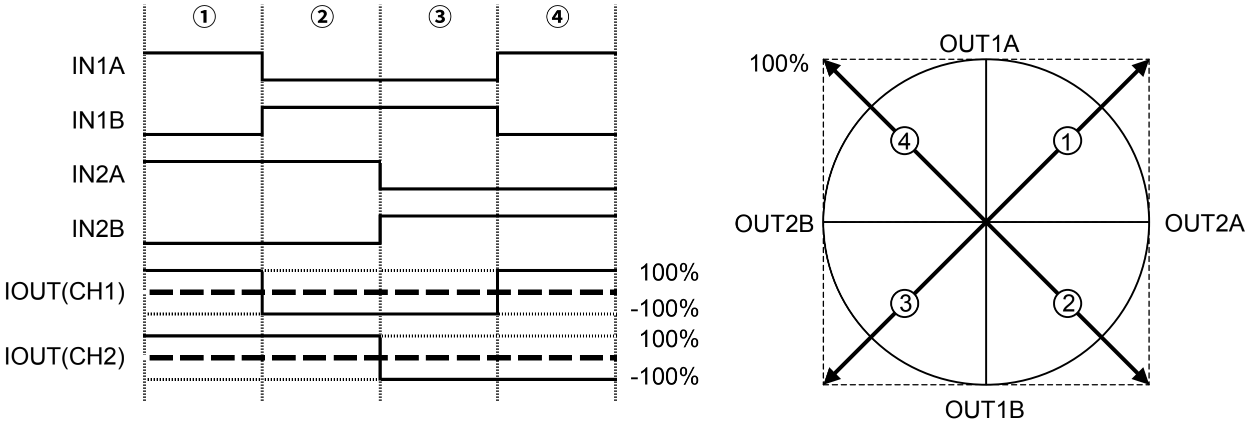
When the current attenuates, the voltage between motor coils is small and the regenerative current decreases slowly, so the current ripple becomes smaller, which is favorable for motor torque. But the output current increases due to deterioration of current control characteristic in small current region, or it is easily affected by motor's BEMF at the time of high pulse rate drive related to the modes of HALF STEP and QUARTER STEP*, so change of current limit value cannot be followed, current waveform distorts and motor vibration may increase. It is most suitable to the FULL STEP mode and the modes of the HALF STEP and QUARTER STEP* of low pulse rate drive.

*There is a necessity of external DAC in order to realize the QUARTER STEP mode with this series.

●Example of control sequence and torque vector

You can drive a stepping motor with FULL step mode and HALF step mode and quarter step mode by the following logic input (IN1A, IN1B, IN2A, IN2B) sequence. See page 6 for current value set.

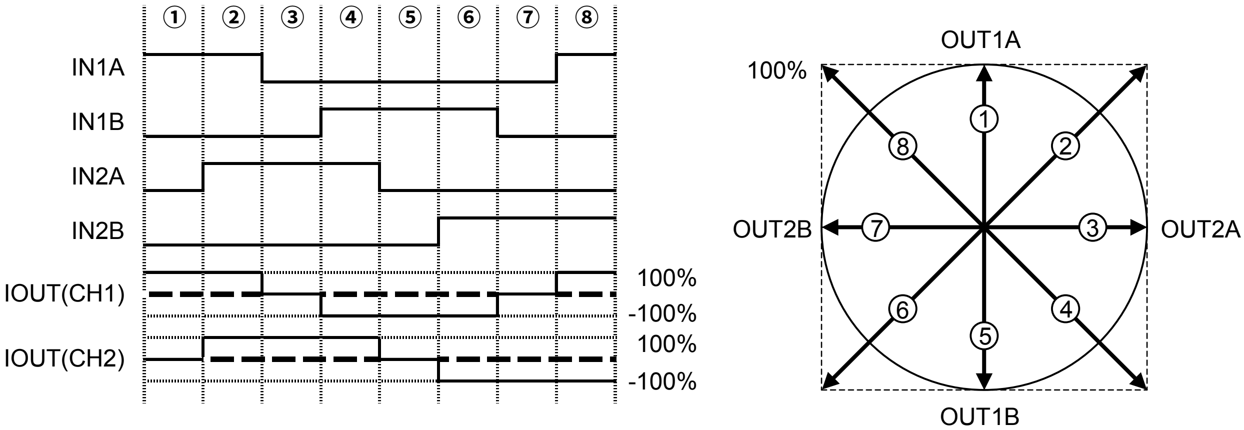
FULL STEP



	IN1A	IN1B	IN2A	IN2B	OUT1A	OUT1B	OUT2A	OUT2B
①	H	L	H	L	H	L	H	L
②	L	H	H	L	L	H	H	L
③	L	H	L	H	L	H	L	H
④	H	L	L	H	H	L	L	H

Fig.11 Control Sequence at FULL STEP

HALF STEP



	IN1A	IN1B	**IN2A**	IN2B	OUT1A	OUT1B	OUT2A	OUT2B
①	H	L	L	L	H	L	OPEN	OPEN
②	H	L	H	L	H	L	H	L
③	L	L	H	L	OPEN	OPEN	H	L
④	L	H	H	L	L	H	H	L
⑤	L	H	L	L	L	H	OPEN	OPEN
⑥	L	H	L	H	L	H	L	H
⑦	L	L	L	H	OPEN	OPEN	L	H
⑧	H	**L**	L	**H**	H	**L**	L	**H**

Fig.12 Control Sequence at HALF STEP

● μSTEP mode

This IC makes it possible to set output current value of CH1, CH2 by VREF1, VREF2 terminal, and output logic of CH1, CH2 by IN1A, IN1B, IN2A, IN2B respectively. Therefore μSTEP drive can be realized by inputting linear voltage into VREF with external DAC and controlling IN1A, IN1B, IN2A, IN2B terminal

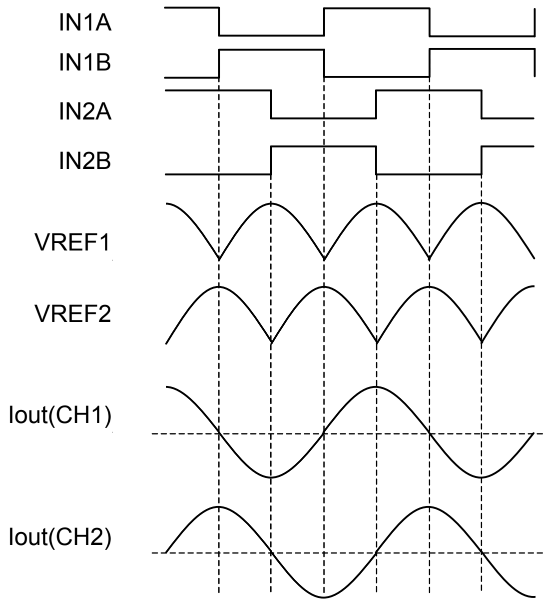


Fig.13 Input signal and motor drive current at μSTEP drive

●Protection Circuits

○Thermal Shutdown (TSD)

This IC has a built-in thermal shutdown circuit for thermal protection. When the IC's chip temperature rises above 175°C (Typ.), the motor output becomes OPEN. Also, when the temperature returns to under 150°C (Typ.), it automatically returns to normal operation. However, even when TSD is in operation, if heat is continued to be added externally, heat overdrive can lead to destruction.

○Over Current Protection (OCP)

This IC has a built in over current protection circuit as a provision against destruction when the motor outputs are shorted each other or Vcc-motor output or motor output-GND is shorted. This circuit latches the motor output to OPEN condition when the regulated threshold current flows for 4μs (Typ.). It returns with power reactivation or a reset of the PS terminal. The over current protection circuit's only aim is to prevent the destruction of the IC from irregular situations such as motor output shorts, and is not meant to be used as protection or security for the set. Therefore, sets should not be designed to take into account this circuit's functions. After OCP operating, if irregular situations continues and the return by power reactivation or a reset of the PS terminal is carried out repeatedly, then OCP operates repeatedly and the IC may generate heat or otherwise deteriorate. When the L value of the wiring is great due to the wiring being long, after the over current has flowed and the output terminal voltage jumps up and the absolute maximum values may be exceeded and as a result, there is a possibility of destruction. Also, when current which is over the output current rating and under the OCP detection current flows, the IC can heat up to over T_{jmax} =150°C and can deteriorate, so current which exceeds the output rating should not be applied.

○Under Voltage Lock Out (UVLO)

This IC has a built-in under voltage lock out function to prevent false operation such as IC output during power supply under voltage. When the applied voltage to the Vcc terminal goes under 15V (Typ.), the motor output is set to OPEN. This switching voltage has a 1V (Typ.) hysteresis to prevent false operation by noise etc. Please be aware that this circuit does not operate during power save mode.

○Over Voltage Lock Out (OVLO)

This IC has a built-in over voltage lock out function to protect the IC output and the motor during power supply over voltage. When the applied voltage to the VCC terminal goes over 32V (Typ.), the motor output is set to OPEN. This switching voltage has a 1V (Typ.) hysteresis and a 4μs (Typ.) mask time to prevent false operation by noise etc. Although this over voltage locked out circuit is built-in, there is a possibility of destruction if the absolute maximum value for power supply voltage is exceeded, therefore the absolute maximum value should not be exceeded. Please be aware that this circuit does not operate during power save mode.

○False operation prevention function in no power supply (Ghost Supply Prevention)

If a logic control signal is input when there is no power supplied to this IC, there is a function which prevents the false operation by voltage supplied via the electrostatic destruction prevention diode from the logic control input terminal to the Vcc, to this IC or to another IC's power supply. Therefore, there is no malfunction of the circuit even when voltage is supplied to the logic control input terminal while there is no power supply.

●Thermal design

Please confirm that the IC's chip temperature Tj is not over 150°C, while considering the IC's power consumption (W), package power (Pd) and ambient temperature (Ta). When Tj=150°C is exceeded the functions as a semiconductor do not operate and problems such as parasitism and leaks occur. Constant use under these circumstances leads to deterioration and eventually destruction of the IC. T_{jmax} =150°C must be strictly obeyed under all circumstances.

○Thermal Calculation

The IC's consumed power can be estimated roughly with the power supply voltage (V_{CC}), circuit current (I_{CC}), output ON resistance (R_{ONH},R_{ONL}) and motor output current value (I_{OUT}).

The calculation method during FULL STEP drive, SLOW DECAY mode is shown here:

Consumed power of the Vcc [W] = V_{CC} [V]・I_{CC} [A] ・・・・・・・①

Consumed power of the output DMOS [W] = $\underline{(R_{ONH}[\Omega] + R_{ONL}[\Omega])\cdot I_{OUT}[A]^2\cdot 2[ch]\cdot on\_duty}$
During output ON

+ $\underline{(2\cdot R_{ONL}[\Omega])\cdot I_{OUT}[A]^2\cdot 2[ch]\cdot (1 - on\_duty)}$ ・・・・・・・②
During current decay (recovery)

However, on_duty: PWM on duty = Ton / (Ton+Toff)

Ton varies depending on the L and R values of the motor coil and the current set value. Please confirm by actual measurement, or make an approximate calculation.

Toff is the OFF time which depends on the external CR. See page 8 for details.

Model Number	Upper PchDMOS ON Resistance $R_{ONH}[\Omega]$ (Typ.)	Lower NchDMOS ON Resistance $R_{ONL}[\Omega]$ (Typ.)
BD63922EFV	2.0	0.8
BD63942EFV	1.0	0.4
BD63962EFV	0.7	0.4

Consumed power of total IC W_total [W] = ① + ②

Junction temperature Tj = Ta[°C] + θ_{ja}[°C/W]・W_total [W]

However, the thermal resistance value θ_{ja} [°C/W] differs greatly depending on circuit board conditions. Refer to the derating curve on page 12. Also, we are taking measurements of thermal resistance value θ_{ja} of boards actually in use. Please feel free to contact our salesman.

The calculated values above are only theoretical. For actual thermal design, please perform sufficient thermal evaluation for the application board used, and create the thermal design with enough margin to not exceed T_{jmax}=150°C.

Although unnecessary with normal use, if the IC is to be used under especially strict heat conditions, please consider externally attaching a Schottky diode between the motor output terminal and GND to abate heat from the IC.

●Temperature Monitoring

There is a way to directly measure the approximate chip temperature by using the TEST terminal. However, temperature monitor using this TEST terminal is only for evaluation and experimenting, and must not be used in actual usage conditions. TEST terminal has a protection diode for prevention from electrostatic discharge. The temperature may be monitored using this protection diode.

(1) Measure the terminal voltage when a current of Idiode=50μA flows from the TEST terminal to the GND, without supplying V_{CC} to the IC. This measurement is of the V_F voltage inside the diode.

(2) Measure the temperature characteristics of this terminal voltage. (V_F has a linear negative temperature factor against the temperature.) With the results of these temperature characteristics, chip temperature may be calibrated from the TEST terminal voltage.

(3) Supply V_{CC}, confirm the TEST terminal voltage while running the motor, and the chip temperature can be approximated from the results of (2).

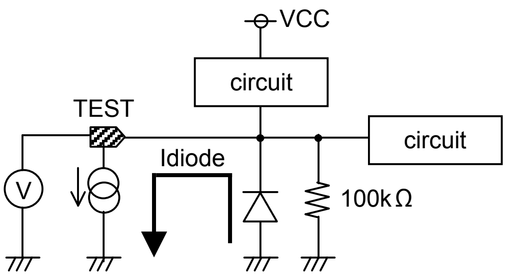


Fig.14 Model diagram for measuring chip temperature

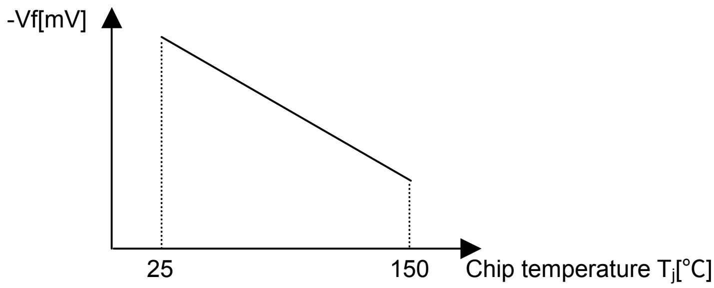


Fig.15 Tj and terminal voltage

●Power dissipation

○HTSSOP-B24 Package (BD63922EFV/BD63942EFV/BD63962EFV))

HTSSOP-B24 has exposed metal on the back, and it is possible to dissipate heat from a through hole in the back. Also, the back of board as well as the surfaces has large areas of copper foil heat dissipation patterns, greatly increasing power dissipation. The back metal is shorted with the back side of the IC chip, being a GND potential, therefore there is a possibility for malfunction if it is shorted with any potential other than GND, which should be avoided. Also, it is recommended that the back metal is soldered onto the GND to short. Please note that it has been assumed that this product will be used in the condition of this back metal performed heat dissipation treatment for increasing heat dissipation efficiency.

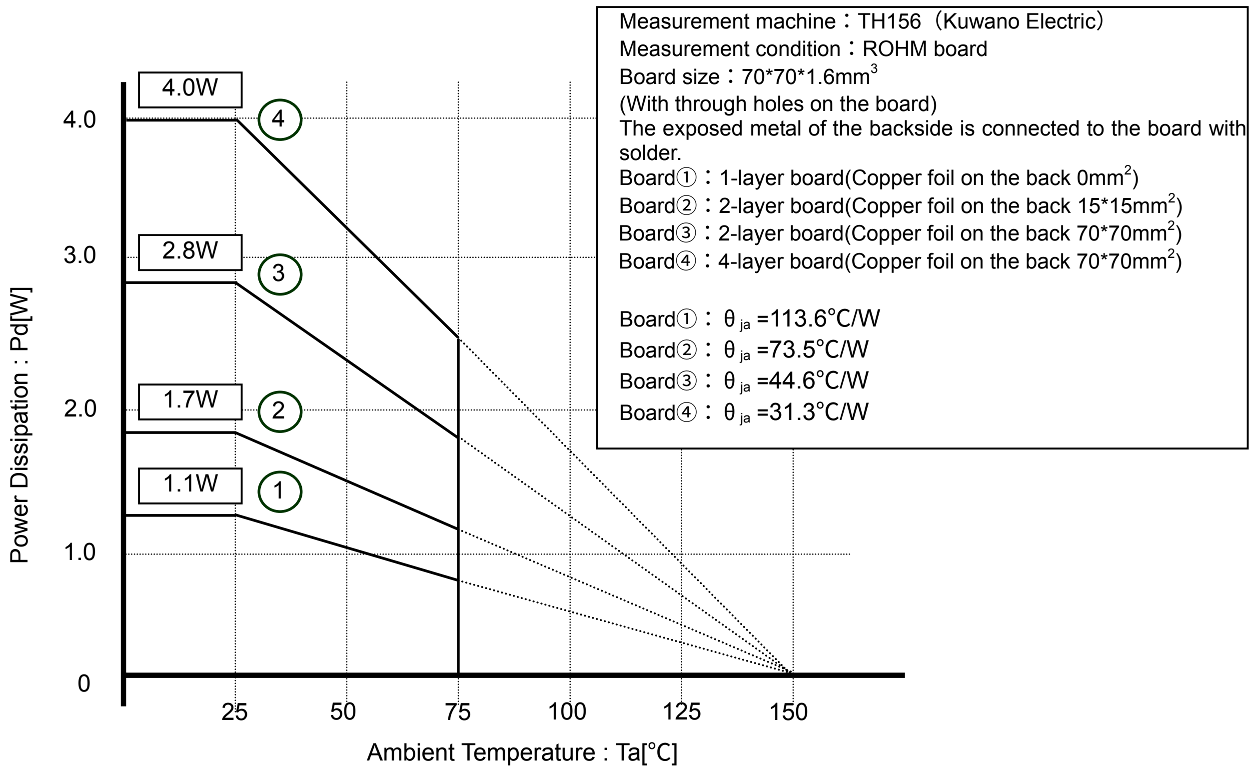


Fig.16 HTSSOP-B24 Derating curve

●Example of application [For BD63922EFV (see page 6)]

○Setting the Current Control Value (VREF and RNF terminals)

We will consider a situation where the RNF terminal's resistance value is the recommended 0.5Ω and the output current is set to 0.288A. Because I_{OUT}=VREF[V] / {RNF[Ω] + 46[mΩ]}
the VREF voltage necessary for I_{OUT}=0.288A is 0.157V.
This means that when the RNF terminal's resistance value is 0.5Ω, VREF voltage=(0.5+0.046)×Output current.
VREF terminal voltage is set to 0.157V due to resistance division.
The VREF terminal's outflow current is max. 2μA when considering the maximum value of the electrical characteristics, yet here, current is max. 4μA at double the current by assuming VREF1 and VREF2 are shorted. As for the bias current of the resistance division, it is necessary to set a sufficient current value that does not fluctuate the reference potential of the resistance division with this current of 4μA.
As an example, we will consider that a current 40 times of 4μA (160μA) is set to be applied.
If the voltage applied to the resistance division is 3.3V,
3.3[V] / 160[μA]=20.6[kΩ]
becomes the sum of R_1 and R_2's resistance values. (R_1+R_2=20.6[kΩ])
Therefore, to make the VREF terminal voltage 0.157V
3.3[V]・R_2 / (R_1+R_2) =0.157[V]
Settings of R_1=20kΩ and R_2=1kΩ is one of good condition.

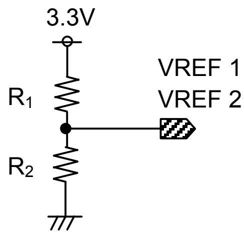


Fig.17 Example of VREF voltage setting

○Setting the PWM Frequency (CR terminal)

The setting method decides the optimal value with respect to the output current ripple, consumed power and noise cancel time T_n (minimum ON time).
The OFF time T_{off} and noise cancel time T_n (minimum ON time t_{ONMIN}) can be set with an external CR constant values. Please see page 8 for details.

[To adjust output current ripple]

The output current ripple depends on the L and R values of the motor coil as well as the current decay mode, so first the current ripple should be confirmed by driving the motor under actual application conditions with the recommended values of C=1000[pF], R=39[kΩ] and OFF time T_{off}=32[μs]. If there are any problems with the ripple, the optimal OFF time should be set by adjusting R values.
At this time, if the OFF time T_{off} needs to be shortened, it is recommended that the R value is adjusted. If the C value is made smaller the noise cancel time T_n is shortened and there is a possibility of malfunction caused by the RNF spike noise, which is generated at output ON.

[To adjust noise cancel time]

Because the noise level of the RNF spike noise varies depending on the capacity or inductance components etc of the board and pattern, if there is any malfunction caused by the RNF spike noise at the recommended value of C=1000[pF], the noise cancel time T_n should be lengthened by making the C value greater. Be aware that if the C value is doubled, the OFF time T_{off} is also doubled and the R value needs to be halved.

There are various combinations of C and R values, but they must be set within the ranges of the recommended values (C:470pF~4700pF, R:10kΩ~100kΩ)(see page 8). Also, if the PWM frequency is low, there is a possibility that it will cause noise by being in the human auditory range, therefore OFF time should not exceed 50μsec. On the other hand, if the frequency is too high, there is a possibility with the relative electrical time constant that the set current is not applied to the motor, depending on the L and R values of the motor coil.

●Usage Notes

(1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

(2) Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

(3) Power supply Lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

(4) GND Potential

The potential of GND pin must be minimum potential in all operating conditions.

(5) Metal on the backside (Define the side where product markings are printed as front)

The metal on the backside is shorted with the backside of IC chip therefore it should be connected to GND. Be aware that there is a possibility of malfunction or destruction if it is shorted with any potential other than GND.

(6) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions. Users should be aware that this series has been designed to expose their frames at the back of the package, and should be used with suitable heat dissipation treatment in this area to improve dissipation. As large a dissipation pattern should be taken as possible, not only on the front of the baseboard but also on the back surface.

(7) Mounting errors and inter-pin shorts

When attaching to a printed circuit board, pay close attention to the direction of the IC and displacement. Improper attachment may lead to destruction of the IC. There is also possibility of destruction from short circuits which can be caused by foreign matter entering between outputs or an output and the power supply or GND.

(8) Operation in a strong electric field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

(9) ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

(10) Thermal shutdown circuit

The IC has a built-in thermal shutdown circuit (TSD circuit). If the chip temperature becomes T_{jmax} =150°C, and higher, coil output to the motor will be open. The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect or indemnify peripheral equipment. Do not use the TSD function to protect peripheral equipment.

TSD on temperature [°C] (Typ.)	Hysteresis Temperature [°C] (Typ.)
175	25

(11) Inspection of the application board

During inspection of the application board, if a capacitor is connected to a pin with low impedance there is a possibility that it could cause stress to the IC, therefore an electrical discharge should be performed after each process. Also, as a measure again electrostatic discharge, it should be earthed during the assembly process and special care should be taken during transport or storage. Furthermore, when connecting to the jig during the inspection process, the power supply should first be turned off and then removed before the inspection.

(12) Input terminal of IC

This IC is a monolithic IC, and between each element there is a P+ isolation for element partition and a P substrate. This P layer and each element's N layer make up the P-N junction, and various parasitic elements are made up. For example, when the resistance and transistor are connected to the terminal as shown in figure 18,

○When GND＞(Terminal A) at the resistance and GND＞(Terminal B) at the transistor (NPN), the P-N junction operates as a parasitic diode.

○Also, when GND＞(Terminal B) at the transistor (NPN) The parasitic NPN transistor operates with the N layers of other elements close to the aforementioned parasitic diode.

Because of the IC's structure, the creation of parasitic elements is inevitable from the electrical potential relationship. The operation of parasitic elements causes interference in circuit operation, and can lead to malfunction and destruction. Therefore, be careful not to use it in a way which causes the parasitic elements to operate, such as by applying voltage that is lower than the GND (P substrate) to the input terminal.

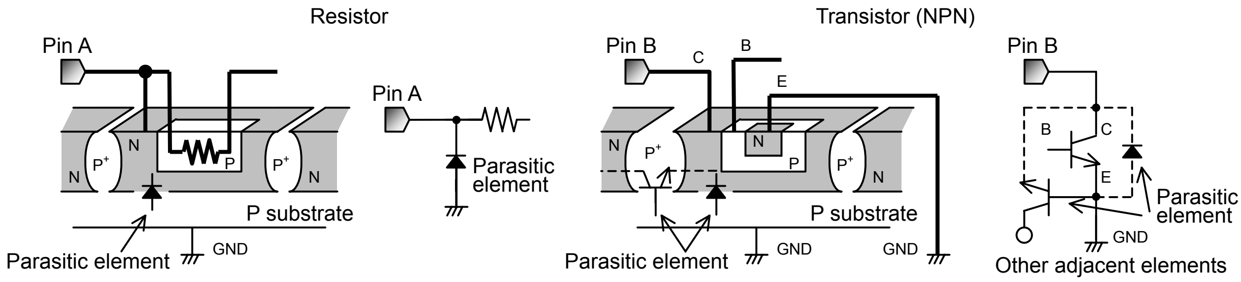


Fig.18 Pattern Diagram of Parasitic Element

(13) Ground Wiring Patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern potential of any external components, either.

(14) TEST Terminal

Be sure to connect TEST pin to GND.

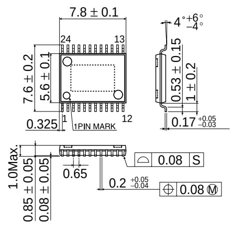
● Selecting a model name when ordering

B	D		6	3	9	X	2		E	F	V	–	E	2

ROHM model — Part number — Package type EFV=HTSSOP-B24 — E2 = Reel-wound embossed taping

HTSSOP-B24

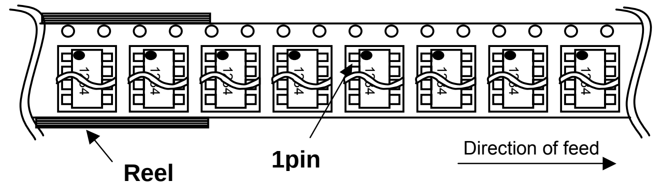
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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Should you intend to use these products with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.

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