

DACs for Electronic Adjustment

High-precision 10bit 4ch/6ch D/A Converters



BU2508FV, BU2507FV

No.11052ECT02

Description

BU2508FV and BU2507FV ICs are high performance 10bit R-2R-type DACs with 4ch and 6ch outputs, respectively. Each channel incorporates a full swing output-type buffer amplifier with high speed output response characteristics, resulting in a greatly shortened wait time. The ICs also utilize the TTL level input method.

Features

- 1) High performance, multi-channels R-2R-type 10bit D/A converter built-in (BU2508FV: 4 channels, BU2507FV: 6 channels)
- 2) Full swing output type buffer amplifier incorporated at each output channel
- 3) The RESET terminal can keep the voltage of all channels within the lower reference voltage range
- 4) Digital input compatible with TTL levels
- 5) 14bit 3-line serial data + RESET signal input (address 4bit + data 10bit)
- 6) Compact package: 14 pins, 0.65mm pitch (SSOP-B14)

Applications

DVDs, CD-Rs, CD-RWs, digital cameras

Lineup

Parameter	BU2507FV	BU2508FV
Power source voltage range	4.5 to 5.5V	4.5 to 5.5V
Number of channels	6ch	4ch
Differential non linearity error	±1.0LSB	±1.0LSB
Integral non linearity error	±3.5LSB	±3.5LSB
Data transfer frequency	10MHz	10MHz
Package	SSOP-B14	SSOP-B14

■Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Ratings	Unit
Power source voltage	VCC	-0.3 to 6.0	V
D/A converter upper standard voltage	VDD	-0.3 to 6.0	V
Input voltage	VIN	-0.3 to 6.0	V
Output voltage	VOUT	-0.3 to 6.0	V
Storage temperature range	Tstg	-55 to 125	°C
Power dissipation	Pd	350 [*]	mW

Derated at 3.5mW/°C at Ta>25°C, mounted on a 70x70x1.6mm FR4 glass epoxy board (copper foil area less than 3%)

Note: These products are not robust against radiation

■ Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage range	VCC	4.5 to 5.5	V
Operating temperature range	Topr	-30 to 85	°C

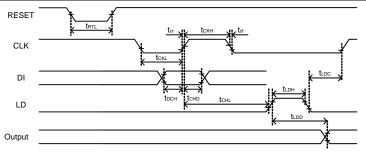
● Electrical Characteristics (Unless otherwise specified, VCC=5V, VrefH=5V, VrefL=0V, Ta=25°C)

	Daramatar	Symbol		Limits		Unit	Conditions	
	Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Conditions	
<digital td="" un<=""><td>it></td><td></td><td></td><td></td><td></td><td></td><td></td></digital>	it>							
Power sou	urce current	ICC	-	0.85	2.8	mA	At CLK = 10MHz, IAO = 0uA	
Input leak	current	IILK	-5	-	5	μA	VIN=0 to VCC	
Input volta	age L	VIL	-	-	0.8	V	-	
Input volta	age H	VIH	2.0	-	-	V	-	
Output vo	Itage L	VOL	0	-	0.4	V	IOL=2.5mA	
Output vo	Itage H	VOH	4.6	-	5	V	IOH=-2.5mA	
<analog td="" u<=""><td>nit></td><td></td><td></td><td></td><td></td><td></td><td></td></analog>	nit>							
C = 12 = 11 = 12	tion or mont	lundi i	-	4.5	7.5	mA	Data and distance at many insures assured	
Consump	tion current	IrefH	-	2.0	3.4	mA ^(*1)	Data condition : at maximum current	
D/A converter upper standard voltage setting range		VrefH	3.0	-	5	V	Outputs does not necessarily take a value in standard voltage setting range.	
D/A conve setting rar	erter lower standard voltage	VrefL	0	-	1.5	V	Value that output may take is in the buffer amplifier output voltage range (VO).	
Duffer om	plifier output voltage range	VO	0.1	-	4.9	V	IO=±100μA	
bullet atti	piller output voltage range	VO	0.2	-	4.75	V	IO=±1.0mA	
Buffer amplifier output drive range		Ю	-2	-	2	mA	Upper side saturation voltage =0.35V (on full scale setting, current sourcing) Lower side saturation voltage =0.23V (on zero scale setting, current sinking)	
	Differential non-linearity error	DNL INL	-1.0	-	1.0	LSB	VrefH =4.796V	
Precision	Precision Integral non-linearity error		-3.5	-	3.5	LOD	VrefL=0.7V	
Zero point error		SZERO	-25	-	25	mV	VCC=5.5V (4mV/LSB)	
Full scale error		SFULL	-25	-	25	111.4	No load (IO = +0mA)	
Buffer am	Buffer amplifier output impedance		-	5	15	Ω	-	
Pull-up I/C	D internal resistance value	Rup	12.5	25	37.5	kΩ	Input voltage 0V (Resistance value changes according to voltage to be impressed.)	

^{*1:} Value in the case where CH1 ~ CH4 are set to maximum current (after reset)

● Timing Characteristics (Unless otherwise specified, VCC=5V, VrefH=5V, VrefL=0V, Ta=25°C)

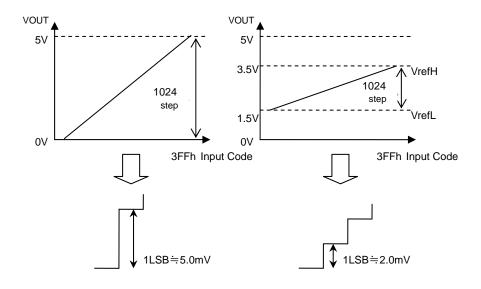
Parameter	Cumbal		Limits		Unit	Conditions
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Judgment level is 80% / 20% of VCC.
Reset L pulse width	tRTL	50	-	-		-
Clock L pulse width	tCKL	50	-	-		-
Clock H pulse width	tCKH	50	-	-		-
Clock rise time	tcr	-	-	50		-
Clock fall time	tcf	-	-	50	nS	-
Data setup time	tDCH	20	-	-	113	-
Data hold time	tCHD	40	-	-		-
Load setup time	tCHL	50	-	-		-
Load hold time	tLDC	50	-	-		-
Load H pulse width	tLDH	50	-	-		-
DA output settling time	tLDD	-	7	20	μS	CL≦100pF, VO:0.5V⇔4.5V . Until output value deference from final value becomes 1/2LSB



(note) LD signal is level triggered. When LD input is on H level, internal shift-register state is loaded to DAC control latch. Clock transition during LD=H is inhibited.

● DAC Variable Output Range Function

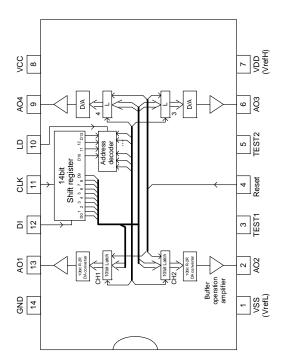
With the variable output range function, the upper / lower limits of the output voltage as well as the power supply voltage can be set. The upper limit value setting terminal VrefH is used as the power supply terminal, while the lower limit value setting terminal VrefL is used as the GND terminal (1LSB = 5mV). In the example below, VrefH = 3.5V / VrefL = 1.5V. Further adjustments can be made in order to achieve greater accuracy (1LSB = 2mV).



Block Diagrams

BU2507FV

BU2508FV

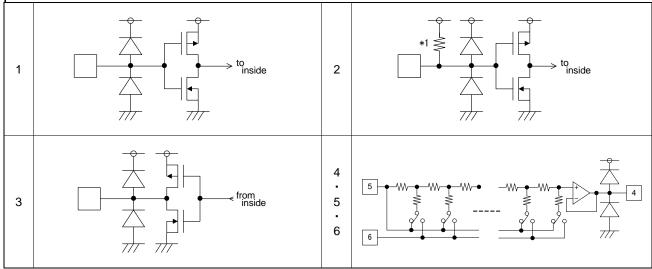


●Terminal Description

<u> </u>	Description				
No	Terminal name	Analog / Digital	I/O	Description of terminal	Equivalent circuit
1	VSS	Analog	-	DA converter lower standard voltage (VrefL) input terminal	6
2	AO2	Analog	0	10bit D/A output (CH2)	4
3	AO3(TEST1)	Analog	0	10bit D/A output (CH3) (BU2508FV : test terminal)	4
4	Reset	Digital	I	All ch analog output L fixed	2
5	AO4(TEST2)	Digital	I	10bit D/A output (CH4) (BU2508FV : test terminal)	4
6	AO5 (AO3)	Analog	0	10bit D/A output (CH5) (BU2508FV : 10bit D/A output (CH3))	4
7	VDD	Analog	-	DA converter upper standard voltage (VrefH) input terminal	5
8	VCC	-	-	Power source terminal	-
9	AO6 (AO4)	Analog	0	10bit D/A output (CH6) (BU2508FV : 10bit D/A output (CH4))	4
10	LD	Digital	I	When High level is input to LD terminal, the value of 14bit shift register is loaded to decoder and D/A output register.	1
11	CLK	Digital	I	Shift clock input terminal. At rise of shift clock, the signal from DI terminal is input to 14bit shift register.	1
12	DI	Digital	I	Serial data input terminal. Serial data whose data length is 14bit (address 4bit + data 10bit) is input.	1
13	AO1	Analog	0	10bit D/A output (CH1)	4
14	GND	-	-	GND terminal	-

^{*}In the case of BU2508FV, be sure to open TEST1 and TEST2 terminals.

● Equivalent Circuits



^{*1:} $25k\Omega$ at Vcc = 5.0V (changes according to voltage supplied)

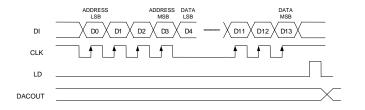
●Command Sending

1) In the case of BU2507FV

(1) Data format [data : LSB first]



(2) Data timing diagram



D3	D2	D1	D0	Address selection
0	0	0	0	Inconsequential
0	0	0	1	Inconsequential
0	0	1	0	AO1 selection
0	0	1	1	AO2 selection
0	1	0	0	Inconsequential
0	1	0	1	AO3 selection
0	1	1	0	AO4 selection
0	1	1	1	Inconsequential
1	0	0	0	AO5 selection
1	0	0	1	AO6 selection
1	0	1	0	Inconsequential
1	0	1	1	Inconsequential
1	1	0	0	Inconsequential
1	1	0	1	Inconsequential
1	1	1	0	Inconsequential
1	1	1	1	Inconsequential

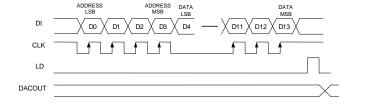
D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D/A output (VrefH=VDD, VrefL=VSS)
0	0	0	0	0	0	0	0	0	0	VrefL
0	0	0	0	0	0	0	0	0	1	(VrefH-VrefL)/1024×1+VrefL
0	0	0	0	0	0	0	0	1	0	(VrefH-VrefL)/1024x2+VrefL
0	0	0	0	0	0	0	0	1	1	(VrefH-VrefL)/1024x3+VrefL
:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	1	0	(VrefH-VrefL)/1024×1022+VrefL
1	1	1	1	1	1	1	1	1	1	(VrefH-VrefL)/1024×1023+VrefL

2) In the case of BU2508FV

(1) Data format [Data: LSB first]

	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ŀ)/A conver	ter output s	etting DAT	Ά				- а	ddress sele	ect —	*

(2) Data timing diagram



D3	D2	D1	D0	Address selection
0	0	0	0	Don't Care
0	0	0	1	Don't Care
0	0	1	0	AO1 selection
0	0	1	1	AO2 selection
0	1	0	0	Don't Care
0	1	0	1	Don't Care
0	1	1	0	Don't Care
0	1	1	1	Don't Care
1	0	0	0	AO3 selection
1	0	0	1	AO4 selection
1	0	1	0	Don't Care
1	0	1	1	Don't Care
1	1	0	0	Don't Care
1	1	0	1	Don't Care
1	1	1	0	Don't Care
1	1	1	1	Don't Care

D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D/A output (VrefH=VDD, VrefL=VSS)
0	0	0	0	0	0	0	0	0	0	VrefL
0	0	0	0	0	0	0	0	0	1	(VrefH-VrefL)/1024×1+VrefL
0	0	0	0	0	0	0	0	1	0	(VrefH-VrefL)/1024x2+VrefL
0	0	0	0	0	0	0	0	1	1	(VrefH-VrefL)/1024x3+VrefL
:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	1	0	(VrefH-VrefL)/1024×1022+VrefL
1	1	1	1	1	1	1	1	1	1	(VrefH-VrefL)/1024×1023+VrefL

Electrical Characteristics Curves

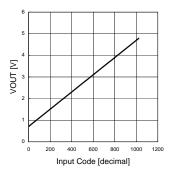


Fig.1 Output voltage linearity (-30°C)

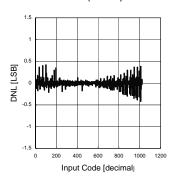


Fig.4 Differential linearity error (-30°C)

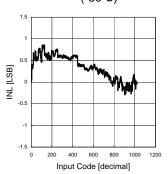


Fig.7 Integral linearity error (-30°C)

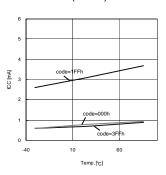


Fig.10 Circuit current temperature characteristic

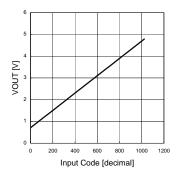


Fig.2 Output voltage linearity (25°C)

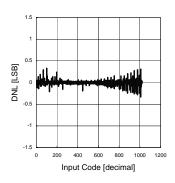


Fig.5 Differential linearity error (25°C)

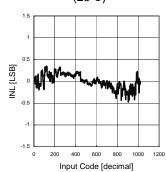


Fig.8 Integral linearity error (25°C)

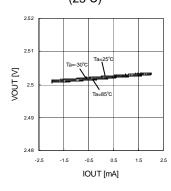


Fig.11 Output load fluctuation characteristic (input code : 1FFh)

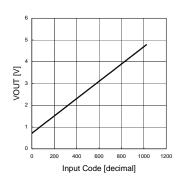


Fig.3 Output voltage linearity (85°C)

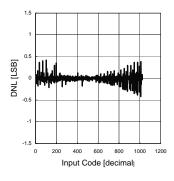


Fig.6 Differential linearity error (85°C)

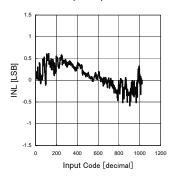


Fig.9 Integral linearity error (85°C)

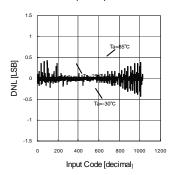
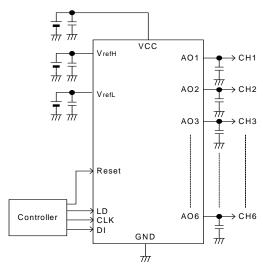


Fig.12 Pull-up built in resistance characteristic

Standard Example Application Circuit



Notes for use

- (1) The electrical characteristic and data on graphs for this datasheet, are typically evaluated value, and not guaranteed.
- (2) We suppose that application circuits are recommendable, but please make sufficient check for characteristics with the actual application. In case that value of external component for this IC is changed, please check characteristic, not only static but also transient.
- (3) About absolute maximum ratings

If operation condition is over the absolute maximum ratings, supply voltage or other operation range, IC will be broken. Please don't apply any voltage or temperature over the absolute maximum ratings. If application have possibilities of become over the absolute maximum ratings, please take safety measures by using fuse and so on. Not to over absolute maximum ratings of IC.

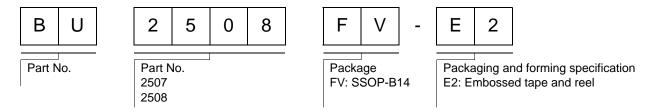
- (4) GND voltage
 - Please keep GND voltage lowest of any other terminal of this IC. Please confirm other terminal voltages is not lower than GND.
- (5) Thermal design

Please making a thermal design that allows for a sufficient margin in light of the power dissipation in actual operating condition.

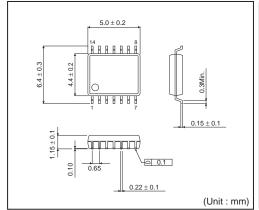
- (6) About terminals short and wrong mounting
 - Please pay full attention to the IC direction and displacement when mounting IC on PCB. If you assemble them by mistake and electrify it, IC might be destroyed. And it is happen to short among IC terminals or terminals and power supply, by foreign substance.
- (7) About operation in strong electromagnetic field

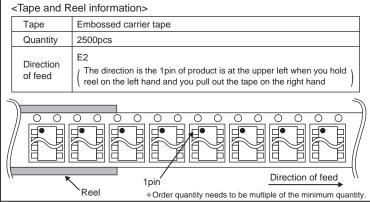
 If you use it in strong electromagnetic field, please evaluate fully as there is a possibility of malfunction.
- (8) Place a bypass capacitor as close as possible between each power supply terminal and ground in order to prevent deterioration of the D/A conversion accuracy due to ripple and noise signals from power supply or GND.
- (9) A capacitor should be inserted between the analog output and ground in order to eliminate noise. A capacitance up to 100pF is recommended (including the capacitance of the wire).

Ordering part number



SSOP-B14





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JAPAN	USA	EU	CHINA	
CLASSⅢ	CLASSⅢ	CLASS II b	CLASSIII	
CLASSIV	CLASSIII	CLASSⅢ		

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 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
- 4. The Products are not subject to radiation-proof design.
- 5. Please verify and confirm characteristics of the final or mounted products in using the Products.
- 6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- 7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- 8. Confirm that operation temperature is within the specified range described in the product specification.
- 9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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- 1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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- Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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