SII

S-89430/89431 Series

MINI ANALOG SERIES
0.5 μA Rail-to-Rail CMOS OPERATIONAL AMPLIFIER

www.sii-ic.com

Rev.2.1_01

The mini-analog series is a group of ICs that incorporate a general purpose analog circuit in a small package.
The S-89430/89431 Series is a CMOS type operational amplifier that feature Rail-to-Rail*1 I/O and an internal phase compensation circuit, and operates at a lower voltage with lower current consumption. These features make this product the ideal solution for small battery-powered portable equipment.
These features enable driving at a lower voltage (from 0.9 V) and with lower current consumption (0.5 μA).
The S-89430A/89431A Series is a single operational amplifier (one circuit).
The S-89430B/89431B Series is a dual operational amplifier (two circuits).

***1.** Rail-to-Rail is a trademark of Motorola, Inc.

■ Features

- Lower operating voltage than the conventional general-purpose: V_{DD} = 0.9 V to 5.5 V
- Low current consumption (per circuit): I_{DD} = 0.5 μA Typ.
- Wide I/O voltage range (Rail-to-Rail): V_{CMR} = V_{SS} to V_{DD}
- Low input offset voltage: V_{IO} = 10.0 mV Max. (S-89430 Series)
  V_{IO} = 5.0 mV Max. (S-89431 Series)
- No external capacitors required for internal phase compensation
- Lead-free, Sn 100%, halogen-free*1

***1.** Refer to "**■ Product Name Structure**" for details.

■ Applications

- Mobile phone
- Notebook PC
- Digital camera
- Digital video camera

■ Packages

- SC-88A
- SOT-23-5
- SNT-8A
- TMSOP-8

■ Block Diagrams

1. S-89430A/89431A Series single operational amplifier (one circuit)

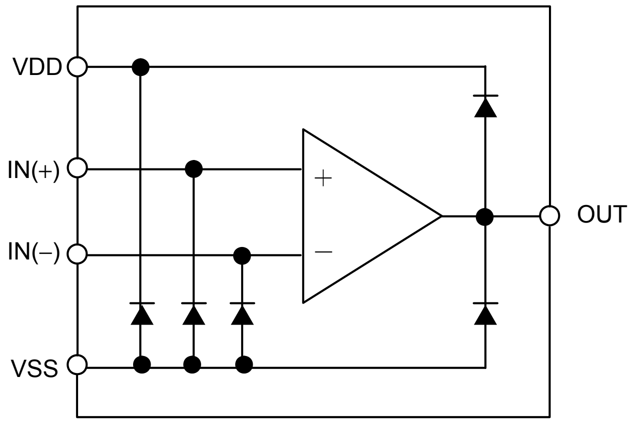


Figure 1

2. S-89430B/89431B Series dual operational amplifier (two circuits)

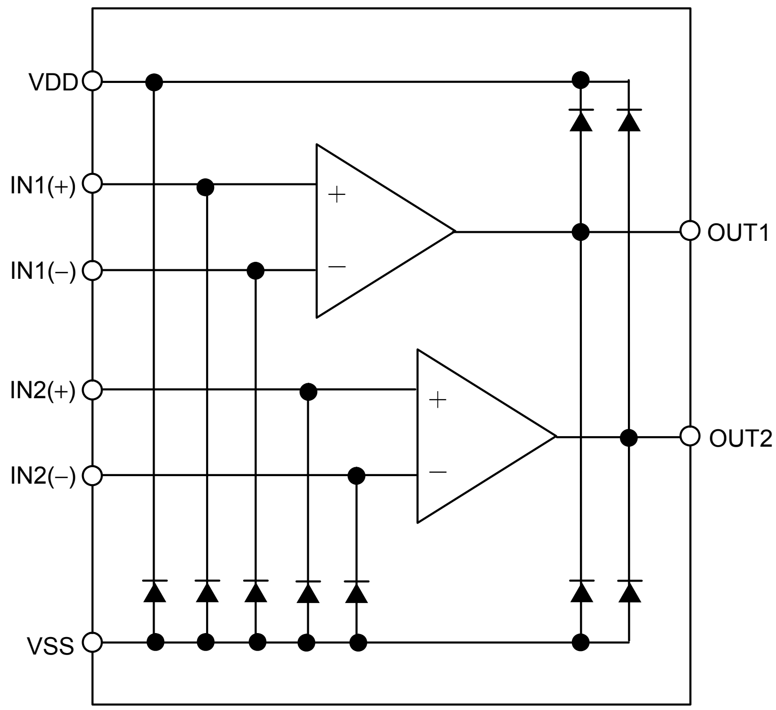


Figure 2

■ Product Name Structure

Users can select the product type for the S-89430/89431 Series. Refer to "**1. Product name**" regarding the contents of product name, "**2. Packages**" regarding the package drawings and "**3. Product name list**" regarding the product type.

1. Product name

(1) SC-88A

S-8943 x A C NC - xxx TF x

- x (last): Environmental code
  - S: Lead-free, halogen-free
  - G: Lead-free (for details, please contact our sales office)
- TF: IC direction in tape specifications*1
- xxx: Product code (abbreviation)*2
- NC: Package name (abbreviation)
  - NC: SC-88A
- A: Number of circuits
  - A: 1
- x (first): Input offset voltage
  - 0: V_{IO} = 10.0 mV Max.
  - 1: V_{IO} = 5.0 mV Max.

***1.** Refer to the tape drawing.
***2.** Refer to **"3. Product name list"**.

(2) SOT-23-5

S-8943 x A C MC - xxx T2 x

- x: Environmental code
  - U: Lead-free (Sn 100%), halogen-free
  - G: Lead-free (for details, please contact our sales office)
- T2: IC direction in tape specifications*1
- xxx: Product code (abbreviation)*2
- MC: Package name (abbreviation)
  - MC: SOT-23-5
- A: Number of circuits
  - A: 1
- x: Input offset voltage
  - 0: V_{IO} = 10.0 mV Max.
  - 1: V_{IO} = 5.0 mV Max.

***1.** Refer to the tape drawing.
***2.** Refer to **"3. Product name list"**.

(3) SNT-8A, TMSOP-8

S-8943 x B C xx - xxx TF U

- U: Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- TF: IC direction in tape specifications*1
- xxx: Product code (abbreviation)*2
- xx: Package name (abbreviation)
  - PH: SNT-8A
  - FM: TMSOP-8
- B: Number of circuits
  - B: 2
- x: Input offset voltage
  - 0: V_{IO} = 10.0 mV Max.
  - 1: V_{IO} = 5.0 mV Max.

***1.** Refer to the tape drawing.
***2.** Refer to **"3. Product name list"**.

2. Packages

Package Name	Drawing Code			
	Package	Tape	Reel	Land
SC-88A	NP005-B-P-SD	NP005-B-C-SD	NP005-B-R-SD	–
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD	–
SNT-8A	PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD	–

3. Product name list

Table 1

Product name	Input offset voltage	Number of circuits	Package
S-89430ACNC-HBUTFz	10 mV Max.	1	SC-88A
S-89430ACMC-HBUT2x	10 mV Max.	1	SOT-23-5
S-89430BCPH-H4CTFU	10 mV Max.	2	SNT-8A
S-89430BCFM-H4CTFU	10 mV Max.	2	TMSOP-8
S-89431ACNC-HBVTFz	5 mV Max.	1	SC-88A
S-89431ACMC-HBVT2x	5 mV Max.	1	SOT-23-5
S-89431BCPH-H4DTFU	5 mV Max.	2	SNT-8A
S-89431BCFM-H4DTFU	5 mV Max.	2	TMSOP-8

Remark 1. x: G or U
2. z: G or S
3. Please select products of environmental code = U for Sn 100%, halogen-free products.

■ Pin Configurations

1. SC-88A

Top view

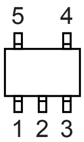


Figure 3

Table 2

(Product with 1 circuit)

Pin No.	Symbol	Description
1	IN(+)	Non-inverted input pin
2	VSS	GND pin
3	IN(−)	Inverted input pin
4	OUT	Output pin
5	VDD	Positive power supply pin

2. SOT-23-5

Top view

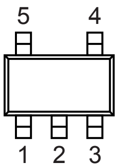


Figure 4

Table 3

(Product with 1 circuit)

Pin No.	Symbol	Description
1	IN(+)	Non-inverted input pin
2	VSS	GND pin
3	IN(−)	Inverted input pin
4	OUT	Output pin
5	VDD	Positive power supply pin

3. SNT-8A

Top view

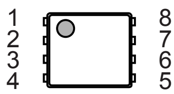


Figure 5

Table 4

(Product with 2 circuits)

Pin No.	Symbol	Description
1	OUT1	Output pin 1
2	IN1(−)	Inverted input pin 1
3	IN1(+)	Non-inverted input pin 1
4	VSS	GND pin
5	IN2(+)	Non-inverted input pin 2
6	IN2(−)	Inverted input pin 2
7	OUT2	Output pin 2
8	VDD	Positive power supply pin

4. TMSOP-8

Top view

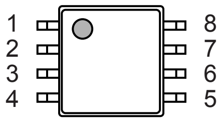


Figure 6

Table 5

(Product with 2 circuits)

Pin No.	Symbol	Description
1	OUT1	Output pin 1
2	IN1(−)	Inverted input pin 1
3	IN1(+)	Non-inverted input pin 1
4	VSS	GND pin
5	IN2(+)	Non-inverted input pin 2
6	IN2(−)	Inverted input pin 2
7	OUT2	Output pin 2
8	VDD	Positive power supply pin

■ Absolute Maximum Ratings

Table 6

(Ta = +25°C unless otherwise specified)

Parameter		Symbol	Absolute Maximum Rating	Unit
Power supply voltage		V_{DD}	V_{SS} − 0.3 to V_{SS} + 7.0	V
Input voltage		V_{IN}	V_{SS} − 0.3 to V_{SS} + 7.0 (7.0 Max.)	V
Output voltage		V_{OUT}	V_{SS} − 0.3 to V_{DD} + 0.3 (7.0 Max.)	V
Differential input voltage		V_{IND}	±5.5	V
Output pin current		I_{SOURCE}	7.0	mA
		I_{SINK}	7.0	mA
Power dissipation	SC-88A	P_D	350*1	mW
	SOT-23-5		600*1	mW
	SNT-8A		450*1	mW
	TMSOP-8		650*1	mW
Operating ambient temperature		T_{opr}	−40 to +85	°C
Storage temperature		T_{stg}	−55 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

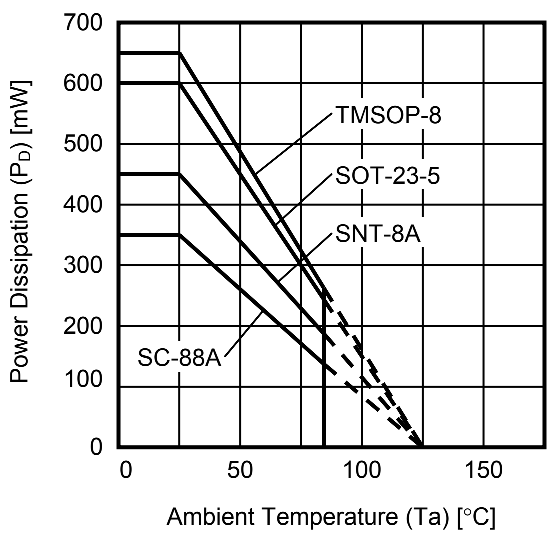


Figure 7 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

Table 7

(Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
Range of operating power supply voltage	V_{DD}	–	0.9	–	5.5	V	–

1. V_{DD} = 3.0 V

Table 8

DC Electrical Characteristics (V_{DD} = 3.0 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test Circuit
Current consumption (per circuit)*1	I_{DD}	V_{CMR} = V_{OUT} = 1.5 V		–	0.50	0.75	μA	6
Input offset voltage	V_{IO}	V_{CMR} = 1.5 V	S-89430 Series	−10	±5	+10	mV	2
			S-89431 Series	−5	±3	+5	mV	2
Input offset current	I_{IO}	–		–	1	–	pA	–
Input bias current	I_{BIAS}	–		–	1	–	pA	–
Common-mode input voltage range	V_{CMR}	–		0	–	3	V	3
Voltage gain (open loop)	A_{VOL}	V_{SS} + 0.1 V ≤ V_{OUT} ≤ V_{DD} − 0.1 V, V_{CMR} = 1.5 V, R_L = 1.0 MΩ		70	80	–	dB	9
Maximum output swing voltage	V_{OH}	R_L = 100 kΩ		2.95	–	–	V	4
	V_{OL}	R_L = 100 kΩ		–	–	0.05	V	5
Common-mode input signal rejection ratio	CMRR	V_{SS} ≤ V_{CMR} ≤ V_{DD}		45	65	–	dB	3
Power supply voltage rejection ratio	PSRR	V_{DD} = 0.9 V to 5.5 V		70	80	–	dB	1
Source current	I_{SOURCE}	V_{OUT} = V_{DD} − 0.1 V		400	500	–	μA	7
		V_{OUT} = 0 V		4800	6000	–	μA	7
Sink current	I_{SINK}	V_{OUT} = 0.1 V		400	550	–	μA	8
		V_{OUT} = V_{DD}		4800	6000	–	μA	8

***1.** When the output is saturated on the V_{DD} side, a current consumption of up to 3 μA to 5 μA may flow.
Refer to "**4. Current consumption (per circuit) vs. Common-mode input voltage range characteristics (voltage follower configuration)**" in "**■ Characteristics (Typical Data)**".

Table 9

AC Electrical Characteristics (V_{DD} = 3.0 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Slew rate	SR	R_L = 1.0 MΩ, C_L = 15 pF (Refer to **Figure 17**)	–	5	–	V/ms
Gain-bandwidth product	GBP	C_L = 0 pF	–	4.8	–	kHz
Maximum load capacitance	C_L	–	–	47	–	pF

2. V_{DD} = 1.8 V

Table 10

DC Electrical Characteristics (V_{DD} = 1.8 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test Circuit
Current consumption (per circuit)*1	I_{DD}	V_{CMR} = V_{OUT} = 0.9 V		–	0.50	0.75	μA	6
Input offset voltage	V_{IO}	V_{CMR} = 0.9 V	S-89430 Series	–10	±5	+10	mV	2
			S-89431 Series	–5	±3	+5	mV	2
Input offset current	I_{IO}	–		–	1	–	pA	–
Input bias current	I_{BIAS}	–		–	1	–	pA	–
Common-mode input voltage range	V_{CMR}	–		0	–	1.8	V	3
Voltage gain (open loop)	A_{VOL}	V_{SS} + 0.1 V ≤ V_{OUT} ≤ V_{DD} – 0.1 V, V_{CMR} = 0.9 V, R_L = 1.0 MΩ		66	75	–	dB	9
Maximum output swing voltage	V_{OH}	R_L = 100 kΩ		1.75	–	–	V	4
	V_{OL}	R_L = 100 kΩ		–	–	0.05	V	5
Common-mode input signal rejection ratio	CMRR	V_{SS} ≤ V_{CMR} ≤ V_{DD}		35	55	–	dB	3
		V_{SS} ≤ V_{CMR} ≤ V_{DD} – 0.3 V		45	60	–	dB	3
Power supply voltage rejection ratio	PSRR	V_{DD} = 0.9 V to 5.5 V		70	80	–	dB	1
Source current	I_{SOURCE}	V_{OUT} = V_{DD} – 0.1 V		220	300	–	μA	7
		V_{OUT} = 0 V		1200	1800	–	μA	7
Sink current	I_{SINK}	V_{OUT} = 0.1 V		220	300	–	μA	8
		V_{OUT} = V_{DD}		1200	1800	–	μA	8

***1.** When the output is saturated on the V_{DD} side, a current consumption of up to 3 μA to 5 μA may flow.
Refer to "**4. Current consumption (per circuit) vs. Common-mode input voltage range characteristics (voltage follower configuration)**" in "**■ Characteristics (Typical Data)**".

Table 11

AC Electrical Characteristics (V_{DD} = 1.8 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Slew rate	SR	R_L = 1.0 MΩ, C_L = 15 pF (Refer to **Figure 17**)	–	4.5	–	V/ms
Gain-bandwidth product	GBP	C_L = 0 pF	–	5	–	kHz
Maximum load capacitance	C_L	–	–	47	–	pF

3. V_{DD} = 0.9 V

Table 12

DC Electrical Characteristics (V_{DD} = 0.9 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test Circuit
Current consumption (per circuit)*1	I_{DD}	V_{CMR} = V_{OUT} = 0.45 V		–	0.50	0.75	μA	6
Input offset voltage	V_{IO}	V_{CMR} = 0.45 V	S-89430 Series	–10	±5	+10	mV	2
			S-89431 Series	–5	±3	+5	mV	2
Input offset current	I_{IO}	–		–	1	–	pA	–
Input bias current	I_{BIAS}	–		–	1	–	pA	–
Common-mode input voltage range	V_{CMR}	–		0	–	0.9	V	3
Voltage gain (open loop)	A_{VOL}	V_{SS} + 0.1 V ≤ V_{OUT} ≤ V_{DD} – 0.1 V, V_{CMR} = 0.45 V, R_L = 1.0 MΩ		60	75	–	dB	9
Maximum output swing voltage	V_{OH}	R_L = 100 kΩ		0.85	–	–	V	4
	V_{OL}	R_L = 100 kΩ		–	–	0.05	V	5
Common-mode input signal rejection ratio	CMRR	V_{SS} ≤ V_{CMR} ≤ V_{DD}		25	55	–	dB	3
		V_{SS} ≤ V_{CMR} ≤ V_{DD} – 0.35 V		40	60	–	dB	3
Power supply voltage rejection ratio	PSRR	V_{DD} = 0.9 V to 5.5 V		70	80	–	dB	1
Source current	I_{SOURCE}	V_{OUT} = V_{DD} – 0.1 V		25	65	–	μA	7
		V_{OUT} = 0 V		40	140	–	μA	7
Sink current	I_{SINK}	V_{OUT} = 0.1 V		10	65	–	μA	8
		V_{OUT} = V_{DD}		12	120	–	μA	8

***1.** When the output is saturated on the V_{DD} side, a current consumption of up to 3 μA to 5 μA may flow.
Refer to "**4. Current consumption (per circuit) vs. Common-mode input voltage range characteristics (voltage follower configuration)**" in "**■ Characteristics (Typical Data)**".

Table 13

AC Electrical Characteristics (V_{DD} = 0.9 V) (Ta = +25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Slew rate	SR	R_L = 1.0 MΩ, C_L = 15 pF (Refer to **Figure 17**)	–	4	–	V/ms
Gain-bandwidth product	GBP	C_L = 0 pF	–	5	–	kHz
Maximum load capacitance	C_L	–	–	47	–	pF

■ Test Circuit (Per Circuit)

1. Power supply voltage rejection ratio

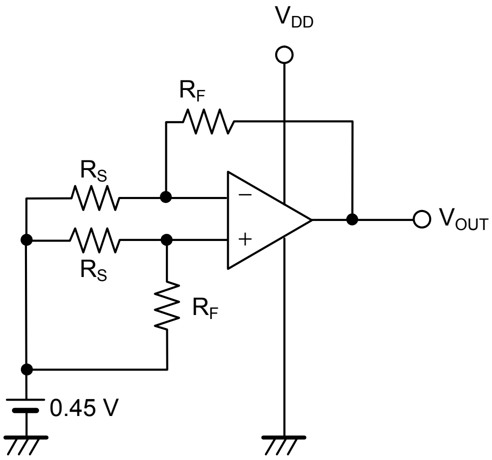


Figure 8

- **Power supply voltage rejection ratio (PSRR)**

  The power supply voltage rejection ratio (PSRR) can be calculated by the following expression, with V_{OUT} measured at each V_{DD}.

  Test conditions:
  When V_{DD} = 0.9 V: $V_{DD} = V_{DD1}$, $V_{OUT} = V_{OUT1}$,
  When V_{DD} = 5.5 V: $V_{DD} = V_{DD2}$, $V_{OUT} = V_{OUT2}$

$$PSRR = 20 \log \left(\left| \frac{V_{DD1} - V_{DD2}}{V_{OUT1} - V_{OUT2}} \right| \times \frac{R_F + R_S}{R_S} \right)$$

2. Input offset voltage

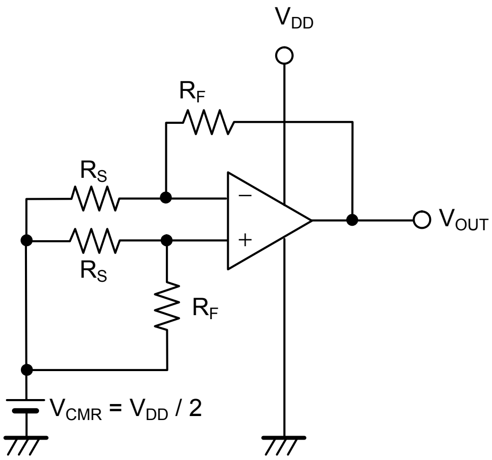


Figure 9

- **Input offset voltage (V_{IO})**

$$V_{IO} = \left(V_{OUT} - \frac{V_{DD}}{2} \right) \times \frac{R_S}{R_F + R_S}$$

3. Common-mode input signal rejection ratio, common-mode input voltage range

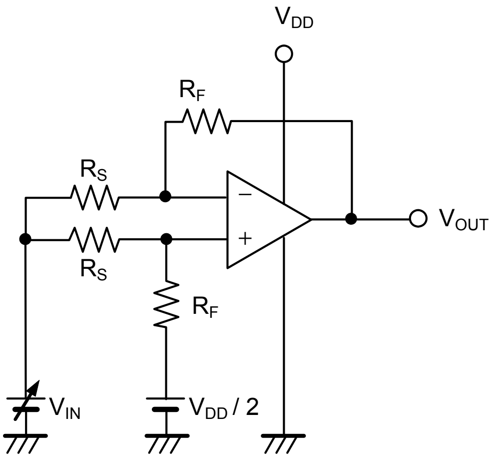


Figure 10

- **Common-mode input signal rejection ratio (CMRR)**

  The common-mode input signal rejection ratio (CMRR) can be calculated by the following expression, with V_{OUT} measured at each V_{IN}.

  Test conditions:
  When $V_{IN} = V_{CMR\ Max.}$: $V_{IN} = V_{IN1}$, $V_{OUT} = V_{OUT1}$,
  When $V_{IN} = V_{CMR\ Min.}$: $V_{IN} = V_{IN2}$, $V_{OUT} = V_{OUT2}$

  $$\mathrm{CMRR} = 20\log\left(\left|\frac{V_{IN1} - V_{IN2}}{V_{OUT1} - V_{OUT2}}\right| \times \frac{R_F + R_S}{R_S}\right)$$

- **Common-mode input voltage range (V_{CMR})**

  The common-mode input voltage range is the range of V_{IN} in which V_{OUT} satisfies the common-mode input signal rejection ratio specifications.

4. Maximum output swing voltage (V_{OH})

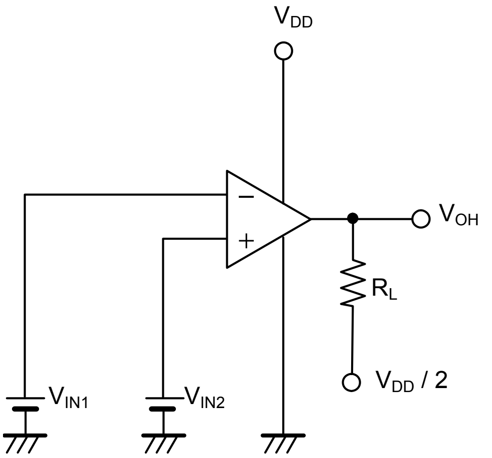


Figure 11

- **Maximum output swing voltage (V_{OH})**

  Test conditions:

  $V_{IN1} = \frac{V_{DD}}{2} - 0.1\ \mathrm{V}$

  $V_{IN2} = \frac{V_{DD}}{2} + 0.1\ \mathrm{V}$

  $R_L = 100\ \mathrm{k\Omega}$

5. Maximum output swing voltage (V_{OL})

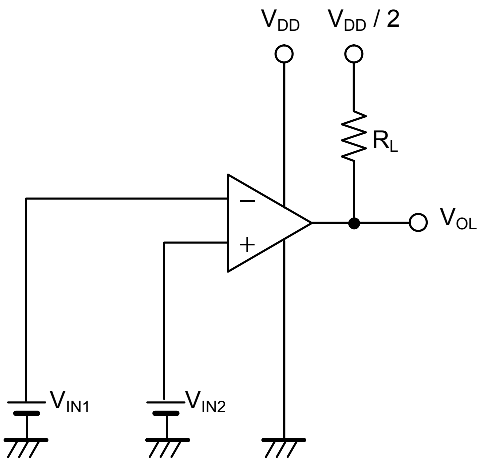


Figure 12

- **Maximum output swing voltage (V_{OL})**

  Test conditions:

  $V_{IN1} = \frac{V_{DD}}{2} + 0.1\ \mathrm{V}$

  $V_{IN2} = \frac{V_{DD}}{2} - 0.1\ \mathrm{V}$

  $R_L = 100\ \mathrm{k\Omega}$

6. Current consumption

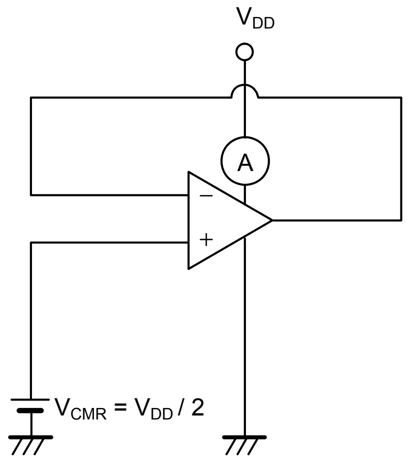


Figure 13

- **Current consumption (I_{DD})**

7. Source current

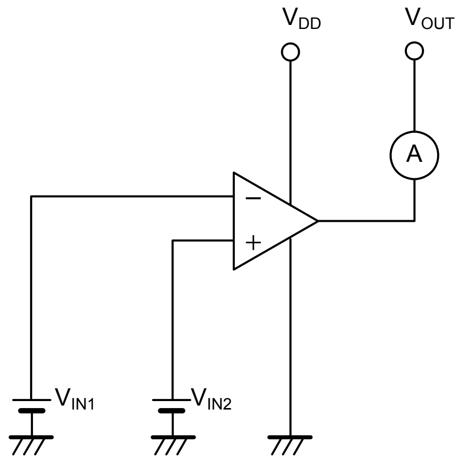


Figure 14

- **Source current (I_{SOURCE})**

Test conditions:
$V_{OUT} = V_{DD} - 0.1$ V or $V_{OUT} = 0$ V
$V_{IN1} = \frac{V_{DD}}{2} - 0.1$ V
$V_{IN2} = \frac{V_{DD}}{2} + 0.1$ V

8. Sink current

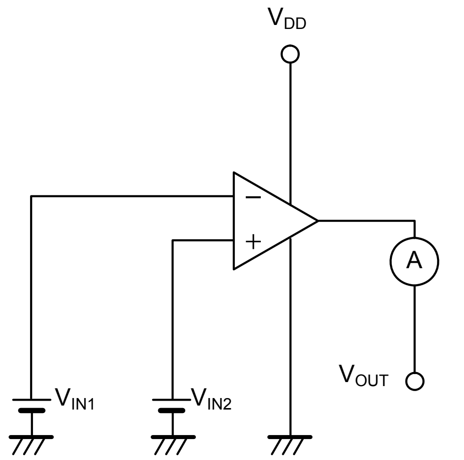


Figure 15

- **Sink current (I_{SINK})**

Test conditions:
$V_{OUT} = 0.1$ V or $V_{OUT} = V_{DD}$
$V_{IN1} = \frac{V_{DD}}{2} + 0.1$ V
$V_{IN2} = \frac{V_{DD}}{2} - 0.1$ V

9. Voltage gain (open loop)

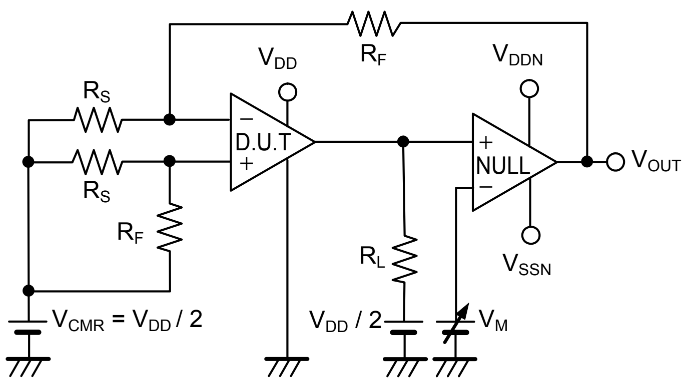


Figure 16

- **Voltage gain (open loop) (A_{VOL})**

  The voltage gain (A_{VOL}) can be calculated by the following expression, with V_{OUT} measured at each V_M.

  Test conditions:
  When $V_M = V_{DD} - 0.1$ V: $V_M = V_{M1}$, $V_{OUT} = V_{OUT1}$,
  When $V_M = V_{SS} - 0.1$ V: $V_M = V_{M2}$, $V_{OUT} = V_{OUT2}$
  $R_L = 1$ MΩ

$$A_{VOL} = 20 \log \left(\left| \frac{V_{M1} - V_{M2}}{V_{OUT1} - V_{OUT2}} \right| \times \frac{R_F + R_S}{R_S} \right)$$

10. Slew rate (SR)

Measured by the voltage follower circuit.

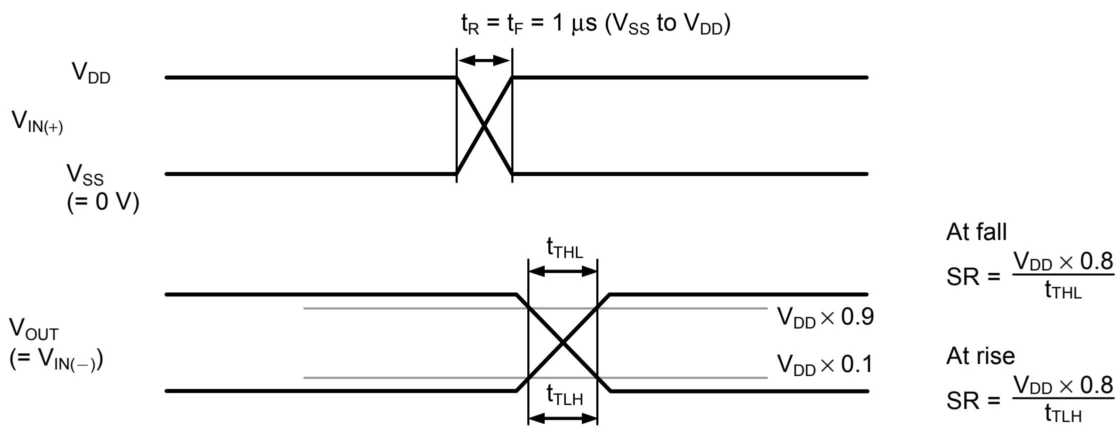


Figure 17

■ Precautions

- When the output is saturated on the V_{DD} side, a current consumption of up to 3 μA to 5 μA may flow.
  Refer to "**4. Current consumption (per circuit) vs. Common-mode input voltage range characteristics (voltage follower configuration)**" in "**■ Characteristics (Typical Data)**".

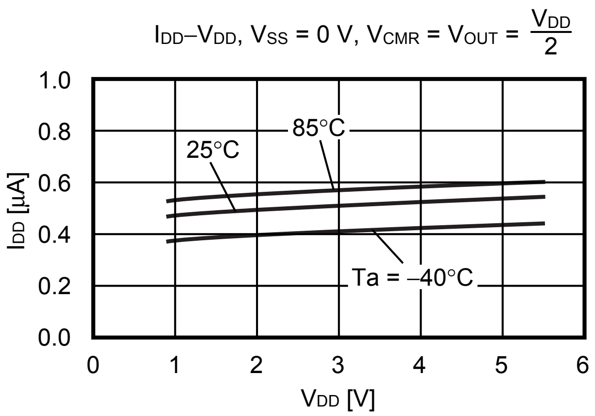
- Do not apply an electrostatic discharge to this IC that exceeds performance ratings of the built-in electrostatic protection circuit.

- Use this IC with the output current 7 mA or less.

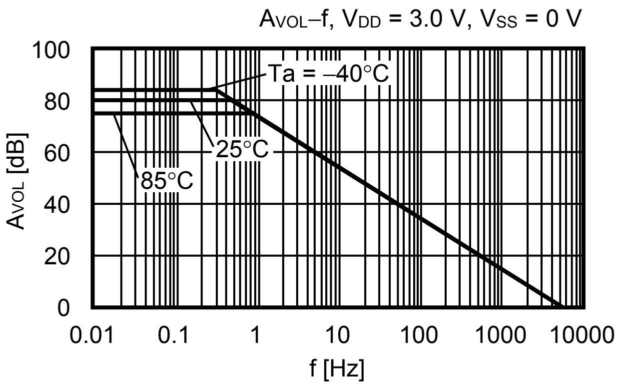
- SII Semiconductor Corporation claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

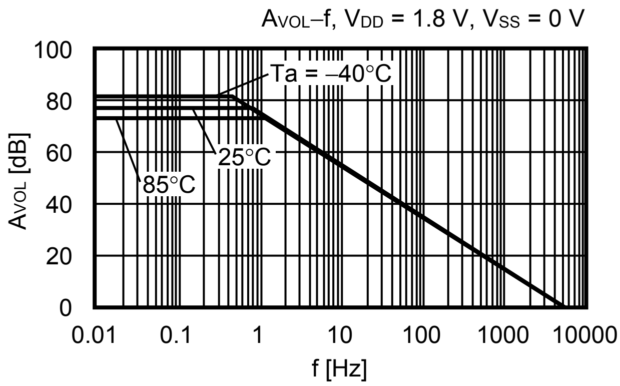
■ Characteristics (Typical Data)

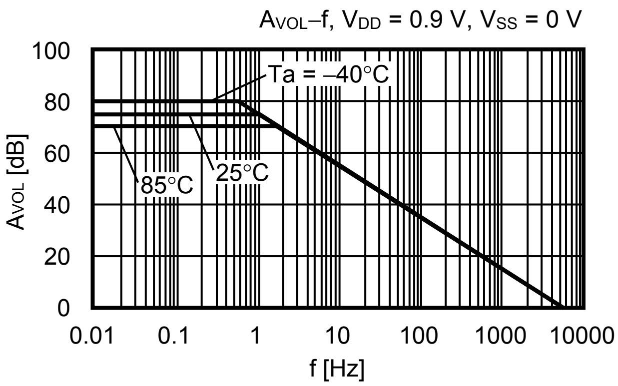
1. Current consumption (per circuit) vs. Power supply voltage



2. Voltage gain vs. Frequency

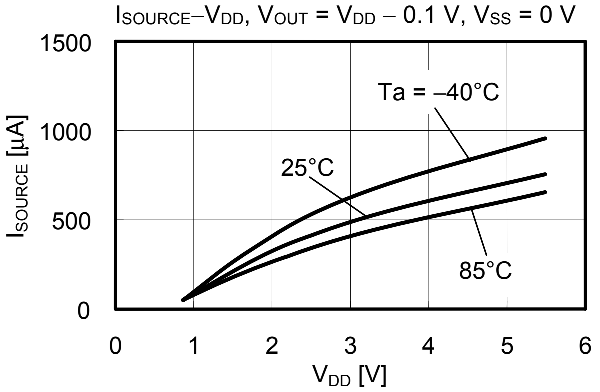




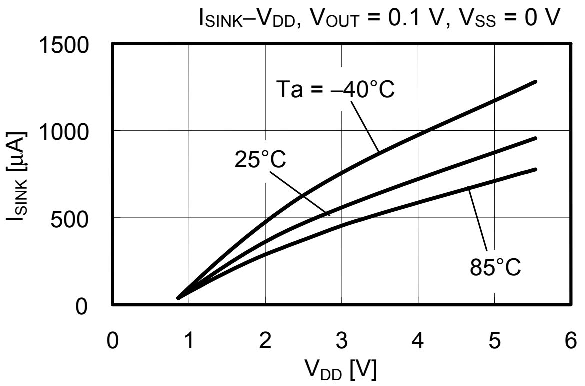


3. Output current

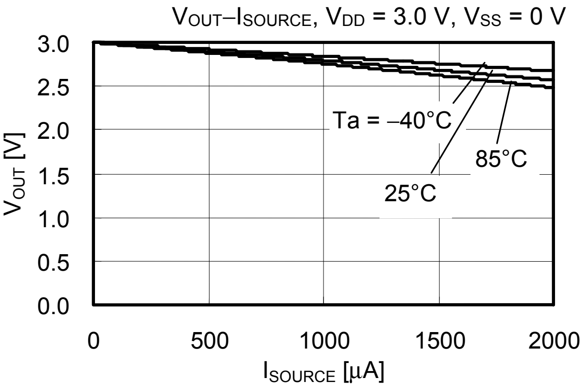
3. 1 I_{SOURCE} vs. Power supply voltage

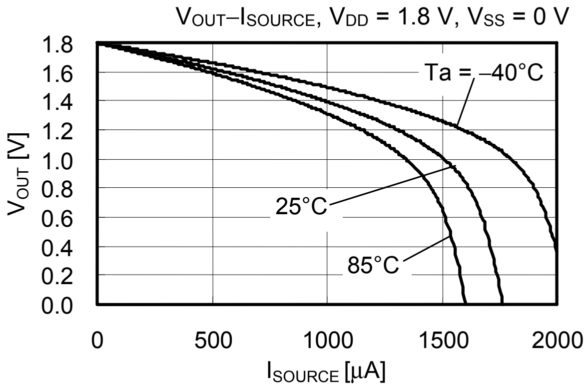


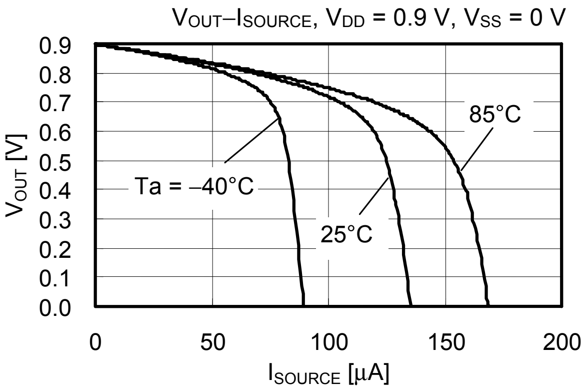
3. 2 I_{SINK} vs. Power supply voltage



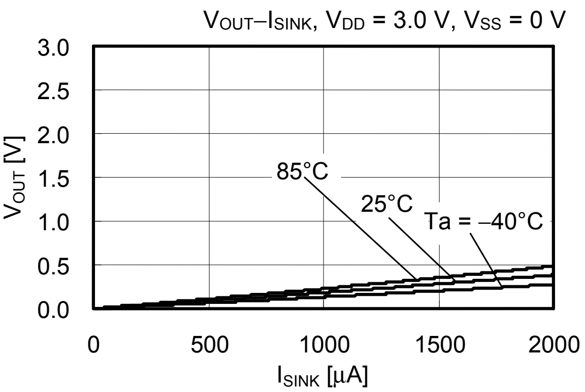
3. 3 Output voltage (V_{OUT}) vs. I_{SOURCE}

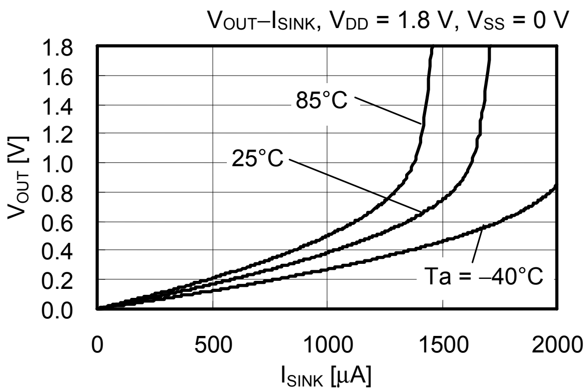


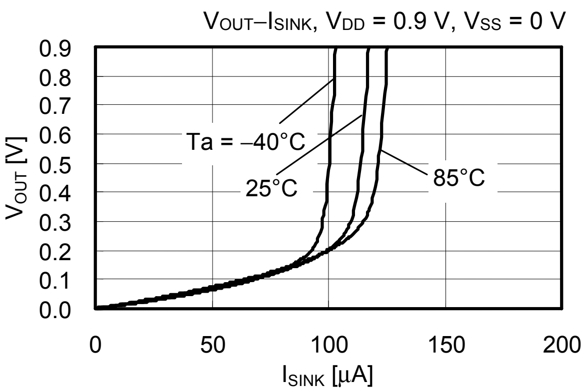




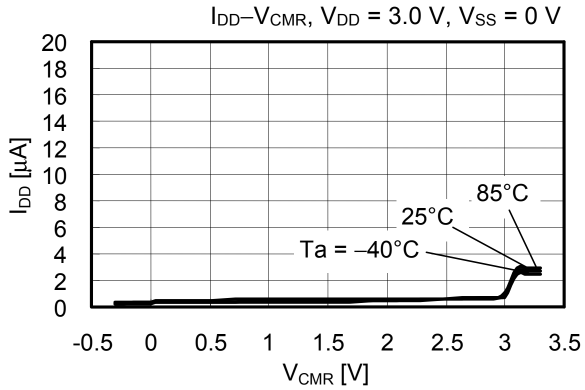
3. 4 Output voltage (V_{OUT}) vs. I_{SINK}

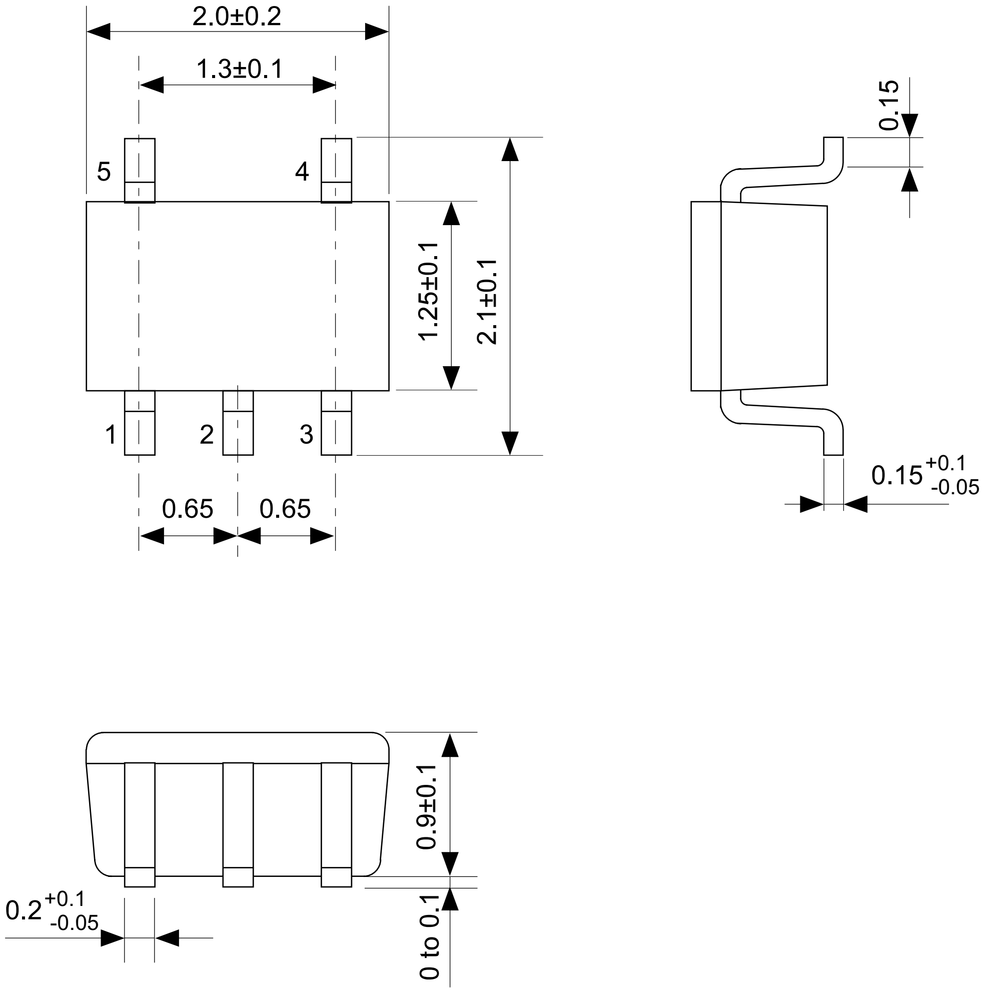






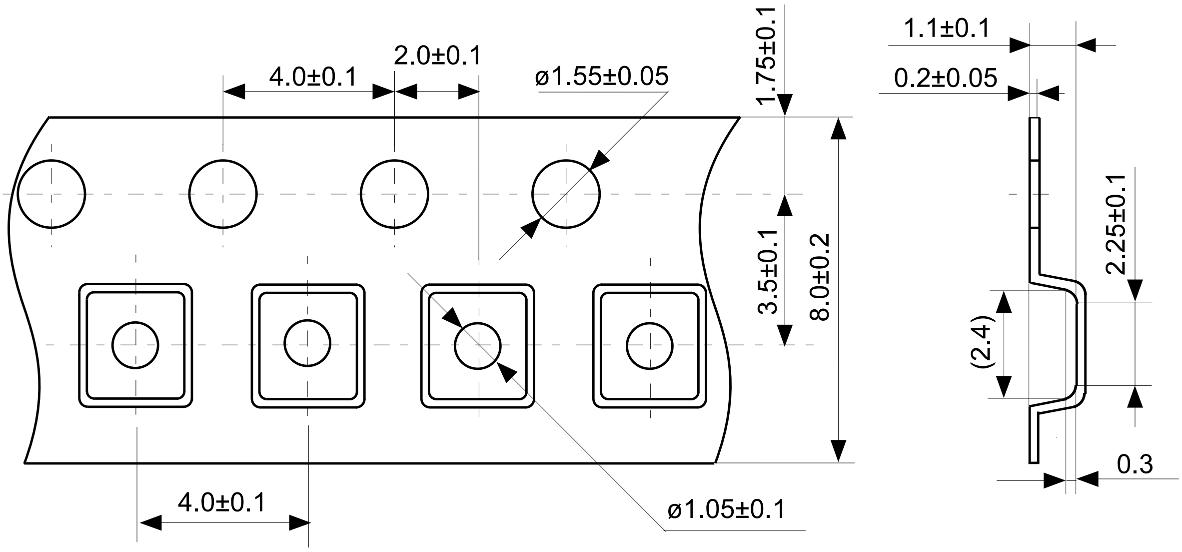
4. **Current consumption (per circuit) vs. Common-mode input voltage range (voltage follower configuration)**

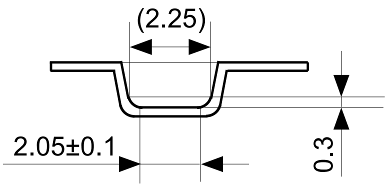


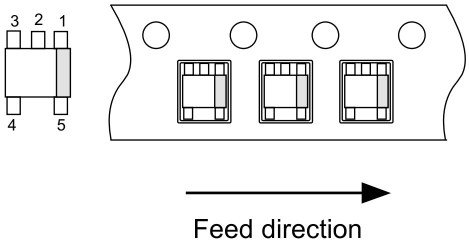


No. NP005-B-P-SD-1.1

TITLE	SC88A-B-PKG Dimensions
No.	NP005-B-P-SD-1.1
SCALE	
UNIT	mm
SII Semiconductor Corporation	



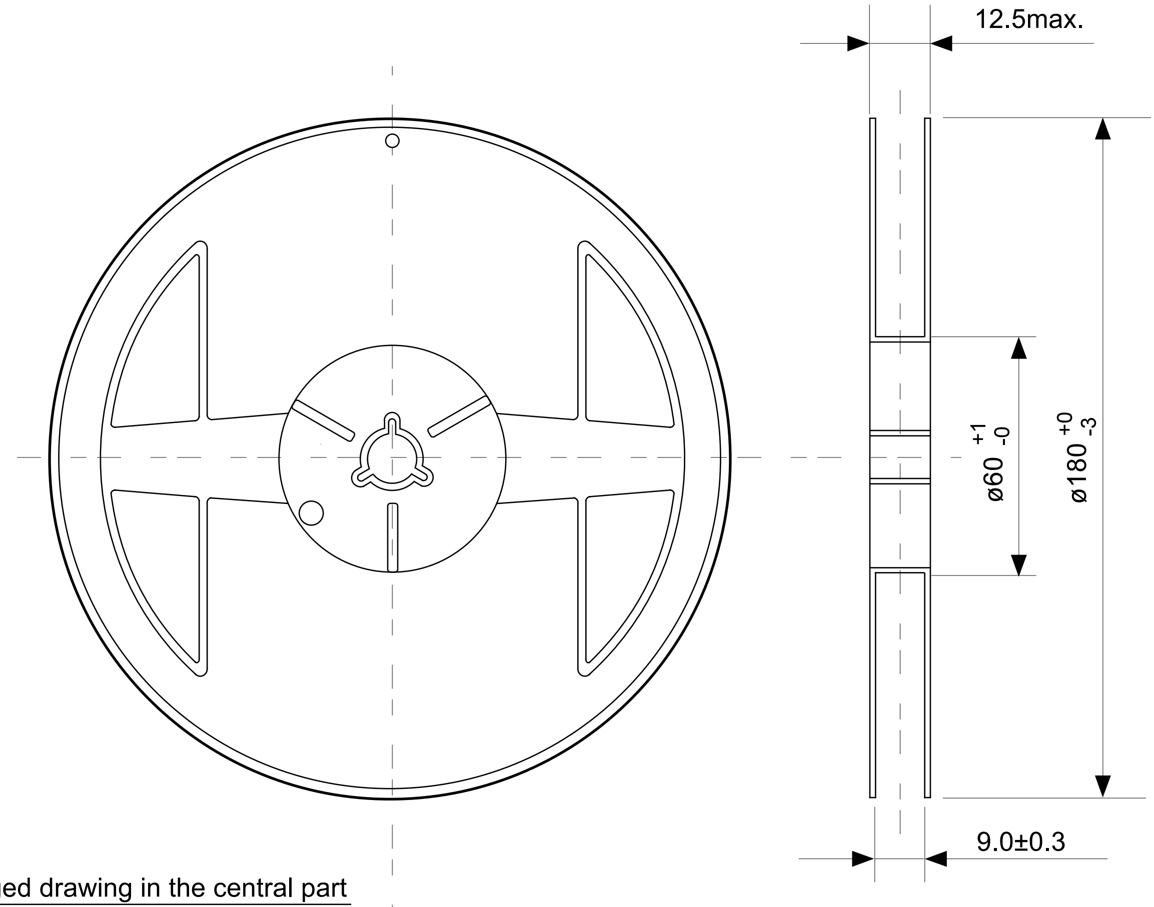




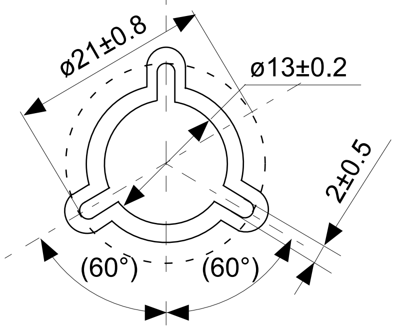
No. NP005-B-C-SD-2.0

TITLE	SC88A-B-Carrier Tape
No.	NP005-B-C-SD-2.0
SCALE	
UNIT	mm

SII Semiconductor Corporation



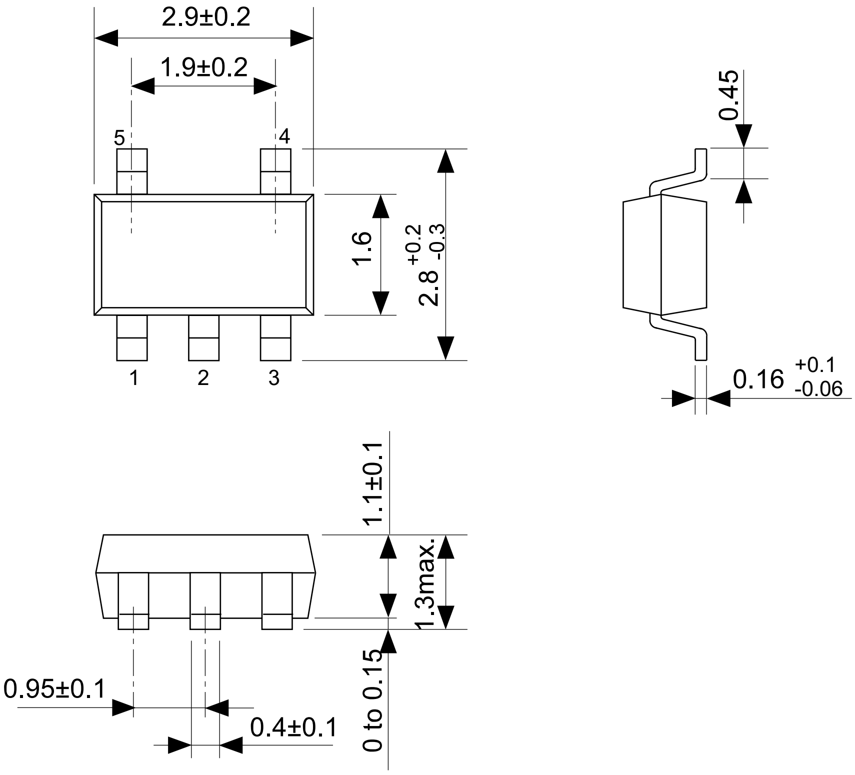
Enlarged drawing in the central part



No. NP005-B-R-SD-2.1

TITLE	SC88A-B-Reel		
No.	NP005-B-R-SD-2.1		
SCALE		QTY.	3000
UNIT	mm		

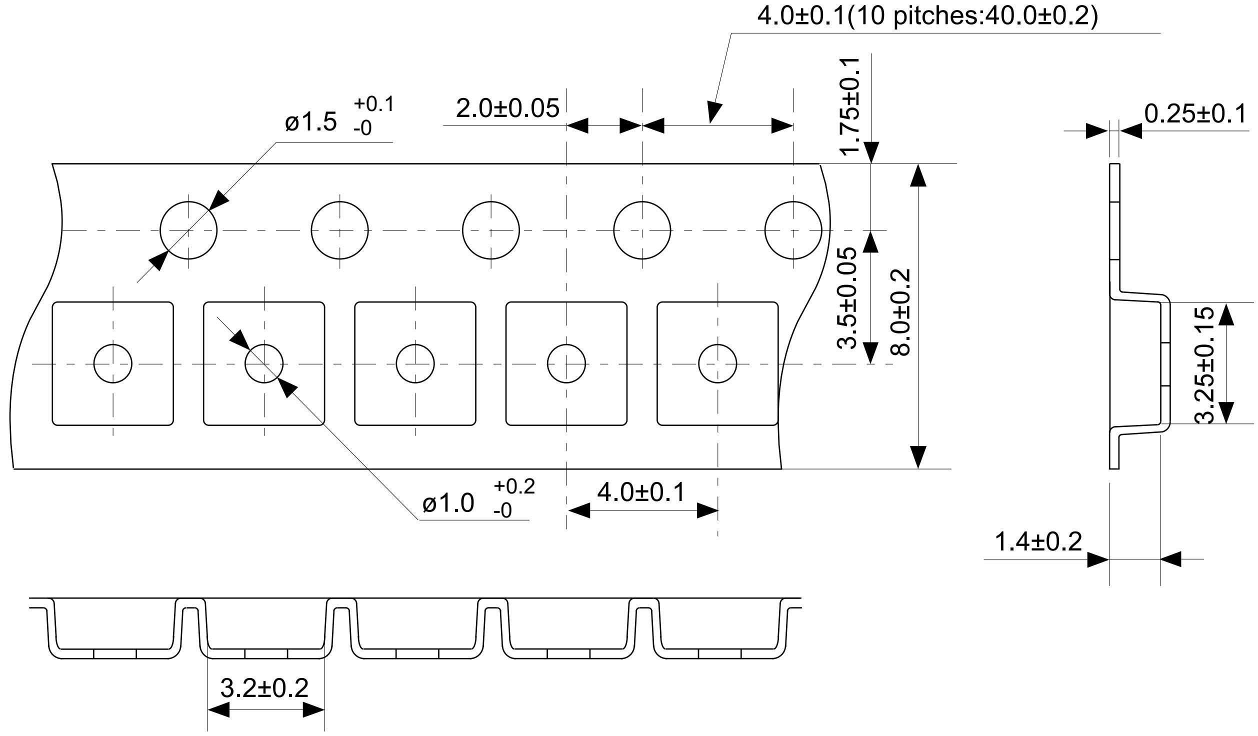
SII Semiconductor Corporation

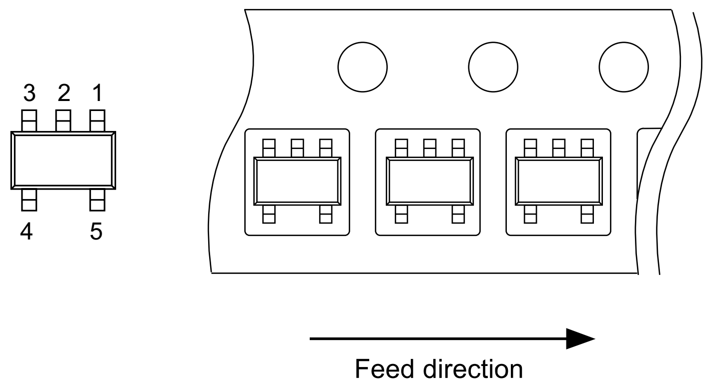


No. MP005-A-P-SD-1.2

TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.2
SCALE	
UNIT	mm

SII Semiconductor Corporation

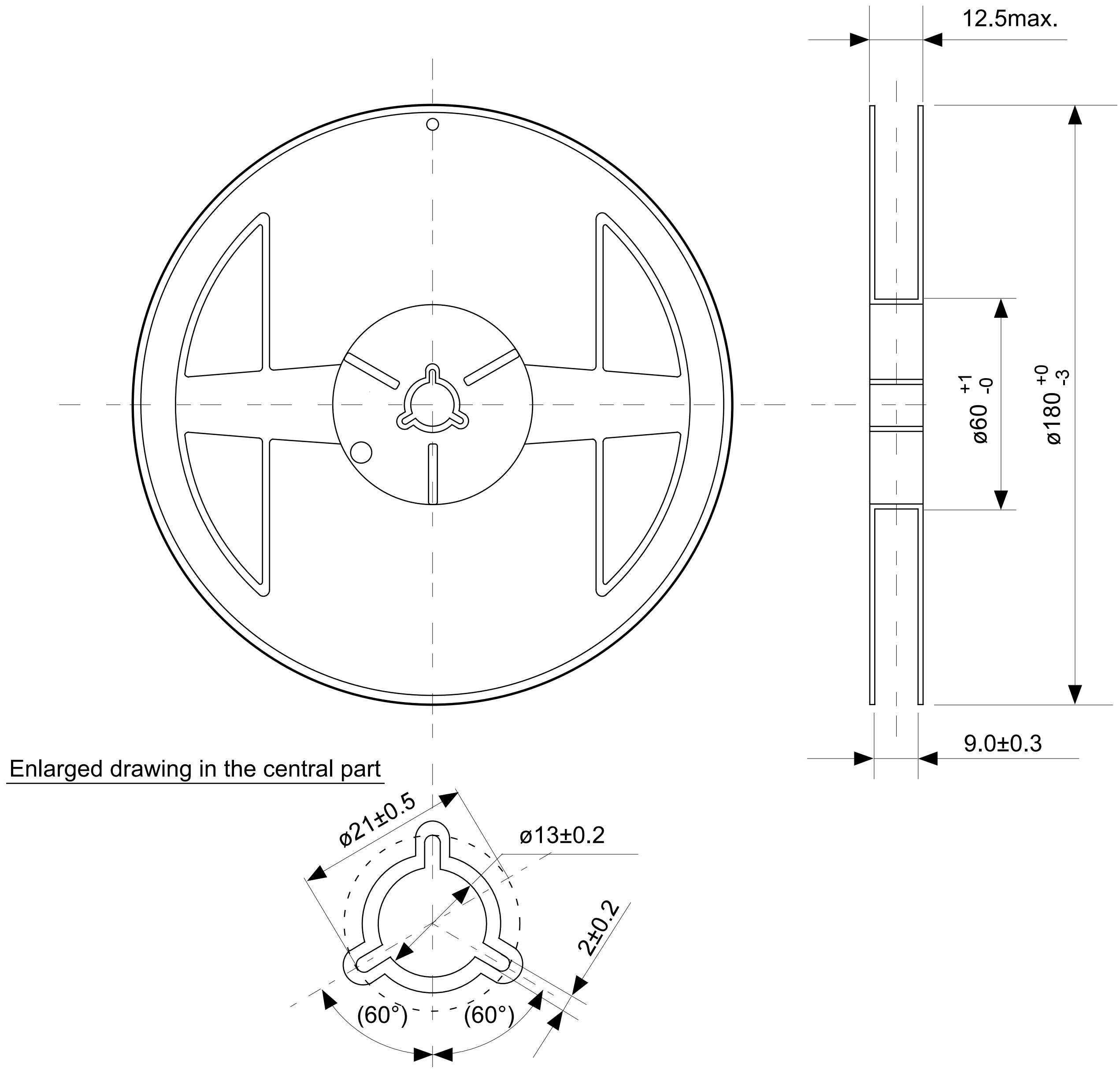




No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
SCALE	
UNIT	mm

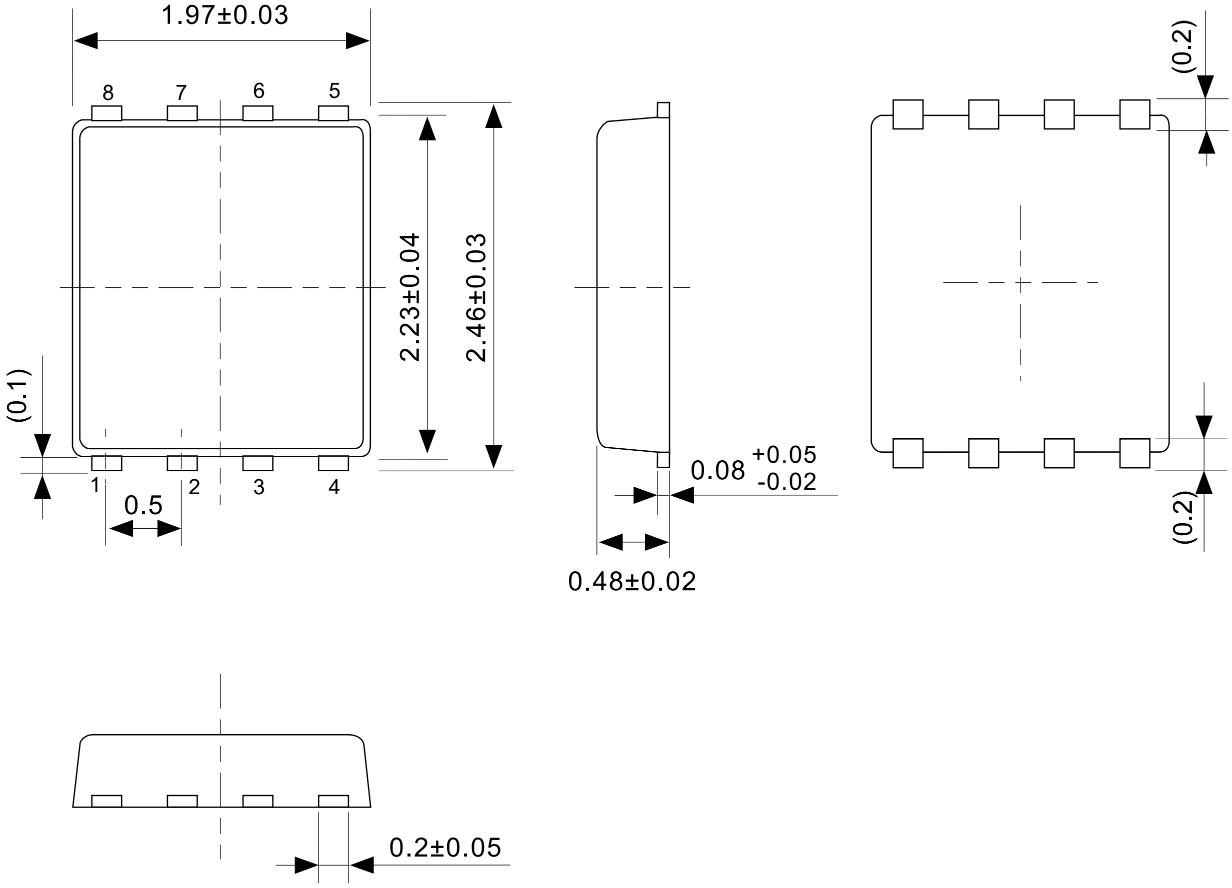
SII Semiconductor Corporation



No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
SCALE		QTY.	3,000
UNIT	mm		

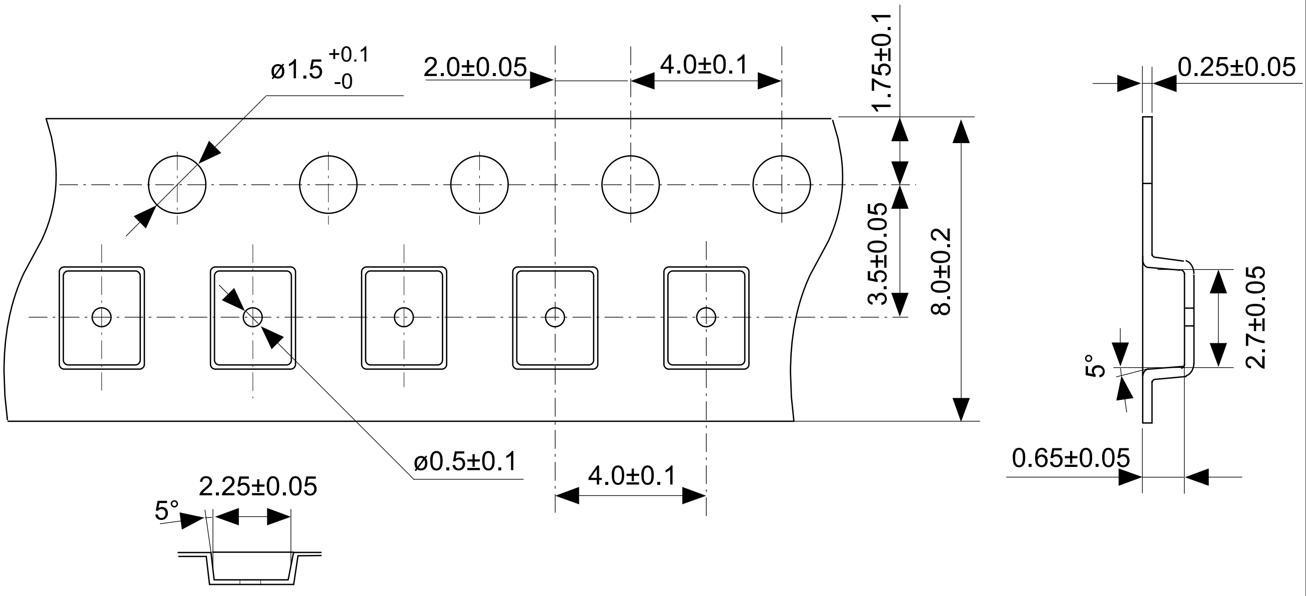
SII Semiconductor Corporation

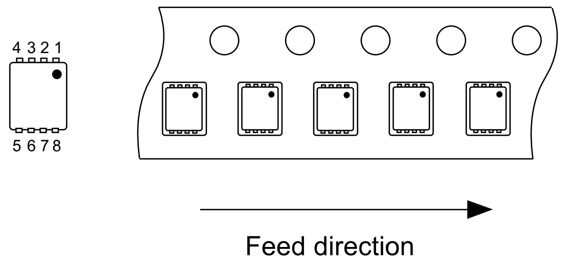


No. PH008-A-P-SD-2.0

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.0
SCALE	
UNIT	mm

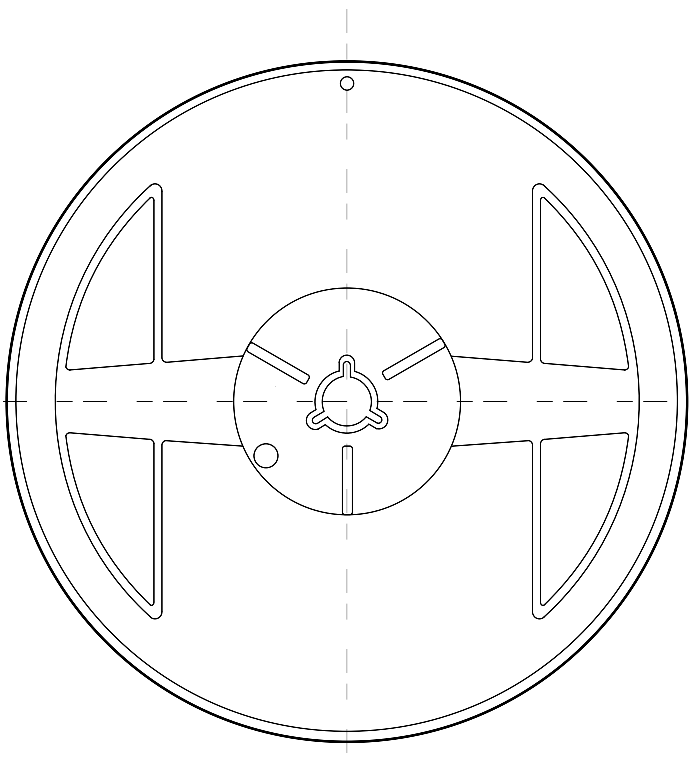
SII Semiconductor Corporation

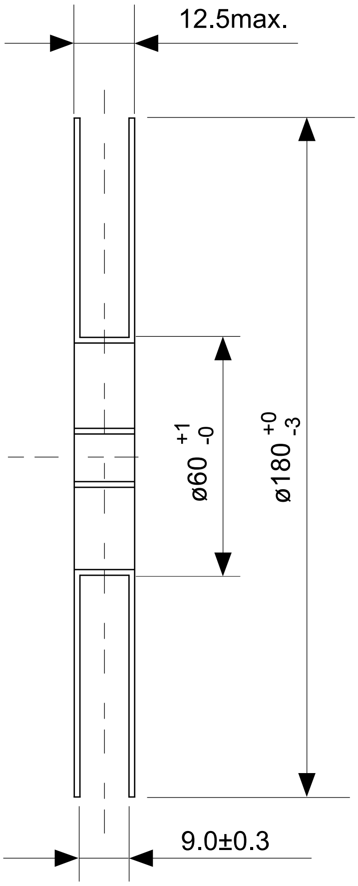




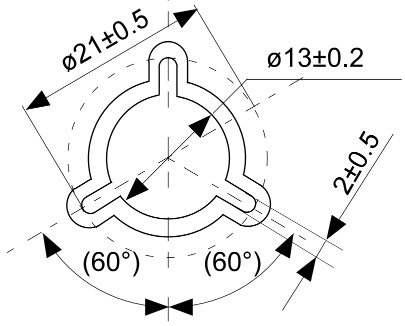
No. PH008-A-C-SD-1.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-1.0
SCALE	
UNIT	mm
SII Semiconductor Corporation	





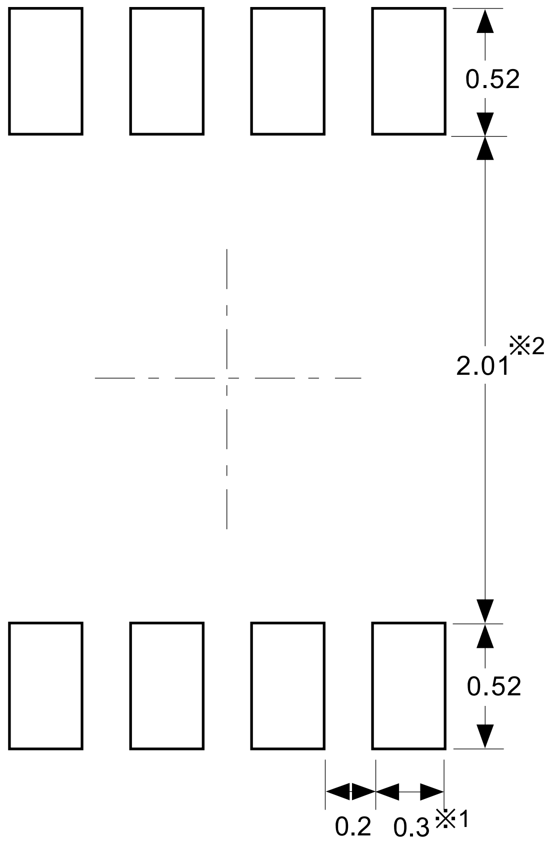
Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
SCALE		QTY.	5,000
UNIT	mm		

SII Semiconductor Corporation



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

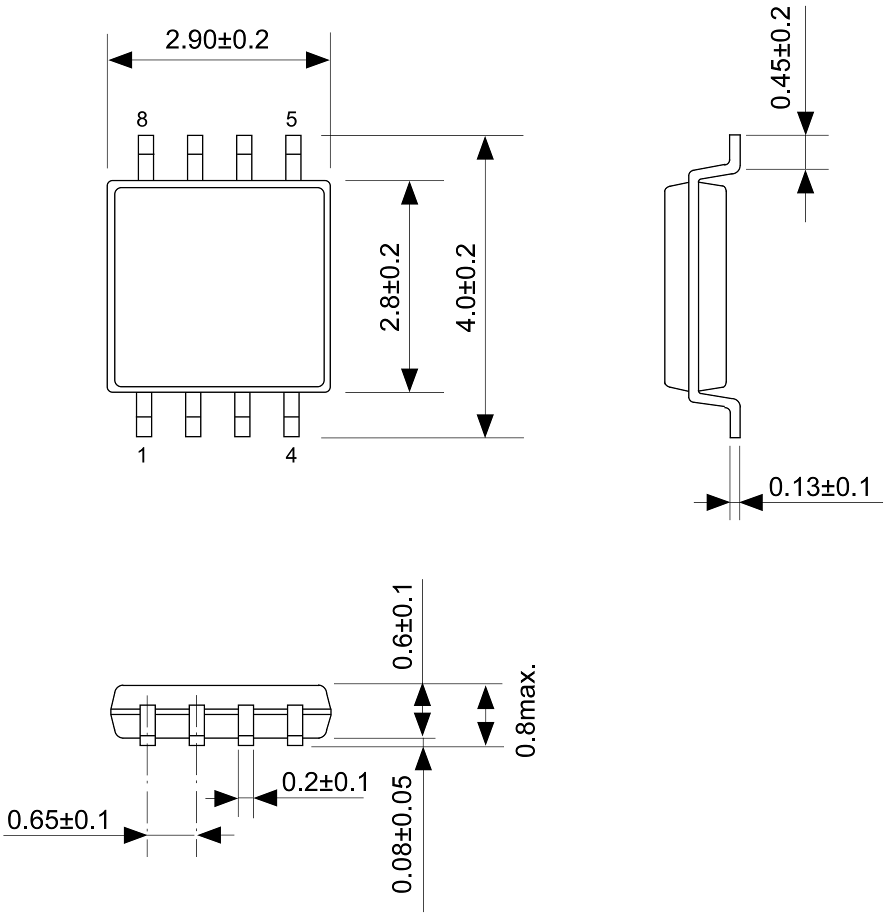
Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度（从焊盘模式表面起）请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

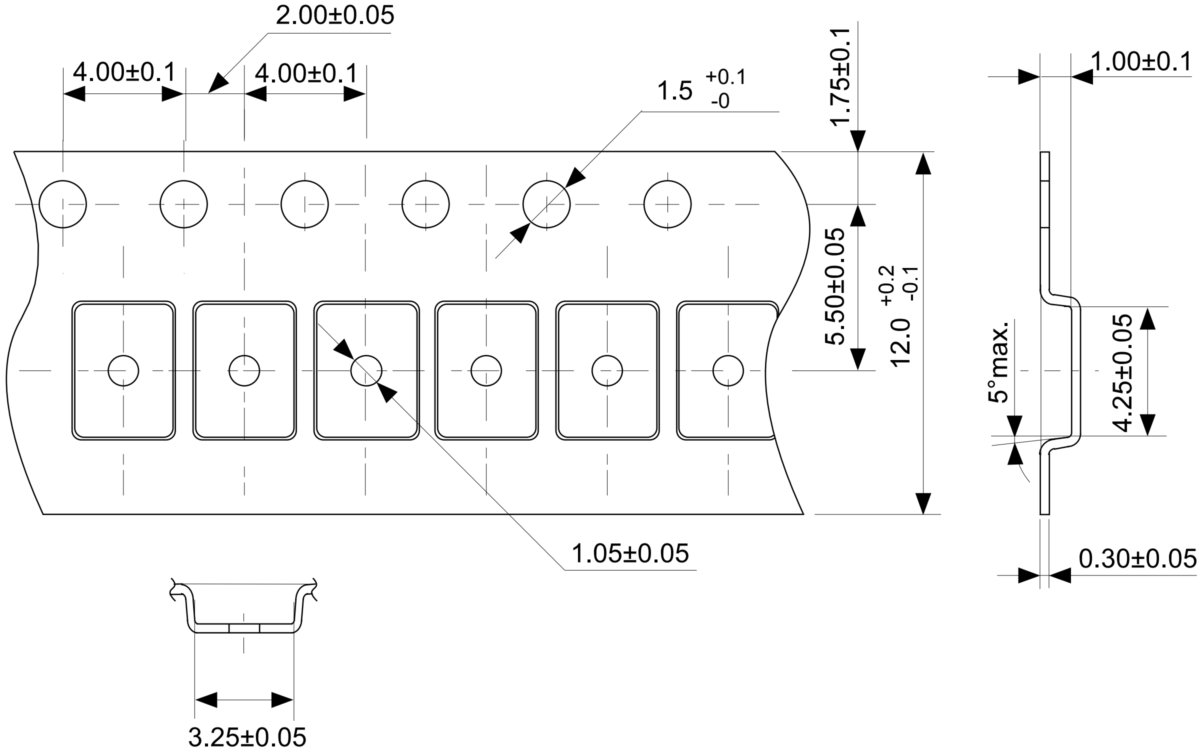
TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
SCALE	
UNIT	mm
SII Semiconductor Corporation	

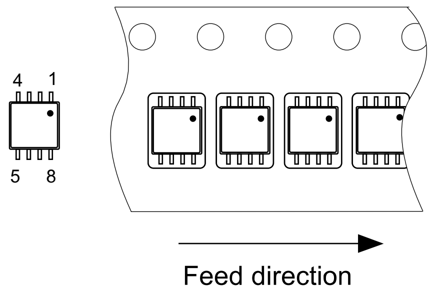


No. FM008-A-P-SD-1.1

TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.1
SCALE	
UNIT	mm

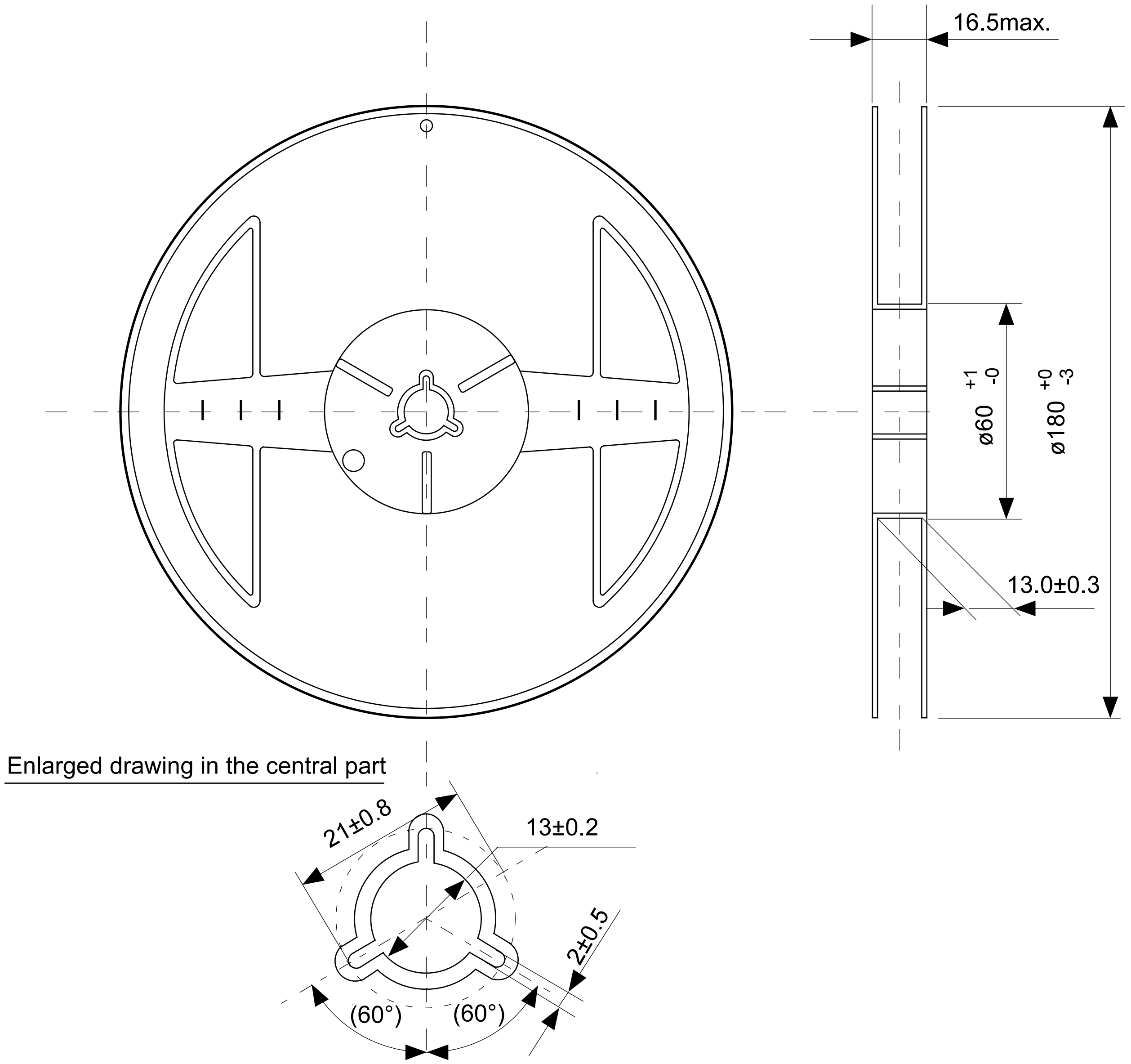
SII Semiconductor Corporation





No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
SCALE	
UNIT	mm
SII Semiconductor Corporation	



No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
SCALE		QTY.	4,000
UNIT	mm		

SII Semiconductor Corporation

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   SII Semiconductor Corporation is not responsible for damages caused by the reasons other than the products or infringement of third-party intellectual property rights and any other rights due to the use of the information described herein.
3. SII Semiconductor Corporation is not responsible for damages caused by the incorrect information described herein.
4. Take care to use the products described herein within their specified ranges. Pay special attention to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   SII Semiconductor Corporation is not responsible for damages caused by failures and/or accidents, etc. that occur due to the use of products outside their specified ranges.
5. When using the products described herein, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products described herein, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products described herein must not be used or provided (exported) for the purposes of the development of weapons of mass destruction or military use. SII Semiconductor Corporation is not responsible for any provision (export) to those whose purpose is to develop, manufacture, use or store nuclear, biological or chemical weapons, missiles, or other military use.
8. The products described herein are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses. Do not use those products without the prior written permission of SII Semiconductor Corporation.
   Especially, the products described herein cannot be used for life support devices, devices implanted in the human body and devices that directly affect human life, etc.
   Prior consultation with our sales office is required when considering the above uses.
   SII Semiconductor Corporation is not responsible for damages caused by unauthorized or unspecified use of our products.
9. Semiconductor products may fail or malfunction with some probability.
   The user of these products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system must be sufficiently evaluated and applied on customer's own responsibility.
10. The products described herein are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products described herein do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Take care when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products described herein, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of SII Semiconductor Corporation.
    The information described herein does not convey any license under any intellectual property rights or any other rights belonging to SII Semiconductor Corporation or a third party. Reproduction or copying of the information described herein for the purpose of disclosing it to a third-party without the express permission of SII Semiconductor Corporation is strictly prohibited.
14. For more details on the information described herein, contact our sales office.

1.0-2016.01