Si595

VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR (VCXO) 10 TO 810 MHZ

Features

- Available with any-rate output frequencies from 10 to 810 MHz
- 3rd generation DSPLL® with superior jitter performance
- Internal fixed fundamental mode crystal frequency ensures high reliability and low aging
- Available CMOS, LVPECL, LVDS, and CML outputs
- 3.3, 2.5, and 1.8 V supply options
- Industry-standard 5 x 7 mm package and pinout
- Pb-free/RoHS-compliant
- –40 to +85 ºC operating range

Applications

- SONET/SDH (OC-3/12/48)
- Networking
- SD/HD SDI/3G SDI video
- FTTx
- Clock recovery and jitter cleanup PLLs
- FPGA/ASIC clock generation

Ordering Information:
See page 7.

Pin Assignments:
See page 6.

(Top View)

V_C	1	6	V_{DD}
OE	2	5	CLK–
GND	3	4	CLK+

Description

The Si595 VCXO utilizes Silicon Laboratories' advanced DSPLL® circuitry to provide a low-jitter clock at high frequencies. The Si595 is available with any-rate output frequency from 10 to 810 MHz. Unlike traditional VCXOs, where a different crystal is required for each output frequency, the Si595 uses one fixed crystal to provide a wide range of output frequencies. This IC-based approach allows the crystal resonator to provide exceptional frequency stability and reliability. In addition, DSPLL clock synthesis provides supply noise rejection, simplifying the task of generating low-jitter clocks in noisy environments. The Si595 IC-based VCXO is factory-configurable for a wide variety of user specifications including frequency, supply voltage, output format, tuning slope, and absolute pull range (APR). Specific configurations are factory programmed at time of shipment, thereby eliminating the long lead times associated with custom oscillators.

Functional Block Diagram

Si595
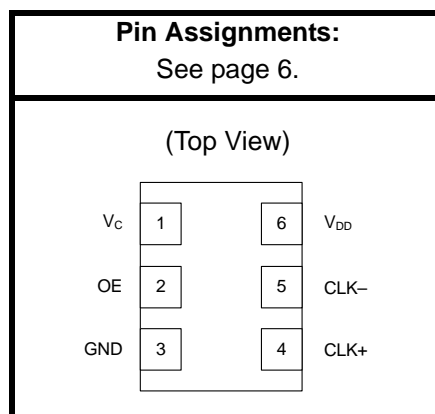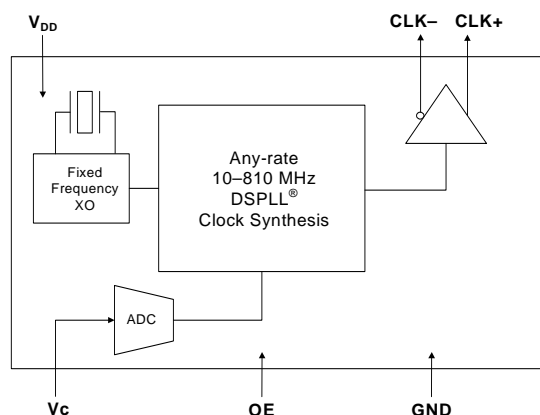
1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage[1]	V_{DD}	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	
		1.8 V option	1.71	1.8	1.89	
Supply Current	I_{DD}	Output enabled LVPECL CML LVDS CMOS	— — — —	120 110 100 90	135 120 110 100	mA
		Tristate mode	—	60	75	
Output Enable (OE)[2]		V_{IH}	0.75 x V_{DD}	—	—	V
		V_{IL}	—	—	0.5	
Operating Temperature Range	T_A		−40	—	85	°C

Notes:
1. Selectable parameter specified by part number. See 3. "Ordering Information" on page 7 for further details.
2. OE pin includes an internal 17 kΩ pullup resistor to V_{DD} for output enable active high or a 17 kΩ pull-down resistor to GND for output enable active low. See 3. "Ordering Information" on page 7.

Table 2. V_C Control Voltage Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Control Voltage Tuning Slope[1,2,3]	K_V	10 to 90% of V_{DD}	—	45 95 125 185 380	—	ppm/V
Control Voltage Linearity[4]	L_{VC}	BSL	−5	±1	+5	%
		Incremental	−10	±5	+10	
Modulation Bandwidth	BW		9.3	10.0	10.7	kHz
V_C Input Impedance	Z_{VC}		500	—	—	kΩ
V_C Input Capacitance	C_{VC}		—	50	—	pF
Nominal Control Voltage	V_{CNOM}	@ f_O	—	V_{DD}/2	—	V
Control Voltage Tuning Range	V_C		0		V_{DD}	V

Notes:
1. Positive slope; selectable option by part number. See 3. "Ordering Information" on page 7.
2. For best jitter and phase noise performance, always choose the smallest K_V that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K_V), Stability, and Absolute Pull Range (APR)" for more information.
3. K_V variation is ±10% of typical values.
4. BSL determined from deviation from best straight line fit with V_C ranging from 10 to 90% of V_{DD}. Incremental slope determined with V_C ranging from 10 to 90% of V_{DD}.

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Table 3. CLK± Output Frequency Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Nominal Frequency[1,2,3]	f_O	LVDS/CML/LVPECL	10	—	810	MHz
		CMOS	10	—	160	
Temperature Stability[1,4]		T_A = –40 to +85 ºC	–20 –50	— —	+20 +50	ppm
Absolute Pull Range[1,4]	APR		±10	—	±370	ppm
Power up Time[5]	t_{OSC}		—	—	10	ms

Notes:
1. See Section 3. "Ordering Information" on page 7 for further details.
2. Specified at time of order by part number.
3. Nominal output frequency set by $V_{CNOM} = V_{DD}/2$.
4. Selectable parameter specified by part number.
5. Time from power up or tristate mode to f_O.

Table 4. CLK± Output Levels and Symmetry

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVPECL Output Option[1]	V_O	mid-level	V_{DD} – 1.42	—	V_{DD} – 1.25	V
	V_{OD}	swing (diff)	1.1	—	1.9	V_{PP}
	V_{SE}	swing (single-ended)	0.55	—	0.95	V_{PP}
LVDS Output Option[2]	V_O	mid-level	1.125	1.20	1.275	V
	V_{OD}	swing (diff)	0.5	0.7	0.9	V_{PP}
CML Output Option[2]	V_O	2.5/3.3 V option mid-level	—	V_{DD} – 1.30	—	V
		1.8 V option mid-level	—	V_{DD} – 0.36	—	
	V_{OD}	2.5/3.3 V option swing (diff)	1.10	1.50	1.90	V_{PP}
		1.8 V option swing (diff)	0.35	0.425	0.50	
CMOS Output Option[3]	V_{OH}		0.8 x V_{DD}	—	V_{DD}	V
	V_{OL}		—	—	0.4	
Rise/Fall time (20/80%)	t_R, t_F	LVPECL/LVDS/CML	—	—	350	ps
		CMOS with C_L = 15 pF	—	2	—	ns
Symmetry (duty cycle)	SYM	LVPECL: V_{DD} – 1.3 V (diff) LVDS: 1.25 V (diff) CMOS: $V_{DD}/2$	45	—	55	%

Notes:
1. 50 Ω to V_{DD} – 2.0 V.
2. R_{term} = 100 Ω (differential).
3. C_L = 15 pF. Sinking or sourcing 12 mA for V_{DD} = 3.3 V, 6 mA for V_{DD} = 2.5 V, 3 mA for V_{DD} = 1.8 V.

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Table 5. CLK± Output Phase Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS)[1,2] for F_{OUT} of 50 MHz $\leq F_{OUT}$ 810 MHz	ϕ_J	Kv = 45 ppm/V 12 kHz to 20 MHz	—	0.5	—	ps
		Kv = 95 ppm/V 12 kHz to 20 MHz	—	0.5	—	
		Kv = 125 ppm/V 12 kHz to 20 MHz	—	0.5	—	
		Kv = 185 ppm/V 12 kHz to 20 MHz	—	0.5	—	
		Kv = 380 ppm/V 12 kHz to 20 MHz	—	0.7	—	

Notes:
1. Refer to AN256 for further information.
2. For best jitter and phase noise performance, always choose the smallest K_V that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K_V), Stability, and Absolute Pull Range (APR)" for more information.

Table 6. CLK± Output Period Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Period Jitter*	J_{PER}	RMS	—	3	—	ps
		Peak-to-Peak	—	35	—	

***Note:** Any output mode, including CMOS, LVPECL, LVDS, CML. N = 1000 cycles. Refer to AN279 for further information.

Table 7. CLK± Output Phase Noise (Typical)

Offset Frequency	74.25 MHz 185 ppm/V LVPECL	148.5 MHz 185 ppm/V LVPECL	155.52 MHz 95 ppm/V LVPECL	Units
100 Hz	−77	−68	−77	
1 kHz	−101	−95	−101	
10 kHz	−121	−116	−119	
100 kHz	−134	−128	−127	dBc/Hz
1 MHz	−149	−144	−144	
10 MHz	−151	−147	−147	
20 MHz	−150	−148	−148	

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Table 8. Environmental Compliance and Package Information

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Moisture Sensitivity Level	J-STD-020, MSL1
Contact Pads	Gold over Nickel

Table 9. Thermal Characteristics

(Typical values TA = 25 ºC, V_{DD} = 3.3 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	—	84.6	—	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	—	38.8	—	°C/W
Ambient Temperature	T_A		–40	—	85	°C
Junction Temperature	T_J		—	—	125	°C

Table 10. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Units
Maximum Operating Temperature	T_{AMAX}	85	ºC
Supply Voltage	V_{DD}	–0.5 to +3.8	V
Input Voltage	V_I	–0.5 to V_{DD} + 0.3	
Storage Temperature	T_S	–55 to +125	ºC
ESD Sensitivity (HBM, per JESD22-A114)	ESD	2500	V
Soldering Temperature (Pb-free profile)[2]	T_{PEAK}	260	ºC
Soldering Temperature Time @ T_{PEAK} (Pb-free profile)[2]	t_P	20–40	seconds

Notes:
1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020C. Refer to Si5xx Packaging FAQ available for download from www.silabs.com/VCXO for further information, including soldering profiles.
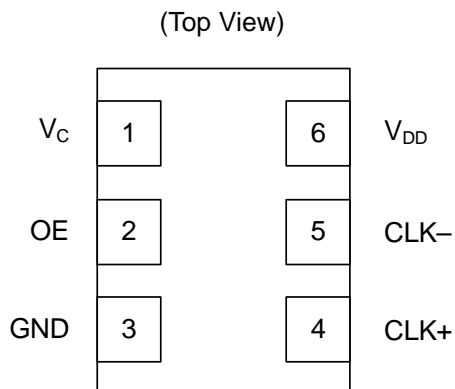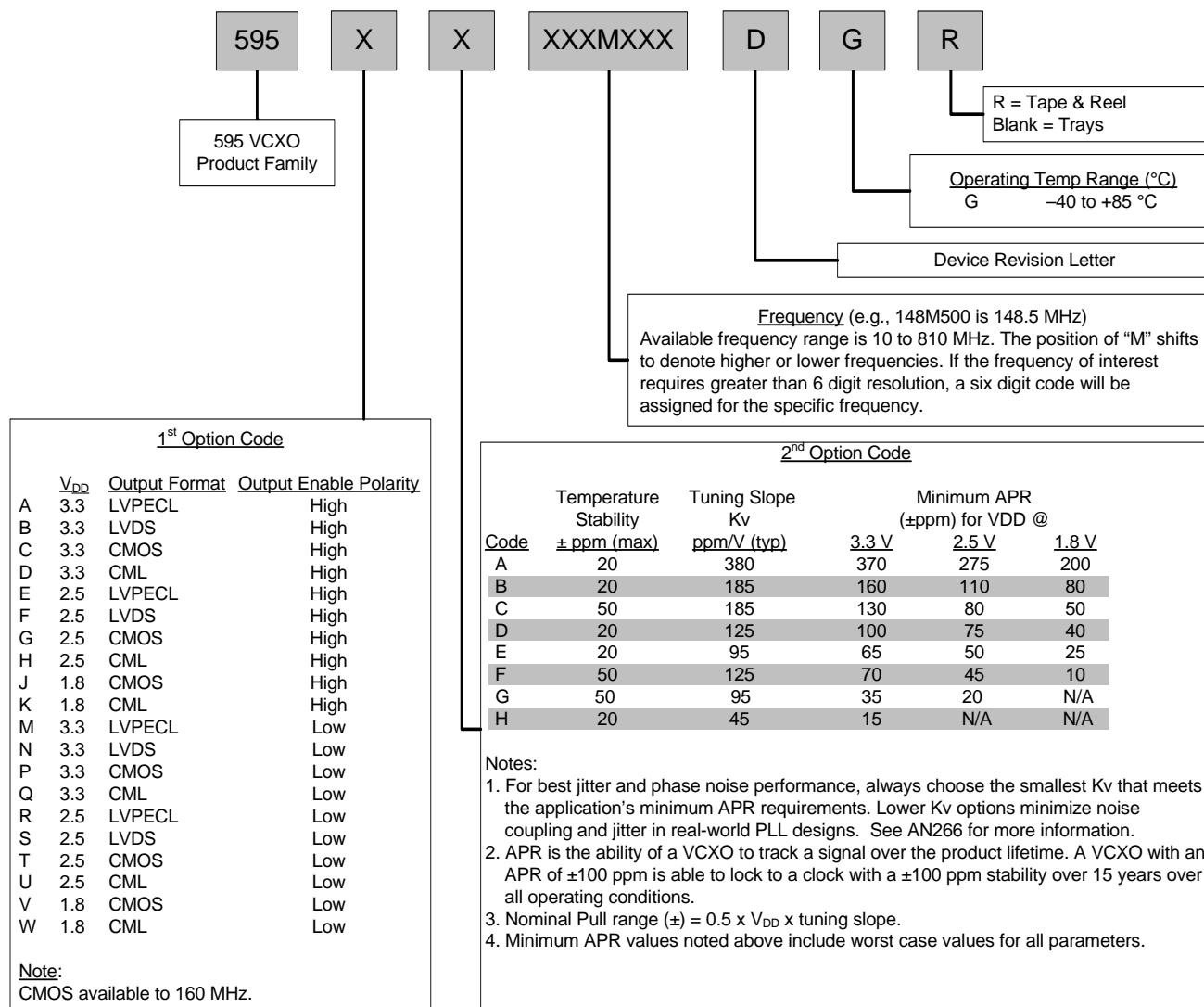
2. Pin Descriptions

(Top View)

V_C [1] [6] V_{DD}

OE [2] [5] CLK–

GND [3] [4] CLK+

Table 11. Si595 Pin Descriptions

Pin	Name	Type	Function
1	V_C	Analog Input	Control Voltage
2	OE*	Input	Output Enable
3	GND	Ground	Electrical and Case Ground
4	CLK+	Output	Oscillator Output
5	CLK– (N/C for CMOS)	Output	Complementary Output (N/C for CMOS, do not make external connection)
6	V_{DD}	Power	Power Supply Voltage
*Note: OE pin includes a 17 kΩ resistor to V_{DD} for OE active high option or 17 kΩ to GND for OE active low option. See 3. "Ordering Information" on page 7.			

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3. Ordering Information

The Si595 supports a variety of options including frequency, temperature stability, tuning slope, output format, and V_{DD}. Specific device configurations are programmed into the Si595 at time of shipment. Configurations are specified using the Part Number Configuration chart shown below. Silicon Labs provides a web browser-based part number configuration utility to simplify this process. Refer to www.silabs.com/VCXOPartNumber to access this tool and for further ordering instructions. The Si595 VCXO series is supplied in an industry-standard, RoHS compliant, lead-free, 6-pad, 5 x 7 mm package. Tape and reel packaging is an ordering option.

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595   X   X   XXXMXXX   D   G   R
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595 VCXO
Product Family

R = Tape & Reel
Blank = Trays

Operating Temp Range (°C)
G   –40 to +85 °C

Device Revision Letter

Frequency (e.g., 148M500 is 148.5 MHz)
Available frequency range is 10 to 810 MHz. The position of "M" shifts to denote higher or lower frequencies. If the frequency of interest requires greater than 6 digit resolution, a six digit code will be assigned for the specific frequency.

1st Option Code

	V_{DD}	Output Format	Output Enable Polarity
A	3.3	LVPECL	High
B	3.3	LVDS	High
C	3.3	CMOS	High
D	3.3	CML	High
E	2.5	LVPECL	High
F	2.5	LVDS	High
G	2.5	CMOS	High
H	2.5	CML	High
J	1.8	CMOS	High
K	1.8	CML	High
M	3.3	LVPECL	Low
N	3.3	LVDS	Low
P	3.3	CMOS	Low
Q	3.3	CML	Low
R	2.5	LVPECL	Low
S	2.5	LVDS	Low
T	2.5	CMOS	Low
U	2.5	CML	Low
V	1.8	CMOS	Low
W	1.8	CML	Low

Note:
CMOS available to 160 MHz.

2nd Option Code

Code	Temperature Stability ± ppm (max)	Tuning Slope Kv ppm/V (typ)	Minimum APR (±ppm) for VDD @ 3.3 V	Minimum APR (±ppm) for VDD @ 2.5 V	Minimum APR (±ppm) for VDD @ 1.8 V
A	20	380	370	275	200
B	20	185	160	110	80
C	50	185	130	80	50
D	20	125	100	75	40
E	20	95	65	50	25
F	50	125	70	45	10
G	50	95	35	20	N/A
H	20	45	15	N/A	N/A

Notes:
1. For best jitter and phase noise performance, always choose the smallest Kv that meets the application's minimum APR requirements. Lower Kv options minimize noise coupling and jitter in real-world PLL designs. See AN266 for more information.
2. APR is the ability of a VCXO to track a signal over the product lifetime. A VCXO with an APR of ±100 ppm is able to lock to a clock with a ±100 ppm stability over 15 years over all operating conditions.
3. Nominal Pull range (±) = 0.5 x V_{DD} x tuning slope.
4. Minimum APR values noted above include worst case values for all parameters.

Example Part Number: 595AE148M500DGR is a 5 x 7 mm VCXO in a 6 pad package. The nominal frequency is 148.5 MHz, with a 3.3 V supply, LVPECL output, and Output Enable active high polarity. Temperature stability is specified as ±20 ppm and the tuning slope is 95 ppm/V. The part is specified for a –40 to +85 C° ambient temperature range operation and is shipped in tape and reel format.

Figure 1. Part Number Convention

4. Outline Diagram and Suggested Pad Layout

Figure 2 illustrates the package details for the Si595. Table 12 lists the values for the dimensions shown in the illustration.
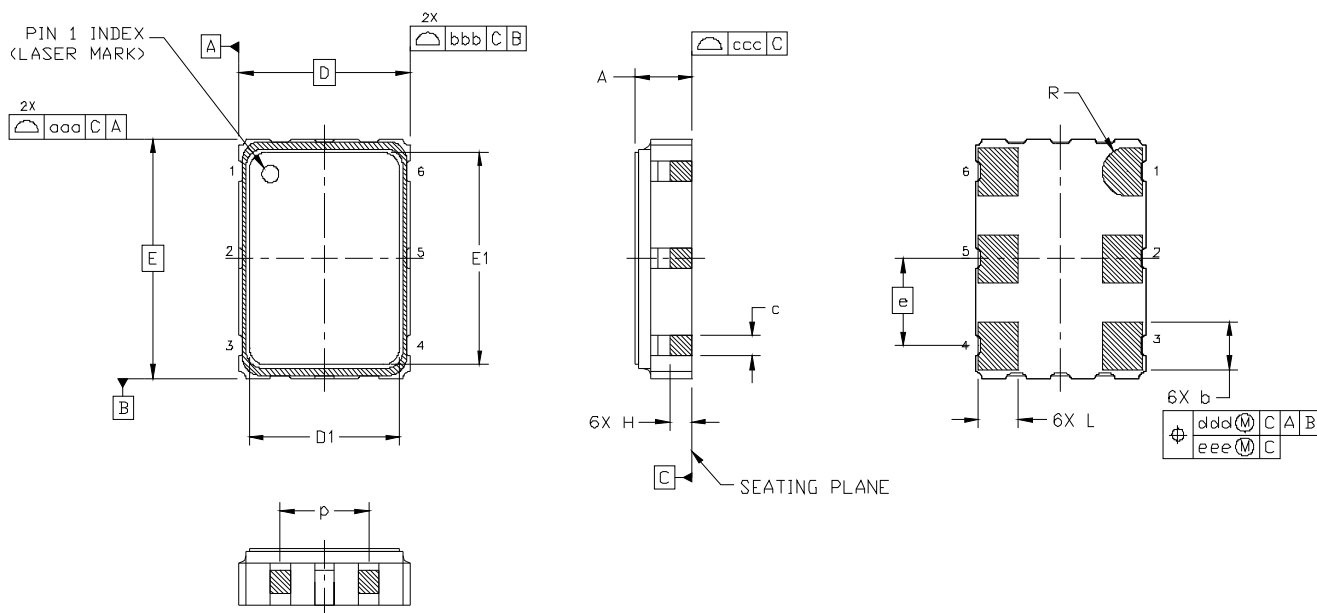

Figure 2. Si595 Outline Diagram

Table 12. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.50	1.65	1.80
b	1.30	1.40	1.50
c	0.50	0.60	0.70
D	5.00 BSC		
D1	4.30	4.40	4.50
e	2.54 BSC.		
E	7.00 BSC.		
E1	6.10	6.20	6.30
H	0.55	0.65	0.75
L	1.17	1.27	1.37
p	1.80	—	2.60
R	0.70 REF		
aaa	0.15		
bbb	0.15		
ccc	0.10		
ddd	0.10		
eee	0.50		

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5. Si5xx Mark Specification

Figure 3 illustrates the mark specification for the Si595. Table 13 lists the line information.
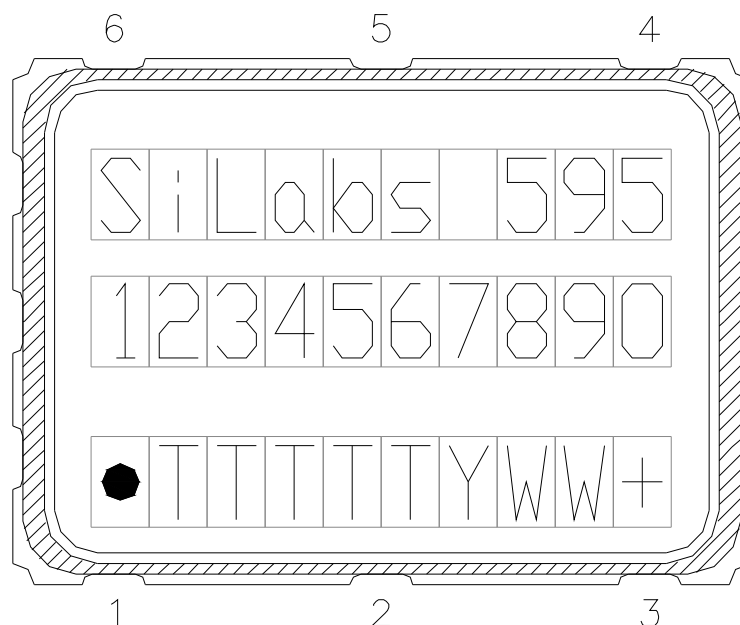
Figure 3. Mark Specification

Table 13. Si595 Top Mark Description

Line	Position	Description
1	1–10	"SiLabs"+ Part Family Number, 595 (First 3 characters in part number)
2	1–10	Si595: Option1+Option2+Freq(7)+Temp Si595 w/ 8-digit resolution: Option1+Option2+ConfigNum(6)+Temp
3	**Trace Code**	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (D)
	Position 3–6	Tiny Trace Code (4 alphanumeric characters per assembly release instructions)
	Position 7	Year (least significant year digit), to be assigned by assembly site (ex: 2009 = 9)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site
	Position 10	"+" to indicate Pb-Free and RoHS-compliant

6. 6-Pin PCB Land Pattern

Figure 4 illustrates the 6-pin PCB land pattern for the Si595. Table 14 lists the values for the dimensions shown in the illustration.
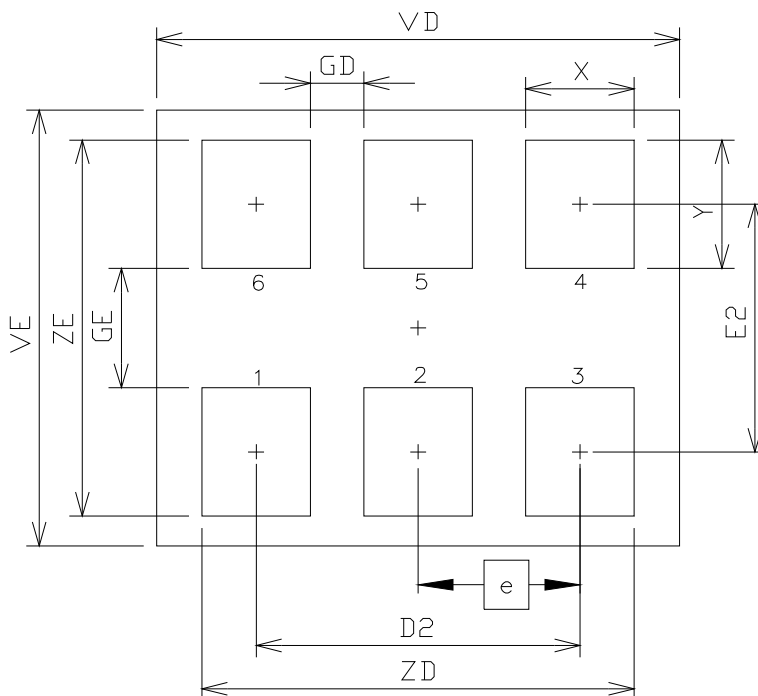
Figure 4. Si595 PCB Land Pattern

Table 14. PCB Land Pattern Dimensions (mm)

Dimension	Min	Max
D2	5.08 REF	
e	2.54 BSC	
E2	4.15 REF	
GD	0.84	—
GE	2.00	—
VD	8.20 REF	
VE	7.30 REF	
X	1.70 TYP	
Y	2.15 REF	
ZD	—	6.78
ZE	—	6.30
Notes:		

Notes:
1. Dimensioning and tolerancing per the ANSI Y14.5M-1994 specification.
2. Land pattern design based on IPC-7351 guidelines.
3. All dimensions shown are at maximum material condition (MMC).
4. Controlling dimension is in millimeters (mm).

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DOCUMENT CHANGE LIST:

Revision 0.1 to Revision 0.2

- Updated Table 5, "CLK± Output Phase Jitter," on page 4.
  - Updated typical phase jitter from 0.6 to 0.7 ps for kV = 380 ppm/V.

Revision 0.2 to Revision 1.0

- Updated 2.5 V/3.3 V and 1.8 V CML output level specifications in Table 4 on page 3.
- Updated Si595 device to support frequencies up to 810 MHz for LVPECL, LVDS, and CML outputs.
- Separated 1.8 V, 2.5 V/3.3 V supply voltage. specifications for CML output in Table 3 on page 5.
- Updated Note 1 of Table 5 on page 4 to refer to AN256.
- Updated Table 8 on page 5 to include the "Moisture Sensitivity Level" and "Contact Pads" rows.
- Updated Figure 3 and Table 13 on page 9 to reflect specific marking information.

Revision 1.0 to Revision 1.1

- Swapped D and E values in Table 12 on page 8.

Revision 1.1 to Revision 1.2

- Added Table 9, "Thermal Characteristics," on page 5.

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CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

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