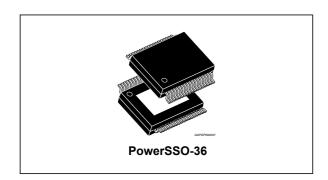
L9960 L9960T

ETC H-bridge

Data brief



Features

- Flexible driving strategy via configurable pins PWM/DIR (IN1/IN2)
- RDSon < 400 m Ω (full path at T_i =150° C)
- Operating battery supply voltage from 4.5 V up to 28 V
- Operating VDD5 supply voltage from 4.5 V to 5.5 V
- Input switching frequency up to 20 kHz
- Built in charge pump supporting 100% duty cycle
- Logic levels compatible to 3.3 V and 5 V
- Monitoring of VDD5 supply voltage with bidirectional switch-off pin
- · Current limitation SPI-adjustable in four steps.
- Output stage current limitation with dependence on temperature

- 2 Programmable voltage and current slew rate control
- Short circuit and programmable thermal warning and shutdown thresholds
- Open Load diagnosis in ON condition
- All I/O pins can withstand up to 19 V
- SPI interface for configuration and diagnosis
- Two independent enable/disable pins NDIS and DIS and SOPC (Switch-off Path Check) available
- Spread Spectrum function for EMI reduction
- Available in single (L9960) and Twin (L9960T) option, both in PSSO36 package

Description

The device is an integrated H-Bridge for resistive and inductive loads for automotive applications, such as throttle control actuators or exhaust gas recirculation control valves.

The driving strategy is enhanced by configurable PWM / DIR pins and IN1/IN2.

The H-Bridge contains integrated free-wheel diodes. In case of freewheeling condition, the low side only is switched on in parallel of its diode to reduce power dissipation.

The integrated Serial Peripheral Interface (SPI) makes it possible to adjust device parameters, to control all operating modes and read out diagnostic information.

Table 1. Device summary

Order code	Package	Packing	
L9960		Tube	
L9960TR	PowerSSO-36	Tape and Reel	
L9960T	Fower330-30	Tube	
L9960T-TR		Tape and Reel	

Contents L9960, L9960T

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1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram for L9960 Ю 3.3V VDDIO C Charge Pump VDD-NDIS 🗗 Monitoring V_S Undervoltage IN1/PWM Logic IN2/DIR OUT1 Gate Control OUT2 DIS 本 SDO Interface SDI Diagnosis SPI SCLK NCS AGND **PGND** GAPGPS02306

1.2 Pin description

1.2.1 PowerSSO36 package

Figure 2. Pin connection of L9960 version (top view)

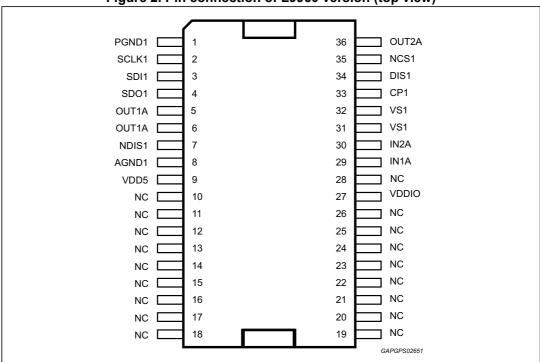
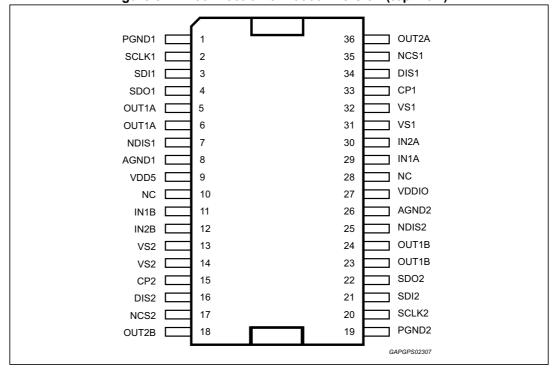


Figure 3. Pin connection of L9960T version (top view)



57/

Table 2. Pin definition (PSSO36twin die) and function

		Table 2. Fin definition (F33036twin die) and function		
Pin#	Pin name	Function		
1	PGND1	Power Ground		
2	SCLK1	SPI Serial Clock Input (internal pull-down)		
3	SDI1	SPI Data In Input (internal pull-down)		
4	SDO1	SPI Serial Data Out. Tri-state output buffer, Transfers data to the μC		
5	OUT1A	O to te CDMOOL With the Africa to All		
6	OUTIA	Output of DMOS half bridge 1 [device A]	0	
7	NDIS1	Bidirectional Enable pin: open drain output pulled low in case of VDD over/under voltage. If the input is pulled low OUT 1-2 go to tri-state.	I/O	
8	AGND1	Analog Ground pin	GND	
9	VDD5	Regulated 5V supply	I	
10	NC	Not connected pin		
11 ⁽¹⁾	IN1B	Input Half Bridge 1 (internal pull-down) [device B]. Acting as PWM at power-up, can be configured to IN1 via SPI frame	I	
12 ⁽¹⁾	IN2B	Input Half Bridge 2 (internal pull-down) [device B]. Acting as DIR at power-up, can be configured as IN2 via SPI frame.		
13 ⁽¹⁾	VS2	Power supply voltage for Power Stages (external reverse protection		
14 ⁽¹⁾	V 32	required)		
15 ⁽¹⁾	CP2	Tank capacitor for Charge Pump output		
16 ⁽¹⁾	DIS2	Disable pin: if it is pulled high Out1-2 are in tri-state (internal pull-up)		
17 ⁽¹⁾	NCS2	SPI Chip Select Input (internal pull-up)		
18 ⁽¹⁾	OUT2B	Output of DMOS half bridge 2 [device B]		
19 ⁽¹⁾	PGND2	Power Ground	GND	
20 ⁽¹⁾	SCLK2	SPI Serial Clock Input (internal pull-down)	I	
21 ⁽¹⁾	SDI2	SPI Data In Input (internal pull-down).	I	
22 ⁽¹⁾	SDO2	SPI Serial Data Out	0	
23 ⁽¹⁾	OLIT4D	Output of DMOC holf heiden 4 Identice D1 moulti honding	0	
24 ⁽¹⁾	OUT1B	Output of DMOS half bridge 1 [device B]. multi-bonding		
25 ⁽¹⁾	NDIS2	Bidirectional Enable pin: open drain output pulled low in case of VDD over/under voltage. If the input is pulled low OUT 1-2 go to tri-state.		
26 ⁽¹⁾	AGND2	Analog Ground pin		
27	VDDIO	Regulated 3.3/5V supply for SDO output buffer	I	
28	NC	Not connected pin		
29	IN1A	Input Half Bridge 1 (internal pull-down) [device A]. Acting as PWM at power-up, can be configured to IN1 via SPI		
30	IN2A	Input Half Bridge 2 (internal pull-down) [device A]. Acting as DIR at power-up, can be configured as IN2 via SPI.	I	



Table 2. Pin definition (PSSO36twin die) and function (continued)

Pin#	Pin name	Function		
31	VS1	Power supply voltage for Power Stages (external reverse protection required)		
32	٧٥١			
33	CP1	Charge Pump output	0	
34	DIS1	Disable pin: if it is pulled high Out1-2 are in tri-state (internal pull-up)	I	
35	NCS1	SPI Chip Select Input (internal pull-up)	I	
36	OUT2A	Output of DMOS half bridge 2 [device A]. multi-bonding	0	
EP	AGND1	Exposed Pad connected to PCB Ground		

^{1.} For L9960 version in PSSO36, the pins from 11 to 26 are not connected.



2 Application description

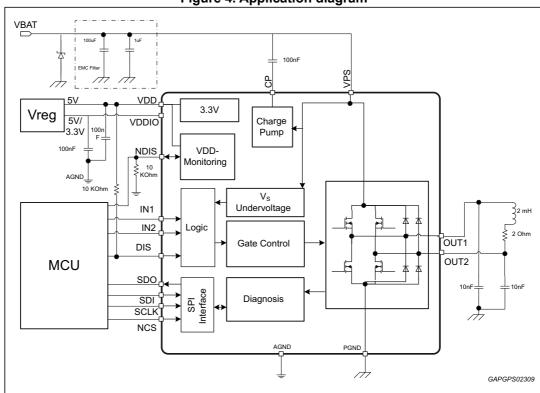


Figure 4. Application diagram

2.1 Functionality

The L9960 is dedicated to be part of an H-Bridge module for automotive applications. The module is used for DC motor driving in applications like ETC, EGR or swirl flap. The L9960 is implemented with a microcontroller, an input filter (fulfillment of the EMC/EMI requirements) and an over-voltage protection diode (optional).

2.2 Example of application circuit

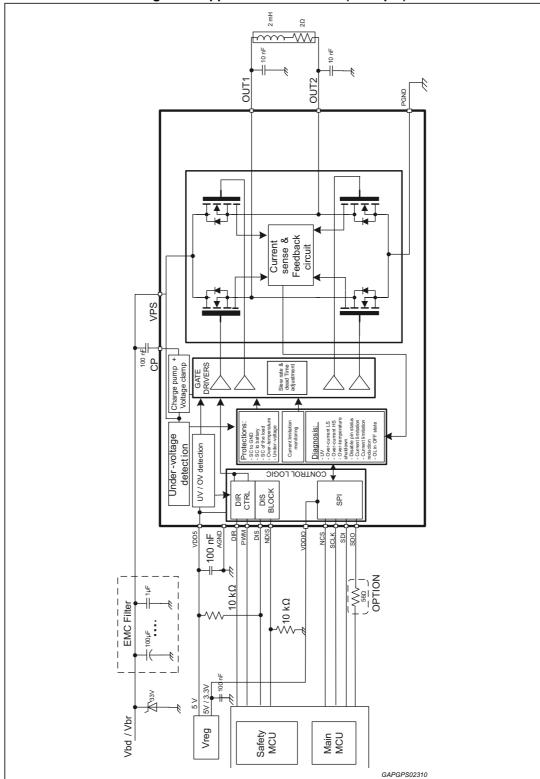


Figure 5. Application schematic (example)

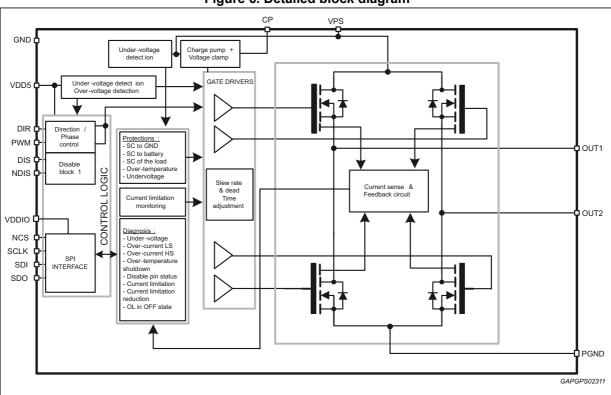


Figure 6. Detailed block diagram



General electrical characteristics 3

Absolute maximum ratings 3.1

Warning:

stressing the device above the rating listed in the "Absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect the device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Condition	Min	Max	Unit
V _{ps}	Supply voltage	Continuous	-1	40	V
V _{out1,2}	Output voltage	Continuous. OUT is limited by VPS	-1	40	V
VDD5	Logic supply voltage	0 V < Vps < 40 V	-0.3	19	٧
VDDIO	SDO supply voltage	0V <vps<40v< td=""><td>-0.3</td><td>19</td><td>٧</td></vps<40v<>	-0.3	19	٧
VCP	VCP output voltage	-	-0.3	Vps+5	V
V _{IN}	Logic input voltage (NCS, SDI, SCLK, DIR, PWM, DIS, NDIS)	0 V < Vps < 40 V	-0.3	19	٧
V _o	Logic output voltage (SDO, NDIS)	0 V < VDD5 < 19 V	-0.3	19	V
-	Human body model ESD compliance for pins: OUTx,VPS (not tested at ATE) ⁽¹⁾	HBM (100 pF/1.5 kohm)	-4	4	kV
-	Human body model ESD compliance for other pins than OUTx, VPS (not tested at ATE)	HBM (100 pF/1.5 kohm)	-2	2	kV
_	Charge Device Model ESD compliance	CDM; according Q100-011	-750	750 ⁽²⁾	V
	for all pins (not tested at ATE)	classification C3B	-500	500 ⁽³⁾	V
-	ISO 7637 pulses	Cf. standards	-	-	-
-	Latch-up immunity	According to JEDEC 78 class 2 leve	l A		

^{1.} Versus GND.

Note: Test circuit according HBM (EIA/JESD22-A114-B) and CDM (EIA/JESD22-C101-C).

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^{2.} Corner pins.

^{3.} All pins.

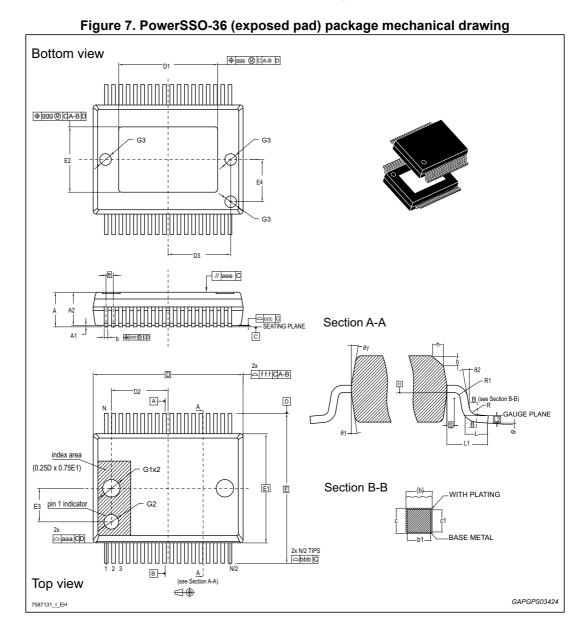
L9960, L9960T Package information

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com.

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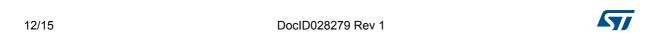
4.1 PowerSSO-36 (exposed pad) package mechanical data



Package information L9960, L9960T

Table 4. PowerSSO-36 (exposed pad) package mechanical data

	Dimensions						
Ref	Millimeters		Inches ⁽¹⁾				
	Min.	Тур.	Max.	Min.	Тур.	Max.	
θ	0°	-	8°	0°	-	8°	
Θ1	5°	-	10°	5°	-	10°	
Θ2	0°	-	-	0°	-	-	
Α	2.15	-	2.45	0.0846	-	0.0965	
A1	0.0	-	0.1	0.0	-	0.0039	
A2	2.15	-	2.35	0.0846	-	0.0925	
b	0.18	-	0.32	0.0071	-	0.0126	
b1	0.13	0.25	0.3	0.0051	0.0098	0.0118	
С	0.23	-	0.32	0.0091	-	0.0126	
c1	0.2	0.2	0.3	0.0079	0.0079	0.0118	
D ⁽²⁾	10.30 BSC 0.4055 BSC						
D1	VARIATION						
D2	-	3.65	-	-	0.1437	-	
D3	-	4.3	-	-	0.1693	-	
е		0.50 BSC	1		0.0197 BSC		
Е		10.30 BSC			0.4055 BSC		
E1 ⁽²⁾		7.50 BSC			0.2953 BSC		
E2			VARI	ATION			
E3	-	2.3	-	-	0.0906	-	
E4	-	2.9	-	-	0.1142	-	
G1	-	1.2	-	-	0.0472	-	
G2	-	1	-	-	0.0394	-	
G3	-	0.8	-	-	0.0315	-	
h	0.3	-	0.4	0.0118	-	0.0157	
L	0.55	0.7	0.85	0.0217	-	0.0335	
L1	1.40 REF			0.0551 REF			
L2	0.25 BSC			0.0098 BSC			
N	36 1.4173						
R	0.3	-	-	0.0118	-	-	
R1	0.2	-	-	0.0079	-	-	
S	0.25	-	-	0.0098	-	-	



L9960, L9960T Package information

Table 4. PowerSSO-36 (exposed pad) package mechanical data (continued)

	Dimensions					
Ref	Millimeters			Inches ⁽¹⁾		
	Min.	Тур.	Max.	Min.	Тур.	Max.
		Toleranc	e of form and	position		
aaa		0.2		0.0079		
bbb		0.2			0.0079	
ccc		0.1			0.0039	
ddd		0.2			0.0079	
eee		0.1		0.0039		
ffff	0.2			0.0079		
999	0.15			0.0059		
VARIATIONS						
Option A						
D1	6.5	-	7.1	0.2559	-	0.2795
E2	4.1 - 4.7		0.1614	-	0.1850	
Option B						
D1	4.9 - 5.5		0.1929	-	0.2165	
E2	4.1 - 4.7			0.1614 - 0.1850		
Option C	Option C					
D1	6.9	-	7.5	0.2717	-	0.2953
E2	4.3	-	5.2	0.1693	-	0.2047

^{1.} Values in inches are converted from mm and rounded to 4 decimal digits.

Dimensions D and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is '0.25 mm' per side D and '0.15 mm' per side E1. D and E1 are Maximum plastic body size dimensions including mold mismatch.

Revision history L9960, L9960T

5 Revision history

Table 5. Document revision history

Date	Revision	Changes
04-Dec-2015	1	Initial release.

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