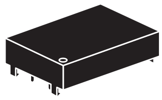
M48T37Y
M48T37V

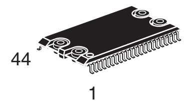
5.0 or 3.3 V, 256 Kbit (32 Kbit x 8) TIMEKEEPER® SRAM

Features

- Integrated ultra low power SRAM, real-time clock, power-fail control circuit, and battery
- Frequency test output for real-time clock software calibration
- Automatic power-fail chip deselect and WRITE protection
- Watchdog timer
- WRITE protect voltage (V_{PFD} = Power-fail deselect voltage):
  - M48T37Y: V_{CC} = 4.5 to 5.5 V
    $4.2 \text{ V} \leq V_{PFD} \leq 4.5 \text{ V}$
  - M48T37V: V_{CC} = 3.0 to 3.6 V
    $2.7 \text{ V} \leq V_{PFD} \leq 3.0 \text{ V}$
- Packaging includes a 44-lead SOIC and SNAPHAT® top (to be ordered separately)
- SOIC package provides direct connection for a SNAPHAT® top which contains the battery and crystal
- Microprocessor power-on reset (valid even during battery backup mode)
- Programmable alarm output active in the battery backup mode
- Battery low flag
- RoHS compliant
  - Lead-free second level interconnect

SNAPHAT® (SH)
Battery/crystal





SOH44 (MH)
44-pin SOIC

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1 Description

The M48T37Y/V TIMEKEEPER® RAM is a 32 Kb x 8 non-volatile static RAM and real-time clock. The monolithic chip is available in a special package which provides a highly integrated battery-backed memory and real-time clock solution.

The 44-lead, 330 mil SOIC package provides sockets with gold-plated contacts at both ends for direct connection to a separate SNAPHAT housing containing the battery and crystal. The unique design allows the SNAPHAT® battery/crystal package to be mounted on top of the SOIC package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SOIC and battery packages are shipped separately in plastic anti-static tubes or in tape & reel form. For the 44-lead SOIC, the battery/crystal package (e.g., SNAPHAT) part number is “M4T28-BR12SH” or “M4T32-BR12SH”.

Caution: Do not place the SNAPHAT battery/crystal top in conductive foam, as this will drain the lithium button-cell battery.

Figure 1. Logic diagram

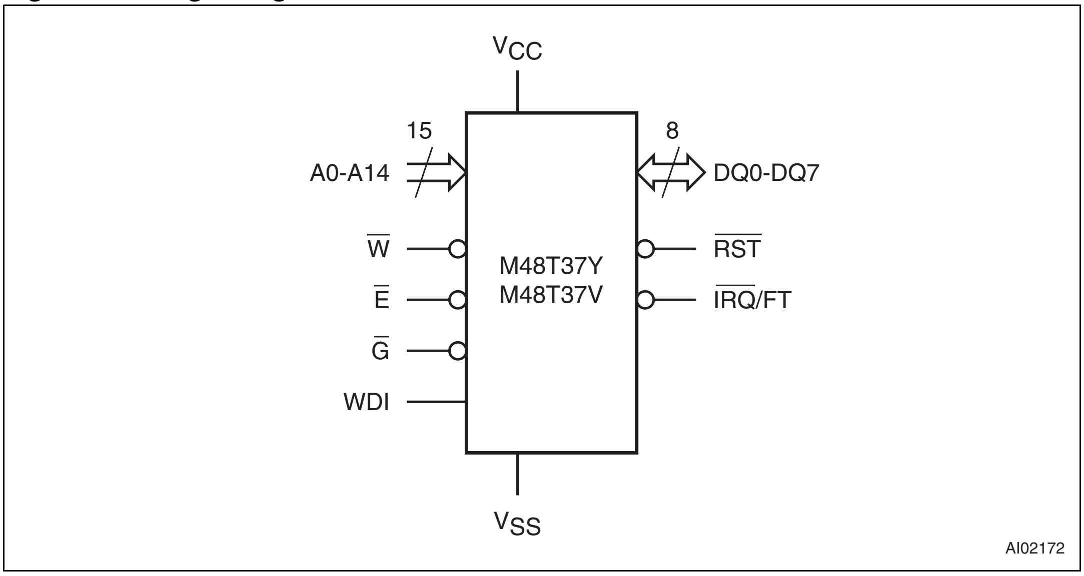


Table 1. Signal names

A0-A14	Address inputs
DQ0-DQ7	Data inputs / outputs
$\overline{RST}$	Reset output (open drain)
$\overline{IRQ}$/FT	Interrupt / frequency test output (open drain)
WDI	Watchdog input
$\overline{E}$	Chip enable
$\overline{G}$	Output enable
$\overline{W}$	WRITE enable
V_{CC}	Supply voltage
V_{SS}	Ground
NC	Not connected internally

Figure 2. SOIC connections

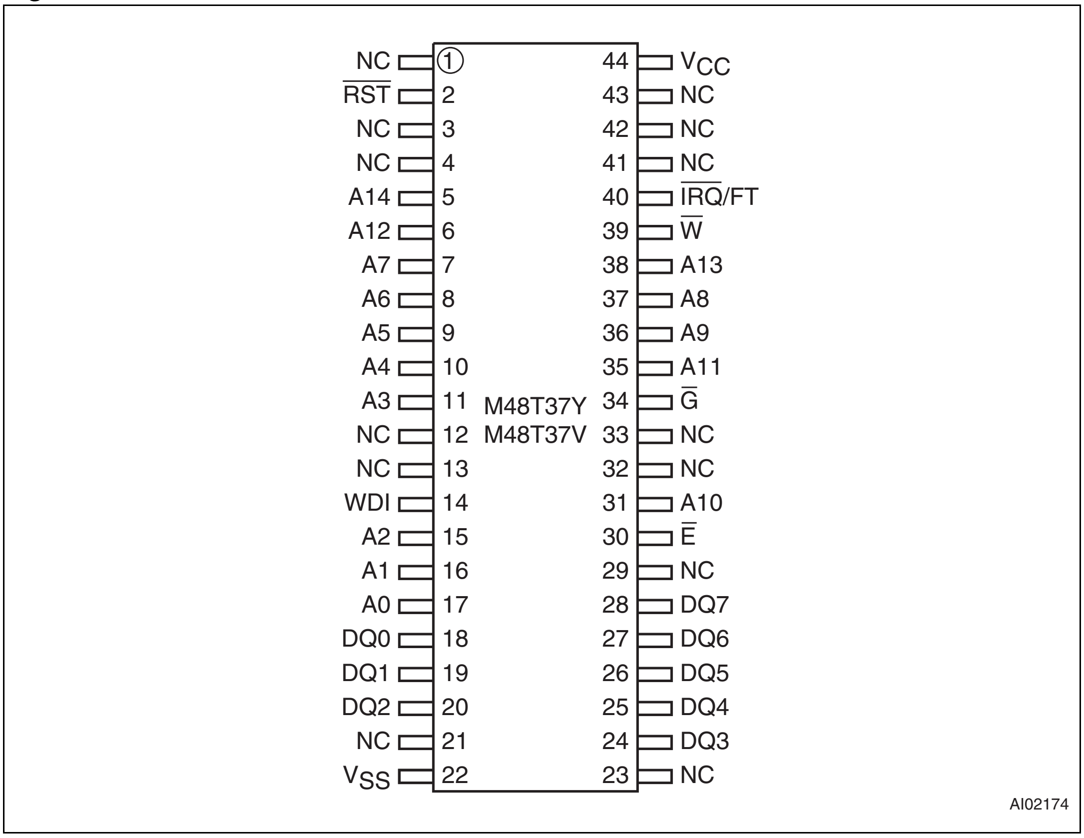
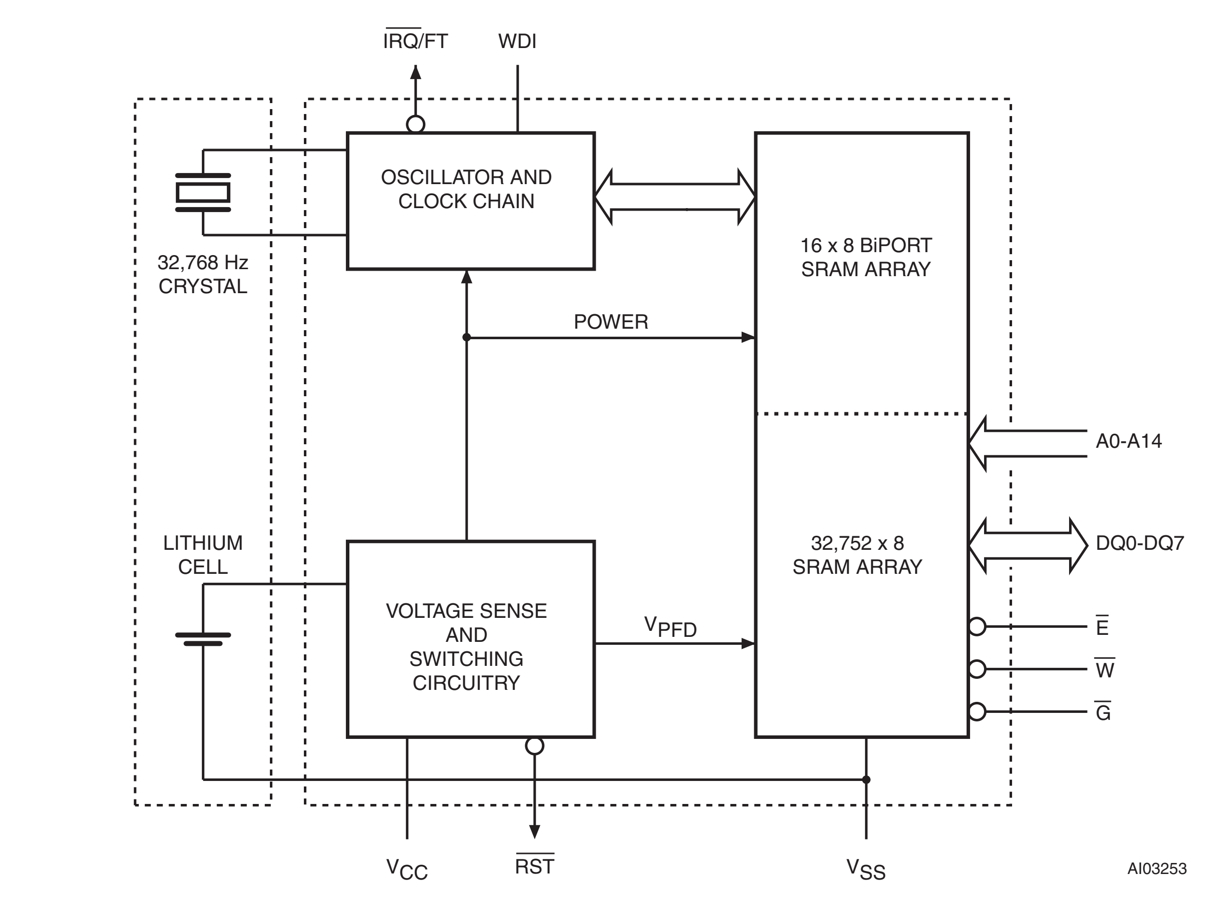


Figure 3. Block diagram



2 Operation modes

As Figure 3 on page 7 shows, the static memory array and the quartz controlled clock oscillator of the M48T37Y/V are integrated on one silicon chip. The memory locations that provide user accessible BYTEWIDE™ clock information are in the bytes with addresses 7FF1 and 7FF9h-7FFFh (located in Table 5 on page 13). The clock locations contain the century, year, month, date, day, hour, minute, and second in 24-hour BCD format. Corrections for 28, 29 (leap year - valid until the year 2100), 30, and 31 day months are made automatically.

Byte 7FF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

Byte 7FF7h contains the watchdog timer setting. The watchdog timer redirects an out-of-control microprocessor and provides a reset or interrupt to it. Bytes 7FF2h-7FF5h are reserved for clock alarm programming. These bytes can be used to set the alarm. This will generate an active low signal on the $\overline{IRQ}$/FT pin when the alarm bytes match the date, hours, minutes, and seconds of the clock. The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT™ READ/WRITE memory cells. The M48T37Y/V includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

The M48T37Y/V also has its own power-fail detect circuit. The control circuitry constantly monitors the single V_{CC} supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below the battery backup switchover voltage (V_{SO}), the control circuitry connects the battery which maintains data and clock operation until valid power returns.

Table 2. Operating modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.5 to 5.5 V or 3.0 to 3.6 V	V_{IH}	X	X	High Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)[1]	X	X	X	High Z	CMOS standby
Deselect	$\leq V_{SO}$[1]	X	X	X	High Z	Battery backup mode

1. See Table on page 23 for details.

Note: $X = V_{IH}$ or V_{IL}; V_{SO} = Battery backup switchover voltage.

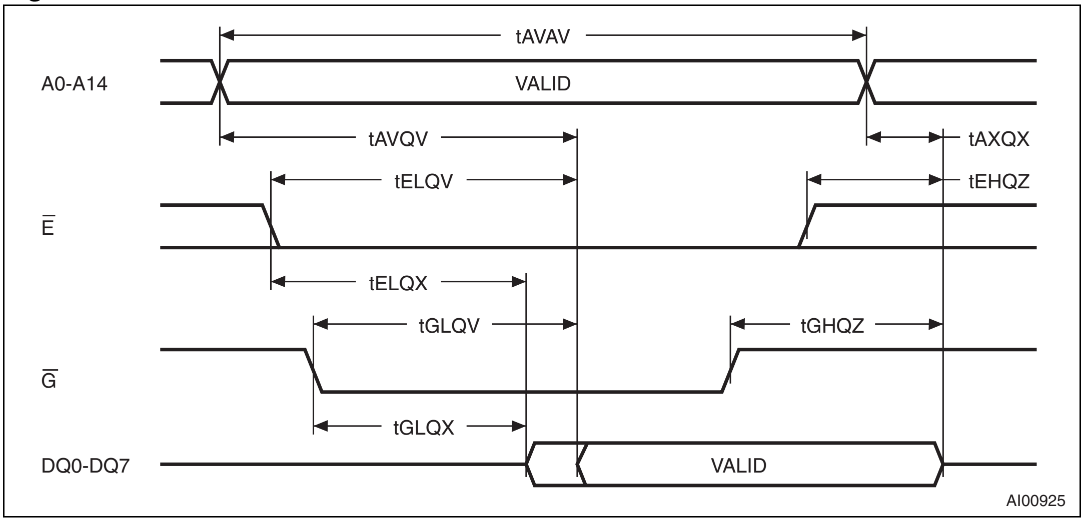
2.1 READ mode

The M48T37Y/V is in the READ mode whenever WRITE enable ($\overline{W}$) is high and chip enable ($\overline{E}$) is low. The unique address specified by the 15 address inputs defines which one of the 32,752 bytes of data is to be accessed. Valid data will be available at the data I/O pins within address access time (t_{AVQV}) after the last address input signal is stable, providing that the $\overline{E}$ and output enable ($\overline{G}$) access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the chip enable access time (t_{ELQV}) or output enable access time (t_{GLQV}).

The state of the eight three-state data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}.

If the address inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for output data hold time (t_{AXQX}) but will be indeterminate until the next address access.

Figure 4. READ mode AC waveforms



Note: WRITE enable ($\overline{W}$) = high.

Table 3. READ mode AC characteristics

Symbol	Parameter(1)	M48T37Y –70 Min	M48T37Y –70 Max	M48T37V –100 Min	M48T37V –100 Max	Unit
t_{AVAV}	READ cycle time	70		100		ns
t_{AVQV}	Address valid to output valid		70		100	ns
t_{ELQV}	Chip enable low to output valid		70		100	ns
t_{GLQV}	Output enable low to output valid		35		50	ns
t_{ELQX}(2)	Chip enable low to output transition	5		10		ns
t_{GLQX}(2)	Output enable low to output transition	5		5		ns
t_{EHQZ}(2)	Chip enable high to output Hi-Z		25		50	ns
t_{GHQZ}(2)	Output enable high to output Hi-Z		25		40	ns
t_{AXQX}	Address transition to output transition	10		10		ns

1. Valid for ambient operating temperature: T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5 to 5.5 V or 3.0 to 3.6 V (except where noted).

2. C_L = 5 pF.

2.2 WRITE mode

The M48T37Y/V is in the WRITE mode whenever $\overline{W}$ and $\overline{E}$ are low. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of t_{EHAX} from chip enable or t_{WHAX} from WRITE enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; however, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 5. WRITE enable controlled, WRITE AC waveform

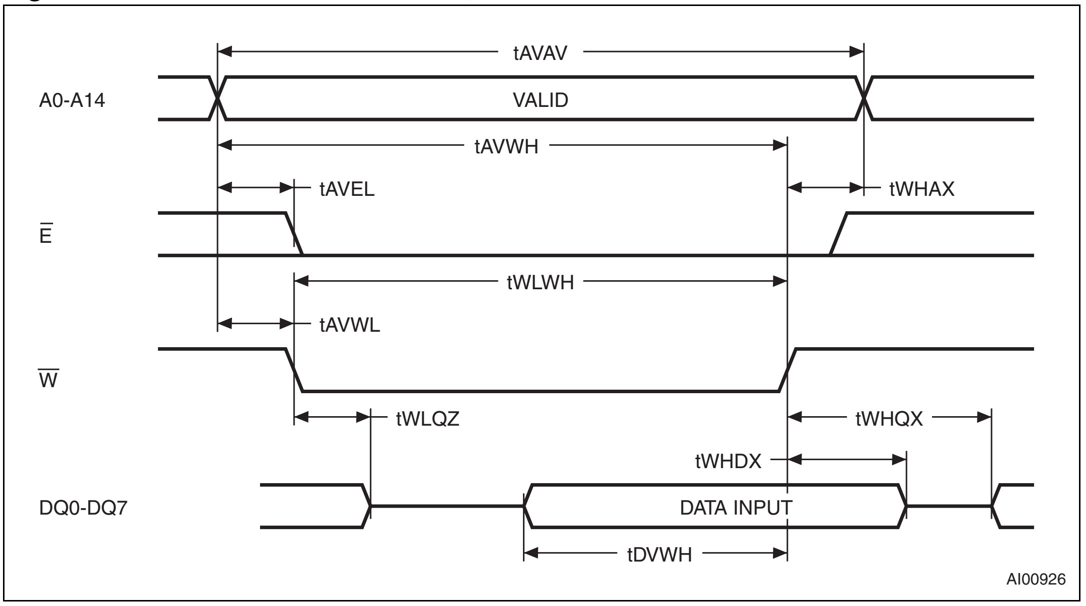


Figure 6. Chip enable controlled, WRITE AC waveforms

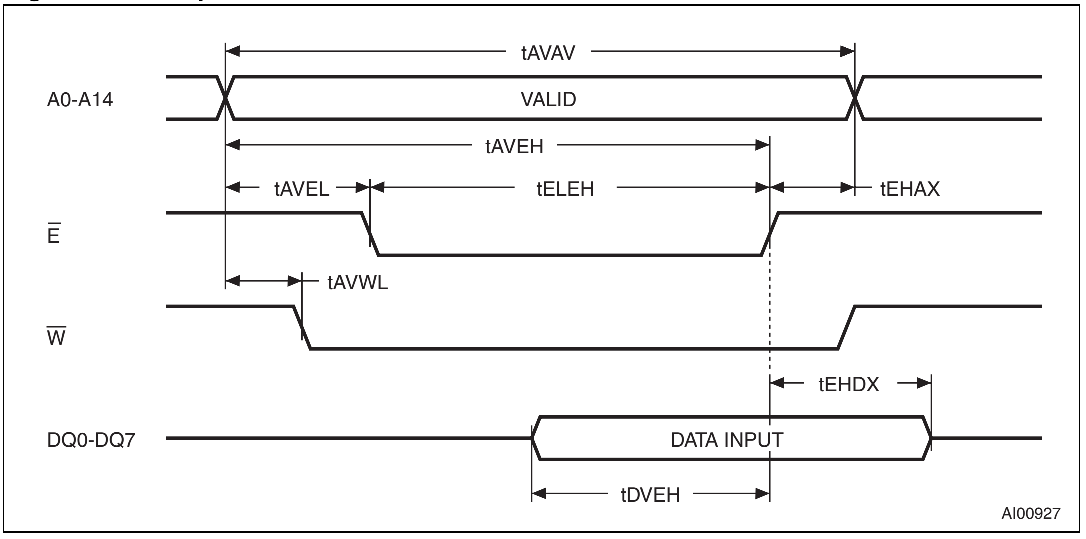


Table 4. WRITE mode AC characteristics

Symbol	Parameter(1)	M48T37Y		M48T37V		Unit
		–70		–100		
		Min	Max	Min	Max	
t_{AVAV}	WRITE cycle time	70		100		ns
t_{AVWL}	Address valid to WRITE enable low	0		0		ns
t_{AVEL}	Address valid to chip enable low	0		0		ns
t_{WLWH}	WRITE enable pulse width	50		80		ns
t_{ELEH}	Chip enable low to chip enable high	55		80		ns
t_{WHAX}	WRITE enable high to address transition	0		10		ns
t_{EHAX}	Chip enable high to address transition	0		10		ns
t_{DVWH}	Input valid to WRITE enable high	30		50		ns
t_{DVEH}	Input valid to chip enable high	30		50		ns
t_{WHDX}	WRITE enable high to input transition	5		5		ns
t_{EHDX}	Chip enable high to input transition	5		5		ns
t_{WLQZ}(2)(3)	WRITE enable low to output Hi-Z		25		50	ns
t_{AVWH}	Address valid to WRITE enable high	60		80		ns
t_{AVEH}	Address valid to chip enable high	60		80		ns
t_{WHQX}(2)(3)	WRITE enable high to output transition	5		10		ns

1. Valid for ambient operating temperature: T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5 to 5.5 V or 3.0 to 3.6 V (except where noted).
2. C_L = 5 pF.
3. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

2.3 Data retention mode

With valid V_{CC} applied, the M48T37Y/V operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. All outputs become high impedance, and all inputs are treated as “Don't care.”

Note: A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F

The M48T37Y/V may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended. When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery which preserves data and powers the clock. The internal button cell will maintain data in the M48T37Y/V for an accumulated period of at least 7 years at room temperature when V_{CC} is less than V_{SO}. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected and the power supply is switched to external V_{CC}. Normal RAM operation can resume t_{REC} after V_{CC} reaches V_{PFD} (max).

For more information on battery storage life refer to the application note AN1012.

3 Clock operations

3.1 Reading the clock

Updates to the TIMEKEEPER® registers should be halted before clock data is read to prevent reading data in transition. The BiPORT™ TIMEKEEPER cells in the RAM array are only data registers and not the actual clock counters, so updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ bit, D6 in the control register 7FF8h. As long as a '1' remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is, the day, date, and the time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating will resume within a second after the bit is reset to a '0.'

3.2 Setting the clock

Bit D7 of the control register (7FF8h) is the WRITE bit. Setting the WRITE bit to a '1,' like the READ bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24-hour BCD format (see *Table 5 on page 13*). Resetting the WRITE bit to a '0' then transfers the values of all time registers (7FF1h, 7FF9h-7FFFh) to the actual TIMEKEEPER counters and allows normal operation to resume. After the WRITE bit is reset, the next clock update will occur in approximately one second.

Note: Upon power-up following a power failure, both the WRITE bit and the READ bit will be reset to '0.'

3.3 Stopping and starting the oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is the MSB of the seconds register. Setting it to a '1' stops the oscillator. When reset to a '0,' the M48T37Y/V oscillator starts within one second.

Note: It is not necessary to set the WRITE bit when setting or resetting the FREQUENCY TEST bit (FT) or the STOP bit (ST).

Table 5. **Register map**

Address	Data								Function/range BCD format	
	D7	D6	D5	D4	D3	D2	D1	D0		
7FFFh	10 years				Year				Year	00-99
7FFEh	0	0	0	10 M	Month				Month	01-12
7FFDh	0	0	10 date		Date: Day of month				Date	01-31
7FFCh	0	FT	0	0	0	Day of week			Day	01-7
7FFBh	0	0	10 hours		Hours				Hours	00-23
7FFAh	0	10 minutes			Minutes				Min	00-59
7FF9h	ST	10 seconds			Seconds				Sec	00-59
7FF8h	W	R	S	Calibration					Control	
7FF7h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
7FF6h	AFE	0	ABE	0	0	0	0	0	Interrupts	
7FF5h	RPT4	0	Alarm 10 date		Alarm date				Alarm date	01-31
7FF4h	RPT3	0	Alarm 10 hours		Alarm hours				Alarm hour	00-23
7FF3h	RPT2	Alarm 10 minutes			Alarm minutes				Alarm min	00-59
7FF2h	RPT1	Alarm 10 seconds			Alarm seconds				Alarm sec	00-59
7FF1h	1000 year				100 year				Century	00-99
7FF0h	WDF	AF	Z	BL	Z	Z	Z	Z	Flags	

Keys:

S = Sign bit
FT = Frequency test bit
R = READ bit
W = WRITE bit
ST = Stop bit
0 = Must be set to '0'
BL = Battery low flag (read only)
BMB0-BMB4 = Watchdog multiplier bits
AFE = Alarm flag enable flag
RB0-RB1 = Watchdog resolution bits
WDS = Watchdog steering bit
ABE = Alarm in battery backup mode enable bit
RPT1-RPT4 = Alarm repeat mode bits
WDF = Watchdog flag (read only)
AF = Alarm flag (read only)
Z = '0' and are read only

3.4 Setting the alarm clock

Registers 7FF5h-7FF2h contain the alarm settings. The alarm can be configured to go off at a predetermined time on a specific day of the month or repeat every day, hour, minute, or second. It can also be programmed to go off while the M48T37Y/V is in the battery backup mode of operation to serve as a system wake-up call.

RPT1-RPT4 put the alarm in the repeat mode of operation. *Table 6* shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

Note: User must transition address (or toggle chip enable) to see flag bit change.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT1-RPT4, AF is set. If AFE is also set, the alarm condition activates the $\overline{\text{IRQ}}$/FT pin. To disable alarm, write '0' to the alarm date registers and RPT1-4. The alarm flag and the $\overline{\text{IRQ}}$/FT output are cleared by a READ to the flags register as shown in *Figure 7*. A subsequent READ of the flags register is necessary to see that the value of the alarm flag has been reset to '0.'

The $\overline{\text{IRQ}}$/FT pin can also be activated in the battery backup mode. The $\overline{\text{IRQ}}$/FT will go low if an alarm occurs and both the alarm in battery backup mode enable (ABE) and the AFE are set. The ABE and AFE bits are reset during power-up, therefore an alarm generated during power-up will only set AF. The user can read the flag register at system boot-up to determine if an alarm was generated while the M48T37Y/V was in the deselect mode during power-up. *Figure 8* illustrates the backup mode alarm timing.

Figure 7. Alarm interrupt reset waveform

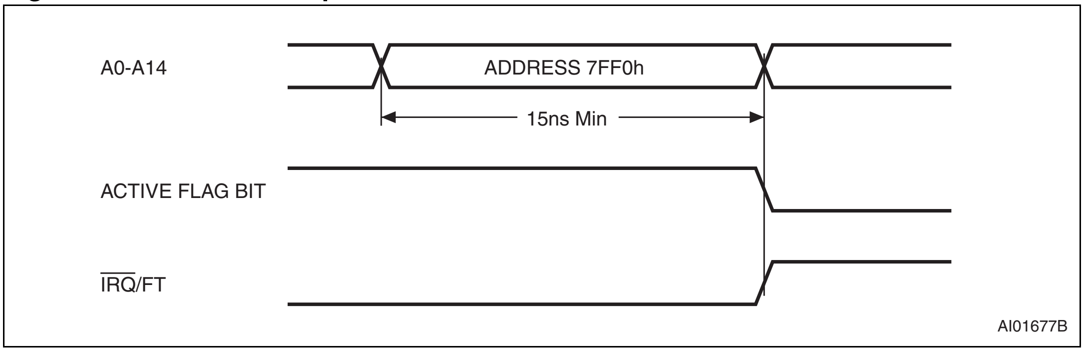
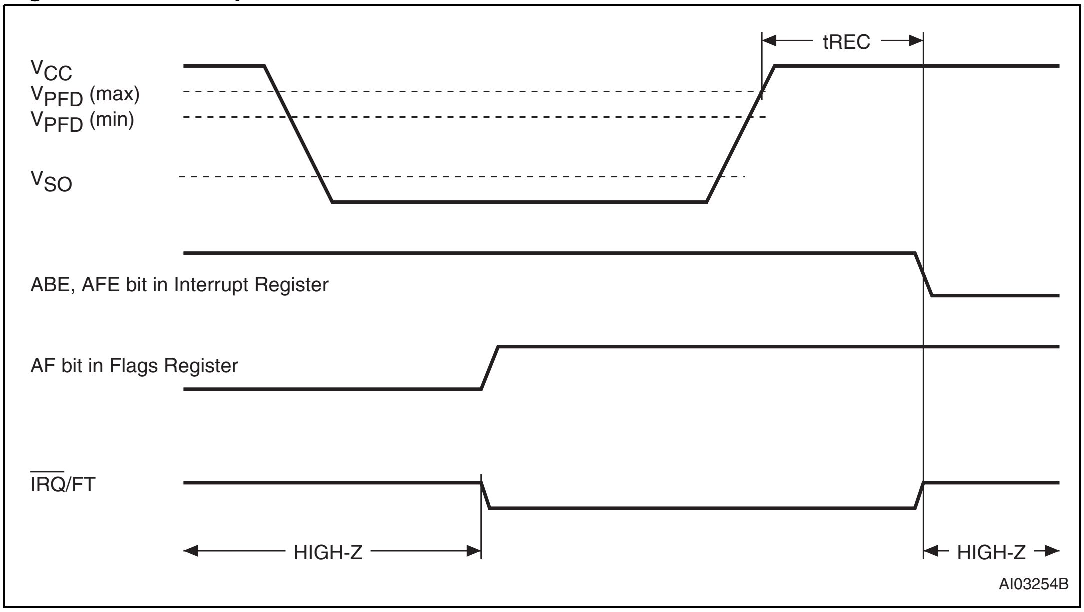


Table 6. Alarm repeat modes

RPT4	RPT3	RPT2	RPT1	Alarm activated
1	1	1	1	Once per second
1	1	1	0	Once per minute
1	1	0	0	Once per hour
1	0	0	0	Once per day
0	0	0	0	Once per month

Figure 8. Backup mode alarm waveforms



3.5 Calibrating the clock

The M48T37Y/V is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not to exceed ±35 ppm (parts per million) oscillator frequency error at 25 °C, which equates to about ±1.53 minutes per month. With the calibration bits properly set, the accuracy of each M48T37Y/V improves to better than +1/–2 ppm at 25 °C.

The oscillation rate of any crystal changes with temperature (see *Figure 10 on page 19*). Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The M48T37Y/V design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in *Figure 11 on page 19*. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five-bit calibration byte found in the control register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The calibration byte occupies the five lower order bits (D4-D0) in the control register 7FF8h. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is the sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125, 829, 120 (64 minutes x 60 seconds/minute x 32,768 cycles/second) actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M48T37Y/V may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWW broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of the $\overline{\text{IRQ}}$/FT pin. The pin will toggle at 512 Hz when the stop bit (ST, D7 of 7FF9h) is '0' the frequency test bit (FT, D6 of 7FFCh) is '1,' the alarm flag enable bit (AFE, D7 of 7FF6h) is '0,' and the watchdog steering bit (WDS, D7 of 7FF7h) is '1' or the watchdog register is reset (7FF7h=0).

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10(WR001010) to be loaded into the calibration byte for correction.

Note: Setting or changing the calibration byte does not affect the frequency test output frequency.

The $\overline{\text{IRQ}}$/FT pin is an open drain output which requires a pull-up resistor for proper operation. A 500-10 kΩ resistor is recommended in order to control the rise time. The FT bit is cleared on power-down.

For more information on calibration, see the application note AN934, “TIMEKEEPER calibration.”

3.6 Watchdog timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the eight-bit watchdog register, address 7FF7h. The five bits (BMB4-BMB0) that store a binary multiplier and the two lower order bits (RB1-RB0) select the resolution, where 00 = $^1/_{16}$ second, 01 = $^1/_4$ second, 10 = 1 second, and 11 = 4 seconds. The amount of time-out is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the watchdog register = 3x1, or 3 seconds).

Note: Accuracy of timer is within ± the selected resolution.

If the processor does not reset the timer within the specified period, the M48T37Y/V sets the watchdog flag (WDF) and generates a watchdog interrupt or a microprocessor reset. WDF is reset by reading the flags register (Address 7FF0h).

Note: User must transition address (or toggle chip enable) to see flag bit change.

Reset will not occur unless the addresses are stable at the flag location for at least 15 ns while the device is in the READ mode as shown in *Figure 9 on page 19*.

The most significant bit of the watchdog register is the watchdog steering bit. When set to a '0,' the watchdog will activate the $\overline{\text{IRQ}}$/FT pin when timed-out. When WDS is set to a '1,' the watchdog will output a negative pulse on the $\overline{\text{RST}}$ pin for a duration of t_{REC}. The watchdog register, the FT bit, AFE bit, and ABE bit will reset to a '0' at the end of a watchdog time-out when the WDS bit is set to a '1.'

The watchdog timer resets when the microprocessor performs a re-write of the watchdog register or an edge transition (low to high / high to low) on the WDI pin occurs. The timeout period then starts over.

The watchdog timer is disabled by writing a value of 00000000 to the eight bits in the watchdog register. Should the watchdog timer time out, a value of 00h needs to be written to the watchdog register in order to clear the IRQ/FT pin.

The watchdog function is automatically disabled upon power-down and the watchdog register is cleared. If the watchdog function is set to output to the $\overline{\text{IRQ}}$/FT pin and the frequency test function is activated, the watchdog or alarm function prevails and the frequency test function is denied. The WDI pin should be connected to V_{SS} if not used.

3.7 Power-on reset

The M48T37Y/V continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{\text{RST}}$ pulls low (open drain) and remains low on power-up for t_{REC} after V_{CC} passes V_{PFD}. $\overline{\text{RST}}$ is valid for all V_{CC} conditions. The $\overline{\text{RST}}$ pin is an open drain output and an appropriate resistor to V_{CC} should be chosen to control rise time (see *Figure 13 on page 22*).

3.8 Programmable interrupts

The M48T37Y/V provides two programmable interrupts: an alarm and a watchdog. When an interrupt condition occurs, the M48T37Y/V sets the appropriate flag bit in the flag register 7FF0h. The interrupt enable bits (AFE and ABE) in 7FF6h and the watchdog steering (WDS) bit in 7FF7h allow the interrupt to activate the $\overline{\text{IRQ}}$/FT pin.

The alarm flag and the $\overline{\text{IRQ}}$/FT output are cleared by a READ to the flags register. An interrupt condition reset will not occur unless the addresses are stable at the flag location for at least 15 ns while the device is in the READ mode as shown in *Figure 7 on page 14*.

The $\overline{\text{IRQ}}$/FT pin is an open drain output and requires a pull-up resistor (10 kΩ recommended) to V_{CC}. The pin remains in the high impedance state unless an interrupt occurs or the frequency test mode is enabled.

3.9 Battery low flag

The M48T37Y/V automatically performs periodic battery voltage monitoring upon power-up. The battery low flag (BL), bit D4 of the flags register 7FF0h, will be asserted high if the SNAPHAT® battery is found to be less than approximately 2.5 V. The BL flag will remain active until completion of battery replacement and subsequent battery low monitoring tests during the next power-up sequence.

If a battery low is generated during a power-up sequence, this indicates the battery voltage is below 2.5 V (approximately), which may be insufficient to maintain data integrity. Data should be considered suspect and verified as correct. A fresh battery should be installed. The SNAPHAT top may be replaced while V_{CC} is applied to the device.

Note: This will cause the clock to lose time during the interval the battery/crystal is removed.

Battery monitoring is a useful technique only when performed periodically. The M48T37Y/V only monitors the battery when a nominal V_{CC} is applied to the device. Thus applications which require extensive durations in the battery back-up mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique.

3.10 Initial power-on defaults

Upon application of power to the device, the following register bits are set to a '0' state: WDS; BMB0-BMB4; RB0-RB1; AFE; ABE; W; R; and FT (see *Table 7*).

Table 7. Default values

Condition	W	R	FT	AFE	ABE	Watchdog register(1)
Initial power-up (Battery attach for SNAPHAT®)(2)	0	0	0	0	0	0
Subsequent power-up / RESET(3)	0	0	0	0	0	0
Power-down(4)	0	0	0	1	1	0

1. WDS, BMB0-BMB4, RBO, RB1.
2. State of other control bits undefined.
3. State of other control bits remains unchanged.
4. Assuming these bits set to '1' prior to power-down.

3.11 V_{CC} noise and negative going transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1 µF (as shown in *Figure 9*) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommended to connect a Schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

Figure 9. Supply voltage protection

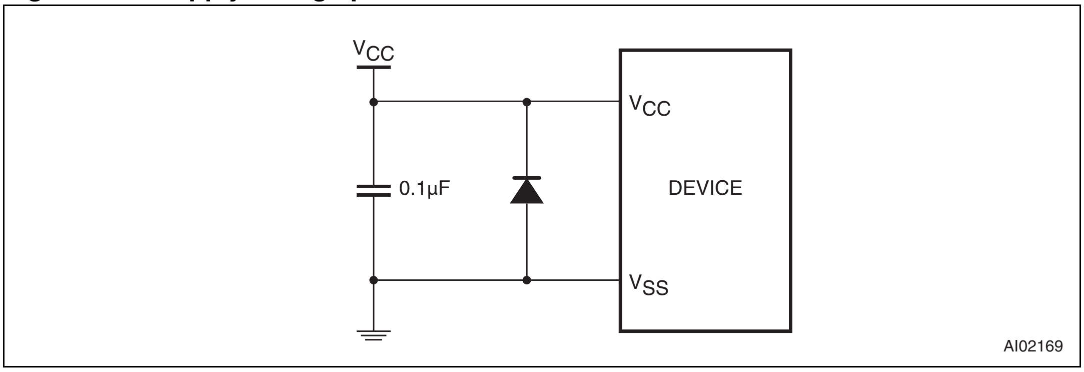


Figure 10. Crystal accuracy across temperature

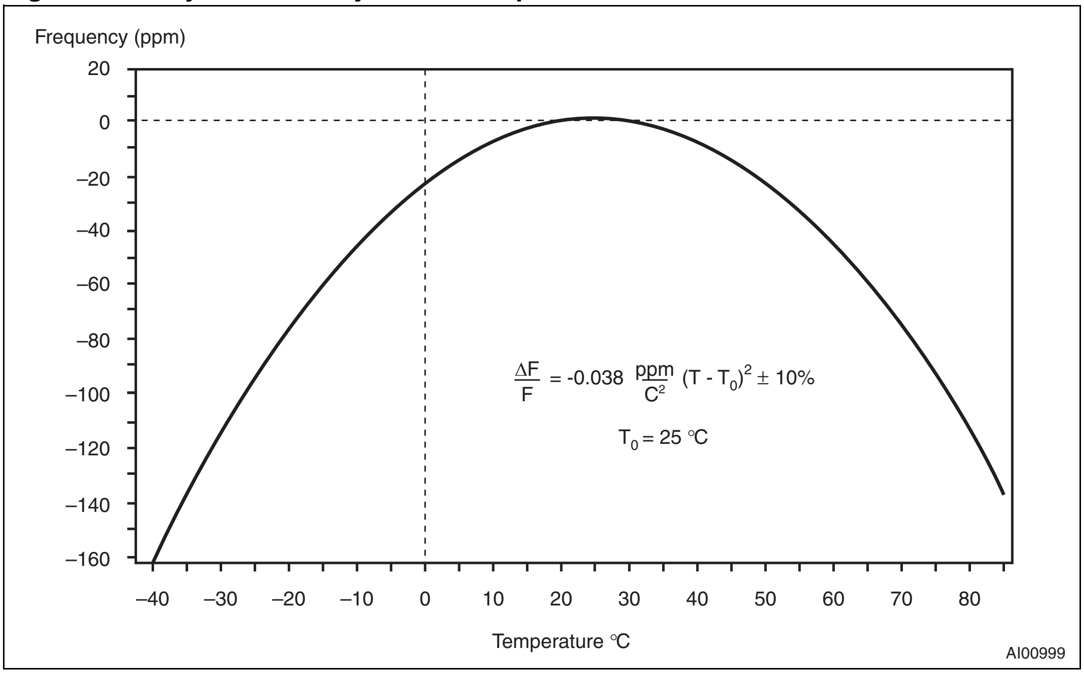
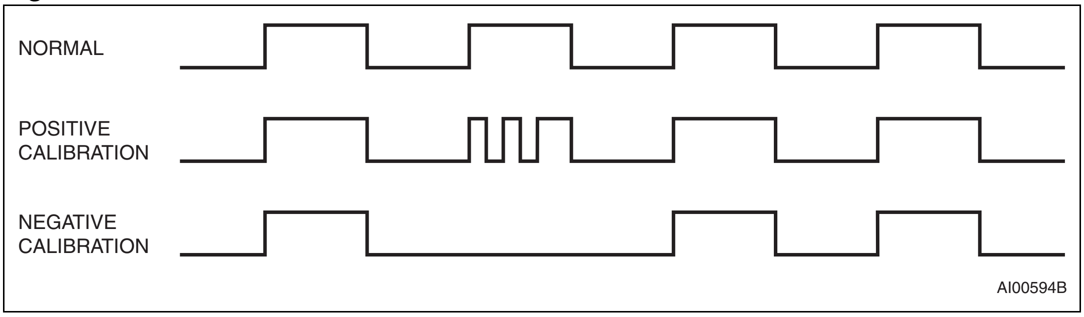


Figure 11. Clock calibration



4 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Parameter		Value	Unit
T_A	Ambient operating temperature	Grade 1	0 to 70	°C
		Grade 6	–40 to 85	°C
T_{STG}	Storage temperature (V_{CC} off, oscillator off)	SNAPHAT®	–40 to 85	°C
		SOH44	–55 to 150	°C
T_{SLD}[(1)]	Lead solder temperature for 10 seconds		260	°C
V_{IO}	Input or output voltages	M48T37Y	–0.3 to 7	V
		M48T37V	–0.3 to 4.6	V
V_{CC}	Supply voltage	M48T37Y	–0.3 to 7	V
		M48T37V	–0.3 to 4.6	V
I_O	Output current		10	mA
P_D	Power dissipation		1	W

1. For SOH44 package, lead-free (Pb-free) lead finish: reflow at peak temperature of 260 °C (the time above 255 °C must not exceed 30 seconds).

Caution: *Negative undershoots below –0.3 V are not allowed on any pin while in the battery backup mode.*

Caution: *Do NOT wave solder SOIC to avoid damaging SNAPHAT® sockets.*

5 DC and AC parameters

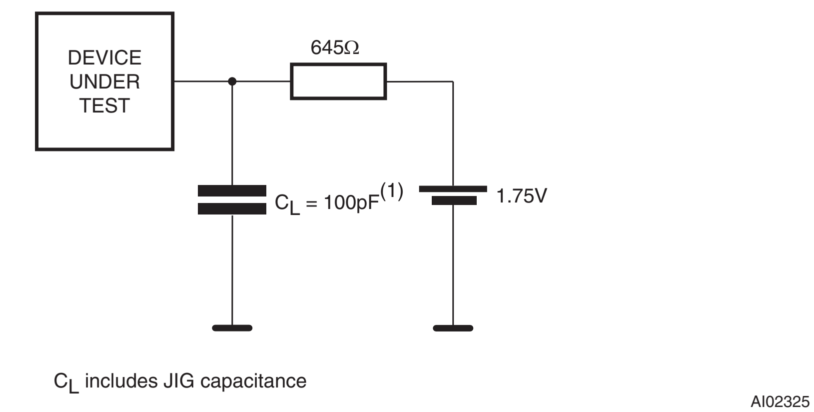
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 9. Operating and AC measurement conditions

Parameter		M48T37Y	M48T37V	Unit
Supply voltage (V_{CC})		4.5 to 5.5	3.0 to 3.6	V
Ambient operating temperature (T_A)	Grade 1	0 to 70	0 to 70	°C
	Grade 6	–40 to 85	–40 to 85	°C
Load capacitance (C_L)		100	50	pF
Input rise and fall times		≤ 10	≤ 10	ns
Input pulse voltages		0 to 3	0 to 3	V
Input and output timing ref. voltages		1.5	1.5	V

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 12. AC testing load circuit



1. 50 pF for M48T37V.

Note: Excluding open-drain output pins

Table 10. Capacitance

Symbol	Parameter[(1)(2)]	Min	Max	Unit
C_{IN}	Input capacitance	-	10	pF
C_{IO}[(3)]	Input / output capacitance	-	10	pF

1. Effective capacitance measured with power supply at 5 V. Sampled only, not 100% tested.
2. At 25 °C, f = 1 MHz.
3. Outputs deselected.

Table 11. DC characteristics

Symbol	Parameter	Test condition(1)	M48T37Y –70 Min	M48T37Y –70 Max	M48T37V –100 Min	M48T37V –100 Max	Unit
I_{LI}(2)	Input leakage current	$0\ V \le V_{IN} \le V_{CC}$		±1		±1	µA
I_{LO}(3)	Output leakage current	$0\ V \le V_{OUT} \le V_{CC}$		±1		±1	µA
I_{CC}	Supply current	Outputs open		50		33	mA
I_{CC1}	Supply current (standby) TTL	$\overline{E} = V_{IH}$		3		2	mA
I_{CC2}	Supply current (standby) CMOS	$\overline{E} = V_{CC} - 0.2\ V$		3		2	mA
V_{IL}	Input low voltage		–0.3	0.8	–0.3	0.8	V
V_{IH}	Input high voltage		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
V_{OL}	Output low voltage (standard)	$I_{OL} = 2.1\ mA$		0.4		0.4	V
	Output low voltage (open drain)	$I_{OL} = 10\ mA$		0.4		0.4	V
V_{OH}	Output high voltage	$I_{OH} = -1\ mA$	2.4		2.4		V

1. Valid for ambient operating temperature: T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5 to 5.5 V or 3.0 to 3.6 V (except where noted).
2. WDI internally pulled down to V_{SS} through a 100 kΩ resistor.
3. Outputs deselected.

Figure 13. Power down/up mode AC waveforms

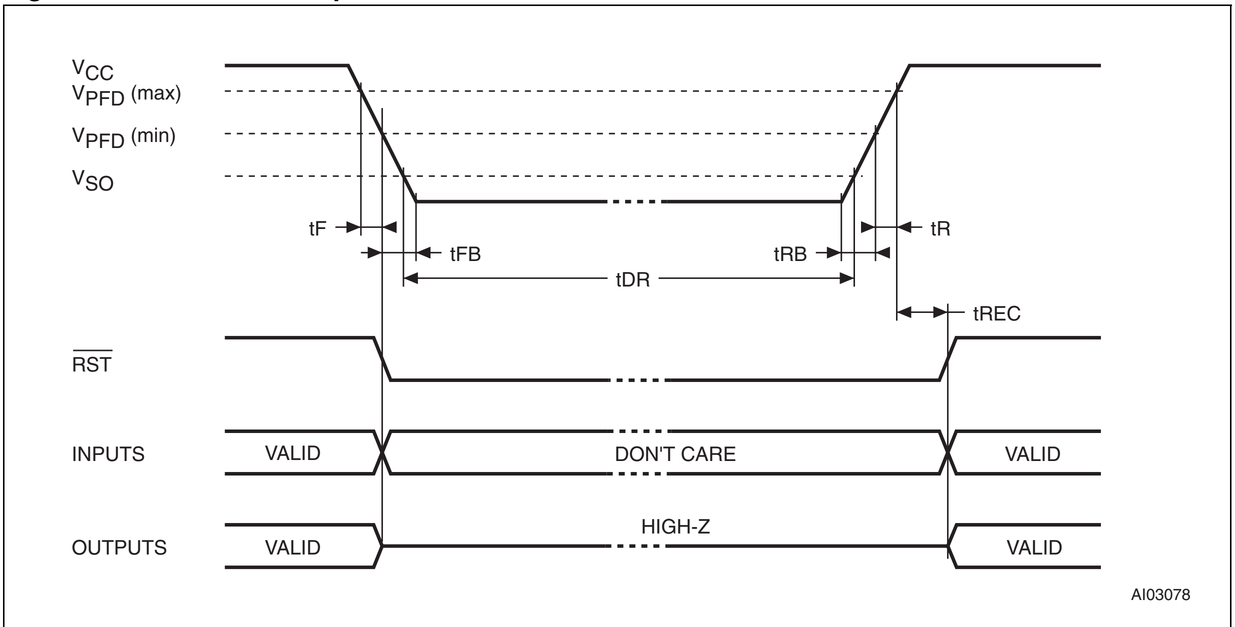


Table 12. Power down/up AC characteristics

Symbol	Parameter(1)	Min	Max	Unit
t_F(2)	V_{PFD} (max) to V_{PFD} (min) V_{CC} fall time	300		µs
t_{FB}(3)	V_{PFD} (min) to V_{SS} V_{CC} fall time	10		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} rise time	10		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} rise time	1		µs
t_{REC}(4)	V_{PFD} (max) to $\overline{RST}$ high	40	200	ms

1. Valid for ambient operating temperature: T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5 to 5.5 V or 3.0 to 3.6 V (except where noted).
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data
4. t_{REC} (min) = 20 ms for industrial temperature range - grade 6 device.

Table 13. Power down/up trip points DC characteristics

Symbol	Parameter(1)		Min	Typ	Max	Unit
V_{PFD}	Power-fail deselect voltage	M48T37Y	4.2	4.4	4.5	V
		M48T37V	2.7	2.9	3.0	V
V_{SO}	Battery backup switchover voltage	M48T37Y		V_{BAT}		V
		M48T37V		V_{PFD} –100 mV		V
t_{DR}(2)	Expected data retention time	Grade 1	5	7		Years
		Grade 6	10(3)			Years

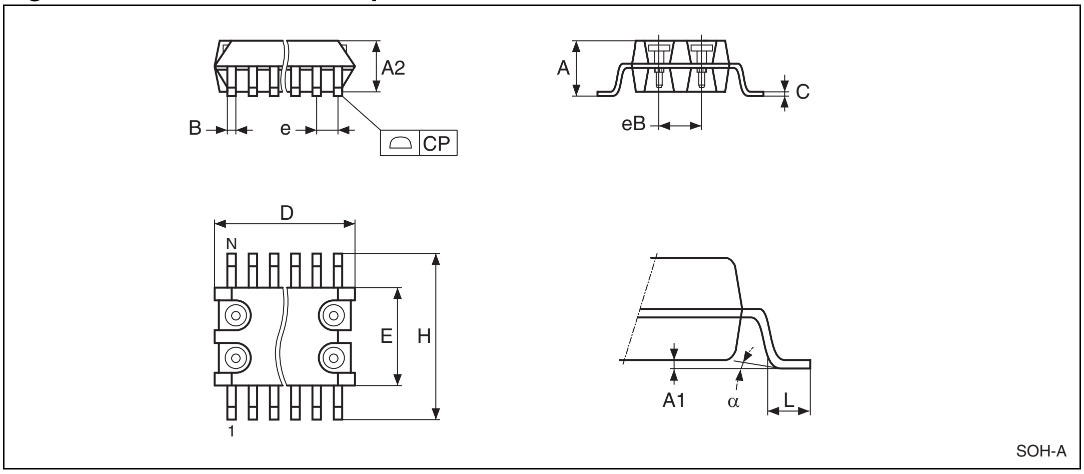
1. Valid for ambient operating temperature: T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5 to 5.5 V or 3.0 to 3.6 V (except where noted).
2. At 25 °C, V_{CC} = 0 V.
3. Using larger M4T32-BR12SH6 SNAPHAT® top (recommended for industrial temperature range - grade 6 device).

Note: All voltages referenced to V_{SS}.

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 14. SOH44 – 44-lead plastic small outline, 4-socket SNAPHAT® outline

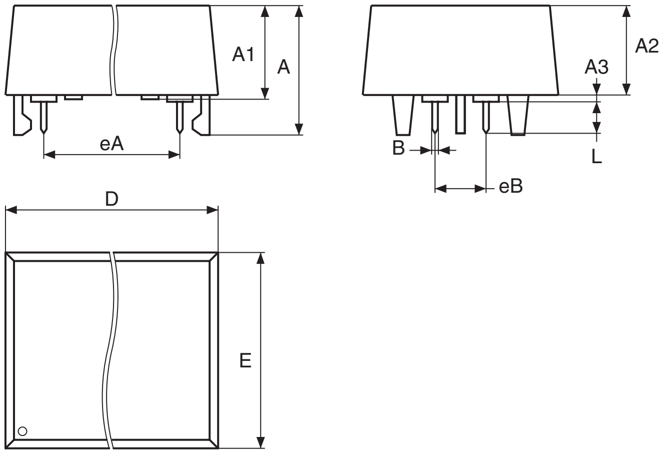


Note: Drawing is not to scale.

Table 14. SOH44 – 44-lead plastic small outline, 4-socket SNAPHAT®, package mechanical data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.46		0.014	0.018
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	0.81	–	–	0.032	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
a		0°	8°		0°	8°
N	44			44		
CP			0.10			0.004

Figure 15. SH – 4-pin SNAPHAT® housing for 48 mAh battery & crystal, pack. outline

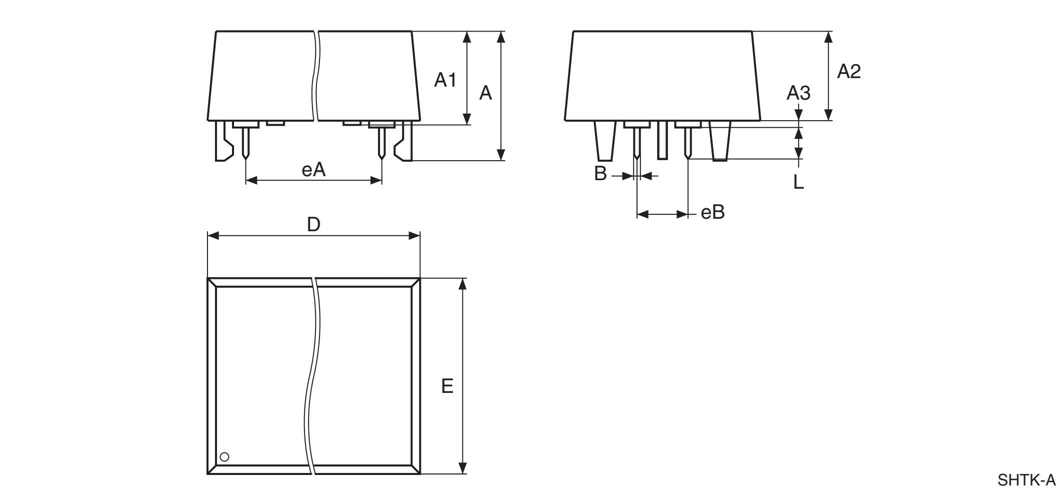


Note: Drawing is not to scale.

Table 15. SH – 4-pin SNAPHAT® housing for 48 mAh battery & crystal, package mechanical data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

Figure 16. SH – 4-pin SNAPHAT® housing for 120 mAh battery & crystal, pack. outline



Note: Drawing is not to scale.

Table 16. SH – 4-pin SNAPHAT® housing for 120 mAh battery & crystal, package mechanical data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			10.54			0.415
A1		8.00	8.51		0.315	.0335
A2		7.24	8.00		0.285	0.315
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		17.27	18.03		0.680	.0710
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

7 Part numbering

Table 17. Ordering information scheme

Example: M48T 37Y –70 MH 1 E

Device type

M48T

Supply voltage and write protect voltage

37Y = V_{CC} = 4.5 to 5.5 V; V_{PFD} = 4.2 to 4.5 V

37V = V_{CC} = 3.0 to 3.6 V; V_{PFD} = 2.7 to 3.0 V

Speed

–70 = 70 ns (37Y)

–10 = 100 ns (37V)

Package

MH[1] = SOH44

Temperature range

1 = 0 to 70 °C

6 = –40 to 85 °C[2]

Shipping method

blank = tubes (not for new design - use E)

E = ECOPACK® package, tubes

F = ECOPACK® package, tape & reel

TR = tape & reel (not for new design - use F)

1. The SOIC package (SOH44) requires the SNAPHAT® battery package which is ordered separately under the part number “M4TXX-BR12SH” in plastic tube or “M4TXX-BR12SHTR” in tape & reel form (see *Table*).
2. Not recommended for new design. Contact ST sales office for availability.

Caution: Do not place the SNAPHAT battery package “M4TXX-BR12SH” in conductive foam as it will drain the lithium button-cell battery.

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

Table 18. SNAPHAT® battery table

Part number	Description	Package
M4T28-BR12SH	Lithium battery (48 mAh) SNAPHAT®	SH
M4T32-BR12SH	Lithium battery (120 mAh) SNAPHAT®	SH

8 Environmental information

Figure 17. Recycling symbols

This product contains a non-rechargeable lithium (lithium carbon monofluoride chemistry) button cell battery fully encapsulated in the final product.

Recycle or dispose of batteries in accordance with the battery manufacturer's instructions and local/national disposal and recycling regulations.

Please refer to the following web site address for additional information regarding compliance statements and waste recycling.

Go to www.st.com/rtc, then select "Lithium Battery Recycling" from "Related Topics".

9 Revision history

Table 19. Document revision history

Date	Revision	Changes
Dec-1999	1	First issue
07-Feb-2000	2	From preliminary data to datasheet; battery low flag paragraph changed; 100 ns speed class identifier changed (*Table* , *4*)
11-Jul-2000	2.1	t_{FB} changed (*Table*); watchdog timer paragraph changed
19-Jun-2001	3	Reformatted; added temp./voltage info. to tables (*Table 10*, *11*, , *4*, ,)
06-Aug-2001	3.1	Fix text for setting the alarm clock (*Figure 7*)
15-Jan-2002	3.2	Fix footnote numbering (*Table*)
20-May-2002	3.3	Modify reflow time and temperature footnote (*Table 8*)
31-Mar-2003	4	v2.2 template applied; data retention condition updated (*Table*)
01-Apr-2004	5	Reformatted; updated with lead-free package information (*Table 8*,)
08-Feb-2006	6	New template; updated lead-free text; fixed DC characteristics (*Table 8*, *11*,)
03-Aug-2007	7	Reformatted; added lead-free second level interconnect information to cover page and *Section 6: Package mechanical data*.
24-Mar-2009	8	Updated *Table 8*; *Section 6: Package mechanical data*; added *Section 8: Environmental information*; minor reformatting.
02-Aug-2010	9	Updated *Features*, *Section 4*, *Table 17*; reformatted document; minor textual changes.