STM32H743xI

32-bit ARM® Cortex®-M7 400MHz MCU, up to 2MB Flash, 1MB RAM, 46 communication and analog interfaces, LCD-TFT & JPEG Codec

Data brief

Features

Core

- 32-bit ARM® Cortex®-M7 core with double-precision FPU and L1 cache: 16 KB of data and 16 KB of instruction cache allowing to fill one cache line in a single access from the 256-bit embedded Flash memory; frequency up to 400 MHz, MPU, 856 DMIPS/ 2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions

Memories

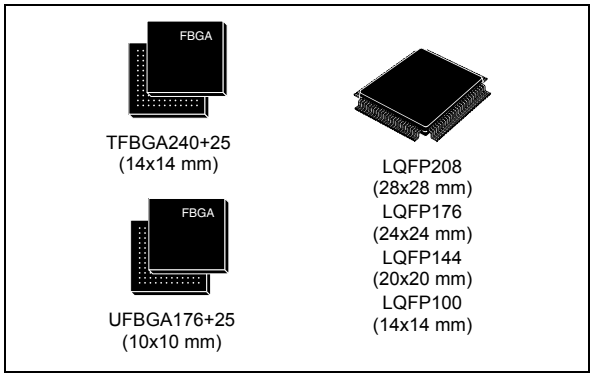
- Up to 2 MB of Flash memory with read while write support
- ~1 MB of RAM: 192 KB of TCM RAM (inc. 64 KB of ITCM RAM + 128 KB of DTCM RAM for time critical routines), 864 KB of user SRAM, and 4 KB of SRAM in Backup domain
- Dual mode Quad-SPI memory interface
- Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, NOR/NAND memories
- CRC calculation unit

Security

- ROP, PC-ROP, active tamper

Reset and power management

- 3 separate power domains which can be independently set in low-power mode to maximize power efficiency (clock gated or switched off):
  - D1: high-performance capabilities for high bandwidth peripherals
  - D2: dedicated to communication peripherals and timers
  - D3: reset and clock control, plus power management



- 1.62 to 3.6 V application supply and I/Os
- POR, PDR, PVD and BOR
- Dedicated USB power embedding a 3.3 V internal regulator to supply the internal PHYs
- Embedded regulator (LDO) with configurable scalable output to supply the digital circuitry
- Voltage scaling in Run and Stop mode
- Backup regulator (~0.9 V)
- Voltage reference for analog peripheral and V_{REF+}
- Low-power modes: Sleep, Stop and Standby

Low-power consumption

- Total current consumption down to 7 µA

Clock management

- Internal oscillators: 64 MHz HSI oscillator, 48 MHz RC oscillator, 4 MHz CSI oscillator, 40 kHz LSI oscillator
- External oscillators: 1-48 MHz HSE oscillator, 32.768 kHz LSE oscillator
- 3x PLLs (1 for the system clock, 2 for kernel clocks) with fractional mode

General-purpose input/outputs

- Up to 168 I/O ports with interrupt capability
  - Up to 4 fast I/Os up to 166 MHz

  - Up to 89 I/Os up to 83 MHz
  - Up to 164 5 V-tolerant I/Os

Interconnect matrix

- 3 bus matrices (1 AXI and 2 AHB)
- Bridges (5 * AHB2APB, 2 * AXI2AHB)

4 DMA controllers to unload the CPU

- 1× high-speed general-purpose master direct memory access controller (MDMA)
- 2× dual-port DMAs with FIFO and request router capabilities for optimal peripheral management
- 1× basic DMA with request router capabilities

Up to 35 communication peripherals

- 4× I2C FM+ interfaces (SMBus/PMBus)
- 4× USART/4x UARTs (ISO7816 interface, LIN, IrDA, modem control) and 1x LPUART
- 6× SPIs, including 3 with muxed duplex I2S audio class accuracy via internal audio PLL or external clock and 1 x I2S in LP domain
- 4x SAIs (serial audio interface)
- SPDIFRX interface
- SWPMI single-wire protocol master I/F
- MDIO Slave interface
- 2× SD/SDIO/MMC interfaces
- 2× CAN controllers supporting CAN FD protocol, out of which one supports time-triggered CAN (TT-CAN)
- 2× USB OTG interfaces (1FS, 1HS/FS)
- Ethernet MAC interface with DMA controller
- HDMI-CEC
- 8- to 14-bit camera interface up to 80 MHz

11 analog peripherals

- 3× ADCs with 16-bit max. resolution (14 bits 2.7 MSPS, 16 bits 168 kSPS)
- 1× temperature sensor
- 2× 12-bit D/A converters (1 MHz)
- 2× ultra-low-power comparators
- 2× operational amplifiers (8 MHz bandwidth)
- 1× digital filters for sigma delta modulator (DFSDM) with 8 channels/4 filters

Graphics

- LCD-TFT controller supporting up to XGA Resolution
- Chrom-ART Accelerator™ graphical hardware accelerator (DMA2D) for enhanced GUI to reduce CPU load
- Hardware JPEG Codec

Up to 22 timers and watchdogs

- 1× high-resolution timer (2.5 ns max resolution)
- 2× 32-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- 2× 16-bit advanced motor control timers
- 10× 16-bit general-purpose timers
- 5× 16-bit low-power timers
- 2× watchdogs (independent and window)
- 1× SysTick timer
- RTC with sub-second accuracy and hardware calendar

Debug mode

- SWD & JTAG interfaces
- 4 Kbyte Embedded Trace Buffer

2× true random number generators (3 oscillators each)

96-bit unique ID

All packages are ECOPACK®2 compliant

Table 1. Device summary

Reference	Part number
STM32H743xI	STM32H743VI, STM32H743ZI, STM32H743II, STM32H743BI, STM32H743XI

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1 Description

The STM32H743xI devices are based on the high-performance ARM® Cortex®-M7 32-bit RISC core operating at up to 400 MHz frequency. The Cortex® -M7 core features a floating point unit (FPU) which supports ARM® double-precision (IEEE 754 compliant) and single-precision data-processing instructions and data types. The STM32H743xI support a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32H743xI devices incorporate high-speed embedded memories with a dual-bank Flash memory up to 2 Mbytes, around 1 Mbytes of RAM (including 192 Kbytes of TCM RAM, 864 Kbytes of user SRAM and 4 Kbytes of backup SRAM), as well as an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses, a 32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memories access.

All the devices offer three ADCs, two DACs, two ultra-low power comparators, a low-power RTC, a high-resolution timer, 12 general-purpose 16-bit timers, two PWM timers for motor control, five low-power timers, a true random number generator (RNG). The devices support four digital filters for external sigma delta modulators (DFSDM). They also feature standard and advanced communication interfaces.

- Standard peripherals
  - Four I^2Cs
  - Four USARTs, four UARTs and one LPUART
  - Six SPIs, three I^2Ss in half-duplex mode. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
  - Four SAI serial audio interfaces
  - One SPDIFRX interface
  - One SWPMI (Single Wire Protocol Master Interface)
  - Management Data Input/Output (MDIO) slaves
  - Two SDMMC interfaces
  - An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI)
  - One FDCAN plus one TT-CAN interface
  - An Ethernet interface
  - Chrom-ART Accelerator™
  - HDMI-CEC
- Advanced peripherals including
  - A flexible memory control (FMC) interface
  - A Quad-SPI Flash memory interface
  - A camera interface for CMOS sensors
  - An LCD-TFT display controller
  - A JPEG hardware compressor/decompressor

Refer to *Table 2: STM32H743xI features and peripheral counts* for the list of peripherals available on each part number.

The STM32H743xI devices operate in the –40 to +85 °C temperature range from a 1.62 to 3.6 V power supply. The supply voltage can drop down to 1.62 V by using an external power supervisor (see *Section 2.5.2: Power supply supervisor)* and connecting PDR_ON pin to V_{SS}. Otherwise the supply voltage must stay above 1.71 V with the embedded power voltage detector enabled.

Dedicated supply inputs for USB (OTG_FS and OTG_HS) are available on all packages except LQFP100 for greater power supply choice.

A comprehensive set of power-saving mode allows designing low-power applications.

The STM32H743xI devices offer devices in 6 packages ranging from 100 pins to 240 pins/balls. The set of included peripherals changes with the device chosen.

These features make the STM32H743xI microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile applications, Internet of Things
- Wearable devices: smart watches.

Figure 1 shows the general block diagram of the device family.

Table 2. STM32H743xI features and peripheral counts

Peripherals		STM32H 743VI	STM32H 743ZI	STM32H 743II	STM32H 743BI	STM32H 743XI
Flash memory in Kbytes		2048				
SRAM in Kbytes	SRAM mapped onto AXI bus	512				
	SRAM1 (D2 domain)	128				
	SRAM2 (D2 domain)	128				
	SRAM3 (D2 domain)	32				
	SRAM4 (D3 domain)	64				
TCM RAM in Kbytes	ITCM RAM (instruction)	64				
	DTCM RAM (data)	128				
Backup SRAM (Kbytes)		4				
FMC		Yes				
Quad-SPI		Yes				
Ethernet		Yes				

Table 2. STM32H743xI features and peripheral counts (continued)

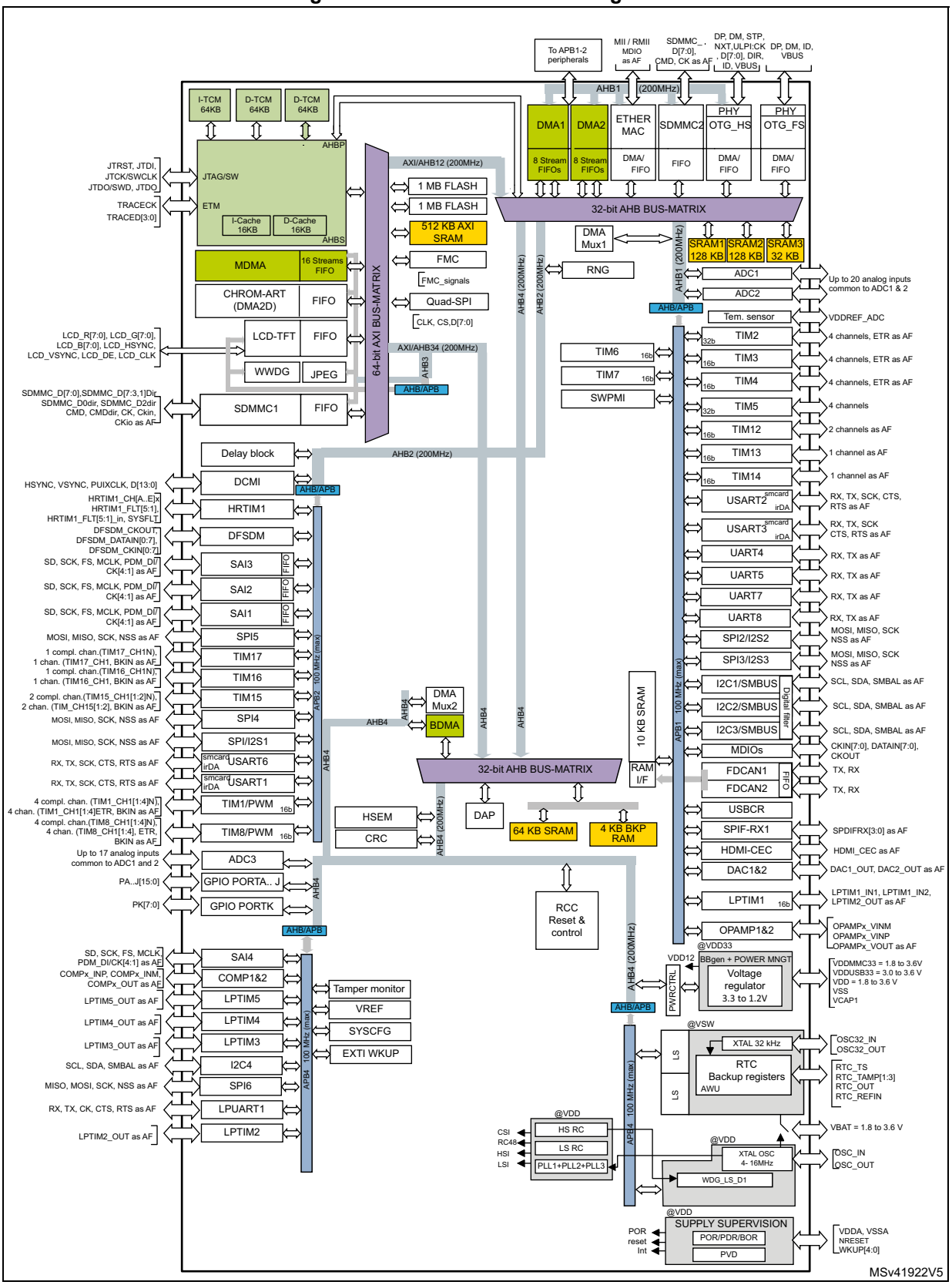
Peripherals		STM32H 743VI	STM32H 743ZI	STM32 743II	STM32H 743BI	STM32H 743XI
Timers	High-resolution	1				
	General-purpose	10				
	Advanced-control (PWM)	2				
	Basic	2				
	Low-power	5				
Random number generator		Yes				
Communication interfaces	SPI / I^2S	6/3(1)				
	I^2C	4				
	USART/UART/ LPUART	4/4 /1				
	SAI	4				
	SPDIFRX	4 inputs				
	SWPMI	Yes				
	MDIO	Yes				
	SDMMC	2				
	FDCAN/TT-CAN	1/1				
	USB OTG FS	Yes				
	USB OTG HS	Yes				
Ethernet and camera interface		Yes				
LCD-TFT		Yes				
JPEG Codec		Yes				
Chrom-ART Accelerator™ (DMA2D)		Yes				
GPIOs		Up to 168				
8 to 16-bit ADCs		3				
Number of channels		20				
12-bit DAC		Yes				
Number of channels		2				
Comparators		2				
Operational amplifiers		2				
DFSDM		Yes				
Maximum CPU frequency		400 MHz				
Operating voltage		1.71 to 3.6 V(2)	1.62 to 3.6 V(3)			

Table 2. STM32H743xI features and peripheral counts (continued)

Peripherals	STM32H 743VI	STM32H 743ZI	STM32 743II	STM32H 743BI	STM32H 743XI
Operating temperatures	Ambient temperatures: –40 to +85 °C				
	Junction temperature: –40 to + 125 °C				
Package	LQFP100	LQFP144	LQFP 176 UFBGA 176+25	LQFP 208	TFBGA 240+25

1. The SPI1, SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
2. Since the LQFP100 package does not feature the PDR_ON pin (tied internally to V_{DD}), the minimum V_{DD} value for this package is 1.71 V.
3. V_{DD}/V_{DDA} can drop down to 1.62 V by using an external power supervisor (see *Section 2.5.2: Power supply supervisor*) and connecting PDR_ON pin to V_{SS}. Otherwise the supply voltage must stay above 1.71 V with the embedded power voltage detector enabled.

Figure 1. STM32H743xI block diagram



2 Functional overview

2.1 ARM® Cortex®-M7 with FPU

The ARM® Cortex®-M7 with double-precision FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and optimized power consumption, while delivering outstanding computational performance and low interrupt latency.

The Cortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard architecture with L1 caches (16 Kbytes of I-cache and 16 Kbytes of D-cache)
- 64-bit AXI4 interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The following memory interfaces are supported:

- Separate Instruction and Data buses (Harvard Architecture) to optimize CPU latency
- Tightly Coupled Memory (TCM) interface designed for fast and deterministic SRAM accesses
- AXI Bus interface to optimize Burst transfers
- Dedicated low-latency AHB-Lite peripheral bus (AHBP) to connect to peripherals.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

It also supports single and double precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

Figure 1 shows the general block diagram of the STM32H743xI family.

Note: Cortex®-M7 with FPU core is binary compatible with the Cortex®-M4 core.

2.2 Memory protection unit (MPU)

The memory protection unit (MPU) manages the CPU access rights and the attributes of the system resources. It has to be programmed and enabled before use. Its main purposes are to prevent an untrusted user program to accidentally corrupt data used by the OS and/or by a privileged task, but also to protect data processes or read-protect memory regions.

The MPU defines access rules for privileged accesses and user program accesses. It allows defining up to 16 protected regions that can in turn be divided into up to 8 independent subregions, where region address, size, and attributes can be configured. The protection area ranges from 32 bytes to 4 Gbytes of addressable memory.

When an unauthorized access is performed, a memory management exception is generated.

2.3 Memories

2.3.1 Embedded Flash memory

The STM32H743xI devices embed up to 2 Mbytes of Flash memory that can be used for storing programs and data.

The Flash memory is organized as 266-bit Flash words memory that can be used for storing both code and data constants. Each word consists of:

- One Flash word (8 words, 32 bytes or 256 bits)
- 10 ECC bits.

The Flash memory is divided into two independent banks. Each bank is organized as follows:

- A 1 Mbyte user Flash memory block containing eight user sectors of 128 Kbytes(4 K Flash words)
- 128 Kbytes of System Flash memory from which the device can boot
- 2 Kbytes (64 Flash words) of user option bytes for user configuration

2.3.2 Embedded SRAM

All devices feature:

- 512 Kbytes of AXI-SRAM mapped onto AXI bus on D1 domain.
- SRAM1 mapped on D2 domain: 128 Kbytes
- SRAM2 mapped on D2 domain: 128 Kbytes
- SRAM3 mapped on D2 domain: 32 Kbytes
- SRAM4 mapped on D3 domain: 64 Kbytes
- 4 Kbytes of backup SRAM

  The content of this area is protected against possible unwanted write accesses, and is retained in Standby or V_{BAT} mode.
- RAM mapped to TCM interface (ITCM and DTCM):

  Both ITCM and DTCM RAMs are 0 wait state memories that are accessible from the CPU, or MDMA (even in Sleep mode) through specific AHB slave of the CPU (AHBP).
  - 64 Kbytes of ITCM-RAM (instruction RAM)

    This RAM is connected to ITCM 64-bit interface designed for execution of critical real-times routines by the CPU.
  - 128 Kbytes of DTCM-RAM (2x 64 Kbyte DTCM-RAMs on 2x32-bit DTCM ports)

    The DTCM-RAM could be used for critical real-time data, such as interrupt service routines or stack/heap memory. Both DTCM-RAMs can be used in parallel (for load/store operations) thanks to the Cortex-M7 dual issue capability.

2.4 Boot modes

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:

- All Flash address space
- All RAM address space: ITCM, DTCM RAMs and SRAMs
- The System memory bootloader

The boot loader is located in non-user system memory. It is used to reprogram the Flash memory through a serial interface (USART, I2C, SPI, USB-DFU, USB-MSC or CAN). Refer to *STM32 microcontroller system memory boot mode* application note (AN2606) for details.

2.5 Power supply management

2.5.1 Power supply scheme

- V_{DD} = 1.62 to 3.6 V: external power supply for I/Os, provided externally through V_{DD} pins.
- V_{DDLDO} = 1.8 to 3.6 V: supply voltage for the internal regulator supplying V_{CORE}
- V_{DDA} = 1.7 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL.
- $V_{DD33USB}$ and $V_{DD50USB}$:
  $V_{DD50USB}$ can be supplied through the USB cable to generate the $V_{DD33USB}$ via the USB internal regulator. This allows supporting a V_{DD} supply different from 3.3 V.
  The USB regulator can be bypassed to supply directly $V_{DD33USB}$ if V_{DD} = 3.3 V.
- V_{BAT} = 1.2 to 3.6 V: power supply for the V_{SW} domain when V_{DD} is not present.
- $V_{CAP1}/V_{CAP2}/V_{CAP3}$: V_{CORE} supplies, which values depend on voltage scaling (0.7 V, 0.9 V, 1.0 V, 1.1 V or 1.2 V). They are configured through VOS bits in PWR_CR3 register. The V_{CORE} domain is split into the following power domains that can be independently switch off.
  - D1 domain containing some peripherals and the Cortex®-M7 core.
  - D2 domain containing a large part of the peripherals.
  - D3 domain containing some peripherals and the system control.

2.5.2 Power supply supervisor

The devices have an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry:

- Power-on reset (POR)

  The POR supervisor monitors V_{DD} power supply and compares it to a fixed threshold. The devices remain in reset mode when V_{DD} is below this threshold,

- Power-down reset (PDR)

  The PDR supervisor monitors V_{DD} power supply. A reset is generated when V_{DD} drops below a fixed threshold.

  The PDR supervisor can be enabled/disabled through PDR_ON pin.

- Brownout reset (BOR)

  The BOR supervisor monitors V_{DD} power supply. Three BOR thresholds (from 2.1 to 2.7 V) can be configured through option bytes. A reset is generated when V_{DD} drops below this threshold.

2.5.3 Voltage regulator

The same voltage regulator supplies the 3 power domains (D1, D2 and D3). D1 and D2 can be independently switched off.

Voltage regulator output can be adjusted according to application needs through 5 power supply levels:

- Run mode (VOS1 to VOS3)
  - Scale 1: high performance
  - Scale 2: medium performance and consumption
  - Scale 3: optimized performance and low-power consumption
- Stop mode (SVOS3 to SVOS5)
  - Scale 3: peripheral with wakeup from stop mode capabilities (UART, SPI, I2C, LPTIM) are operational
  - Scale 4 and 5 where the peripheral with wakeup from Stop mode is disabled

    The peripheral functionality is disabled but wakeup from Stop mode is possible through GPIO or asynchronous interrupt.

2.6 Low-power strategy

There are several ways to reduce power consumption on STM32H743xI:

- Decrease dynamic power consumption by slowing down the system clocks even in Run mode and individually clock gating the peripherals that are not used.
- Save power consumption when the CPU is IDLE, by selecting among the available low-power mode according to the user application needs. This allows achieving the best compromise between short startup time, low-power consumption, as well as available wakeup sources.

The devices feature several low-power modes:

- CSleep (CPU clock stopped)
- CStop (CPU sub-system clock stopped)
- DStop (Domain bus matrix clock stopped)
- Stop (System clock stopped)
- DStandby (Domain powered down)
- Standby (System powered down)

CSleep and CStop low-power modes are entered by the MCU when executing the WFI (Wait for Interrupt) or WFE (Wait for Event) instructions, or when the SLEEPONEXIT bit of the Cortex-Mx core is set after returning from an interrupt service routine.

A domain can enter low-power mode (DStop or DStandby) when the processor, its subsystem and the peripherals allocated in the domain enter low-power mode.

If part of the domain is not in low-power mode, the domain remains in the current mode.

Finally the system can enter Stop or Standby when all EXTI wakeup sources are cleared and the power domains are in DStop or DStandby mode.

Table 3. System vs domain low-power mode

System power mode	D1 domain power mode	D2 domain power mode	D3 domain power mode
Run	DRun/DStop/DStandby	DRun/DStop/DStandby	DRun
Stop	DStop/DStandby	DStop/DStandby	DStop
Standby	DStandby	DStandby	DStandby

2.7 Reset and clock controller (RCC)

The clock and reset controller is located in D3 domain. The RCC manages the generation of all the clocks, as well as the clock gating and the control of the system and peripheral resets. It provides a high flexibility in the choice of clock sources and allows to apply clock ratios to improve the power consumption. In addition, on some communication peripherals that are capable to work with two different clock domains (either a bus interface clock or a kernel peripheral clock), the system frequency can be changed without modifying the baudrate.

2.7.1 Clock management

The devices embed four internal oscillators, two oscillators with external crystal or resonator, two internal oscillators with fast startup time and three PLLs.

The RCC receives the following clock source inputs:

- Internal oscillators:
  - 64 MHz HSI clock (1% accuracy)
  - 48 MHz RC oscillator
  - 4 MHz CSI clock
  - 32 kHz LSI clock
- External oscillators:
  - 4-48 MHz HSE clock
  - 32.768 kHz LSE clock

The RCC provides three PLLs: one for system clock, two for kernel clocks.

The system starts on the HSI clock. The user application can then select the clock configuration.

2.7.2 System reset sources

Power-on reset initializes all registers while system reset reinitializes the system except for the debug, part of the RCC and power controller status registers, as well as the backup power domain.

A system reset is generated in the following cases:

- Power-on reset (pwr_por_rst)
- Brownout reset
- Low level on NRST pin (external reset)
- Window watchdog
- Independent watchdog
- Software reset
- Low-power mode security reset
- Exit from Standby
- Exit for DStandby.

2.8 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

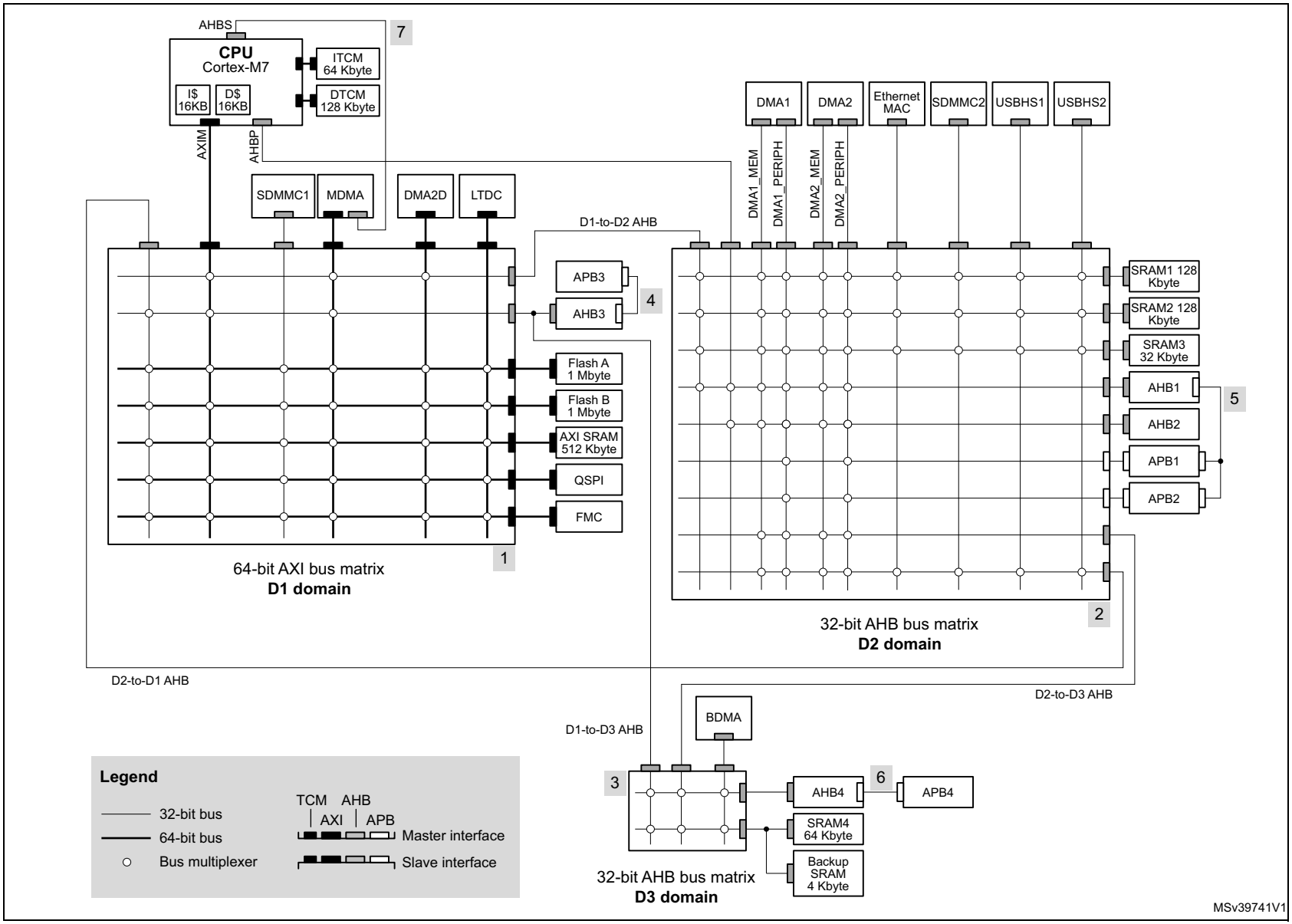
After reset, all GPIOs are in Analog mode to reduce power consumption.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.9 Bus-interconnect matrix

The devices feature an AXI bus matrix, two AHB bus matrices and bus bridges that allow interconnecting bus masters with bus slaves (see *Figure 2*).

Figure 2. STM32H743xI bus matrix



2.10 DMA controllers

The devices feature four DMA instances to unload CPU activity:

- A master direct memory access (MDMA)

  The MDMA is a high-speed DMA controller, which is in charge of all types of memory transfers (peripheral to memory, memory to memory, memory to peripheral), without any CPU action. It features a master AXI interface and a dedicated AHB interface to access Cortex-M7 TCM memories.

  The MDMA is located in D1 domain. It is able to interface with the other DMA controllers located in D2 domain to extend the standard DMA capabilities, or can manage peripheral DMA requests directly.

  Each of the 16 channels can perform single block transfers, repeated block transfers and linked list transfers.
- Two dual-port DMAs (DMA1, DMA2) located in D2 domain, with FIFO and request router capabilities.
- One basic DMA (BDMA) located in D3 domain, with request router capabilities.

The DMA request router could be considered as an extension of the DMA controller. It routes the DMA peripheral requests to the DMA controller itself. This allowing managing the DMA requests with a high flexibility, maximizing the number of DMA requests that run concurrently, as well as generating DMA requests from peripheral output trigger or DMA event.

2.11 Chrom-ART Accelerator™ (DMA2D)

The Chrom-Art Accelerator™ (DMA2D) is a graphical accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion

Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables. The DMA2D also supports block based YCbCr to handle JPEG decoder output.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

2.12 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 150 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M7 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor context automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

2.13 Extended interrupt and event controller (EXTI)

The EXTI controller performs interrupt and event management. In addition, it can wake up the processor, power domains and/or D3 domain from Stop mode.

The EXTI handles up to 89 independent event/interrupt lines split as 28 configurable events and 61 direct events.

Configurable events have dedicated pending flags, active edge selection, and software trigger capable.

Direct events provide interrupts or events from peripherals having a status flag.

2.14 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a programmable polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.15 Flexible memory controller (FMC)

The FMC controller main features are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (4 memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- 8-,16-,32-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is HCLK/2

2.16 Quad-SPI memory interface (QUADSPI)

All devices embed a Quad-SPI memory interface, which is a specialized communication interface targeting Single, Dual or Quad-SPI Flash memories. It supports both single and double datarate operations.

It can operate in any of the following modes:

- Direct mode through registers
- External flash status register polling mode
- Memory mapped mode.

Up to 256 Mbytes of external Flash memory can be mapped, and 8-, 16- and 32-bit data accesses are supported as well as code execution.

The opcode and the frame format are fully programmable.

2.17 Analog-to-digital converters (ADCs)

The STM32H743xI devices embed three analog-to-digital converters, which resolution can be configured to 16, 14, 12, 10 or 8 bits. Each ADC shares up to 20 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller, thus allowing to automatically transfer ADC converted values to a destination location without any software action.

In addition, an analog watchdog feature can accurately monitor the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM6, TIM8, TIM15, HRTIM1 and LPTIM1 timer.

2.18 Temperature sensor

The STM32H743xI embeds a temperature sensor that generates a voltage (V_{TS}) that varies linearly with the temperature. This temperature sensor is internally connected to ADC3_IN18. The conversion range is between 1.7 V and 3.6 V. It can measure the device ambient temperature ranging from − 40 to +125 °C with a precision of +-2%.

The temperature sensor have a good linearity, but it has to be calibrated to obtain a good overall accuracy of the temperature measurement. As the temperature sensor offset varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only. To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, which is accessible in read-only mode.

2.19 V_{BAT} operation

The V_{BAT} power domain contains the RTC, the backup registers and the backup SRAM.

To optimize battery duration, this power domain is supplied by V_{DD} when available or by the voltage applied on VBAT pin (when V_{DD} supply is not present). V_{BAT} power is switched when the PDR detects that V_{DD} dropped below the PDR level.

The voltage on the VBAT pin could be provided by an external battery, a supercapacitor or directly by V_{DD}, in which case, the V_{DD} mode is not functional.

V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers and the backup SRAM.

Note: When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.

When PDR_ON pin is connected to V_{SS} (Internal Reset OFF), the V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}.

2.20 Digital-to-analog converters (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel including DMA underrun error detection
- external triggers for conversion
- input voltage reference V_{REF+} or internal VREFBUF reference.

The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

2.21 Ultra-low-power comparators (COMP)

The STM32H743xI devices embed two rail-to-rail comparators (COMP1 and COMP2). They feature programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) as well as selectable output polarity.

The reference voltage can be one of the following:

- An external I/O
- A DAC output channel
- An internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers, and be combined into a window comparator.

2.22 Operational amplifiers (OPAMP)

The STM32H743xI devices embed two rail-to-rail operational amplifiers (OPAMP1 and OPAMP2) with external or internal follower routing and PGA capability.

The operational amplifier main features are:

- PGA with a non-inverting gain ranging of 2, 4, 8 or 16 or inverting gain ranging of -1, -3, -7 or -15
- One positive input connected to DAC
- Output connected to internal ADC
- Low input bias current down to 1 nA
- Low input offset voltage down to 1.5 mV
- Gain bandwidth up to 8 MHz

The devices embeds two operational amplifiers (OPMAP1 and OPAMP2) with two inputs and one output each. These three I/Os can be connected to the external pins, thus enabling any type of external interconnections. The operational amplifiers can be configured internally as a follower, as an amplifier with a non-inverting gain ranging from 2 to 16 or with inverting gain ranging from -1 to -15.

2.23 Digital filter for Sigma-Delta Modulators (DFSDM)

The device embeds one DFSDM with 4 digital filters modules and 8 external input serial channels (transceivers) or alternately 8 internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs). DFSDM can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in hardware. DFSDM features optional parallel data stream inputs from internal ADC peripherals or microcontroller memory (through DMA/CPU transfers into DFSDM).

DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators). DFSDM digital filter modules perform digital processing according user selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- 8 multiplexed input digital serial channels:
  - configurable SPI interface to connect various SD modulator(s)
  - configurable Manchester coded 1 wire interface support
  - PDM (Pulse Density Modulation) microphone input support
  - maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - clock output for SD modulator(s): 0..20 MHz
- alternative inputs from 8 internal digital parallel channels (up to 16 bit input resolution):
  - internal sources: ADC data or memory data streams (DMA)
- 4 digital filter modules with adjustable digital signal processing:
  - $Sinc^x$ filter: filter order/type (1..5), oversampling ratio (up to 1..1024)
  - integrator: oversampling ratio (1..256)
- up to 24-bit output data resolution, signed output data format
- automatic data offset correction (offset stored in register by user)
- continuous or single conversion
- start-of-conversion triggered by:
  - software trigger
  - internal timers
  - external events
  - start-of-conversion synchronously with first digital filter module (DFSDM0)
- analog watchdog feature:
  - low value and high value data threshold registers
  - dedicated configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
  - input from final output data or from selected input digital serial channels
  - continuous monitoring independently from standard conversion

- short circuit detector to detect saturated analog input values (bottom and top range):
  - up to 8-bit counter to detect 1..256 consecutive 0's or 1's on serial data stream
  - monitoring continuously each input serial channel
- break signal generation on analog watchdog event or on short circuit detector event
- extremes detector:
  - storage of minimum and maximum values of final conversion data
  - refreshed by software
- DMA capability to read the final conversion data
- interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence
- "regular" or "injected" conversions:
  - "regular" conversions can be requested at any time or even in continuous mode without having any impact on the timing of "injected" conversions
  - "injected" conversions for precise timing and with high conversion priority

2.24 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can achieve a data transfer rate up to 140 Mbyte/s using a 80 MHz pixel clock. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

2.25 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 display layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events
- AXI master interface with burst of 16 words

2.26 JPEG Codec (JPEG)

The JPEG Codec can encode and decode a JPEG stream as defined in the ***ISO/IEC 10918-1*** specification. It provides an fast and simple hardware compressor and decompressor of JPEG images with full management of JPEG headers.

The JPEG codec main features are as follows:

- 8-bit/channel pixel depths
- Single clock per pixel encoding and decoding
- Support for JPEG header generation and parsing
- Up to four programmable quantization tables
- Fully programmable Huffman tables (two AC and two DC)
- Fully programmable minimum coded unit (MCU)
- Encode/decode support (non simultaneous)
- Single clock Huffman coding and decoding
- Two-channel interface: Pixel/Compress In, Pixel/Compressed Out
- Stallable design
- Support for single greyscale component
- Ability to enable/disable header processing
- Internal register interface
- Fully synchronous design
- Configuration for high-speed decode mode

2.27 Random number generator (RNG)

All the devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

2.28 Timers and watchdogs

The devices include one high-resolution timer, two advanced-control timers, ten general-purpose timers, two basic timers, five low-power timers, two watchdogs and a SysTick timer.

All timer counters can be frozen in debug mode.

Table 4 compares the features of the advanced-control, general-purpose and basic timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output	Max interface clock (MHz)	Max timer clock (MHz)(1)
High-resolution timer	HRTIM1	16-bit	Up	/1 /2 /4 (x2 x4 x8 x16 x32, with DLL)	Yes	10	Yes	400	400
Advanced -control	TIM1, TIM8	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	100	200
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	100	200
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	100	200
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	100	200
	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	100	200
	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1	100	200
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1	100	200

Table 4. Timer feature comparison (continued)

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output	Max interface clock (MHz)	Max timer clock (MHz)(1)
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	100	200
Low-power timer	LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5	16-bit	Up	1, 2, 4, 8, 16, 32, 64, 128	No	0	No	100	200

1. The maximum timer clock is up to 400 MHz depending on TIMPRE bit in the RCC_CFGR register and D2PRE1/2 bits in RCC_D2CFGR register.

2.28.1 High-resolution timer (HRTIM1)

The high-resolution timer (HRTIM1) allows generating digital signals with high-accuracy timings, such as PWM or phase-shifted pulses.

It consists of 6 timers, 1 master and 5 slaves, totaling 10 high-resolution outputs, which can be coupled by pairs for deadtime insertion. It also features 5 fault inputs for protection purposes and 10 inputs to handle external events such as current limitation, zero voltage or zero current switching.

HRTIM1 timer is made of a digital kernel clocked at 400 MHz The high-resolution is available on the 10 outputs in all operating modes: variable duty cycle, variable frequency, and constant ON time.

The slave timers can be combined to control multiswitch complex converters or operate independently to manage multiple independent converters.

The waveforms are defined by a combination of user-defined timings and external events such as analog or digital feedbacks signals.

HRTIM1 timer includes options for blanking and filtering out spurious events or faults. It also offers specific modes and features to offload the CPU: DMA requests, burst mode controller, push-pull and resonant mode.

It supports many topologies including LLC, Full bridge phase shifted, buck or boost converters, either in voltage or current mode, as well as lighting application (fluorescent or LED). It can also be used as a general purpose timer, for instance to achieve high-resolution PWM-emulated DAC.

2.28.2 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

2.28.3 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32H743xI devices (see *Table 4* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The devices include 4 full-featured general-purpose timers: TIM2, TIM3, TIM4 and TIM5. TIM2 and TIM5 are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler while TIM3 and TIM4 are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. All timers feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  TIM2, TIM3, TIM4 and TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM12, TIM13, TIM14, TIM15, TIM16, TIM17**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13, TIM14, TIM16 and TIM17 feature one independent channel, whereas TIM12 and TIM15 have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers or used as simple timebases.

2.28.4 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

2.28.5 Low-power timers (LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5)

The low-power timers have an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one-shot mode
- Selectable software / hardware input trigger
- Selectable clock source:
- Internal clock source: LSE, LSI, HSI or APB clock
- External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

2.28.6 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

2.28.7 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.28.8 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

2.29 Real-time clock (RTC), backup SRAM and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V_{BAT} mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the V_{BAT} pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in V_{BAT} mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in V_{BAT} mode, but is functional in all low-power modes.

All RTC events (Alarm, Wakeup Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

2.30 Inter-integrated circuit interface (I2C)

The STM32H743xI embed four I^2C interfaces.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBus^{TM}) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

2.31 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32H743xI devices have four embedded universal synchronous receiver transmitters (USART1, USART2, USART3 and USART6) and four universal asynchronous receiver transmitters (UART4, UART5, UART7 and UART8). Refer to *Table 5* for a summary of USARTx and UARTx features.

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 10Mbit/s.

USART1, USART2, USART3 and USART6 also provide Smartcard mode (ISO 7816 compliant) and SPI-like communication capability.

All USART have a clock domain independent from the CPU clock, allowing the USARTx to wake up the MCU from Stop mode using baudrates up to 200 Kbaud.The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 5. USART features

USART modes/features(1)	USART1/2/3/6	UART4/5/7/8
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode (Master/Slave)	X	-
Smartcard mode	X	-
Single-wire Half-duplex communication	X	X
IrDA SIR ENDEC block	X	X
LIN mode	X	X
Dual clock domain and wakeup from low power mode	X	X
Receiver timeout interrupt	X	X
Modbus communication	X	X
Auto baud rate detection	X	X
Driver Enable	X	X
USART data length	7, 8 and 9 bits	

1. X = supported.

2.32 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-Power UART (LPUART1). The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode using baudrates up to 220 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame

while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

2.33 Serial peripheral interface (SPI)/inter- integrated sound interfaces (I2S)

The devices feature up to six SPIs (SPI2S1, SPI2S2, SPI2S3, SPI4, SPI5 and SPI6) that allow communicating up to 50 Mbits/s in master and slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable from 4 to 16 bits. All SPI interfaces support NSS pulse mode, TI mode, Hardware CRC calculation and 8x 8-bit embedded Rx and Tx FIFOs with DMA capability.

Three standard I^2S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available. They can be operated in master or slave mode, in simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency. All I^2S interfaces support 16x 8-bit embedded Rx and Tx FIFOs with DMA capability.

2.34 Serial audio interfaces (SAI)

The devices embed 4 SAIs (SAI1, SAI2, SAI3 and SAI4) that allow designing many stereo or mono audio protocols such as I2S, LSB or MSB-justified, PCM/DSP, TDM or AC’97. An SPDIF output is available when the audio block is configured as a transmitter. To bring this level of flexibility and reconfigurability, the SAI contains two independent audio sub-blocks. Each block has it own clock generator and I/O line controller.
Audio sampling frequencies up to 192 kHz are supported.
In addition, up to 8 microphones can be supported thanks to an embedded PDM interface.
The SAI can work in master or slave configuration. The audio sub-blocks can be either receiver or transmitter and can work synchronously or asynchronously (with respect to the other one). The SAI can be connected with other SAIs to work synchronously.

2.35 SPDIFRX Receiver Interface (SPDIFRX)

The SPDIFRX peripheral is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC-61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby or DTS (up to 5.1).

The main SPDIFRX features are the following:

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports Audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIFRX receiver provides all the necessary features to detect the symbol rate, and decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal will be available, the SPDIFRX will re-sample the incoming signal, decode the Manchester stream, recognize frames, sub-frames and blocks elements. It delivers to the CPU decoded data, and associated status flags.

The SPDIFRX also offers a signal named spdif_frame_sync, which toggles at the S/PDIF sub-frame rate that will be used to compute the exact sample rate for clock drift algorithms.

2.36 Single wire protocol master interface (SWPMI)

The Single wire protocol master interface (SWPMI) is the master interface corresponding to the Contactless Frontend (CLF) defined in the ETSI TS 102 613 technical specification. The main features are:

- full-duplex communication mode
- automatic SWP bus state management (active, suspend, resume)
- configurable bitrate up to 2 Mbit/s
- automatic SOF, EOF and CRC handling

SWPMI can be served by the DMA controller.

2.37 Management Data Input/Output (MDIO) slaves

The devices embed a MDIO slave interface it includes the following features:

- 32 MDIO Registers addresses, each of which is managed using separate input and output data registers:
  - 32 x 16-bit firmware read/write, MDIO read-only output data registers
  - 32 x 16-bit firmware read-only, MDIO write-only input data registers
- Configurable slave (port) address
- Independently maskable interrupts/events:
  - MDIO Register write
  - MDIO Register read
  - MDIO protocol error
- Able to operate in and wake up from STOP mode

2.38 SD/SDIO/MMC card host interfaces (SDMMC)

Two SDMMCD host interfaces are available. They support *MultiMediaCard System Specification Version 4.51* in three different databus modes: 1 bit (default), 4 bits and 8 bits.

Both interfaces support the *SD memory card specifications version 4.1.* and the *SDIO card specification version 4.0.* in two different databus modes: 1 bit (default) and 4 bits.

Each SDMMC host interface supports only one SD/SDIO/MMC card at any one time and a stack of MMC Version 4.51 or previous.

The SDMMC host interface embeds a dedicated DMA controller allowing high-speed transfers between the interface and the SRAM.

2.39 Controller area network (FDCAN1, FDCAN2)

The controller area network (CAN) subsystem consists of two CAN modules, a shared message RAM memory and a clock calibration unit.

Both CAN modules (FDCAN1 and FDCAN2) are compliant with ISO 11898-1 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

FDCAN1 supports time triggered CAN (TTCAN) specified in ISO 11898-4, including event synchronized time-triggered communication, global system time, and clock drift compensation. The FDCAN1 contains additional registers, specific to the time triggered feature. The CAN FD option can be used together with event-triggered and time-triggered CAN communication.

A 10 Kbytes message RAM memory implements filters, receive FIFOs, receive buffers, transmit event FIFOs, transmit buffers (and triggers for TTCAN). This message RAM is shared between the two FDCAN1 and FDCAN2 modules.

The common clock calibration unit is optional. It can be used to generate a calibrated clock for both FDCAN1 and FDCAN2 from the HSI internal RC oscillator and the PLL, by evaluating CAN messages received by the FDCAN1.

2.40 Universal serial bus on-the-go high-speed (OTG_HS)

The devices embed two USB OTG high-speed (up to 480 Mbit/s) device/host/OTG peripheral. OTG-HS1 supports both full-speed and high-speed operations, while OTG-HS2 supports only full-speed operations. They both integrate the transceivers for full-speed operation (12 Mbit/s). OTG-HS1 features a UTMI low-pin interface (ULPI) for high-speed operation (480 Mbit/s). When using the USB OTG-HS1 in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripherals are compliant with the USB 2.0 specification and with the OTG 2.0 specification. They have software-configurable endpoint setting and supports suspend/resume. The USB OTG controllers require a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The main features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode (OTG_HS1 only)

  The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

2.41 Ethernet MAC interface with dedicated DMA controller (ETH)

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

2.42 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wakeup the MCU from Stop mode on data reception.

2.43 Debug infrastructure

The devices offer a comprehensive set of debug and trace features to support software development and system integration.

- Breakpoint debugging
- Code execution tracing
- Software instrumentation
- JTAG debug port
- Serial-wire debug port
- Trigger input and output
- Serial-wire trace port
- Trace port
- ARM® CoreSight™ debug and trace components

The debug can be controlled via a JTAG/Serial-wire debug access port, using industry standard debugging tools.

A trace port allows data to be captured for logging and analysis.

3 Memory mapping

Refer to the product line reference manual for a details diagram illustrating memory mapping as well as the boundary addresses for all peripherals.

4 Pin descriptions

Figure 3. TFBGA240+25 ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS	PI6	PI5	PI4	PB5	VDD LDO3	VCAP3	PK5	PG10	PG9	PD5	PD4	PC10	PA15	PI1	PI0	VSS
B	VBAT	VSS	PI7	PE1	PB6	VSS	PB4	PK4	PG11	PJ15	PD6	PD3	PC11	PA14	PI2	PH15	PH14
C	PC15-OSC32_OUT	PC14-OSC32_IN	PE2	PE0	PB7	PB3	PK6	PK3	PG12	VSS	PD7	PC12	VSS	PI3	PA13	VSS	VDD LDO2
D	PE5	PE4	PE3	PB9	PB8	PG15	PK7	PG14	PG13	PJ14	PJ12	PD2	PD0	PA10	PA9	PH13	VCAP2
E	NC	PI9	PC13	PI8	PE6	VDD	PDR_ON	BOOT0	VDD	PJ13	VDD	PD1	PC8	PC9	PA8	PA12	PA11
F	NC	NC	PI10	PI11	VDD								PC7	PC6	PG8	PG7	VDD33 USB
G	PF2	NC	PF1	PF0	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PG5	PG6	VSS	VDD50 USB
H	PI12	PI13	PI14	PF3	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PG4	PG3	PG2	PK2
J	PH0-OSC_OUT	PH0-OSC_IN	VSS	PF5	PF4		VSS	VSS	VSS	VSS	VSS		VDD	PK0	PK1	VSS	VSS
K	NRST	PF6	PF7	PF8	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PJ11	VSS	NC	NC
L	VDDA	PC0	PF10	PF9	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PJ10	VSS	NC	NC
M	VREF+	PC1	PC2	PC3	VDD								VDD	PJ9	VSS	NC	NC
N	VREF-	PH2	PA2	PA1	PA0	PJ0	VDD	VDD	PE10	VDD	VDD	VDD	PJ8	PJ7	PJ6	VSS	NC
P	VSSA	PH3	PH4	PH5	PI15	PJ1	PF13	PF14	PE9	PE11	PB10	PB11	PH10	PH11	PD15	PD14	VDD
R	PC2_C	PC3_C	PA6	VSS	PA7	PB2	PF12	VSS	PF15	PE12	PE15	PJ5	PH9	PH12	PD11	PD12	PD13
T	PA0_C	PA1_C	PA5	PC4	PB1	PJ2	PF11	PG0	PE8	PE13	PH6	VSS	PH8	PB12	PB15	PD10	PD9
U	VSS	PA3	PA4	PC5	PB0	PJ3	PJ4	PG1	PE7	PE14	VCAP1	VDD LDO1	PH7	PB13	PB14	PD8	VSS

MSv41911V1

Figure 4. LQFP208 pinout

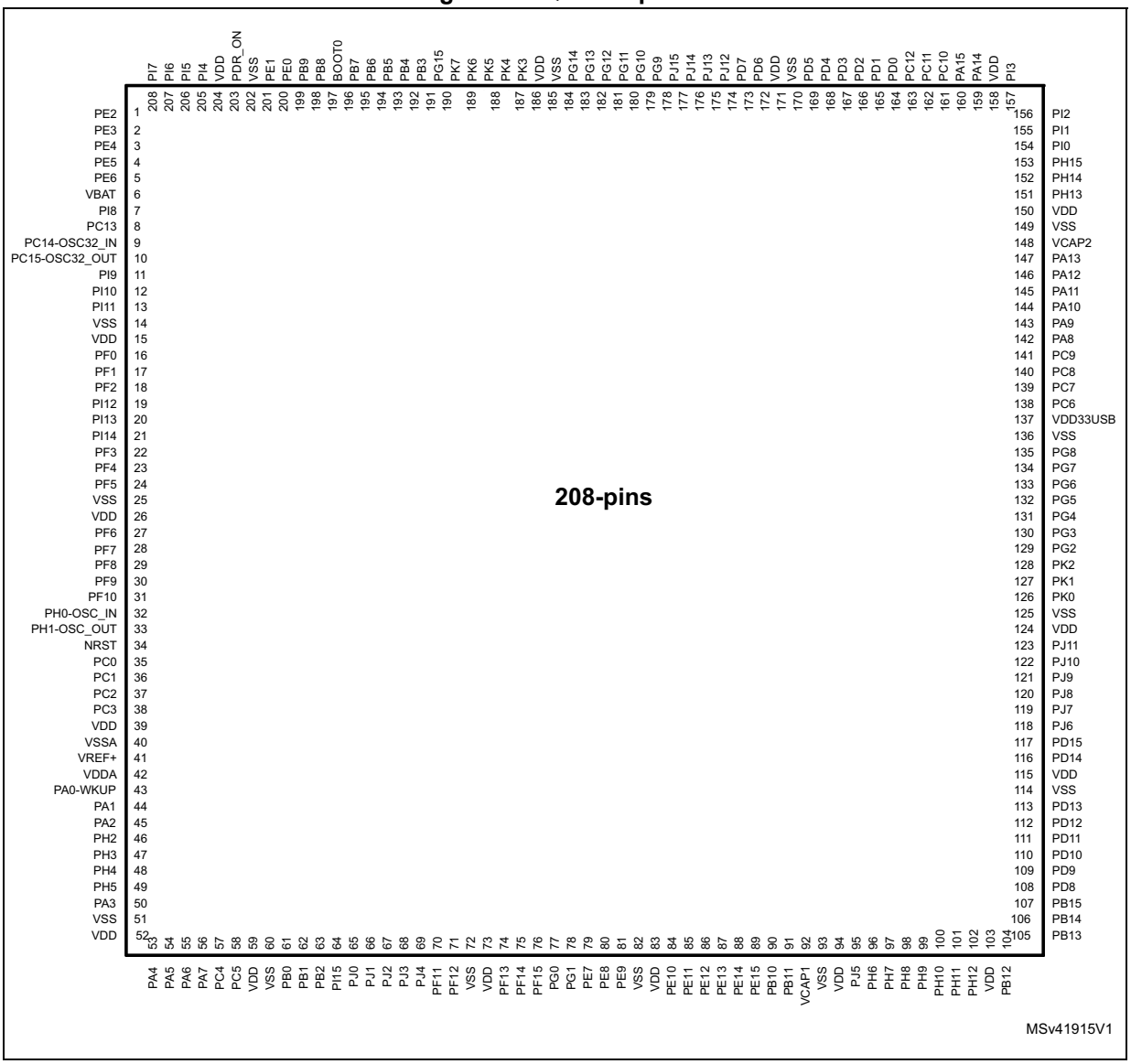


Figure 5. LQFP176 pinout

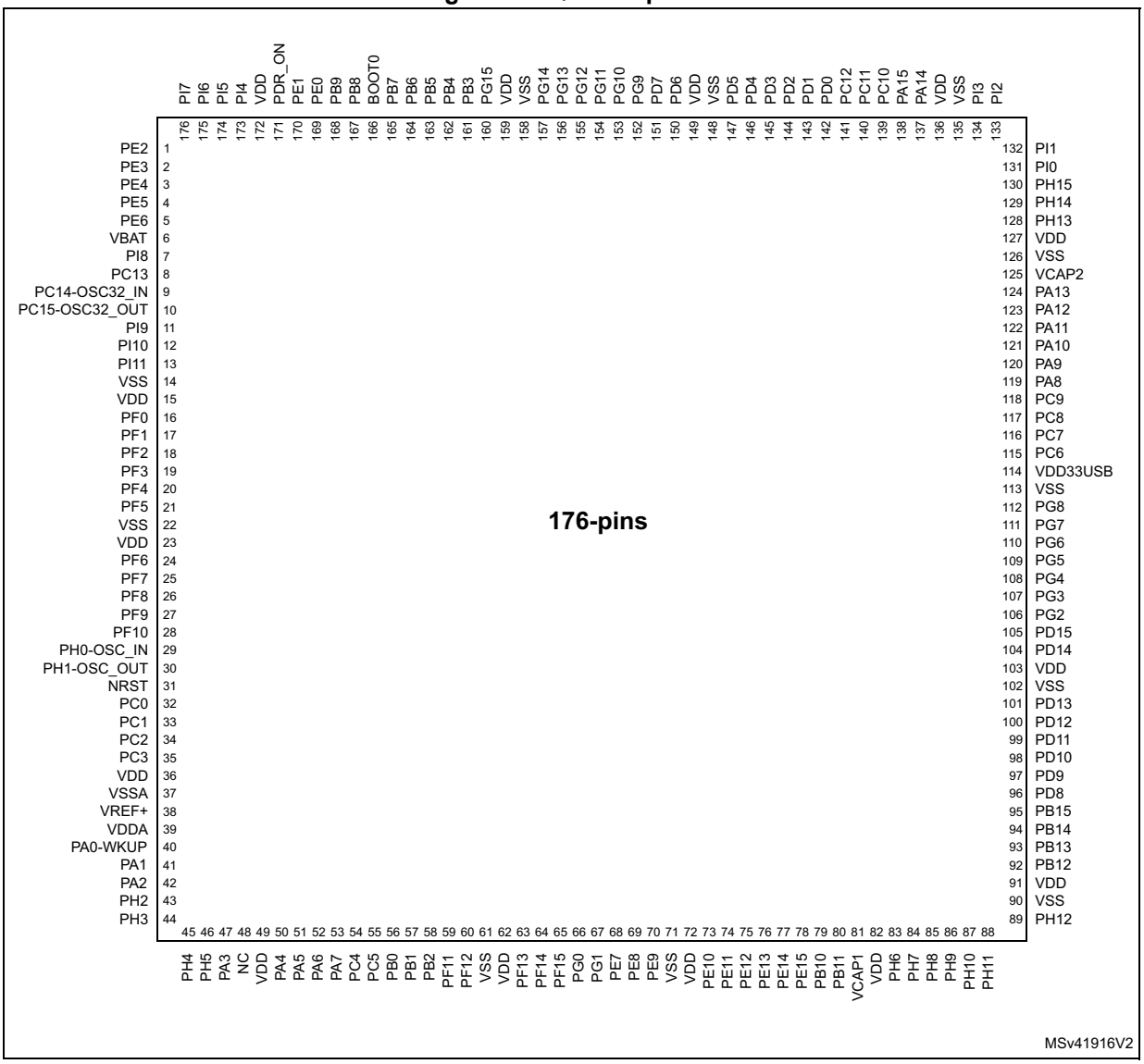


Figure 6. UFBGA176+25 ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	PE3	PE2	PE1	PE0	PB8	PB5	PG14	PG13	PB4	PB3	PD7	PC12	PA15	PA14	PA13
B	PE4	PE5	PE6	PB9	PB7	PB6	PG15	PG12	PG11	PG10	PD6	PD0	PC11	PC10	PA12
C	VBAT	PI7	PI6	PI5	VDD	PDR_ON	VDD	VDD	VDD	PG9	PD5	PD1	PI3	PI2	PA11
D	PC13	PI8	PI9	PI4	VSS	BOOT0	VSS	VSS	VSS	PD4	PD3	PD2	PH15	PI1	PA10
E	PC14-OSC32_IN	PF0	PI10	PI11								PH13	PH14	PI0	PA9
F	PC15-OSC32_OUT	VSS	VDD	PH2		VSS	VSS	VSS	VSS	VSS		VSS	VCAP2	PC9	PA8
G	PH0-OSC_IN	VSS	VDD	PH3		VSS	VSS	VSS	VSS	VSS		VSS	VDD	PC8	PC7
H	PH1-OSC_OUT	PF2	PF1	PH4		VSS	VSS	VSS	VSS	VSS		VSS	VDD 33USB	PG8	PC6
J	NRST	PF3	PF4	PH5		VSS	VSS	VSS	VSS	VSS		VDD	VDD	PG7	PG6
K	PF7	PF6	PF5	VDD		VSS	VSS	VSS	VSS	VSS		PH12	PG5	PG4	PG3
L	PF10	PF9	PF8	NC								PH11	PH10	PD15	PG2
M	VSSA	PC0	PC1	PC2_C	PC3_C	PB2	PG1	VSS	VSS	VCAP1	PH6	PH8	PH9	PD14	PD13
N	VREF-	PA1	PA0	PA4	PC4	PF13	PG0	VDD	VDD	VDD	PE13	PH7	PD12	PD11	PD10
P	VREF+	PA2	PA6	PA5	PC5	PF12	PF15	PE8	PE9	PE11	PE14	PB12	PB13	PD9	PD8
R	VDDA	PA3	PA7	PB1	PB0	PF11	PF14	PE7	PE10	PE12	PE15	PB10	PB11	PB14	PB15

MSv41912V2

Figure 7. LQFP144 pinout

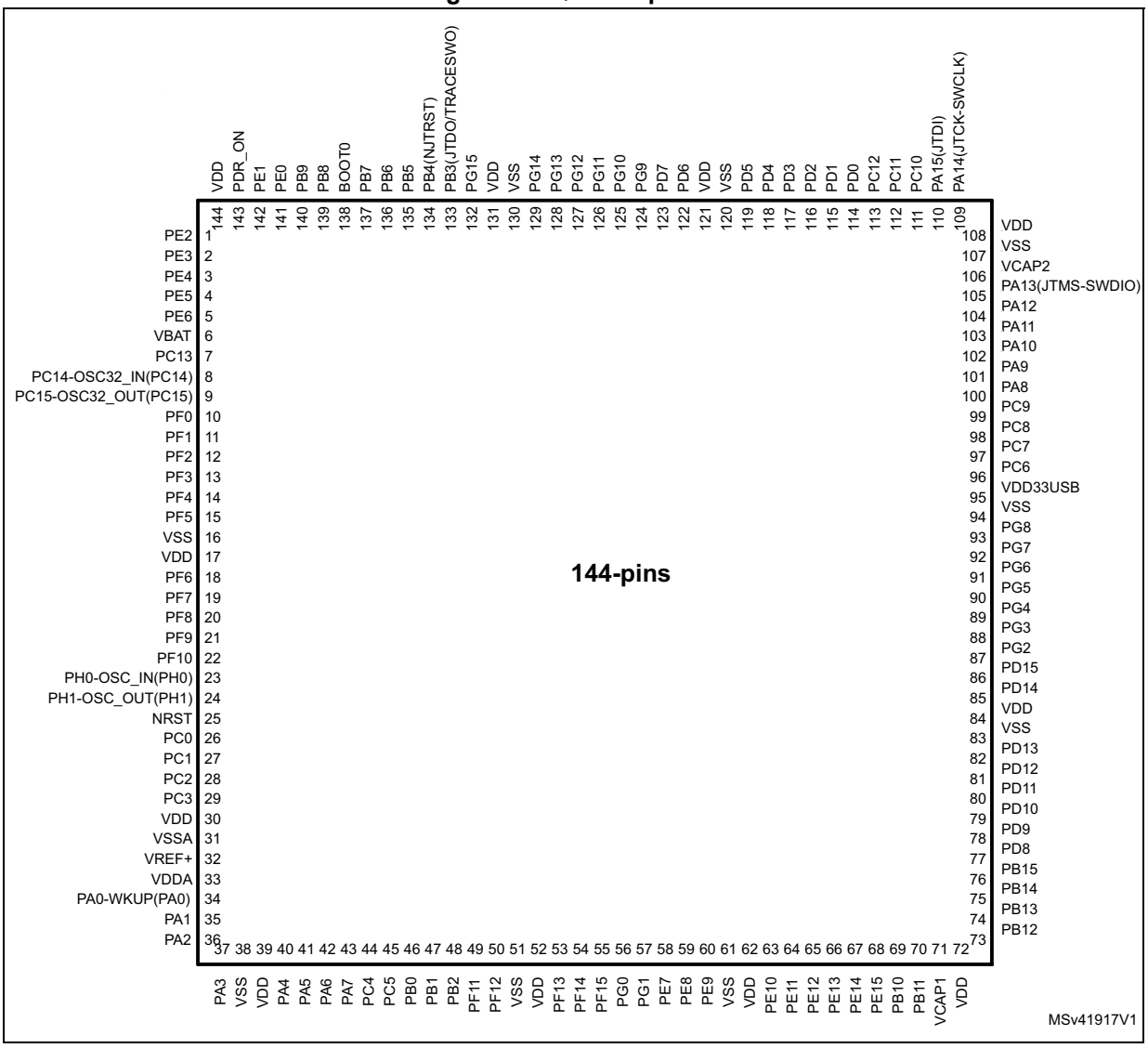


Figure 8. LQFP100 pinout

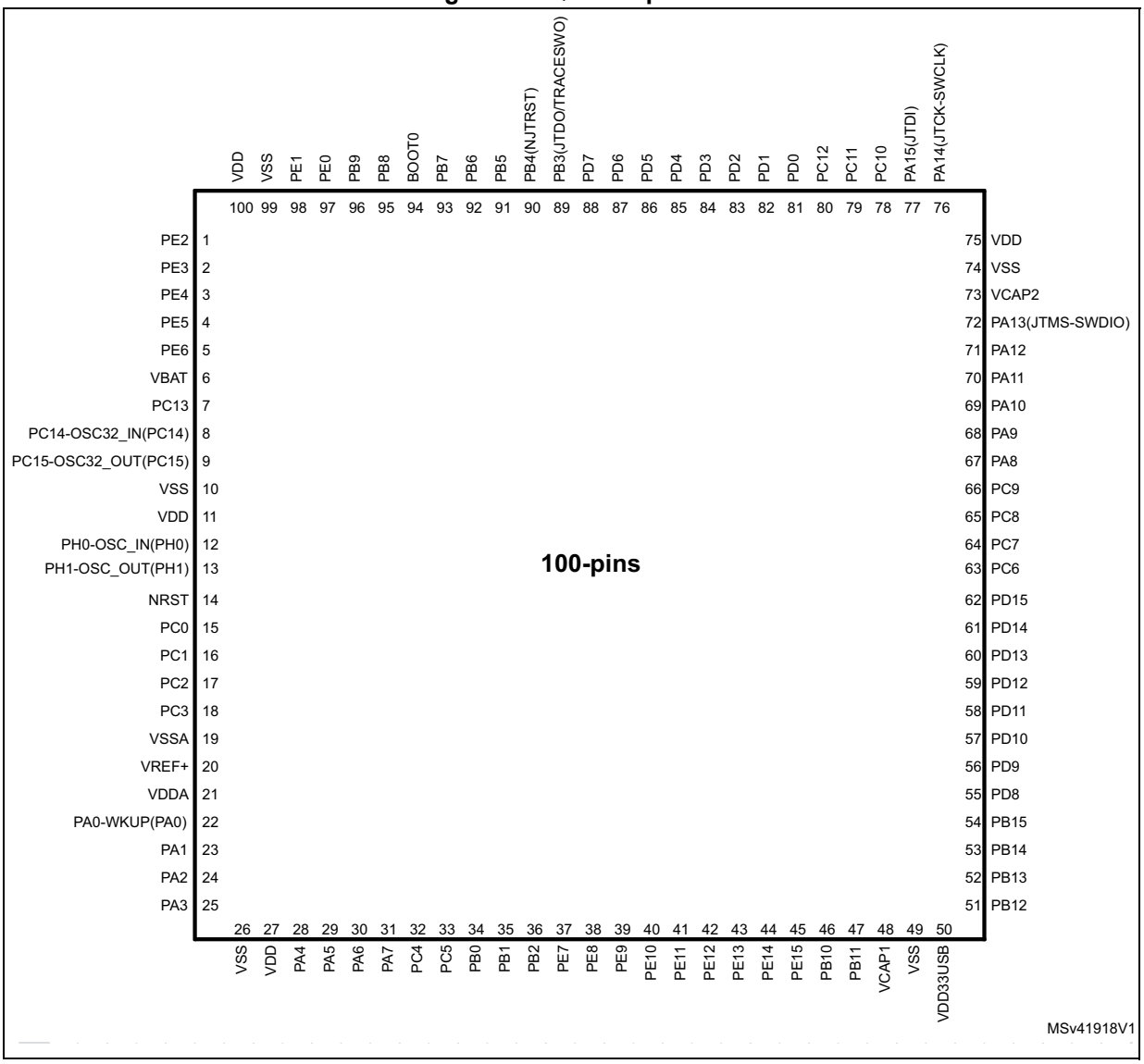


Table 6. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
	ANA	Analog-only Input

Table 6. Legend/abbreviations used in the pinout table (continued)

Name		Abbreviation	Definition
I/O structure		FT	5 V tolerant I/O
		TTa	3.6 V tolerant Input/output with resistive diode connected to V_{DDA}
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 7. STM32H743xI pin/ball definition

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
1	1	A2	1	1	C3	PE2	I/O	FT	-	TRACECLK, SAI1_CK1, SPI4_SCK, SAI1_MCLK_A, SAI4_MCLK_A, QUADSPI_BK1_IO2, SAI4_CK1, ETH_MII_TXD3, FMC_A23, EVENTOUT	-
2	2	A1	2	2	D3	PE3	I/O	FT	-	TRACED0, TIM15_BKIN, SAI1_SD_B, SAI4_SD_B, FMC_A19, EVENTOUT	-
3	3	B1	3	3	D2	PE4	I/O	FT	-	TRACED1, SAI1_D2, DFSDM_DATIN3, TIM15_CH1N, SPI4_NSS, SAI1_FS_A, SAI4_FS_A, SAI4_D2, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
4	4	B2	4	4	D1	PE5	I/O	FT	-	TRACED2, SAI1_CK2, DFSDM_CKIN3, TIM15_CH1, SPI4_MISO, SAI1_SCK_A, SAI4_SCK_A, SAI4_CK2, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT	-
5	5	B3	5	5	E5	PE6	I/O	FT	-	TRACED3, TIM1_BKIN2, SAI1_D1, TIM15_CH2, SPI4_MOSI, SAI1_SD_A, SAI4_SD_A, SAI4_D1, SAI2_MCK_B, TIM1_BKIN2_COMP1, TIM1_BKIN2_COMP2, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT	-
-	-	-	-	-	A1	VSS	S	-	-	-	-
-	-	-	-	-	E6	VDD	S	-	-	-	-
6	6	C1	6	6	B1	VBAT	S	-	-	-	-
-	-	-	-	-	A1	VSS	-	-	-	-	-
-	-	D2	7	7	E4	PI8	I/O	FT	-	EVENTOUT	RTC_TAMP_2/ RTC_TS/WKUP3
7	7	D1	8	8	E3	PC13	I/O	FT		EVENTOUT	RTC_TAMP_1/ RTC_TS/WKUP2
-	-	-	-	-	A1	VSS	-	-	-	-	-
8	8	E1	9	9	C2	PC14-OSC32_IN (PC14)	I/O	FT	-	EVENTOUT	OSC32_IN
9	9	F1	10	10	C1	PC15-OSC32_ OUT (PC15)	I/O	FT	-	EVENTOUT	OSC32_OUT
-	-	D3	11	11	E2	PI9	I/O	FT	-	UART4_RX, CAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
-	-	E3	12	12	F3	PI10	I/O	FT	-	CAN1_RXFD, ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT	-
-	-	E4	13	13	F4	PI11	I/O	FT	-	LCD_G6, OTG_HS_ULPI_DIR, EVENTOUT	WKUP4
-	-	F2	14	14	A1	VSS	S	-	-	-	-
-	-	F3	15	15	E6	VDD	S	-	-	-	-
-	-	-	-	-	F2	NC	-	-	-	-	-
-	-	-	-	-	E1	NC	-	-	-	-	-
-	-	-	-	-	F1	NC	-	-	-	-	-
-	-	-	-	-	G2	NC	-	-	-	-	-
-	10	E2	16	16	G4	PF0	I/O	FT	-	I2C2_SDA, FMC_A0, EVENTOUT	-
-	11	H3	17	17	G3	PF1	I/O	FT	-	I2C2_SCL, FMC_A1, EVENTOUT	-
-	12	H2	18	18	G1	PF2	I/O	FT	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	-	-	19	H1	PI12	I/O	FT	-	ETH_TX_ER, LCD_HSYNC, EVENTOUT	-
-	-	-	-	20	H2	PI13	I/O	FT	-	LCD_VSYNC, EVENTOUT	-
-	-	-	-	21	H3	PI14	I/O	FT	-	LCD_CLK, EVENTOUT	-
-	13	J2	19	22	H4	PF3	I/O	FT	-	FMC_A3, EVENTOUT	ADC3_INP5
-	14	J3	20	23	J5	PF4	I/O	FT	-	FMC_A4, EVENTOUT	ADC3_INP9, ADC3_INN5
-	15	K3	21	24	J4	PF5	I/O	FT	-	FMC_A5, EVENTOUT	ADC3_INP4
10	16	G2	22	25	B2	VSS	S	-	-	-	-
11	17	G3	23	26	E11	VDD	S	-	-	-	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
-	18	K2	24	27	K2	PF6	I/O	FT	-	TIM16_CH1, SPI5_NSS, SAI1_SD_B, UART7_RX, SAI4_SD_B, QUADSPI_BK1_IO3, EVENTOUT	ADC3_INP8, ADC3_INN4
-	19	K1	25	28	K3	PF7	I/O	FT	-	TIM17_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_TX, SAI4_MCLK_B, QUADSPI_BK1_IO2, EVENTOUT	ADC3_INP3
-	20	L3	26	29	K4	PF8	I/O	FT	-	TIM16_CH1N, SPI5_MISO, SAI1_SCK_B, UART7_RTS, SAI4_SCK_B, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT	ADC3_INP7, ADC3_INN3
-	-	L4	-	-	-	NC	-	-	-	-	-
-	21	L2	27	30	L4	PF9	I/O	FT	-	TIM17_CH1N, SPI5_MOSI, SAI1_FS_B, UART7_CTS, SAI4_FS_B, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT	ADC3_INP2
-	22	L1	28	31	L3	PF10	I/O	FT	-	TIM16_BKIN, SAI1_D3, QUADSPI_CLK, SAI4_D3, DCMI_D11, LCD_DE, EVENTOUT	ADC3_INP6, ADC3_INN2
12	23	G1	29	32	J2	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
13	24	H1	30	33	J1	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
14	25	J1	31	34	K1	NRST	I/O	RST	-	-	-
15	26	M2	32	35	L2	PC0	I/O	FT	-	DFSDM_CKIN0, DFSDM_DATIN4, SAI2_FS_B, OTG_HS_ULPI_STP, FMC_SDNWE, LCD_R5, EVENTOUT	ADC123_INP10
16	27	M3	33	36	M2	PC1	I/O	FT	-	TRACED0, SAI1_D1, DFSDM_DATIN0, DFSDM_CKIN4, SPI2_MOSI/I2S2_SDO, SAI1_SD_A, SAI4_SD_A, SDMMC2_CK, SAI4_D1, ETH_MDC, MDIOS_MDC, EVENTOUT	ADC123_INP11, ADC123_INN10, RTC_TAMP_3/ WKUP5
-	-	-	-	-	M3	PC2	I/O	FT	-	DFSDM_CKIN1, SPI2_MISO/I2S2_SDI, DFSDM_CKOUT, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT	ADC123_INP12, ADC123_INN11
17	28	M4	34	37	R1	PC2_C	ANA		-	-	ADC3_INP0, ADC3_INN2
-	-	-	-	-	M4	PC3	I/O	FT	-	DFSDM_DATIN1, SPI2_MOSI/I2S2_SDO, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, FMC_SDCKE0, EVENTOUT	ADC12_INP13, ADC12_INN12
18	29	M5	35	38	R2	PC3_C	ANA	-	-	-	ADC3_INP1
-	30	G3	36	39	F5	VDD	S	-	-	-	-
-	-	-	-	-	B6	VSS	S	-	-	-	-
19	31	M1	37	40	P1	VSSA	S	-	-	-	-
-	-	N1	-	-	N1	VREF-	S	-	-	-	-
20	32	P1	38	41	M1	VREF+	S	-	-	-	-
21	33	R1	39	42	L1	VDDA	S	-	-	-	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
22	34	N3	40	43	N5	PA0-WKUP (PA0)	I/O	FT	-	TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, TIM15_BKIN, USART2_CTS_NSS, UART4_TX, SDMMC2_CMD, SAI2_SD_B, ETH_MII_CRS, EVENTOUT	ADC1_INP16, WKUP0
-	-	-	-	-	T1	PA0_C	ANA	-	-	-	ADC12_INP0, ADC12_INN1
23	35	N2	41	44	N4	PA1	I/O	FT	-	TIM2_CH2, TIM5_CH2, LPTIM3_OUT, TIM15_CH1N, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCK_B, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, LCD_R2, EVENTOUT	ADC1_INP17, ADC1_INN16
-	-	-	-	-	T2	PA1_C	ANA	-	-	-	ADC12_INP1
24	36	P2	42	45	N3	PA2	I/O	FT	-	TIM2_CH3, TIM5_CH3, LPTIM4_OUT, TIM15_CH1, USART2_TX, SAI2_SCK_B, ETH_MDIO, MDIOS_MDIO, LCD_R1, EVENTOUT	ADC12_INP14, WKUP1
-	-	F4	43	46	N2	PH2	I/O	FT	-	LPTIM1_IN2, QUADSPI_BK2_IO0, SAI2_SCK_B, ETH_MII_CRS, FMC_SDCKE0, LCD_R0, EVENTOUT	ADC3_INP13
-	-	-	-	-	F5	VDD	S	-	-	-	-
-	-	-	-	-	C10	VSS	S	-	-	-	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
-	-	G4	44	47	P2	PH3	I/O	FT	-	QUADSPI_BK2_IO1, SAI2_MCK_B, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT	ADC3_INP14, ADC3_INN13
-	-	H4	45	48	P3	PH4	I/O	FT	-	I2C2_SCL, LCD_G5, OTG_HS_ULPI_NXT, LCD_G4, EVENTOUT	ADC3_INP15, ADC3_INN14
-	-	J4	46	49	P4	PH5	I/O	FT	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	ADC3_INP16, ADC3_INN15
25	37	R2	47	50	U2	PA3	I/O	FT	-	TIM2_CH4, TIM5_CH4, LPTIM5_OUT, TIM15_CH2, USART2_RX, LCD_B2, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC12_IN15
-	-	-	48	-	-	NC	-	-	-	-	-
26	38	-	-	51	C13	VSS	S		-	-	-
27	39	K4	49	52	G5	VDD	S		-	-	-
28	40	N4	50	53	U3	PA4	I/O	TTa	-	TIM5_ETR, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC12_INP18, DAC1_OUT1
29	41	P4	51	54	T3	PA5	I/O	TTa	-	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, SPI6_SCK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT	ADC12_INP19, ADC12_INN18, DAC1_OUT2

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
30	42	P3	52	55	R3	PA6	I/O	FT	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO/I2S1_SDI, SPI6_MISO, TIM13_CH1, TIM8_BKIN_COMP1, TIM8_BKIN_COMP2, MDIOS_MDC, TIM1_BKIN_COMP1, TIM1_BKIN_COMP2, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC12_INP3
31	43	R3	53	56	R5	PA7	I/O	FT	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SDO, SPI6_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, EVENTOUT	ADC12_INP7, ADC12_INN3, OPAMP1_VINM
32	44	N5	54	57	T4	PC4	I/O	FT	-	DFSDM_CKIN2, I2S1_MCK, SPDIFRX_IN2, ETH_MII_RXD0/ ETH_RMII_RXD0, FMC_SDNE0, EVENTOUT	ADC12_INP4, OPAMP1_VOUT, COMP1_INM
33	45	P5	55	58	U4	PC5	I/O	FT	-	SAI1_D3, DFSDM_DATIN2, SPDIFRX_IN3, SAI4_D3, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, COMP1_OUT, EVENTOUT	ADC12_INP8, ADC12_INN4, OPAMP1_VINM
-	-	-	-	59	G13	VDD	S	-	-	-	-
-	-	-	-	60	C16	VSS	S		-	-	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
34	46	R5	56	61	U5	PB0	I/O	FT	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, DFSDM_CKOUT, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, LCD_G1, EVENTOUT	ADC12_INP9, ADC12_INN5, OPAMP1_VINP, COMP1_INP
35	47	R4	57	62	T5	PB1	I/O	FT	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM_DATIN1, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, LCD_G0, EVENTOUT	ADC12_INP5, COMP1_INM
36	48	M6	58	63	R6	PB2	I/O	FT	-	SAI1_D1, DFSDM_CKIN1, SAI1_SD_A, SPI3_MOSI/I2S3_SDO, SAI4_SD_A, QUADSPI_CLK, SAI4_D1, ETH_TX_ER, EVENTOUT	COMP1_INP
-	-	-	-	64	P5	PI15	I/O	FT	-	LCD_G2, LCD_R0, EVENTOUT	-
-	-	-	-	65	N6	PJ0	I/O	FT	-	LCD_R7, LCD_R1, EVENTOUT	-
-	-	-	-	66	P6	PJ1	I/O	FT	-	LCD_R2, EVENTOUT	-
-	-	-	-	67	T6	PJ2	I/O	FT	-	LCD_R3, EVENTOUT	-
-	-	-	-	68	U6	PJ3	I/O	FT	-	LCD_R4, EVENTOUT	-
-	-	-	-	69	U7	PJ4	I/O	FT	-	LCD_R5, EVENTOUT	-
-	49	R6	59	70	T7	PF11	I/O	FT	-	SPI5_MOSI, SAI2_SD_B, FMC_SDNRAS, DCMI_D12, EVENTOUT	ADC1_INP2
-	50	P6	60	71	R7	PF12	I/O	FT	-	FMC_A6, EVENTOUT	ADC1_INP6, ADC1_INN2
-	51	M8	61	72	F2	VSS	S	-	-		

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
-	52	N8	62	73	H5	VDD	S	-	-		
-	53	N6	63	74	P7	PF13	I/O	FT	-	DFSDM_DATIN6, I2C4_SMBA, FMC_A7, EVENTOUT	ADC2_INP2
-	54	R7	64	75	P8	PF14	I/O	FT	-	DFSDM_CKIN6, I2C4_SCL, FMC_A8, EVENTOUT	ADC2_INP6, ADC2_INN2
-	55	P7	65	76	R9	PF15	I/O	FT	-	I2C4_SDA, FMC_A9, EVENTOUT	-
-	56	N7	66	77	T8	PG0	I/O	FT	-	FMC_A10, EVENTOUT	-
-	-	-	-	-	G7	VSS	S	-	-		-
-	-	-	-	-	H13	VDD	S	-	-		-
-	57	M7	67	78	U8	PG1	I/O	FT	-	FMC_A11, EVENTOUT	OPAMP2_VINM
37	58	R8	68	79	U9	PE7	I/O	FT	-	TIM1_ETR, DFSDM_DATIN2, UART7_RX, QUADSPI_BK2_IO0, FMC_D4/FMC_DA4, EVENTOUT	OPAMP2_VOUT, COMP2_INM
38	59	P8	69	80	T9	PE8	I/O	FT	-	TIM1_CH1N, DFSDM_CKIN2, UART7_TX, QUADSPI_BK2_IO1, FMC_D5/FMC_DA5, COMP2_OUT, EVENTOUT	OPAMP2_VINM
39	60	P9	70	81	P9	PE9	I/O	FT	-	TIM1_CH1, DFSDM_CKOUT, UART7_RTS, QUADSPI_BK2_IO2, FMC_D6/FMC_DA6, EVENTOUT	OPAMP2_VINP, COMP2_INP
-	61	M9	71	82	G8	VSS	S	-	-	-	-
-	62	N9	72	83	J13	VDD	S	-	-	-	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
40	63	R9	73	84	N9	PE10	I/O	FT	-	TIM1_CH2N, DFSDM_DATIN4, UART7_CTS, QUADSPI_BK2_IO3, FMC_D7/FMC_DA7, EVENTOUT	COMP2_INM
41	64	P10	74	85	P10	PE11	I/O	FT	-	TIM1_CH2, DFSDM_CKIN4, SPI4_NSS, SAI2_SD_B, FMC_D8/FMC_DA8, LCD_G3, EVENTOUT	COMP2_INP
42	65	R10	75	86	R10	PE12	I/O	FT	-	TIM1_CH3N, DFSDM_DATIN5, SPI4_SCK, SAI2_SCK_B, FMC_D9/FMC_DA9, COMP1_OUT, LCD_B4, EVENTOUT	-
43	66	N11	76	87	T10	PE13	I/O	FT		TIM1_CH3, DFSDM_CKIN5, SPI4_MISO, SAI2_FS_B, FMC_D10/FMC_DA10, COMP2_OUT, LCD_DE, EVENTOUT	-
-	-	-	-	-	G9	VSS	S	-	-	-	-
-	-	-	-	-	K5	VDD	S	-	-	-	-
44	67	P11	77	88	U10	PE14	I/O	FT	-	TIM1_CH4, SPI4_MOSI, SAI2_MCK_B, FMC_D11/FMC_DA11, LCD_CLK, EVENTOUT	-
45	68	R11	78	89	R11	PE15	I/O	FT	-	TIM1_BKIN, FMC_D12/FMC_DA12, TIM1_BKIN_COMP1, TIM1_BKIN_COMP2, LCD_R7, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
46	69	R12	79	90	P11	PB10	I/O	FT	-	TIM2_CH3, HRTIM_SCOUT, I2C2_SCL, SPI2_SCK/I2S2_CK, DFSDM_DATIN7, USART3_TX, QUADSPI_BK1_NCS, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT	-
47	70	R13	80	91	P12	PB11	I/O	FT	-	TIM2_CH4, HRTIM_SCIN, LPTIM2_ETR, I2C2_SDA, DFSDM_CKIN7, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, LCD_G5, EVENTOUT	-
48	71	M10	81	92	U11	VCAP1	S	-	-	-	-
49	-	-	-	93	G10	VSS	S	-	-	-	-
-	-	-	-	-	U12	VDDLDO1	S	-	-	-	-
-	72	N10	82	94	K13	VDD	S	-	-	-	-
50	-	-	-	-	-	VDD33 USB	-	-	-	-	-
-	-	-	-	95	R12	PJ5	I/O	FT	-	LCD_R6, EVENTOUT	-
-	-	M11	83	96	T11	PH6	I/O	FT	-	TIM12_CH1, I2C2_SMBA, SPI5_SCK, ETH_MII_RXD2, FMC_SDNE1, DCMI_D8, EVENTOUT	-
-	-	N12	84	97	U13	PH7	I/O	FT	-	I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, DCMI_D9, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
-	-	M12	85	98	T13	PH8	I/O	FT	-	TIM5_ETR, I2C3_SDA, FMC_D16, DCMI_HSYNC, LCD_R2, EVENTOUT	-
-	-	-	-	-	G11	VSS	S	-	-	-	-
-	-	-	-	-	L5	VDD	S	-	-	-	-
-	-	M13	86	99	R13	PH9	I/O	FT	-	TIM12_CH2, I2C3_SMBA, FMC_D17, DCMI_D0, LCD_R3, EVENTOUT	-
-	-	L13	87	100	P13	PH10	I/O	FT	-	TIM5_CH1, I2C4_SMBA, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT	-
-	-	L12	88	101	P14	PH11	I/O	FT	-	TIM5_CH2, I2C4_SCL, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT	-
-	-	K12	89	102	R14	PH12	I/O	FT	-	TIM5_CH3, I2C4_SDA, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT	-
-	-	H12	90	-	H7	VSS	S		-	-	-
-	-	J12	91	103	L13	VDD	S		-	-	-
51	73	P12	92	104	T14	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, DFSDM_DATIN1, USART3_CK, CAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ ETH_RMII_TXD0, OTG_HS_ID, TIM1_BKIN_COMP1, TIM1_BKIN_COMP2, UART5_RX, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
52	74	P13	93	105	U14	PB13	I/O	FT	-	TIM1_CH1N, LPTIM2_OUT, SPI2_SCK/I2S2_CK, DFSDM_CKIN1, USART3_CTS_NSS, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, UART5_TX, EVENTOUT	OTG_HS_VBUS
53	75	R14	94	106	U15	PB14	I/O	FT	-	TIM1_CH2N, TIM12_CH1, TIM8_CH2N, USART1_TX, SPI2_MISO/I2S2_SDI, DFSDM_DATIN2, USART3_RTS, UART4_RTS, SDMMC2_D0, OTG_HS_DM, EVENTOUT	-
54	76	R15	95	107	T15	PB15	I/O	FT	-	RTC_REFIN, TIM1_CH3N, TIM12_CH2, TIM8_CH3N, USART1_RX, SPI2_MOSI/I2S2_SDO, DFSDM_CKIN2, UART4_CTS, SDMMC2_D1, OTG_HS_DP, EVENTOUT	-
55	77	P15	96	108	U16	PD8	I/O	FT	-	DFSDM_CKIN3, SAI3_SCK_B, USART3_TX, SPDIFRX_IN1, FMC_D13/FMC_DA13, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
56	78	P14	97	109	T17	PD9	I/O	FT	-	DFSDM_DATIN3, SAI3_SD_B, USART3_RX, CAN2_RXFD, FMC_D14/FMC_DA14, EVENTOUT	-
57	79	N15	98	110	T16	PD10	I/O	FT	-	DFSDM_CKOUT, SAI3_FS_B, USART3_CK, CAN2_TXFD, FMC_D15/FMC_DA15, LCD_B3, EVENTOUT	-
-	-	-	-	-	M5	VDD	S	-	-	-	-
-	-	-	-	-	H8	VSS	S	-	-	-	-
58	80	N14	99	111	R15	PD11	I/O	FT	-	I2C4_SMBA, USART3_CTS_NSS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16, EVENTOUT	-
59	81	N13	100	112	R16	PD12	I/O	FT	-	LPTIM1_IN1, TIM4_CH1, I2C4_SCL, USART3_RTS, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17, EVENTOUT	-
60	82	M15	101	113	R17	PD13	I/O	FT	-	LPTIM1_OUT, TIM4_CH2, I2C4_SDA, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT	-
-	83	-	102	114	H9	VSS	S	-	-	-	-
-	84	J13	103	115	M13	VDD	S	-	-	-	-
61	85	M14	104	116	P16	PD14	I/O	FT	-	TIM4_CH3, SAI3_MCLK_B, UART8_CTS, FMC_D0/FMC_DA0, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
62	86	L14	105	117	P15	PD15	I/O	FT	-	TIM4_CH4, SAI3_MCLK_A, UART8_RTS, FMC_D1/FMC_DA1, EVENTOUT	-
-	-	-	-	118	N15	PJ6	I/O	FT	-	TIM8_CH2, LCD_R7, EVENTOUT	-
-	-	-	-	119	N14	PJ7	I/O	FT	-	TRGIN, TIM8_CH2N, LCD_G0, EVENTOUT	-
-	-	-	-	-	N7	VDD	S	-	-	-	-
-	-	-	-	-	H10	VSS	S	-	-	-	-
-	-	-	-	120	N13	PJ8	I/O	FT	-	TIM1_CH3N, TIM8_CH1, UART8_TX, LCD_G1, EVENTOUT	-
-	-	-	-	121	M14	PJ9	I/O	FT	-	TIM1_CH3, TIM8_CH1N, UART8_RX, LCD_G2, EVENTOUT	-
-	-	-	-	122	L14	PJ10	I/O	FT	-	TIM1_CH2N, TIM8_CH2, SPI5_MOSI, LCD_G3, EVENTOUT	-
-	-	-	-	123	K14	PJ11	I/O	FT	-	TIM1_CH2, TIM8_CH2N, SPI5_MISO, LCD_G4, EVENTOUT	-
-	-	-	-	124	N8	VDD	S	-	-	-	-
-	-	-	-	-	N10	VDD	S	-	-	-	-
-	-	-	-	125	H11	VSS	S	-	-	-	-
-	-	-	-	-	N17	NC	S	-	-	-	-
-	-	-	-	-	N11	VDD	S	-	-	-	-
-	-	-	-	-	M16	NC	-	-	-	-	-
-	-	-	-	-	M17	NC	-	-	-	-	-
-	-	-	-	-	J7	VSS	S	-	-	-	-
-	-	-	-	-	L16	NC	-	-	-	-	-
-	-	-	-	-	L17	NC	-	-	-	-	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
-	-	-	-	-	N12	VDD	S	-	-	-	-
-	-	-	-	-	K16	NC	-	-	-	-	-
-	-	-	-	-	K17	NC	-	-	-	-	-
-	-	-	-	-	J8	VSS	S	-	-	-	-
-	-	-	-	126	J14	PK0	I/O	FT	-	TIM1_CH1N, TIM8_CH3, SPI5_SCK, LCD_G5, EVENTOUT	-
-	-	-	-	127	J15	PK1	I/O	FT	-	TIM1_CH1, TIM8_CH3N, SPI5_NSS, LCD_G6, EVENTOUT	-
-	-	-	-	128	H17	PK2	I/O	FT	-	TIM1_BKIN, TIM8_BKIN, TIM8_BKIN_COMP1, TIM8_BKIN_COMP2, TIM1_BKIN_COMP1, TIM1_BKIN_COMP2, LCD_G7, EVENTOUT	-
-	87	L15	106	129	H16	PG2	I/O	FT	-	TIM8_BKIN, TIM8_BKIN_COMP1, TIM8_BKIN_COMP2, FMC_A12, EVENTOUT	-
-	88	K15	107	130	H15	PG3	I/O	FT	-	TIM8_BKIN2, TIM8_BKIN2_COMP1, TIM8_BKIN2_COMP2, FMC_A13, EVENTOUT	-
-	-	-	-	-	J9	VSS	S	-	-	-	-
-	-	-	-	-	P17	VDD	S	-	-	-	-
-	89	K14	108	131	H14	PG4	I/O	FT	-	TIM1_BKIN2, TIM1_BKIN2_COMP1, TIM1_BKIN2_COMP2, FMC_A14/FMC_BA0, EVENTOUT	
-	90	K13	109	132	G14	PG5	I/O	FT	-	TIM1_ETR, FMC_A15/FMC_BA1, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
-	91	J15	110	133	G15	PG6	I/O	FT	-	TIM17_BKIN, HRTIM_CHE1, QUADSPI_BK1_NCS, FMC_NE3, DCMI_D12, LCD_R7, EVENTOUT	-
-	92	J14	111	134	F16	PG7	I/O	FT	-	HRTIM_CHE2, SAI1_MCLK_A, USART6_CK, FMC_INT, DCMI_D13, LCD_CLK, EVENTOUT	-
-	93	H14	112	135	F15	PG8	I/O	FT	-	TIM8_ETR, SPI6_NSS, USART6_RTS, SPDIFRX_IN2, ETH_PPS_OUT, FMC_SDCLK, LCD_G7, EVENTOUT	-
-	94	G12	113	136	J10	VSS	S	-	-	-	-
-	-	-	-	-	G17	VDD50 USB	S	-	-	-	-
-	95	H13	114	137	F17	VDD33 USB	S	-	-	-	-
-	-	-	-	-	E9	VDD	S	-	-	-	-
63	96	H15	115	138	F14	PC6	I/O	FT	-	HRTIM_CHA1, TIM3_CH1, TIM8_CH1, DFSDM_CKIN3, I2S2_MCK, USART6_TX, SDMMC1_D0DIR, FMC_NWAIT, SDMMC2_D6, SDMMC1_D6, DCMI_D0, LCD_HSYNC, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
64	97	G15	116	139	F13	PC7	I/O	FT	-	TRGIO, HRTIM_CHA2, TIM3_CH2, TIM8_CH2, DFSDM_DATIN3, I2S3_MCK, USART6_RX, SDMMC1_D123DIR, FMC_NE1, SDMMC2_D7, SWPMI_TX, SDMMC1_D7, DCMI_D1, LCD_G6, EVENTOUT	-
65	98	G14	117	140	E13	PC8	I/O	FT	-	TRACED1, HRTIM_CHB1, TIM3_CH3, TIM8_CH3, USART6_CK, UART5_RTS, FMC_NE2/FMC_NCE, SWPMI_RX, SDMMC1_D0, DCMI_D2, EVENTOUT	-
66	99	F14	118	141	E14	PC9	I/O	FT	-	MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, LCD_G3, SWPMI_SUSPEND, SDMMC1_D1, DCMI_D3, LCD_B2, EVENTOUT	-
-	-	-	-	-	J11	VSS	S	-	-	-	-
-	-	-	-	-	E11	VDD	S	-	-	-	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
67	100	F15	119	142	E15	PA8	I/O	FT	-	MCO1, TIM1_CH1, HRTIM_CHB2, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, UART7_RX, TIM8_BKIN2_COMP1, TIM8_BKIN2_COMP2, LCD_B3, LCD_R6, EVENTOUT	-
68	101	E15	120	143	D15	PA9	I/O	FT	-	TIM1_CH2, HRTIM_CHC1, LPUART1_TX, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, CAN1_RXFD, ETH_TX_ER, DCMI_D0, LCD_R5, EVENTOUT	OTG_FS_VBUS
69	102	D15	121	144	D14	PA10	I/O	FT	-	TIM1_CH3, HRTIM_CHC2, LPUART1_RX, USART1_RX, CAN1_TXFD, OTG_FS_ID, MDIOS_MDIO, LCD_B4, DCMI_D1, LCD_B1, EVENTOUT	-
70	103	C15	122	145	E17	PA11	I/O	FT	-	TIM1_CH4, HRTIM_CHD1, LPUART1_CTS, SPI2_NSS/I2S2_WS, UART4_RX, USART1_CTS_NSS, CAN1_RX, OTG_FS_DM, LCD_R4, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
71	104	B15	123	146	E16	PA12	I/O	FT	-	TIM1_ETR, HRTIM_CHD2, LPUART1_RTS, SPI2_SCK/I2S2_CK, UART4_TX, USART1_RTS, SAI2_FS_B, CAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT	-
72	105	A15	124	147	C15	PA13 (JTMS-SWDIO)	I/O	FT	-	JTMS-SWDIO, EVENTOUT	-
73	106	F13	125	148	D17	VCAP2	S	-	-	-	-
74	107	F12	126	149	K7	VSS	S	-	-	-	-
-	-	-	-	-	C17	VDDLDO2		-	-	-	-
75	108	G13	127	150	F5	VDD	S	-	-	-	-
-	-	E12	128	151	D16	PH13	I/O	FT	-	TIM8_CH1N, UART4_TX, CAN1_TX, FMC_D21, LCD_G2, EVENTOUT	-
-	-	E13	129	152	B17	PH14	I/O	FT	-	TIM8_CH2N, UART4_RX, CAN1_RX, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT	-
-	-	D13	130	153	B16	PH15	I/O	FT	-	TIM8_CH3N, CAN1_TXFD, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT	-
-	-	E14	131	154	A16	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS/I2S2_WS, CAN1_RXFD, FMC_D24, DCMI_D13, LCD_G5, EVENTOUT	-
-	-	-	-	-	K8	VSS	S	-	-	-	-
-	-	-	-	-	F5	VDD	S	-	-	-	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
-	-	D14	132	155	A15	PI1	I/O	FT	-	TIM8_BKIN2, SPI2_SCK/I2S2_CK, TIM8_BKIN2_COMP1, TIM8_BKIN2_COMP2, FMC_D25, DCMI_D8, LCD_G6, EVENTOUT	-
-	-	C14	133	156	B15	PI2	I/O	FT	-	TIM8_CH4, SPI2_MISO/I2S2_SDI, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT	-
-	-	C13	134	157	C14	PI3	I/O	FT	-	TIM8_ETR, SPI2_MOSI/I2S2_SDO, FMC_D27, DCMI_D10, EVENTOUT	-
-	-	D9	135	-	K9	VSS	S		-		-
-	-	C9	136	158	G5	VDD	S		-		-
76	109	A14	137	159	B14	PA14 (JTCK-SWCLK)	I/O	FT	-	JTCK-SWCLK, EVENTOUT	-
77	110	A13	138	160	A14	PA15(JTDI)	I/O	FT	-	JTDI, TIM2_CH1/TIM2_ETR, HRTIM_FLT1, HDMI_CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI6_NSS, UART4_RTS, UART7_TX, EVENTOUT	-
78	111	B14	139	161	A13	PC10	I/O	FT	-	HRTIM_EEV1, DFSDM_CKIN5, SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDMMC1_D2, DCMI_D8, LCD_R2, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
79	112	B13	140	162	B13	PC11	I/O	FT	-	HRTIM_FLT2, DFSDM_DATIN5, SPI3_MISO/I2S3_SDI, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDMMC1_D3, DCMI_D4, EVENTOUT	-
80	113	A12	141	163	C12	PC12	I/O	FT	-	TRACED3, HRTIM_EEV2, SPI3_MOSI/I2S3_SDO, USART3_CK, UART5_TX, SDMMC1_CK, DCMI_D9, EVENTOUT	-
-	-	-	-	-	K10	VSS	S		-	-	-
-	-	-	-	-	G13	VDD	S		-	-	-
81	114	B12	142	164	D13	PD0	I/O	FT	-	DFSDM_CKIN6, SAI3_SCK_A, UART4_RX, CAN1_RX, FMC_D2/FMC_DA2, EVENTOUT	-
82	115	C12	143	165	E12	PD1	I/O	FT	-	DFSDM_DATIN6, SAI3_SD_A, UART4_TX, CAN1_TX, FMC_D3/FMC_DA3, EVENTOUT	-
83	116	D12	144	166	D12	PD2	I/O	FT	-	TRACED2, TIM3_ETR, UART5_RX, SDMMC1_CMD, DCMI_D11, EVENTOUT	-
84	117	D11	145	167	B12	PD3	I/O	FT	-	DFSDM_CKOUT, SPI2_SCK/I2S2_CK, USART2_CTS_NSS, FMC_CLK, DCMI_D5, LCD_G7, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
85	118	D10	146	168	A12	PD4	I/O	FT	-	HRTIM_FLT3, SAI3_FS_A, USART2_RTS, CAN1_RXFD, FMC_NOE, EVENTOUT	-
86	119	C11	147	169	A11	PD5	I/O	FT	-	HRTIM_EEV3, USART2_TX, CAN1_TXFD, FMC_NWE, EVENTOUT	-
-	120	D8	148	170	K11	VSS	S	-	-	-	-
-	121	C8	149	171	H5	VDD	S	-	-	-	-
87	122	B11	150	172	B11	PD6	I/O	FT	-	SAI1_D1, DFSDM_CKIN4, DFSDM_DATIN1, SPI3_MOSI/I2S3_SDO, SAI1_SD_A, USART2_RX, SAI4_SD_A, CAN2_RXFD, SAI4_D1, SDMMC2_CK, FMC_NWAIT, DCMI_D10, LCD_B2, EVENTOUT	-
88	123	A11	151	173	C11	PD7	I/O	FT	-	DFSDM_DATIN4, SPI1_MOSI/I2S1_SDO, DFSDM_CKIN1, USART2_CK, SPDIFRX_IN0, SDMMC2_CMD, FMC_NE1, EVENTOUT	-
-	-	-	-	174	D11	PJ12	I/O	FT	-	TRGOUT, LCD_G3, LCD_B0, EVENTOUT	-
-	-	-	-	175	E10	PJ13	I/O	FT	-	LCD_B4, LCD_B1, EVENTOUT	-
-	-	-	-	176	D10	PJ14	I/O	FT	-	LCD_B2, EVENTOUT	-
-	-	-	-	177	B10	PJ15	I/O	FT	-	LCD_B3, EVENTOUT	-
-	-	-	-	-	L7	VSS	S	-	-	-	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
-	-	-	-	-	H13	VDD	S	-	-	-	-
-	124	C10	152	178	A10	PG9	I/O	FT	-	SPI1_MISO/I2S1_SDI, USART6_RX, SPDIFRX_IN3, QUADSPI_BK2_IO2, SAI2_FS_B, FMC_NE2/FMC_NCE, DCMI_VSYNC, EVENTOUT	-
-	125	B10	153	179	A9	PG10	I/O	FT	-	HRTIM_FLT5, SPI1_NSS/I2S1_WS, LCD_G3, SAI2_SD_B, FMC_NE3, DCMI_D2, LCD_B2, EVENTOUT	-
-	126	B9	154	180	B9	PG11	I/O	FT	-	HRTIM_EEV4, SPI1_SCK/I2S1_CK, SPDIFRX_IN0, SDMMC2_D2, ETH_MII_TX_EN/ ETH_RMII_TX_EN, DCMI_D3, LCD_B3, EVENTOUT	-
-	127	B8	155	181	C9	PG12	I/O	FT	-	LPTIM1_IN1, HRTIM_EEV5, SPI6_MISO, USART6_RTS, SPDIFRX_IN1, LCD_B4, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_NE4, LCD_B1, EVENTOUT	-
-	128	A8	156	182	D9	PG13	I/O	FT	-	TRACED0, LPTIM1_OUT, HRTIM_EEV10, SPI6_SCK, USART6_CTS_NSS, ETH_MII_TXD0/ETH_RMII_TXD0, FMC_A24, LCD_R0, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
-	129	A7	157	183	D8	PG14	I/O	FT	-	TRACED1, LPTIM1_ETR, SPI6_MOSI, USART6_TX, QUADSPI_BK2_IO3, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_A25, LCD_B0, EVENTOUT	-
-	130	D7	158	184	L8	VSS	S	-	-	-	-
-	131	C7	159	185	J13	VDD	S	-	-	-	-
-	-	-	-	186	C8	PK3	I/O	FT	-	LCD_B4, EVENTOUT	-
-	-	-	-	187	B8	PK4	I/O	FT	-	LCD_B5, EVENTOUT	-
-	-	-	-	188	A8	PK5	I/O	FT	-	LCD_B6, EVENTOUT	-
-	-	-	-	189	C7	PK6	I/O	FT	-	LCD_B7, EVENTOUT	-
-	-	-	-	190	D7	PK7	I/O	FT	-	LCD_DE, EVENTOUT	-
-	-	-	-	-	L9	VSS	S	-	-	-	-
-	-	-	-	-	K5	VDD	S	-	-	-	-
-	132	B7	160	191	D6	PG15	I/O	FT	-	USART6_CTS_NSS, FMC_SDNCAS, DCMI_D13, EVENTOUT	-
89	133	A10	161	192	C6	PB3 (JTDO/TRACESWO)	I/O	FT	-	JTDO/TRACESWO, TIM2_CH2, HRTIM_FLT4, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, SPI6_SCK, SDMMC2_D2, UART7_RX, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
90	134	A9	162	193	B7	PB4 (NJTRST)	I/O	FT	-	NJTRST, TIM16_BKIN, TIM3_CH1, HRTIM_EEV6, SPI1_MISO/I2S1_SDI, SPI3_MISO/I2S3_SDI, SPI2_NSS/I2S2_WS, SPI6_MISO, SDMMC2_D3, UART7_TX, EVENTOUT	-
91	135	A6	163	194	A5	PB5	I/O	FT	-	TIM17_BKIN, TIM3_CH2, HRTIM_EEV7, I2C1_SMBA, SPI1_MOSI/I2S1_SDO, I2C4_SMBA, SPI3_MOSI/I2S3_SDO, SPI6_MOSI, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, FMC_SDCKE1, DCMI_D10, UART5_RX, EVENTOUT	-
-	-	-	-	-	L10	VSS	S	-	-	-	-
-	-	-	-	-	K13	VDD	S	-	-	-	-
92	136	B6	164	195	B5	PB6	I/O	FT	-	TIM16_CH1N, TIM4_CH1, HRTIM_EEV8, I2C1_SCL, HDMI_CEC, I2C4_SCL, USART1_TX, LPUART1_TX, CAN2_TX, QUADSPI_BK1_NCS, DFSDM_DATIN5, FMC_SDNE1, DCMI_D5, UART5_TX, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
93	137	B5	165	196	C5	PB7	I/O	FT	-	TIM17_CH1N, TIM4_CH2, HRTIM_EEV9, I2C1_SDA, I2C4_SDA, USART1_RX, LPUART1_RX, CAN2_TXFD, DFSDM_CKIN5, FMC_NL, DCMI_VSYNC, EVENTOUT	PVD_IN
94	138	D6	166	197	E8	BOOT0	I	B	-	-	VPP
95	139	A5	167	198	D5	PB8	I/O	FT	-	TIM16_CH1, TIM4_CH3, DFSDM_CKIN7, I2C1_SCL, I2C4_SCL, SDMMC1_CKIN, UART4_RX, CAN1_RX, SDMMC2_D4, ETH_MII_TXD3, SDMMC1_D4, DCMI_D6, LCD_B6, EVENTOUT	-
96	140	B4	168	199	D4	PB9	I/O	FT	-	TIM17_CH1, TIM4_CH4, DFSDM_DATIN7, I2C1_SDA, SPI2_NSS/I2S2_WS, I2C4_SDA, SDMMC1_CDIR, UART4_TX, CAN1_TX, SDMMC2_D5, I2C4_SMBA, SDMMC1_D5, DCMI_D7, LCD_B7, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
97	141	A4	169	200	C4	PE0	I/O	FT	-	LPTIM1_ETR, TIM4_ETR, HRTIM_SCIN, LPTIM2_ETR, UART8_RX, CAN1_RXFD, SAI2_MCK_A, FMC_NBL0, DCMI_D2, EVENTOUT	-
98	142	A3	170	201	B4	PE1	I/O	FT	-	LPTIM1_IN2, HRTIM_SCOUT, UART8_TX, CAN1_TXFD, FMC_NBL1, DCMI_D3, EVENTOUT	-
-	-	-	-	-	A7	VCAP3	S		-	-	-
99	-	D5	-	202	L11	VSS	S		-	-	-
-	143	C6	171	203	E7	PDR_ON	S		-	-	-
-	-	-	-	-	A6	VDDLDO3	S		-	-	-
100	144	C5	172	204	L5	VDD	S		-	-	-
-	-	D4	173	205	A4	PI4	I/O	FT	-	TIM8_BKIN, SAI2_MCK_A, TIM8_BKIN_COMP1, TIM8_BKIN_COMP2, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	C4	174	206	A3	PI5	I/O	FT	-	TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	C3	175	207	A2	PI6	I/O	FT	-	TIM8_CH2, SAI2_SD_A, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	C2	176	208	B3	PI7	I/O	FT	-	TIM8_CH3, SAI2_FS_A, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-

Table 7. STM32H743xI pin/ball definition (continued)

Pin/ball name						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240+25						
-	-	-	-	-	J16	VSS	S	-	-	-	-
-	-	-	-	-	L13	VDD	S	-	-	-	-

Table 8. Port A alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/	TIM3/4/5/12/HRTIM1	LPUART1/TIM8/LPTIM2/3/4/5	I2C1/2/3/4/TIM15/LPTIM2/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4	SPI2/3/6/USART1/2/3/6/UART7	SPI6/SAI2/4/UART4/5/8/LPUART1/	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS/LCD/COMP1/2	I2C4/UART7/SWP/DFSDM/SDMMC2/MDIOS/ETH	FMC/SDMMC1/MDIOS/OTG2_FS/LCD/COMP1/2	DCMI/LCD	UART5/LCD	SYS
Port A	PA0	-	TIM2_CH1/TIM2_ETR	TIM5_CH1	TIM8_ETR	TIM15_BKIN	-	-	USART2_CTS_NSS	UART4_TX	SDMMC2_CMD	SAI2_SD_B	ETH_MII_CRS	-	-		EVENT OUT
	PA1	-	TIM2_CH2	TIM5_CH2	LPTIM3_OUT	TIM15_CH1N	-	-	USART2_RTS	UART4_RX	QUADSPI_BK1_IO3	SAI2_MCK_B	ETH_MII_RX_CLK/ETH_RMII_REF_CLK	-	-	LCD_R2	EVENT OUT
	PA2	-	TIM2_CH3	TIM5_CH3	LPTIM4_OUT	TIM15_CH1	-	-	USART2_TX	SAI2_SCK_B	-	-	ETH_MDIO	MDIOS_MDIO	-	LCD_R1	EVENT OUT
	PA3	-	TIM2_CH4	TIM5_CH4	LPTIM5_OUT	TIM15_CH2	-	-	USART2_RX	-	LCD_B2	OTG_HS_ULPI_D0	ETH_MII_COL	-	-	LCD_B5	EVENT OUT
	PA4	-	-	TIM5_ETR	-	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK	SPI6_NSS	-	-	-	OTG_HS_SOF	DCMI_HSYNC	LCD_VSYNC	EVENT OUT
	PA5	-	TIM2_CH1/TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK/I2S1_CK	-	-	SPI6_SCK	-	OTG_HS_ULPI_CK	-	-	-	LCD_R4	EVENT OUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO/I2S1_SDI	-	-	SPI6_MISO	TIM13_CH1	TIM8_BKIN_COMP1/TIM8_BKIN_COMP2	MDIOS_MDC	TIM1_BKIN_COMP1/TIM1_BKIN_COMP2	DCMI_PIXCLK	LCD_G2	EVENT OUT

Table 8. Port A alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/	TIM3/4/5/12/HRTIM1	LPUART1/TIM8/LPTIM2/3/4/5	I2C1/2/3/4/TIM15/LPTIM2/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4	SPI2/3/6/USART1/2/3/6/UART7	SPI6/SAI2/4/UART4/5/8/LPUART1/	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS/LCD/COMP1/2	I2C4/UART7/SWP/DFSDM/SDMMC2/MDIOS/ETH	FMC/SDMMC1/MDIOS/OTG2_FS/LCD/COMP1/2	DCMI/LCD	UART5/LCD	SYS
Port A	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI/I2S1_SDO	-	-	SPI6_MOSI	TIM14_CH1	-	ETH_MII_RX_DV/ETH_RMII_CRS_DV	FMC_SDNWE	-	-	EVENTOUT
	PA8	MCO1	TIM1_CH1	HRTIM_CHB2	TIM8_BKIN2	I2C3_SCL	-	-	USART1_CK	-	-	OTG_FS_SOF	UART7_RX	TIM8_BKIN2_COMP1/TIM8_BKIN2_COMP2	LCD_B3	LCD_R6	EVENTOUT
	PA9	-	TIM1_CH2	HRTIM_CHC1	LPUART1_TX	I2C3_SMBA	SPI2_SCK/I2S2_CK		USART1_TX	-	CAN1_RXFD	-	ETH_TX_ER	-	DCMI_D0	LCD_R5	EVENTOUT
	PA10	-	TIM1_CH3	HRTIM_CHC2	LPUART1_RX	-	-		USART1_RX	-	CAN1_TXFD	OTG_FS_ID	MDIOS_MDIO	LCD_B4	DCMI_D1	LCD_B1	EVENTOUT
	PA11	-	TIM1_CH4	HRTIM_CHD1	LPUART1_CTS	-	SPI2_NSS/I2S2_WS	UART4_RX	USART1_CTS_NSS	-	CAN1_RX	OTG_FS_DM	-	-	-	LCD_R4	EVENTOUT
	PA12	-	TIM1_ETR	HRTIM_CHD2	LPUART1_RTS	-	SPI2_SCK/I2S2_CK	UART4_TX	USART1_RTS	SAI2_FS_B	CAN1_TX	OTG_FS_DP	-	-	-	LCD_R5	EVENTOUT
	PA13	JTMS-SWDIO	-	-	-	-	--	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1/TIM2_ETR	HRTIM_FLT1	-	HDMI_CEC	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	SPI6_NSS	UART4_RTS			UART7_TX	-	-	-	EVENTOUT

Table 9. Port B alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART1/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART1/SDMMC1/SPDIFRX	FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD	SAI2/4/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS/LCD	I2C4/UART7/SWP/DFSDM/SDMMC2/MDIOS/ETH	FMC/SDMMC1/MDIOS/OTG2_FS/LCD	DCMI/LCD/COMP1/2	UART5/LCD	SYS
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	DFSDM_CKOUT	-	UART4_CTS	LCD_R3	OTG_HS_ULPI_D1	ETH_MII_RXD2	-	-	LCD_G1	EVENTOUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM_DATIN1	-	-	LCD_R6	OTG_HS_ULPI_D2	ETH_MII_RXD3	-	-	LCD_G0	EVENTOUT
	PB2	-	-	SAI1_D1	-	DFSDM_CKIN1	-	SAI1_SD_A	SPI3_MOSI/I2S3_SDO	SAI4_SD_A	QUADSPI_CLK	SAI4_D1	ETH_TX_ER	-	-	-	EVENTOUT
	PB3	JTDO/TRACESWO	TIM2_CH2	HRTIM_FLT4	-	-	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	-	SPI6_SCK	SDMMC2_D2	-	UART7_RX	-	-	-	EVENTOUT
	PB4	NJTRST	TIM16_BKIN	TIM3_CH1	HRTIM_EEV6	-	SPI1_MISO/I2S1_SDI	SPI3_MISO/I2S3_SDI	SPI2_NSS/I2S2_WS	SPI6_MISO	SDMMC2_D3	-	UART7_TX	-	-	-	EVENTOUT
	PB5	-	TIM17_BKIN	TIM3_CH2	HRTIM_EEV7	I2C1_SMBA	SPI1_MOSI/I2S1_SDO	I2C4_SMBA	SPI3_MOSI/I2S3_SDO	SPI6_MOSI	CAN2_RX	OTG_HS_ULPI_D7	ETH_PPS_OUT	FMC_SDCKE1	DCMI_D10	UART5_RX	EVENTOUT
	PB6	-	TIM16_CH1N	TIM4_CH1	HRTIM_EEV8	I2C1_SCL	HDMI_CEC	I2C4_SCL	USART1_TX	LPUART1_TX	CAN2_TX	QUADSPI_BK1_NCS	DFSDM_DATIN5	FMC_SDNE1	DCMI_D5	UART5_TX	EVENTOUT
	PB7	-	TIM17_CH1N	TIM4_CH2	HRTIM_EEV9	I2C1_SDA	-	I2C4_SDA	USART1_RX	LPUART1_RX	CAN2_TXFD	-	DFSDM_CKIN5	FMC_NL	DCMI_VSYNC	-	EVENTOUT
	PB8	-	TIM16_CH1	TIM4_CH3	DFSDM_CKIN7	I2C1_SCL	-	I2C4_SCL	SDMMC1_CKIN	UART4_RX	CAN1_RX	SDMMC2_D4	ETH_MII_TXD3	SDMMC1_D4	DCMI_D6	LCD_B6	EVENTOUT
	PB9	-	TIM17_CH1	TIM4_CH4	DFSDM_DATIN7	I2C1_SDA	SPI2_NSS/I2S2_WS	I2C4_SDA	SDMMC1_CDIR	UART4_TX	CAN1_TX	SDMMC2_D5	I2C4_SMBA	SDMMC1_D5	DCMI_D7	LCD_B7	EVENTOUT
	PB10	-	TIM2_CH3	HRTIM_SCOUT	LPTIM2_IN1	I2C2_SCL	SPI2_SCK/I2S2_CK	DFSDM_DATIN7	USART3_TX	-	QUADSPI_BK1_NCS	OTG_HS_ULPI_D3	ETH_MII_RX_ER	-	-	LCD_G4	EVENTOUT
	PB11	-	TIM2_CH4	HRTIM_SCIN	LPTIM2_ETR	I2C2_SDA	-	DFSDM_CKIN7	USART3_RX	-	-	OTG_HS_ULPI_D4	ETH_MII_TX_EN/ETH_RMII_TX_EN	-	-	LCD_G5	EVENTOUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMBA	SPI2_NSS/I2S2_WS	DFSDM_DATIN1	USART3_CK	-	CAN2_RX	OTG_HS_ULPI_D5	ETH_MII_TXD0/ETH_RMII_TXD0	OTG_HS_ID	TIM1_BKIN_COMP1/TIM1_BKIN_COMP2	UART5_RX	EVENTOUT
	PB13	-	TIM1_CH1N	-	LPTIM2_OUT	-	SPI2_SCK/I2S2_CK	DFSDM_CKIN1	USART3_CTS_NSS	-	CAN2_TX	OTG_HS_ULPI_D6	ETH_MII_TXD1/ETH_RMII_TXD1	-	-	UART5_TX	EVENTOUT

Table 9. Port B alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART1/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART1/SDMMC1/SPDIFRX	FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD	SAI2/4/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS/LCD	I2C4/UART7/SWP/DFSDM/SDMMC2/MDIOS/ETH	FMC/SDMMC1/MDIOS/OTG2_FS/LCD	DCMI/LCD/COMP1/2	UART5/LCD	SYS
Port B	PB14	-	TIM1_CH2N	TIM12_CH1	TIM8_CH2N	USART1_TX	SPI2_MISO/I2S2_SDI	DFSDM_DATIN2	USART3_RTS	UART4_RTS	SDMMC2_D0	-	-	OTG_HS_DM	-	-	EVENT OUT
	PB15	RTC_REFIN	TIM1_CH3N	TIM12_CH2	TIM8_CH3N	USART1_RX	SPI2_MOSI/I2S2_SDO	DFSDM_CKIN2	-	UART4_CTS	SDMMC2_D1	-	-	OTG_HS_DP	-	-	EVENT OUT

Table 10. Port C alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART1/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART1/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS/LCD	I2C4/UART7/SWP/DFSDM/SDMMC2/MDIOS/ETH	FMC/SDMMC1/MDIOS/OTG2_FS/LCD	DCMI/LCD/COMP1/2	UART5/LCD	SYS
Port C	PC0	-	-	-	DFSDM_CKIN0	-	-	DFSDM_DATIN4	-	SAI2_FS_B	-	OTG_HS_ULPI_STP	-	FMC_SDNWE	-	LCD_R5	EVENT OUT
	PC1	TRACED0	-	SAI1_D1	DFSDM_DATIN0	DFSDM_CKIN4	SPI2_MOSI/I2S2_SDO	SAI1_SD_A	-	SAI4_SD_A	SDMMC2_CK	SAI4_D1	ETH_MDC	MDIOS_MDC	-	-	EVENT OUT
	PC2	-	-	-	DFSDM_CKIN1	-	SPI2_MISO/I2S2_SDI	DFSDM_CKOUT	-	-	-	OTG_HS_ULPI_DIR	ETH_MII_TXD2	FMC_SDNE0	-	-	EVENT OUT
	PC3	-	-	-	DFSDM_DATIN1	-	SPI2_MOSI/I2S2_SDO	-	-	-	-	OTG_HS_ULPI_NXT	ETH_MII_TX_CLK	FMC_SDCKE0	-	-	EVENT OUT
	PC4	-	-	-	DFSDM_CKIN2	-	I2S1_MCK	-	-	-	SPDIFRX_IN2	-	ETH_MII_RXD0/ETH_RMII_RXD0	FMC_SDNE0	-	-	EVENT OUT
	PC5	-	-	SAI1_D3	DFSDM_DATIN2	-	-	-	-	-	SPDIFRX_IN3	SAI4_D3	ETH_MII_RXD1/ETH_RMII_RXD1	FMC_SDCKE0	COMP1_OUT	-	EVENT OUT
	PC6	-	HRTIM_CHA1	TIM3_CH1	TIM8_CH1	DFSDM_CKIN3	I2S2_MCK	-	USART6_TX	SDMMC1_D0DIR	FMC_NWAIT	SDMMC2_D6	-	SDMMC1_D6	DCMI_D0	LCD_HSYNC	EVENT OUT
	PC7	TRGIO	HRTIM_CHA2	TIM3_CH2	TIM8_CH2	DFSDM_DATIN3	-	I2S3_MCK	USART6_RX	SDMMC1_D123DIR	FMC_NE1	SDMMC2_D7	SWPMI_TX	SDMMC1_D7	DCMI_D1	LCD_G6	EVENT OUT

Table 10. Port C alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART1/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART1/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS/LCD	I2C4/UART7/SWP/DFSDM/SDMMC2/MDIOS/ETH	FMC/SDMMC1/MDIOS/OTG2_FS/LCD	DCMI/LCD/COMP1/2	UART5/LCD	SYS
Port C	PC8	TRACED1	HRTIM_CHB1	TIM3_CH3	TIM8_CH3	-	-	-	USART6_CK	UART5_RTS	FMC_NE2/FMC_NCE	-	SWPMI_RX	SDMMC1_D0	DCMI_D2	-	EVENTOUT
	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S_CKIN	-	-	UART5_CTS	QUADSPI_BK1_IO0	LCD_G3	SWPMI_SUSPEND	SDMMC1_D1	DCMI_D3	LCD_B2	EVENTOUT
	PC10	-	-	HRTIM_EEV1	DFSDM_CKIN5	-	-	SPI3_SCK/I2S3_CK	USART3_TX	UART4_TX	QUADSPI_BK1_IO1	-	-	SDMMC1_D2	DCMI_D8	LCD_R2	EVENTOUT
	PC11	-	-	HRTIM_FLT2	DFSDM_DATIN5	-	-	SPI3_MISO/I2S3_SDI	USART3_RX	UART4_RX	QUADSPI_BK2_NCS	-	-	SDMMC1_D3	DCMI_D4	-	EVENTOUT
	PC12	TRACED3	-	HRTIM_EEV2	-	-	-	SPI3_MOSI/I2S3_SDO	USART3_CK	UART5_TX	-	-	-	SDMMC1_CK	DCMI_D9	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 11. Port D alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART1/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART1/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS/LCD	I2C4/UART7/SWP/DFSDM/SDMMC2/MDIOS/ETH	FMC/SDMMC1/MDIOS/OTG2_FS/LCD	DCMI/LCD	UART5/LCD	SYS
Port D	PD0	-	-	-	DFSDM_CKIN6	-	-	SAI3_SCK_A	-	UART4_RX	CAN1_RX	-	-	FMC_D2/FMC_DA2	-	-	EVENTOUT
	PD1	-	-	-	DFSDM_DATIN6	-	-	SAI3_SD_A	-	UART4_TX	CAN1_TX	-	-	FMC_D3/FMC_DA3	-	-	EVENTOUT
	PD2	TRACED2	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	-	-	SDMMC1_CMD	DCMI_D11	-	EVENTOUT

Table 11. Port D alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/4/5/12/ HRTIM1	LPUART1/ TIM8/ LPTIM2/3/4/5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/ CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/ SAI1/3/ I2C4/UART4/DFSDM	SPI2/3/6/ USART1/2/3/6/UART7/ SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART1/SDMMC1/SPDIFRX	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX	SAI2/4/ QUADSPI/ SDMMC2/ OTG2_HS/ OTG1_FS/ LCD	I2C4/ UART7/ SWP/ DFSDM/ SDMMC2/ MDIOS/ ETH	FMC/ SDMMC1/ MDIOS/ OTG2_FS/LCD	DCMI/LCD	UART5/ LCD	SYS
Port D	PD3	-	-	-	DFSDM_ CKOUT	-	SPI2_SCK/ I2S2_CK	-	USART2_ CTS_NSS	-	-	-	-	FMC_CLK	DCMI_D5	LCD_G7	EVENT OUT
	PD4	-	-	HRTIM_ FLT3	-	-	-	SAI3_FS_A	USART2_ RTS	-	CAN1_ RXFD	-	-	FMC_NOE	-	-	EVENT OUT
	PD5	-	-	HRTIM_ EEV3	-	-	-	-	USART2_ TX	-	CAN1_ TXFD	-	-	FMC_NWE	-	-	EVENT OUT
	PD6	-	-	SAI1_D1	DFSDM_ CKIN4	DFSDM_ DATIN1	SPI3_MOSI /I2S3_SDO	SAI1_SD_A	USART2_ RX	SAI4_SD_ A	CAN2_ RXFD	SAI4_D1	SDMMC2_ CK	FMC_ NWAIT	DCMI_D10	LCD_B2	EVENT OUT
	PD7	-	-	-	DFSDM_ DATIN4	-	SPI1_MOSI /I2S1_SDO	DFSDM_ CKIN1	USART2_ CK	-	SPDIFRX_ IN0	-	SDMMC2_ CMD	FMC_NE1	-	-	EVENT OUT
	PD8	-	-	-	DFSDM_ CKIN3	-	-	SAI3_SCK_ B	USART3_ TX	-	SPDIFRX_ IN1	-	-	FMC_D13/ FMC_DA13	-	-	EVENT OUT
	PD9	-	-	-	DFSDM_ DATIN3	-	-	SAI3_SD_B	USART3_ RX	-	CAN2_ RXFD	-	-	FMC_D14/ FMC_DA14	-	-	EVENT OUT
	PD10	-	-	-	DFSDM_ CKOUT	-	-	SAI3_FS_B	USART3_ CK	-	CAN2_ TXFD	-	-	FMC_D15/ FMC_DA15	-	LCD_B3	EVENT OUT
	PD11	-	-	-	LPTIM2_ IN2	I2C4_SMBA	-	-	USART3_ CTS	-	QUADSPI_ BK1_IO0	SAI2_SD_A	-	FMC_A16	-	-	EVENT OUT
	PD12	-	LPTIM1_IN1	TIM4_CH1	LPTIM2_ IN1	I2C4_SCL	-	-	USART3_ RTS	-	QUADSPI_ BK1_IO1	SAI2_FS_A	-	FMC_A17	-	-	EVENT OUT
	PD13	-	LPTIM1_ OUT	TIM4_CH2	-	I2C4_SDA	-	-	-	-	QUADSPI_ BK1_IO3	SAI2_SCK_ A	-	FMC_A18	-	-	EVENT OUT
	PD14	-	-	TIM4_CH3	-	-	-	SAI3_MCLK _B	-	UART8_ CTS	-	-	-	FMC_D0/ FMC_DA0	-	-	EVENT OUT
	PD15	-	-	TIM4_CH4	-	-	-	SAI3_MCLK _A	-	UART8_ RTS	-	-	-	FMC_D1/ FMC_DA1	-	-	EVENT OUT

Table 12. Port E alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/4/5/12/ HRTIM1	LPUART1/ TIM8/ LPTIM2/3/4/5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/ SAI1/3/ I2C4/UART4/DFSDM	SPI2/3/6/ USART1/2/3/6/UART7/ SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART1/SDMMC1/SPDIFRX	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD	SAI2/4/ QUADSPI/ OTG2_HS/ OTG1_FS/ LCD	TIM1/ SDMMC2/ MDIOS/ ETH/ COMP1/2	FMC/ SDMMC1/ MDIOS/ OTG2_FS/ LCD	DCMI/LCD/ /COMP1/2	UART5/ LCD	SYS
Port E	PE0	-	LPTIM1_ ETR	TIM4_ETR	HRTIM_ SCIN	LPTIM2_ ETR	-	-	-	UART8_RX	CAN1_ RXFD	SAI2_MCK _A	-	FMC_ NBL0	DCMI_D2	-	EVENT OUT
	PE1	-	LPTIM1_IN2	-	HRTIM_ SCOUT	-	-	-	-	UART8_TX	CAN1_ TXFD	-	-	FMC_ NBL1	DCMI_D3	-	EVENT OUT
	PE2	TRACECLK	-	SAI1_CK1	-	-	SPI4_SCK	SAI1_MCLK _A	-	SAI4_MCL K_A	QUADSPI_ BK1_IO2	SAI4_CK1	ETH_MII_ TXD3	FMC_A23	-	-	EVENT OUT
	PE3	TRACED0	-	-	-	TIM15_BKIN	-	SAI1_SD_B	-	SAI4_SD_ B	-	-	-	FMC_A19	-	-	EVENT OUT
	PE4	TRACED1	-	SAI1_D2	DFSDM_ DATIN3	TIM15_ CH1N	SPI4_NSS	SAI1_FS_A	-	SAI4_FS_A	-	SAI4_D2	-	FMC_A20	DCMI_D4	LCD_B0	EVENT OUT
	PE5	TRACED2	-	SAI1_CK2	DFSDM_ CKIN3	TIM15_CH1	SPI4_MISO	SAI1_SCK_ A	-	SAI4_SCK _A	-	SAI4_CK2	-	FMC_A21	DCMI_D6	LCD_ G0	EVENT OUT
	PE6	TRACED3	TIM1_ BKIN2	SAI1_D1	-	TIM15_CH2	SPI4_MOSI	SAI1_SD_A	-	SAI4_SD_ A	SAI4_D1	SAI2_MCK _B	TIM1_BKIN 2_COMP1/ TIM1_BKIN 2_COMP2	FMC_A22	DCMI_D7	LCD_G1	EVENT OUT
	PE7	-	TIM1_ETR	-	DFSDM_ DATIN2	-	-	-	UART7_RX	-	-	QUADSPI_ BK2_IO0	-	FMC_D4/ FMC_DA4	-	-	EVENT OUT
	PE8	-	TIM1_CH1N	-	DFSDM_ CKIN2	-	-	-	UART7_TX	-	-	QUADSPI_ BK2_IO1	-	FMC_D5/ FMC_DA5	COMP2_ OUT	-	EVENT OUT
	PE9	-	TIM1_CH1	-	DFSDM_ CKOUT	-	-	-	UART7_ RTS	-	-	QUADSPI_ BK2_IO2	-	FMC_D6/ FMC_DA6	-	-	EVENT OUT
	PE10	-	TIM1_CH2N	-	DFSDM_ DATIN4	-	-	-	UART7_ CTS	-	-	QUADSPI_ BK2_IO3	-	FMC_D7/ FMC_DA7	-	-	EVENT OUT
	PE11	-	TIM1_CH2	-	DFSDM_ CKIN4	-	SPI4_NSS	-	-	-	-	SAI2_SD_B	-	FMC_D8/ FMC_DA8	-	LCD_G3	EVENT OUT
	PE12	-	TIM1_CH3N	-	DFSDM_ DATIN5	-	SPI4_SCK	-	-	-	-	SAI2_SCK_ B	-	FMC_D9/ FMC_DA9	COMP1_ OUT	LCD_B4	EVENT OUT
	PE13	-	TIM1_CH3	-	DFSDM_ CKIN5	-	SPI4_MISO	-	-	-	-	SAI2_FS_B	-	FMC_D10/ FMC_DA10	COMP2_ OUT	LCD_DE	EVENT OUT
	PE14	-	TIM1_CH4	-	-	-	SPI4_MOSI	-	-	-	-	SAI2_MCK _B	-	FMC_D11/ FMC_DA11	-	LCD_CLK	EVENT OUT
	PE15	-	TIM1_BKIN	-	-	-	-	-	-	-	-	-	-	FMC_D12/ FMC_DA12	TIM1_BKIN _COMP1/ TIM1_BKIN _COMP2	LCD_R7	EVENT OUT

Table 13. Port F alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART1/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART1/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS/LCD	I2C4/UART7/SWP/DFSDM/SDMMC2/MDIOS/ETH	FMC/SDMMC1/MDIOS/OTG2_FS/LCD	DCMI/LCD	UART5/LCD	SYS
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	FMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	-	FMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	-	FMC_A2	-		EVENTOUT
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A3	-		EVENTOUT
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A4	-		EVENTOUT
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A5	-		EVENTOUT
	PF6	-	TIM16_CH1	-	-	-	SPI5_NSS	SAI1_SD_B	UART7_RX	SAI4_SD_B	QUADSPI_BK1_IO3	-	-	-	-		EVENTOUT
	PF7	-	TIM17_CH1	-	-	-	SPI5_SCK	SAI1_MCLK_B	UART7_TX	SAI4_MCLK_B	QUADSPI_BK1_IO2	-	-	-	-		EVENTOUT
	PF8	-	TIM16_CH1N	-	-	-	SPI5_MISO	SAI1_SCK_B	UART7_RTS	SAI4_SCK_B	TIM13_CH1	QUADSPI_BK1_IO0	-	-	-	-	EVENTOUT
	PF9	-	TIM17_CH1N	-	-	-	SPI5_MOSI	SAI1_FS_B	UART7_CTS	SAI4_FS_B	TIM14_CH1	QUADSPI_BK1_IO1	-	-	-	-	EVENTOUT
	PF10	-	TIM16_BKIN	SAI1_D3	-	-	-	-	-	-	QUADSPI_CLK	SAI4_D3	-	-	DCMI_D11	LCD_DE	EVENTOUT
	PF11	-	-	-	-	-	SPI5_MOSI	-	-	-	-	SAI2_SD_B	-	FMC_SDNRAS	DCMI_D12	-	EVENTOUT
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	EVENTOUT
	PF13	-	-	-	DFSDM_DATIN6	I2C4_SMBA	-	-	-	-	-	-	-	FMC_A7	-	-	EVENTOUT
	PF14	-	-	-	DFSDM_CKIN6	I2C4_SCL	-	-	-	-	-	-	-	FMC_A8	-	-	EVENTOUT
	PF15	-	-	-	-	I2C4_SDA	-	-	-	-	-	-	-	FMC_A9	-	-	EVENTOUT

Table 14. Port G alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/4/5/12/ HRTIM1	LPUART1/ TIM8/ LPTIM2/3/4/5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/ SAI1/3/ I2C4/UART4/DFSDM	SPI2/3/6/ USART1/2/3/6/UART7/ SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART1/SDMMC1/SPDIFRX	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX	SAI2/4/ QUADSPI/ SDMMC2/ OTG2_HS/ OTG1_FS/ LCD	I2C4/ UART7/ SWP/ DFSDM/ SDMMC2/ MDIOS/ ETH/ COMP1/2	FMC/ SDMMC1/ MDIOS/ OTG2_FS/ LCD	DCMI/LCD	UART5/ LCD	SYS
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A10	-	-	EVENT OUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A11	-	-	EVENT OUT
	PG2	-	-	-	TIM8_BKIN	-	-	-	-	-	-	-	TIM8_BKIN_COMP1/ TIM8_BKIN_COMP2	FMC_A12	-	-	EVENT OUT
	PG3	-	-	-	TIM8_ BKIN2	-	-	-	-	-	-	-	TIM8_BKIN2_COMP1/ TIM8_BKIN2_COMP2	FMC_A13	-	-	EVENT OUT
	PG4	-	TIM1_ BKIN2	-	-	-	-	-	-	-	-	-	TIM1_ BKIN2_ COMP1/ TIM1_ BKIN2_ COMP2	FMC_A14/ FMC_BA0	-	-	EVENT OUT
	PG5	-	TIM1_ETR	-	-	-	-	-	-	-	-	-	-	FMC_A15/ FMC_BA1	-	-	EVENT OUT
	PG6	-	TIM17_ BKIN	HRTIM_ CHE1	-	-	-	-	-	-	-	QUADSPI_ BK1_NCS	-	FMC_NE3	DCMI_D12	LCD_R7	EVENT OUT
	PG7	-	-	HRTIM_ CHE2	-	-	-	SAI1_MCLK_A	USART6_ CK	-	-	-	-	FMC_INT	DCMI_D13	LCD_ CLK	EVENT OUT
	PG8	-	-	-	TIM8_ETR	-	SPI6_NSS	-	USART6_ RTS	SPDIFRX_ IN2	-	-	ETH_PPS_ OUT	FMC_ SDCLK	-	LCD_G7	EVENT OUT
	PG9	-	-	-		-	SPI1_MISO /I2S1_SDI	-	USART6_R X	SPDIFRX_ IN3	QUADSPI_ BK2_IO2	SAI2_FS_B	-	FMC_NE2/ FMC_NCE	DCMI_ VSYNC	-	EVENT OUT
	PG10	-	-	HRTIM_ FLT5	-	-	SPI1_NSS/ I2S1_WS	-	-	-	LCD_G3	SAI2_SD_B	-	FMC_NE3	DCMI_D2	LCD_B2	EVENT OUT
	PG11	-	-	HRTIM_ EEV4	-	-	SPI1_SCK/ I2S1_CK	-		SPDIFRX_ IN0	-	SDMMC2_ D2	-	-	DCMI_D3	LCD_B3	EVENT OUT
	PG12	-	LPTIM1_IN1	HRTIM_EE V5	-	-	SPI6_MISO	-	USART6_R TS	SPDIFRX_ IN1	LCD_B4	-	-	FMC_NE4	-	LCD_B1	EVENT OUT
	PG13	TRACED0	LPTIM1_ OUT	HRTIM_ EEV10	-	-	SPI6_SCK	-	USART6_ CTS_NSS	-	-	-	-	FMC_A24	-	LCD_R0	EVENT OUT

Table 14. Port G alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART1/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART1/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS/LCD	I2C4/UART7/SWP/DFSDM/SDMMC2/MDIOS/ETH/COMP1/2	FMC/SDMMC1/MDIOS/OTG2_FS/LCD	DCMI/LCD	UART5/LCD	SYS
Port G	PG14	TRACED1	LPTIM1_ETR	-	-	-	SPI6_MOSI	-	USART6_TX	-	QUADSPI_BK2_IO3	-	ETH_MII_TXD1/ETH_RMII_TXD1	FMC_A25	-	LCD_B0	EVENT OUT
	PG15	-	-	-	-	-	-	-	USART6_CTS_NSS	-	-	-	-	FMC_SDNCAS	DCMI_D13	-	EVENT OUT

Table 15. Port H alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART1/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART1/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS/LCD	I2C4/UART7/SWP/DFSDM/SDMMC2/MDIOS/ETH	FMC/SDMMC1/MDIOS/OTG2_FS/LCD	DCMI/LCD	UART5/LCD	SYS
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PH2	-	LPTIM1_IN2	-	-	-	-	-	-	-	QUADSPI_BK2_IO0	SAI2_SCK_B	ETH_MII_CRS	FMC_SDCKE0	-	LCD_R0	EVENT OUT
	PH3	-	-	-	-	-	-	-	-	-	QUADSPI_BK2_IO1	SAI2_MCK_B	ETH_MII_COL	FMC_SDNE0	-	LCD_R1	EVENT OUT
	PH4	-	-	-	-	I2C2_SCL	-	-	-	-	LCD_G5	OTG_HS_ULPI_NXT	-	-	-	LCD_G4	EVENT OUT
	PH5	-	-	-	-	I2C2_SDA	SPI5_NSS	-	-	-	-	-	-	FMC_SDNWE	-	-	EVENT OUT
	PH6	-	-	TIM12_CH1	-	I2C2_SMBA	SPI5_SCK	-	-	-	-	-	ETH_MII_RXD2	FMC_SDNE1	DCMI_D8	-	EVENT OUT
	PH7	-	-		-	I2C3_SCL	SPI5_MISO	-	-	-	-	-	ETH_MII_RXD3	FMC_SDCKE1	DCMI_D9	-	EVENT OUT
	PH8	-	-	TIM5_ETR	-	I2C3_SDA	-	-	-	-	-	-	-	FMC_D16	DCMI_HSYNC	LCD_R2	EVENT OUT

Table 15. Port H alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/4/5/12/ HRTIM1	LPUART1/ TIM8/ LPTIM2/3/4/5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/ SAI1/3/ I2C4/UART4/DFSDM	SPI2/3/6/ USART1/2/3/6/UART7/ SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART1/SDMMC1/SPDIFRX	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX	SAI2/4/ QUADSPI/ SDMMC2/ OTG2_HS/ OTG1_FS/ LCD	I2C4/ UART7/ SWP/ DFSDM/ SDMMC2/ MDIOS/ ETH	FMC/ SDMMC1/ MDIOS/ OTG2_FS/ LCD	DCMI/LCD	UART5/ LCD	SYS
Port H	PH9	-	-	TIM12_CH2	-	I2C3_SMBA	-	-	-	-	-	-	-	FMC_D17	DCMI_D0	LCD_R3	EVENTOUT
	PH10	-	-	TIM5_CH1	-	I2C4_SMBA	-	-	-	-	-	-	-	FMC_D18	DCMI_D1	LCD_R4	EVENTOUT
	PH11	-	-	TIM5_CH2	-	I2C4_SCL								FMC_D19	DCMI_D2	LCD_R5	EVENTOUT
	PH12	-	-	TIM5_CH3	-	I2C4_SDA	-	-	-	-	-	-	-	FMC_D20	DCMI_D3	LCD_R6	EVENTOUT
	PH13	-	-	-	TIM8_CH1N	-	-	-	-	UART4_TX	CAN1_TX	-	-	FMC_D21	-	LCD_G2	EVENTOUT
	PH14	-	-	-	TIM8_CH2N	-	-	-	-	UART4_RX	CAN1_RX	-	-	FMC_D22	DCMI_D4	LCD_G3	EVENTOUT
	PH15	-	-	-	TIM8_CH3N	-	-	-	-	-	CAN1_TXFD	-	-	FMC_D23	DCMI_D11	LCD_G4	EVENTOUT

Table 16. Port I alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/4/5/12/ HRTIM1	LPUART1/ TIM8/ LPTIM2/3/4/5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/ SAI1/3/ I2C4/UART4/DFSDM	SPI2/3/6/ USART1/2/3/6/UART7/ SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART1/SDMMC1/SPDIFRX	SAI4/ FDCAN1/2/ TIM13/14/ SDMMC2/ LCD	SAI2/4/ QUADSPI/ SDMMC2/ OTG2_HS/ OTG1_FS/ LCD/	I2C4/ UART7/ SWP/ MDIOS/ ETH/ COMP1/2	FMC/ SDMMC1/ MDIOS/ OTG2_FS/ LCD	DCMI/LCD	UART5/ LCD	SYS
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS/ I2S2_WS	-	-	-	CAN1_ RXFD	-	-	FMC_D24	DCMI_D13	LCD_G5	EVENT OUT
	PI1	-	-	-	TIM8_ BKIN2	-	SPI2_SCK/ I2S2_CK	-	-	-	-	-	TIM8_BKIN 2_COMP1/ TIM8_BKIN 2_COMP2	FMC_D25	DCMI_D8	LCD_G6	EVENT OUT
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO /I2S2_SDI	-	-	-	-	-	-	FMC_D26	DCMI_D9	LCD_G7	EVENT OUT
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI /I2S2_SDO	-	-	-	-	-	-	FMC_D27	DCMI_D10	-	EVENT OUT
	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	SAI2_MCK _A	TIM8_BKIN _COMP1/ TIM8_BKIN _COMP2	FMC_NBL2	DCMI_D5	LCD_B4	EVENT OUT
	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	SAI2_SCK_ A	-	FMC_NBL3	DCMI_ VSYNC	LCD_B5	EVENT OUT
	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	SAI2_SD_A	-	FMC_D28	DCMI_D6	LCD_B6	EVENT OUT
	PI7	-	-	-	TIM8_CH3	-	-	-	-	-	-	SAI2_FS_A	-	FMC_D29	DCMI_D7	LCD_B7	EVENT OUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PI9	-	-	-	-	-	-	-	-	UART4_RX	CAN1_RX	-	-	FMC_D30	-	LCD_ VSYNC	EVENT OUT
	PI10	-	-	-	-	-	-	-	-	-	CAN1_ RXFD	-	ETH_MII_ RX_ER	FMC_D31	-	LCD_ HSYNC	EVENT OUT
	PI11	-	-	-	-	-	-	-	-	-	LCD_G6	OTG_HS_U LPI_DIR	-	-	-	-	EVENT OUT
	PI12	-	-	-	-	-	-	-	-	-	-	-	ETH_TX_ ER	-	-	LCD_ HSYNC	EVENT OUT
	PI13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_ VSYNC	EVENT OUT
	PI14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK	EVENT OUT
	PI15	-	-	-	-	-	-	-	-	-	LCD_G2	-	-	-	-	LCD_R0	EVENT OUT

Table 17. Port J alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/ 4/5/12/ HRTIM1	LPUART1/ TIM8/ LPTIM2/3/4 /5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/ 5/6/CEC	SPI2/3/ SAI1/3/ I2C4/UART 4/DFSDM	SPI2/3/6/ USART1/2/ 3/6/UART7/ SDMMC1	SPI6/SAI2/ 4/UART4/5 /8/LPUART 1/SDMMC1 /SPDIFRX	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX	SAI2/4/ QUADSPI/ SDMMC2/ OTG2_HS/ OTG1_FS/ LCD	I2C4/ UART7/ SWP/ DFSDM/ SDMMC2/ MDIOS/ ETH	FMC/ SDMMC1/ MDIOS/ OTG2_FS/ LCD	DCMI/LCD	UART5/ LCD	SYS
Port J	PJ0	-	-	-	-	-	-	-	-	-	LCD_R7	-	-	-	-	LCD_R1	EVENTOUT
	PJ1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R2	EVENTOUT
	PJ2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R3	EVENTOUT
	PJ3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R4	EVENTOUT
	PJ4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R5	EVENTOUT
	PJ5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_R6	EVENTOUT
	PJ6	-	-	-	TIM8_CH2	-	-	-	-	-	-	-	-	-	-	LCD_R7	EVENTOUT
	PJ7	TRGIN	-	-	TIM8_ CH2N	-	-	-	-	-	-	-	-	-	-	LCD_G0	EVENTOUT
	PJ8	-	TIM1_CH3N	-	TIM8_CH1	-	-	-	-	UART8_TX	-	-	-	-	-	LCD_G1	EVENTOUT
	PJ9	-	TIM1_CH3	-	TIM8_ CH1N	-	-	-	-	UART8_RX	-	-	-	-	-	LCD_G2	EVENTOUT
	PJ10	-	TIM1_CH2N	-	TIM8_CH2	-	SPI5_MOSI	-	-	-	-	-	-	-	-	LCD_G3	EVENTOUT
	PJ11	-	TIM1_CH2	-	TIM8_ CH2N	-	SPI5_MISO	-	-	-	-	-	-	-	-	LCD_G4	EVENTOUT
	PJ12	TRGOUT	-	-	-	-	-	-	-	-	LCD_G3	-	-	-	-	LCD_B0	EVENTOUT
	PJ13	-	-	-	-	-	-	-	-	-	LCD_B4	-	-	-	-	LCD_B1	EVENTOUT
	PJ14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B2	EVENTOUT
	PJ15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B3	EVENTOUT

Table 18. Port K alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/ 4/5/12/ HRTIM1	LPUART1/ TIM8/ LPTIM2/3/4 /5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/ 5/6/CEC	SPI2/3/ SAI1/3/ I2C4/UART 4/DFSDM	SPI2/3/6/ USART1/2/ 3/6/UART7/ SDMMC1	SPI6/SAI2/ 4/UART4/5 /8/LPUART 1/SDMMC1 /SPDIFRX	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/ SPDIFRX	SAI2/4/ QUADSPI/ SDMMC2/ OTG2_HS/ OTG1_FS/ LCD/COMP	I2C4/ UART7/ SWP/ DFSDM/ SDMMC2/ MDIOS/ ETH/COMP	FMC/ SDMMC1/ MDIOS/ OTG2_FS/ LCD	DCMI/LCD	UART5/ LCD	SYS
Port K	PK0	-	TIM1_CH1N	-	TIM8_CH3	-	SPI5_SCK	-	-	-	-	-	-	-	-	LCD_G5	EVENT OUT
	PK1	-	TIM1_CH1	-	TIM8_ CH3N	-	SPI5_NSS	-	-	-	-	-	-	-	-	LCD_G6	EVENT OUT
	PK2	-	TIM1_BKIN	-	TIM8_BKIN	-	-	-	-	-	-	TIM8_BKIN _COMP1/ TIM8_BKIN _COMP2	TIM1_BKIN _COMP1/ TIM1_BKIN _COMP2	-	-	LCD_G7	EVENT OUT
	PK3		-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B4	EVENT OUT
	PK4		-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B5	EVENT OUT
	PK5		-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B6	EVENT OUT
	PK6		-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_B7	EVENT OUT
	PK7		-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DE	EVENT OUT

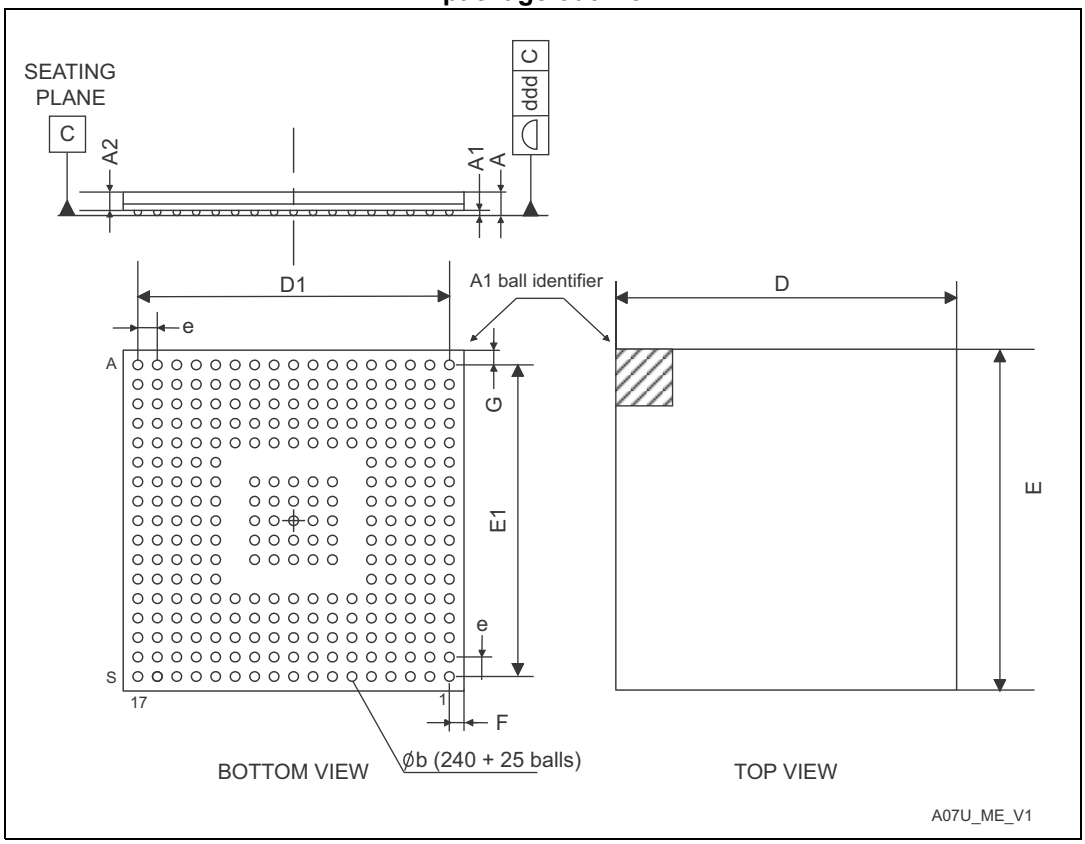
5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status *are available at www.st.com.* ECOPACK® is an ST trademark.

5.1 TFBGA240+25 package information

TFBGA265 package information is preliminary information which are subject to change.

Figure 9. TFBGA240+25 - 265 pin, 14x14 mm, 0.8 mm pitch, fine pitch ball grid array package outline



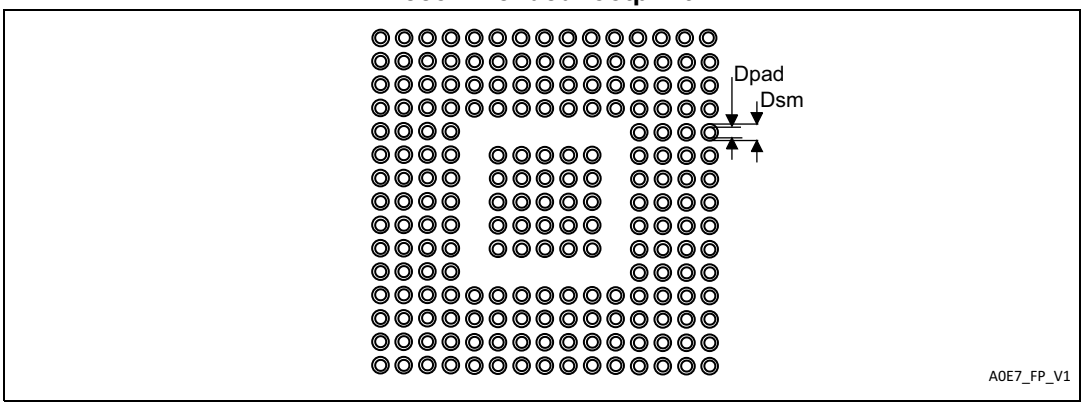
1. Dimensions are expressed in millimeters.

Table 19. TFBGA240+25 - 265 pin, 14x14 mm, 0.8 mm pitch, fine pitch ball grid array mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	13.850	14.000	14.150	0.5453	0.5512	0.5571
D1	-	12.800	-	-	0.5039	-
E	13.850	14.000	14.150	0.5453	0.5512	0.5571
E1	-	12.800	-	-	0.5039	-
e	-	0.800	-	-	0.0315	-
F	-	0.600	-	-	0.0236	-
G	-	0.600	-	-	0.0236	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 10. TFBGA240+25 - 265 pin pin, 14x14 mm 0.8 mm pitch recommended footprint



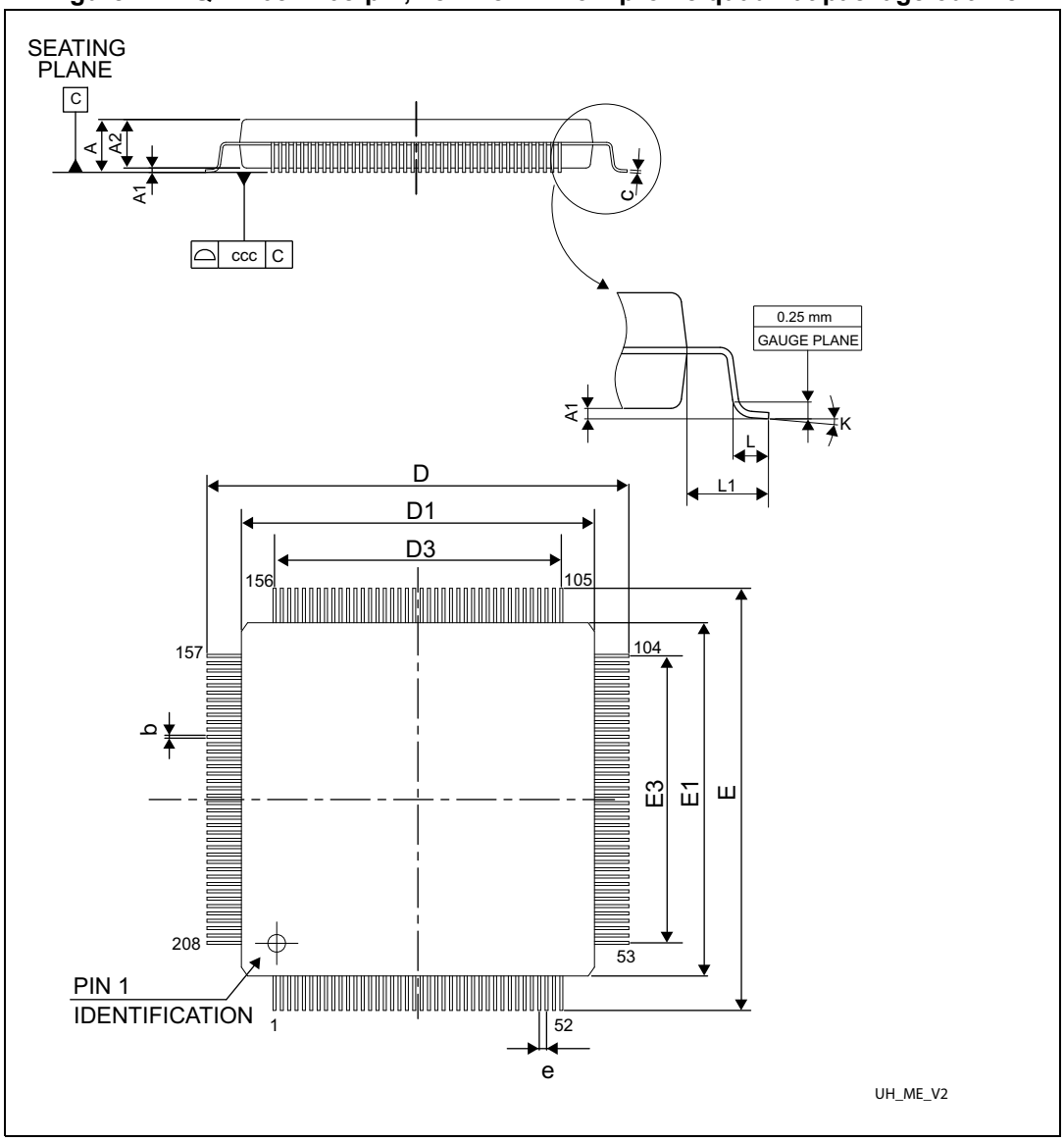
1. Dimensions are expressed in millimeters.

Table 20. TFBGA240+25, 265 pin recommended PCB design rules (0.8 mm pitch)

Dimension	Recommended values
Pitch	0.8 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

5.2 LQFP208 package information

Figure 11. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package outline



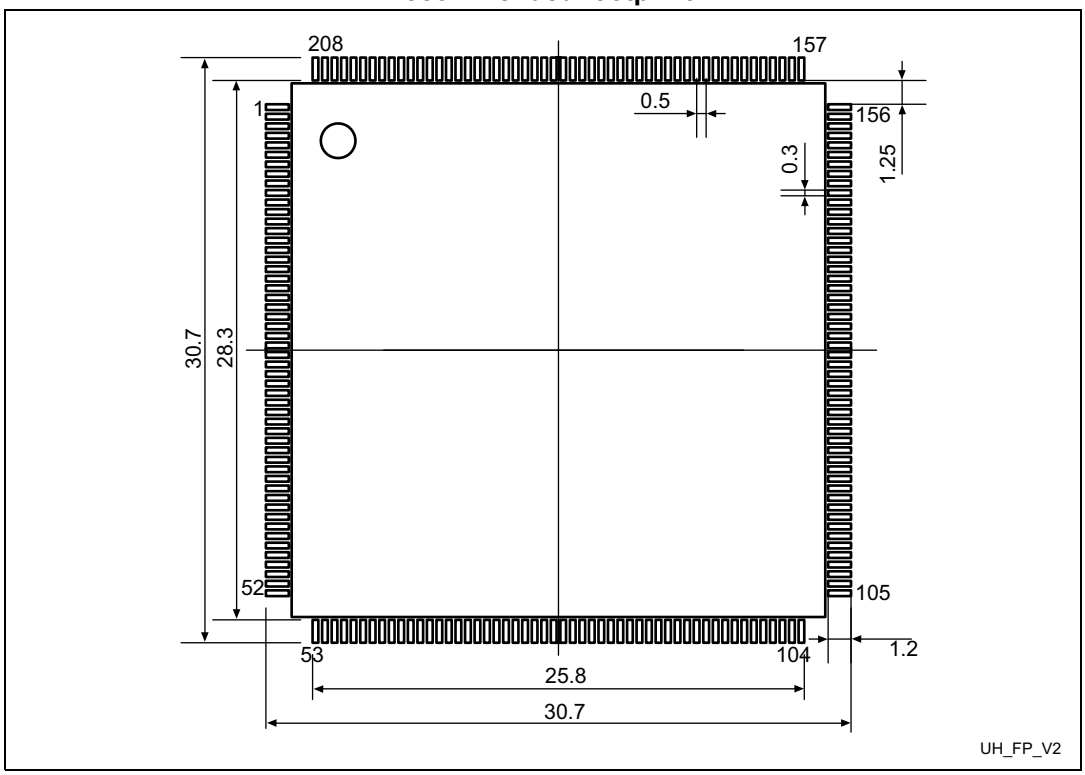
1. Drawing is not to scale.

Table 21. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	29.800	30.000	30.200	1.1811	1.1732	1.1890
D1	27.800	28.000	28.200	1.1024	1.0945	1.1102
D3	-	25.500	-	-	1.0039	-
E	29.800	30.000	30.200	1.1811	1.1732	1.1890
E1	27.800	28.000	28.200	1.1024	1.0945	1.1102
E3	-	25.500	-	-	1.0039	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

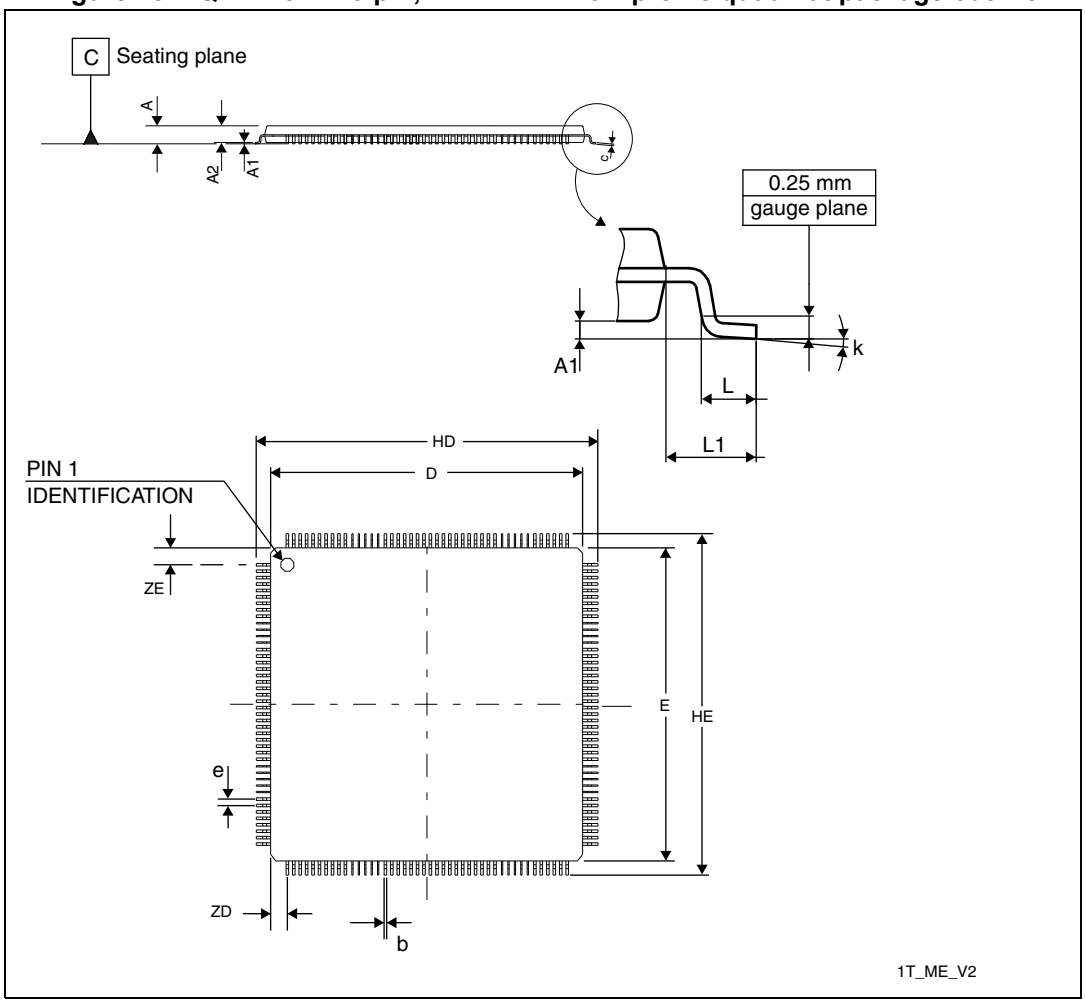
Figure 12. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

5.3 LQFP176 package information

Figure 13. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package outline



1. Drawing is not to scale.

Table 22. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package mechanical data

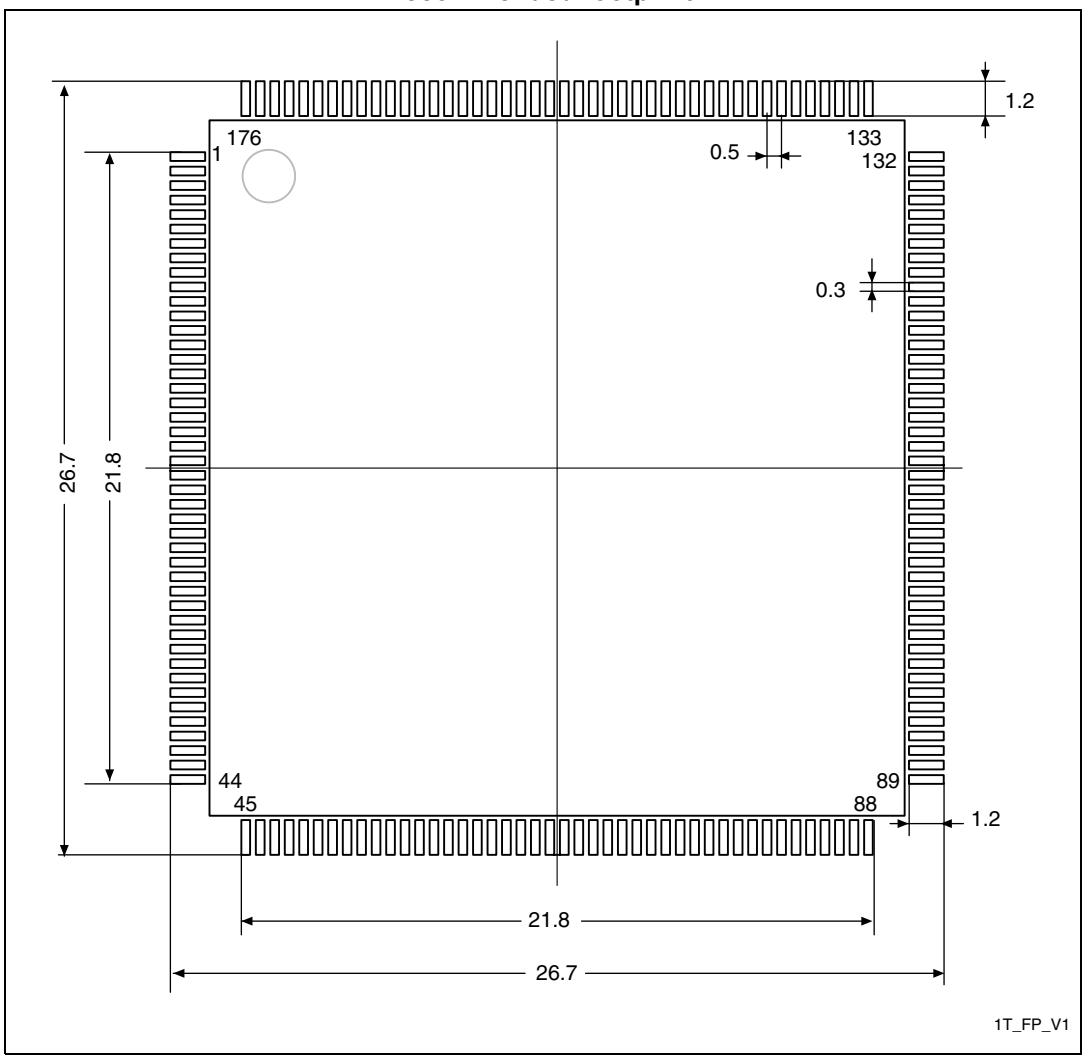
Ref.	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	-	1.450	0.0531	-	0.0571
b	0.170	-	0.270	0.0067	-	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	23.900	-	24.100	0.9409	-	0.9488

Table 22. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package mechanical data (continued)

Ref.	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
HD	25.900	-	26.100	1.0197	-	1.0276
ZD	-	1.250	-	-	0.0492	-
E	23.900	-	24.100	0.9409	-	0.9488
HE	25.900	-	26.100	1.0197	-	1.0276
ZE	-	1.250	-	-	0.0492	-
e	-	0.500	-	-	0.0197	-
L[2]	0.450	-	0.750	0.0177	-	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	7°	0°	-	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. L dimension is measured at gauge plane at 0.25 mm above the seating plane.

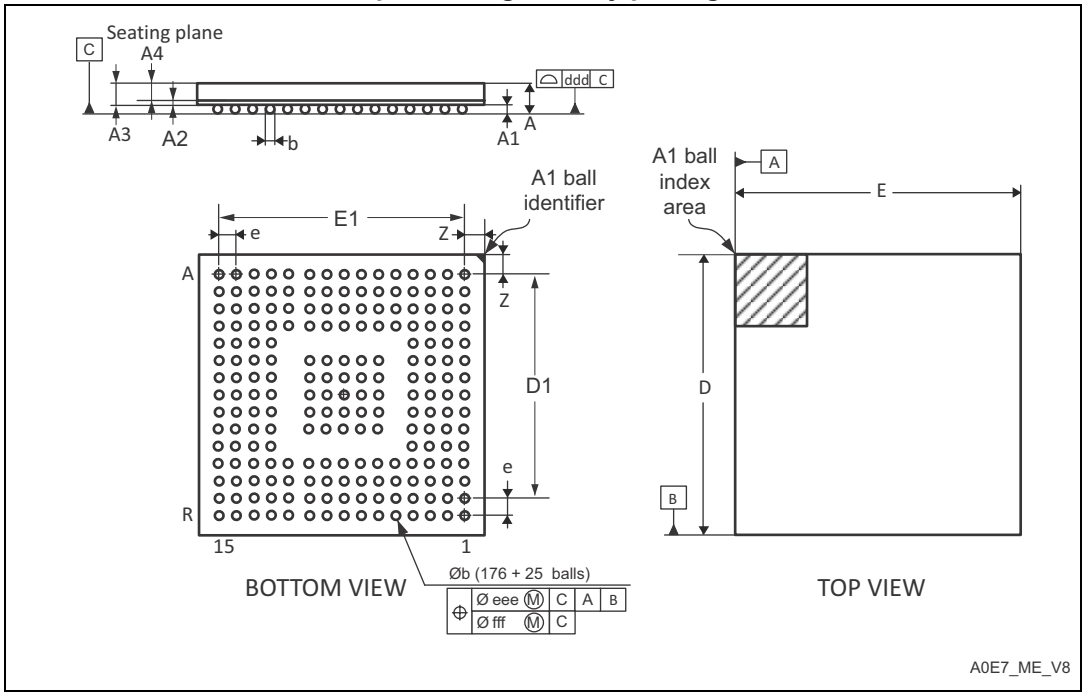
Figure 14. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

5.4 UFBGA176+25 package information

Figure 15. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 23. UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.130	-	-	0.0051	-
A3	-	0.450	-	-	0.0177	-
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
Z	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

Table 23. UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 16. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package recommended footprint

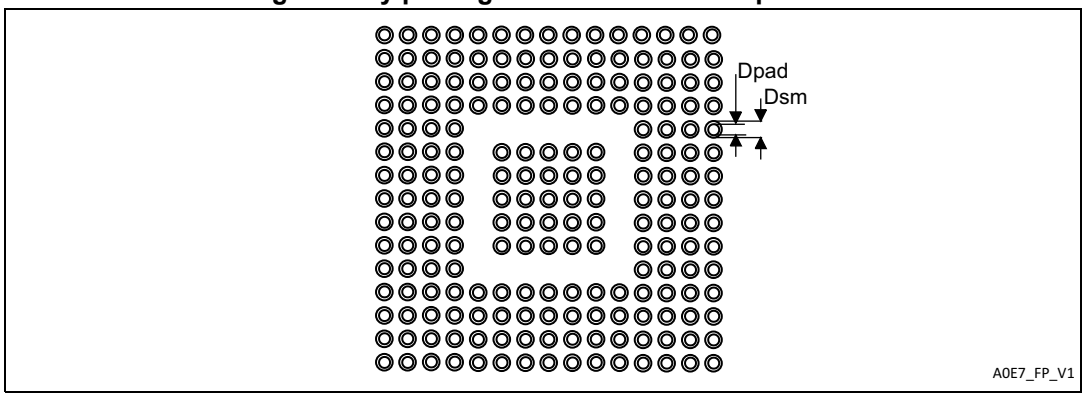
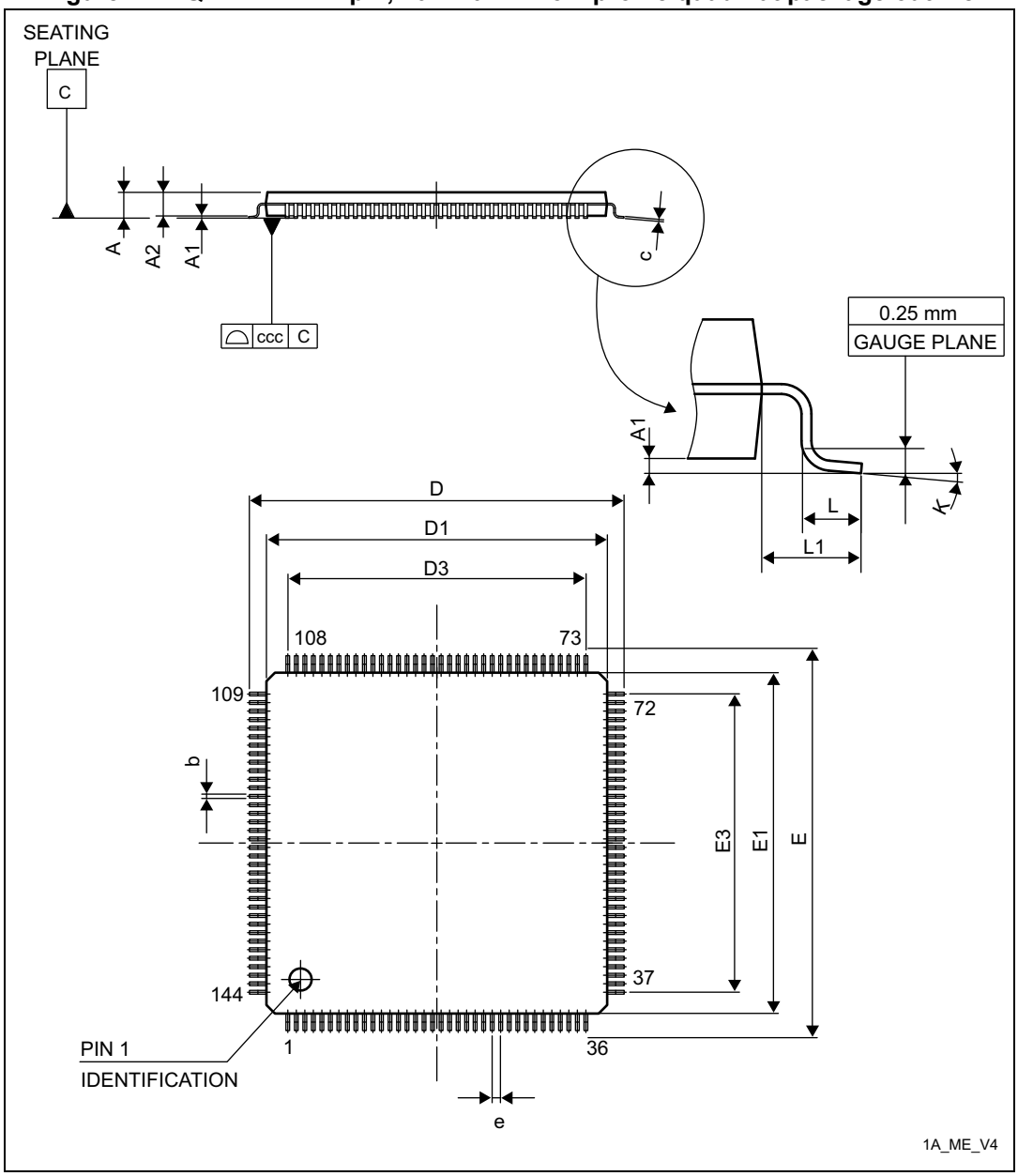


Table 24. UFBGA 176+25 recommended PCB design rules (0.65 mm pitch BGA)

Dimension	Recommended values
Pitch	0.65 mm
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.300 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

5.5 LQFP144 package information

Figure 17. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



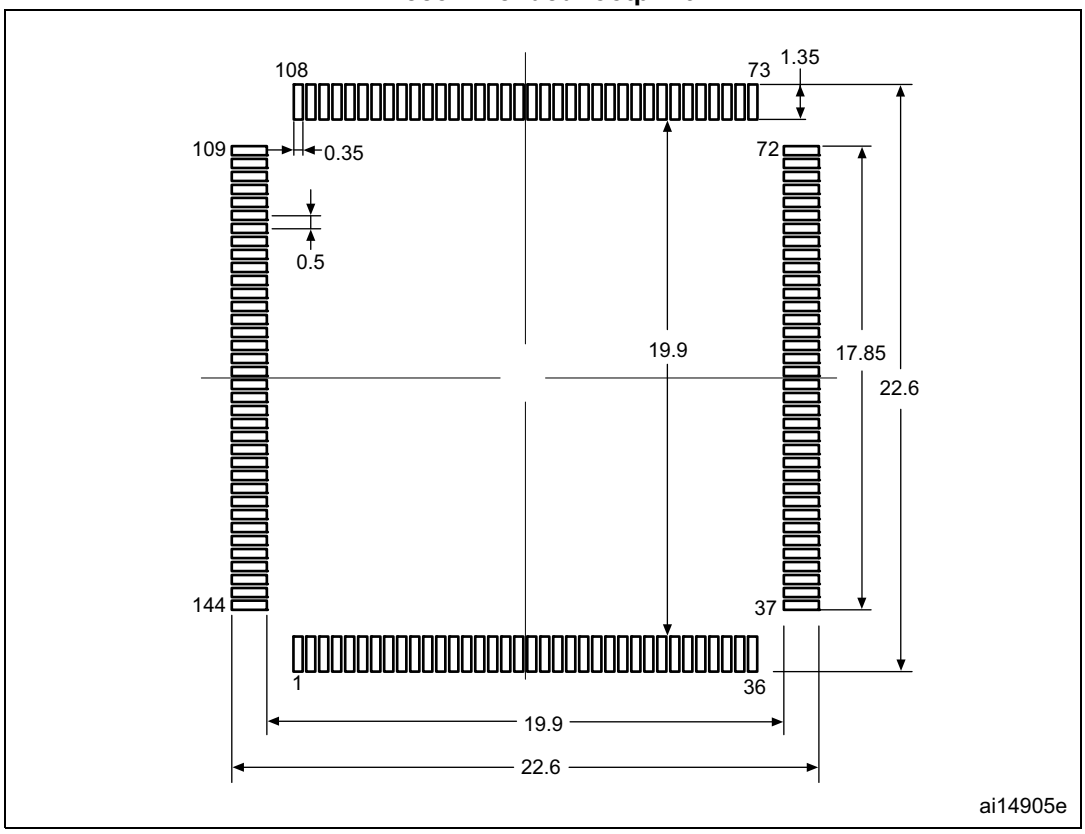
1. Drawing is not to scale.

Table 25. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

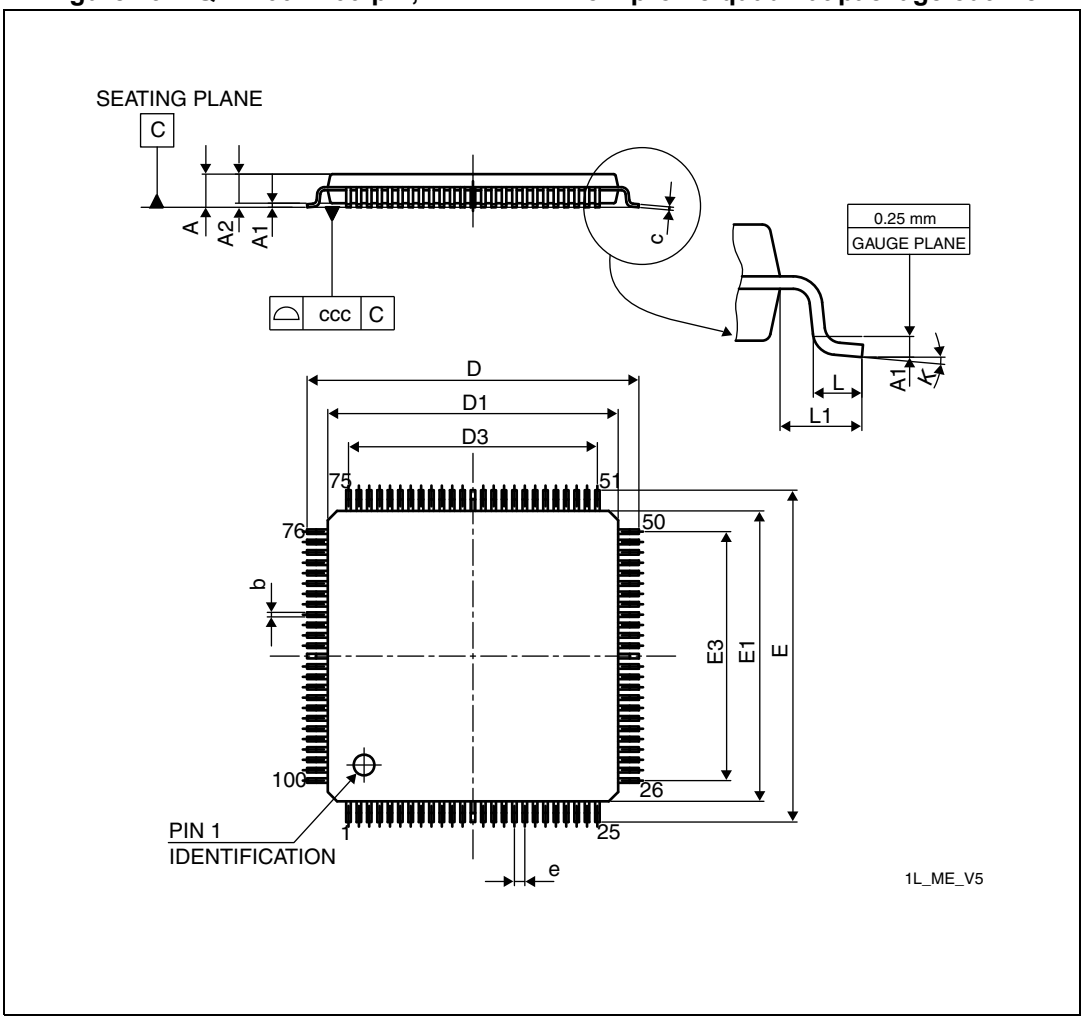
Figure 18. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

5.6 LQFP100 package information

Figure 19. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 26. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

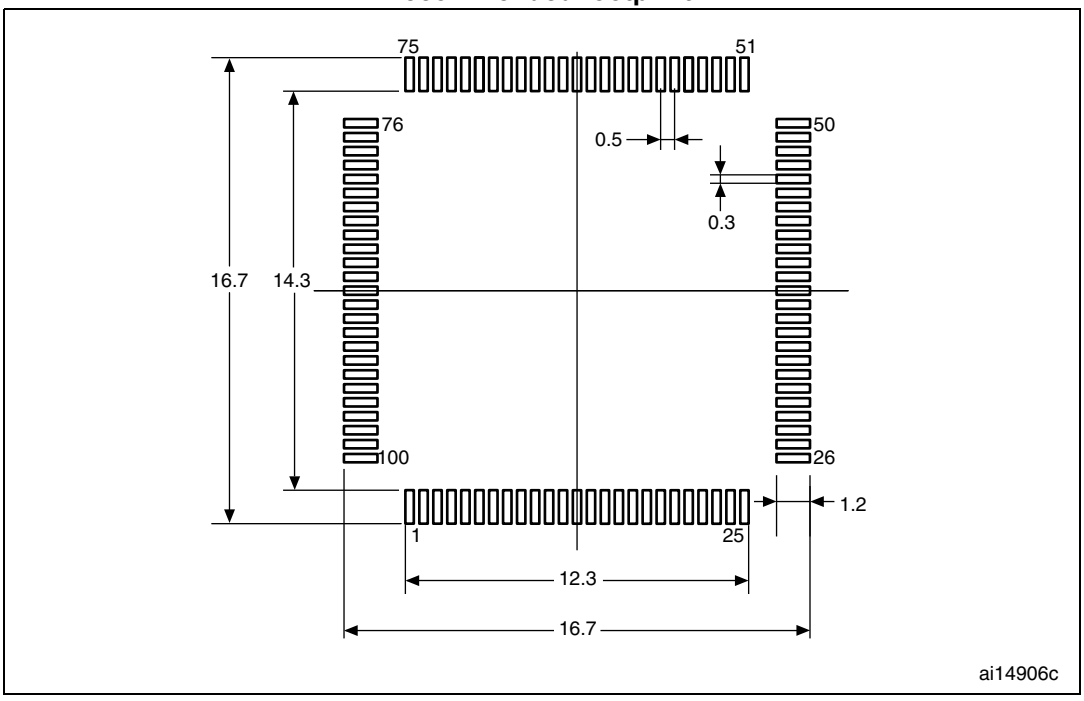
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591

Table 26. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 20. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

6 Ordering information

Table 27. STM32H743xI ordering information scheme

Example: STM32 H 743 V I T 6 TR

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

H = High performance

Device subfamily

743 = STM32H7x3 line

Pin count

V = 100 pins

Z = 144 pins

I = 176 pins/balls

B = 208 pins

X = 240 balls

Flash memory size

G = 1 Mbytes

I = 2 Mbytes

Package

T = LQFP

K = UFBGA

H = TFBGA

Temperature range

6 = Industrial temperature range, –40 to 85 °C

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

7 Revision history

Table 28. Document revision history

Date	Revision	Changes
14-Oct-2016	1	Initial release.
19-Oct-2016	2	*Features*: updated total current consumption and ADC sampling rate.