



# 12-Bit 10 $\mu$ s Serial CMOS Sampling ANALOG-to-DIGITAL CONVERTER

## FEATURES

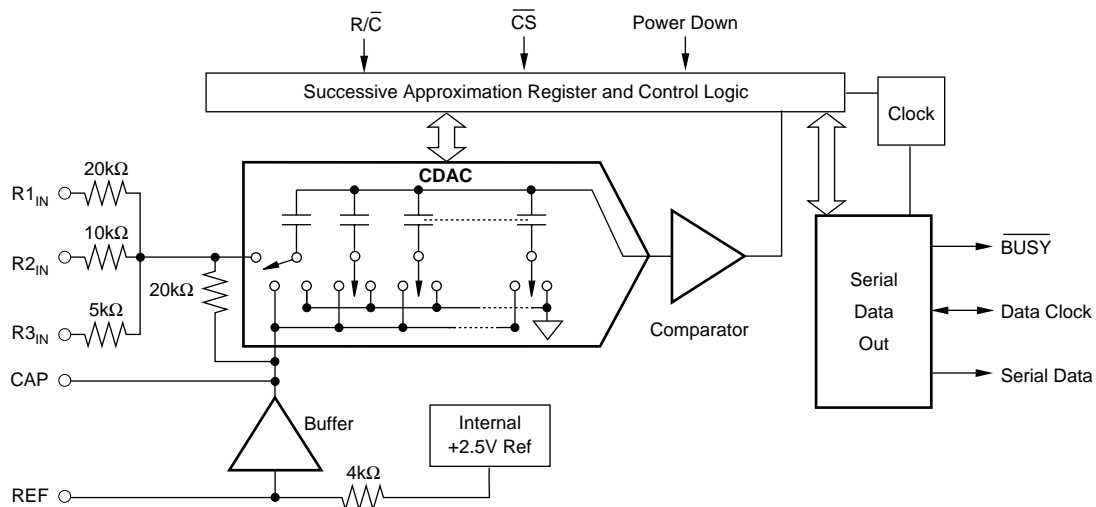
- 100kHz SAMPLING RATE
- 72dB SINAD WITH 45kHz INPUT
- $\pm 1/2$  LSB INL AND DNL
- SIX SPECIFIED INPUT RANGES
- SERIAL OUTPUT
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 16-BIT ADS7809
- USES INTERNAL OR EXTERNAL REFERENCE
- 100mW MAX POWER DISSIPATION
- 0.3" SO-20
- SIMPLE DSP INTERFACE

## DESCRIPTION

The ADS7808 is a complete 12-bit sampling analog-to-digital using state-of-the-art CMOS structures. It contains a 12-bit capacitor-based SAR A/D with S/H, reference, clock, and a serial data interface. Data can be output using the internal clock, or can be synchronized to an external data clock. The ADS7808 also provides an output synchronization pulse for ease of use with standard DSP processors.

The ADS7808 is specified at a 100kHz sampling rate, and specified over the full temperature range. Laser-trimmed scaling resistors provide various input ranges including  $\pm 10V$  and 0V to 5V, while an innovative design operates from a single +5V supply, with power dissipation under 100mW.

The ADS7808 is available in a 0.3" SO-20, fully specified for operation over the industrial  $-40^{\circ}C$  to  $+85^{\circ}C$  range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Analog Inputs: R1 <sub>IN</sub> .....	±25V
R2 <sub>IN</sub> .....	±25V
R3 <sub>IN</sub> .....	±25V
CAP .....	V <sub>ANA</sub> +0.3V to AGND2 -0.3V
REF .....	Indefinite Short to AGND2, Momentary Short to V <sub>ANA</sub>
Ground Voltage Differences: DGND, AGND2 .....	±0.3V
V <sub>ANA</sub> .....	7V
V <sub>DIG</sub> to V <sub>ANA</sub> .....	+0.3
V <sub>DIG</sub> .....	7V
Digital Inputs .....	-0.3V to V <sub>DIG</sub> +0.3V
Maximum Junction Temperature .....	+165°C
Internal Power Dissipation .....	700mW
Lead Temperature (soldering, 10s) .....	+300°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (DB)	PACKAGE-LEAD	PACKAGE DESIGNATOR <sup>(1)</sup>	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7808U	±0.9	70	SO-20	DW	-40°C to +85°C	ADS7808U	ADS7808U	Tube, 38
"	"	"	"	"	"	"	ADS7808U/1K	Tape and Reel, 1000
ADS7808UB	±0.45	72	"	"	"	ADS7808UB	ADS7808UB	Tube, 38
"	"	"	"	"	"	"	ADS7808UB/1K	Tape and Reel, 1000

NOTE: (1) For the most current specifications and package information, refer to our web site at [www.ti.com](http://www.ti.com).

## ELECTRICAL CHARACTERISTICS

At T<sub>A</sub> = -40°C to +85°C, f<sub>S</sub> = 100kHz, V<sub>DIG</sub> = V<sub>ANA</sub> = +5V, using internal reference and fixed resistors as shown in Figure 4, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7808U			ADS7808UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>RESOLUTION</b>				12			*	Bits
<b>ANALOG INPUT</b> Voltage Ranges Impedance Capacitance				±10V, 0V to 5V, etc. (See Table I) See Table I		*		pF
<b>THROUGHPUT SPEED</b> Conversion Time Complete Cycle Throughput Rate	Acquire and Convert		5.7	8 10		*	*	µs µs kHz
<b>DC ACCURACY</b> Integral Linearity Error Differential Linearity Error No Missing Codes Transition Noise <sup>(2)</sup> Full Scale Error <sup>(3,4)</sup> Full Scale Error Drift Full Scale Error <sup>(3,4)</sup> Full Scale Error Drift Bipolar Zero Error <sup>(3)</sup> Bipolar Zero Error Drift Unipolar Zero Error <sup>(3)</sup>  Unipolar Zero Error Drift Recovery to Rated Accuracy after Power Down Power Supply Sensitivity (V <sub>DIG</sub> = V <sub>ANA</sub> = V <sub>D</sub> )	Ext. 2.5000V Ref Ext. 2.5000V Ref Bipolar Ranges Bipolar Ranges 0V to 10V Range 0V to 4V Range 0V to 5V Range Unipolar Ranges 1µF Capacitor to CAP  +4.75V < V <sub>D</sub> < +5.25V		Specified 0.1	±0.9 ±0.9  ±0.5 ±0.5 ±10 ±5 ±3 ±3  ±2		*	*	LSB <sup>(1)</sup> LSB  LSB % ppm/°C % ppm/°C mV ppm/°C mV mV mV ppm/°C ms  LSB
<b>AC ACCURACY</b> Spurious-Free Dynamic Range Total Harmonic Distortion Signal-to-(Noise+Distortion) Signal-to-Noise Full-Power Bandwidth <sup>(6)</sup>	f <sub>IN</sub> = 45kHz f <sub>IN</sub> = 45kHz f <sub>IN</sub> = 45kHz f <sub>IN</sub> = 45kHz	80 70 70	90 -90 73 73 250	-80	*	*	*	dB <sup>(5)</sup> dB dB dB kHz

# ELECTRICAL CHARACTERISTICS (Cont.)

At  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $f_S = 100\text{kHz}$ ,  $V_{\text{DIG}} = V_{\text{ANA}} = +5\text{V}$ , using internal reference and fixed resistors shown in Figure 4, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7808U			ADS7808UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>SAMPLING DYNAMICS</b> Aperture Delay Aperture Jitter Transient Response Overvoltage Recovery <sup>(7)</sup>	FS Step		40 Sufficient to meet AC specs 150			*	*	ns ns $\mu\text{s}$ ns
<b>REFERENCE</b> Internal Reference Voltage Internal Reference Source Current (Must use external buffer) External Reference Voltage Range for Specified Linearity External Reference Current Drain	No Load  Ext. 2.5000V Ref	2.48  2.3	2.5 1 2.5	2.52  2.7 100	*	*	*	V $\mu\text{A}$ V $\mu\text{A}$
<b>DIGITAL INPUTS</b> Logic Levels $V_{\text{IL}}$ $V_{\text{IH}}^{(8)}$ $I_{\text{IL}}$ $I_{\text{IH}}$	$V_{\text{IL}} = 0\text{V}$ $V_{\text{IH}} = 5\text{V}$	-0.3 +2.0		+0.8 $V_{\text{D}} + 0.3\text{V}$ $\pm 10$ $\pm 10$	*	*	*	V V $\mu\text{A}$ $\mu\text{A}$
<b>DIGITAL OUTPUTS</b> Data Format Data Coding Pipeline Delay Data Clock Internal (Output Only When Transmitting Data) External (Can Run Continually) $V_{\text{OL}}$ $V_{\text{OH}}$ Leakage Current Output Capacitance	EXT/ $\overline{\text{INT}}$ LOW  EXT/ $\overline{\text{INT}}$ HIGH  $I_{\text{SINK}} = 1.6\text{mA}$ $I_{\text{SOURCE}} = 500\mu\text{A}$ High-Z State, $V_{\text{OUT}} = 0\text{V}$ to $V_{\text{DIG}}$ High-Z State			Serial 12 bits Binary Two's Complement or Straight Binary Conversion results only available after completed conversion. Selectable for internal or external data clock 2.3 10 +0.4 $\pm 5$ 15	*	*	*	MHz MHz V V $\mu\text{A}$ pF
<b>POWER SUPPLIES</b> Specified Performance $V_{\text{DIG}}$ $V_{\text{ANA}}$ $I_{\text{DIG}}$ $I_{\text{ANA}}$ Power Dissipation: PWRD LOW PWRD HIGH	Must be $\leq V_{\text{ANA}}$ +4.75  $V_{\text{DIG}} = V_{\text{ANA}} = 5\text{V}$ , $f_S = 100\text{kHz}$	+4.75 +5 0.3 16	+5 +5.25  50	+5.25 *  100	*	*	*	V V mA mA mW $\mu\text{W}$
<b>TEMPERATURE RANGE</b> Specified Performance Derated Performance Storage Thermal Resistance ( $\theta_{\text{JA}}$ ) SO		-40 -55 -65 75		+85 +125 +150	*	*	*	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C/W}$

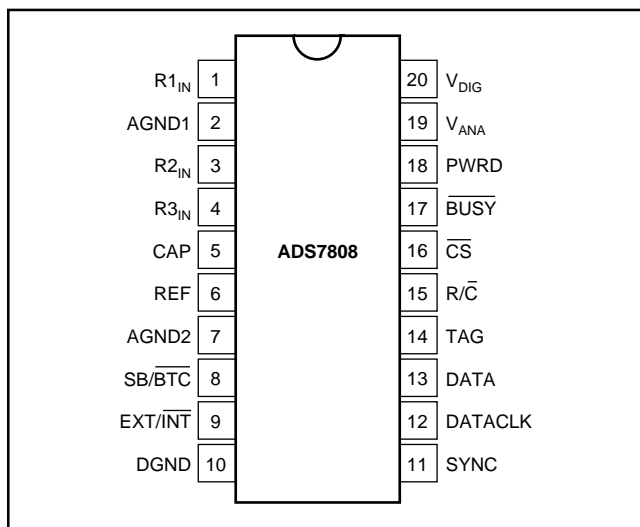
\* Specifications same as ADS7808U.

NOTES: (1) LSB means Least Significant Bit. For the  $\pm 10\text{V}$  input range, one LSB is 4.88mV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors in Figure 4. Adjustable to zero with external potentiometer. (4) For bipolar input ranges, full scale error is the worst case of -Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error. (5) All specifications in dB are referred to a full-scale  $\pm 10\text{V}$  input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage. (8) The minimum  $V_{\text{IH}}$  level for the DATACLK signal is 3V.

## PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	R1 <sub>IN</sub>	Analog Input. See Table I and Figure 4 for input range connections.
2	AGND1	Analog Ground. Used internally as ground reference point. Minimal current flow.
3	R2 <sub>IN</sub>	Analog Input. See Table I and Figure 4 for input range connections.
4	R3 <sub>IN</sub>	Analog Input. See Table I and Figure 4 for input range connections.
5	CAP	Reference Buffer Capacitor. 2.2μF Tantalum to ground.
6	REF	Reference Input/Output. Outputs internal 2.5V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2μF Tantalum capacitor.
7	AGND2	Analog Ground.
8	SB/ $\overline{\text{BTC}}$	Select Straight Binary or Binary Two's Complement data output format. If HIGH, data will be output in a Straight Binary format. If LOW, data will be output in a Binary Two's complement format.
9	EXT/ $\overline{\text{INT}}$	Select External or Internal Clock for transmitting data. If HIGH, data will be output synchronized to the clock input on DATACLK. If LOW, a convert command will initiate the transmission of the data from the previous conversion, along with 12 clock pulses output on DATACLK.
10	DGND	Digital Ground.
11	SYNC	Synch Output. If EXT/ $\overline{\text{INT}}$ is HIGH, either a rising edge on R/ $\overline{\text{C}}$ with $\overline{\text{CS}}$ LOW or a falling edge on $\overline{\text{CS}}$ with R/ $\overline{\text{C}}$ HIGH will output a pulse on SYNC synchronized to the external DATACLK.
12	DATACLK	Either an input or an output depending on the EXT/ $\overline{\text{INT}}$ level. Output data will be synchronized to this clock. If EXT/ $\overline{\text{INT}}$ is LOW, DATACLK will transmit 12 pulses after each conversion, and then remain LOW between conversions.
13	DATA	Serial Data Output. Data will be synchronized to DATACLK, with the format determined by the level of SB/ $\overline{\text{BTC}}$ . In the external clock mode, after 12-bits of data, the ADS7808 will output the level input on TAG as long as $\overline{\text{CS}}$ is LOW and R/ $\overline{\text{C}}$ is HIGH (see Figure 3.) If EXT/ $\overline{\text{INT}}$ is LOW, data will be valid on both the rising and falling edges of DATACLK, and between conversions DATA will stay at the level of the TAG input when the conversion was started.
14	TAG	Tag Input for use in external clock mode. If EXT/ $\overline{\text{INT}}$ is HIGH, digital data input on TAG will be output on DATA with a delay of 12 DATACLK pulses as long as $\overline{\text{CS}}$ is LOW and R/ $\overline{\text{C}}$ is HIGH. See Figure 3.
15	R/ $\overline{\text{C}}$	Read/Convert Input. With $\overline{\text{CS}}$ LOW, a falling edge on R/ $\overline{\text{C}}$ puts the internal sample/hold into the hold state and starts a conversion. When EXT/ $\overline{\text{INT}}$ is LOW, this also initiates the transmission of the data results from the previous conversion. If EXT/ $\overline{\text{INT}}$ is HIGH, a rising edge on R/ $\overline{\text{C}}$ with $\overline{\text{CS}}$ LOW, or a falling edge on $\overline{\text{CS}}$ with R/ $\overline{\text{C}}$ HIGH, transmits a pulse on SYNC and initiates the transmission of data from the previous conversion.
16	$\overline{\text{CS}}$	Chip Select. Internally OR'ed with R/ $\overline{\text{C}}$ .
17	$\overline{\text{BUSY}}$	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output shift register. $\overline{\text{CS}}$ or R/ $\overline{\text{C}}$ must be HIGH when $\overline{\text{BUSY}}$ rises, or another conversion will start without time for signal acquisition.
18	PWRD	Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register.
19	V <sub>ANA</sub>	Analog Supply Input. Nominally +5V. Connect directly to pin 20, and decouple to ground with 0.1μF ceramic and 10μF Tantalum capacitors.
20	V <sub>DIG</sub>	Digital Supply Input. Nominally +5V. Connect directly to pin 19. Must be ≤ V <sub>ANA</sub> .

## PIN CONFIGURATION



ANALOG INPUT RANGE	CONNECT R1 <sub>IN</sub> VIA 200Ω TO	CONNECT R2 <sub>IN</sub> VIA 100Ω TO	CONNECT R3 <sub>IN</sub> TO	IMPEDANCE
±10V	V <sub>IN</sub>	AGND	CAP	22.9kΩ
±5V	AGND	V <sub>IN</sub>	CAP	13.3kΩ
±3.33	V <sub>IN</sub>	V <sub>IN</sub>	CAP	10.7kΩ
0V to 10V	AGND	V <sub>IN</sub>	AGND	13.3kΩ
0V to 5V	AGND	AGND	V <sub>IN</sub>	10.0kΩ
0V to 4V	V <sub>IN</sub>	AGND	V <sub>IN</sub>	10.7kΩ

TABLE I. Input Range Connections. See Figure 4 for complete information.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_1$	Convert Pulse Width	40		4500	ns
$t_2$	$\overline{\text{BUSY}}$ Delay			65	ns
$t_3$	$\overline{\text{BUSY}}$ LOW			8	$\mu\text{s}$
$t_4$	$\overline{\text{BUSY}}$ Delay after End of Conversion		220		ns
$t_5$	Aperture Delay		40		ns
$t_6$	Conversion Time		5.7	8	$\mu\text{s}$
$t_7$	Acquisition Time			2	$\mu\text{s}$
$t_6 + t_7$	Throughput Time		9	10	$\mu\text{s}$
$t_8$	$\overline{\text{R/C}}$ LOW to $\text{DATACLK}$ Delay		450		ns
$t_9$	$\text{DATACLK}$ Period		440		ns
$t_{10}$	Data Valid to $\text{DATACLK}$ HIGH Delay	20	75		ns
$t_{11}$	Data Valid after $\text{DATACLK}$ LOW Delay	100	125		ns
$t_{12}$	External $\text{DATACLK}$ Period	100			ns
$t_{13}$	External $\text{DATACLK}$ HIGH	20			ns
$t_{14}$	External $\text{DATACLK}$ LOW	30			ns
$t_{15}$	$\text{DATACLK}$ HIGH Setup Time	20		$t_{12} + 5$	ns
$t_{16}$	$\overline{\text{R/C}}$ to $\overline{\text{CS}}$ Setup Time	10			ns
$t_{17}$	SYNC Delay After $\text{DATACLK}$ HIGH	15		35	ns
$t_{18}$	Data Valid Delay	25		55	ns
$t_{19}$	$\overline{\text{CS}}$ to Rising Edge Delay	25			ns
$t_{20}$	Data Available after $\overline{\text{CS}}$ LOW	4.5			$\mu\text{s}$

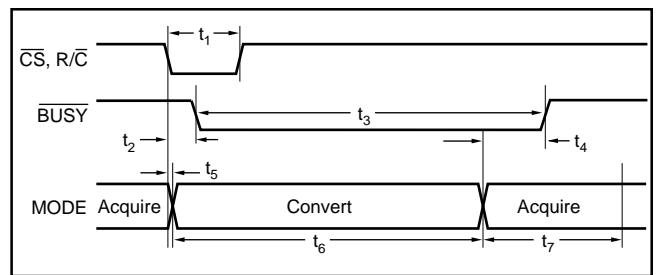


FIGURE 1. Basic Conversion Timing.

TABLE II. Conversion and Data Timing  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

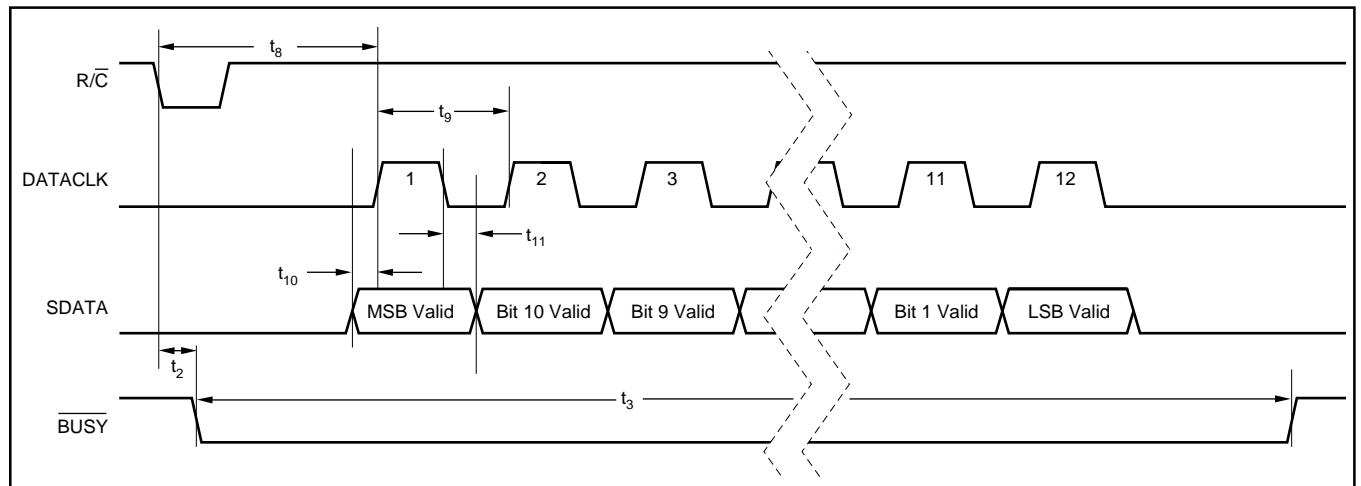


FIGURE 2. Serial Data Timing Using Internal Clock. ( $\overline{\text{CS}}$ ,  $\overline{\text{EXT/INT}}$  and  $\overline{\text{TAG}}$  Tied LOW.)

SPECIFIC FUNCTION	$\overline{CS}$	$R/\overline{C}$	$\overline{BUSY}$	$\overline{EXT}/\overline{INT}$	DATACLK	PWRD	$SB/\overline{BTC}$	OPERATION
Initiate Conversion and Output Data Using Internal Clock	1>0	0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n-1" clocked out on DATA synchronized to 12 clock pulses output on DATACLK.
	0	1>0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n-1" clocked out on DATA synchronized to 12 clock pulses output on DATACLK.
Initiate Conversion and Output Data Using External Clock	1>0	0	1	1	Input	0	x	Initiates conversion "n".
	0	1>0	1	1	Input	0	x	Initiates conversion "n".
	1>0	1	1	1	Input	x	x	Outputs a pulse on SYNC followed by data from conversion "n" clocked out synchronized to external DATACLK.
	1>0	1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion "n-1" clocked out synchronized to external DATACLK. <sup>(1)</sup> Conversion "n" in process.
Incorrect Conversions	0	0	0>1	x	x	0	x	$\overline{CS}$ or $R/\overline{C}$ must be HIGH or a new conversion will be initiated without time for acquisition.
	x	x	x	x	x	0	x	Analog circuitry powered. Conversion can proceed.
Power Down	x	x	x	x	x	1	x	Analog circuitry disabled. Data from previous conversion maintained in output registers.
	x	x	x	x	x	x	0	Serial data is output in Binary Two's Complement format.
Selecting Output Format	x	x	x	x	x	x	1	Serial data is output in Straight Binary format.

NOTE: (1) See Figure 3b for constraints on previous data valid during conversion.

Table III. Control Truth Table.

DESCRIPTION	ANALOG INPUT						DIGITAL OUTPUT			
							BINARY TWO'S COMPLEMENT (SB/BTC LOW)		STRAIGHT BINARY (SB/BTC HIGH)	
							HEX BINARY CODE	CODE	HEX BINARY CODE	CODE
Full-Scale Range	±10	±5	±3.33V	0V to 5V	0V to 10V	0V to 4V				
Least Significant Bit (LSB)	4.88mV	2.44mV	1.63mV	1.22mV	2.44mV	0.98mV				
+Full Scale (FS - 1LSB)	9.99512V	4.99756V	3.33171V	4.99878V	9.99756V	3.99902V	0111 1111 1111	7FF	1111 1111 1111	FFF
Midscale	0V	0V	0V	2.5V	5V	2V	0000 0000 0000	000	1000 0000 0000	800
One LSB Below Midscale	-4.88mV	-2.44mV	-1.63mV	2.49878V	4.99756V	1.99902V	1111 1111 1111	FFF	0111 1111 1111	7FF
-Full Scale	-10V	-5V	-3.33333V	0V	0V	0V	1000 0000 0000	800	0000 0000 0000	000

Table IV. Output Codes and Ideal Input Voltages.

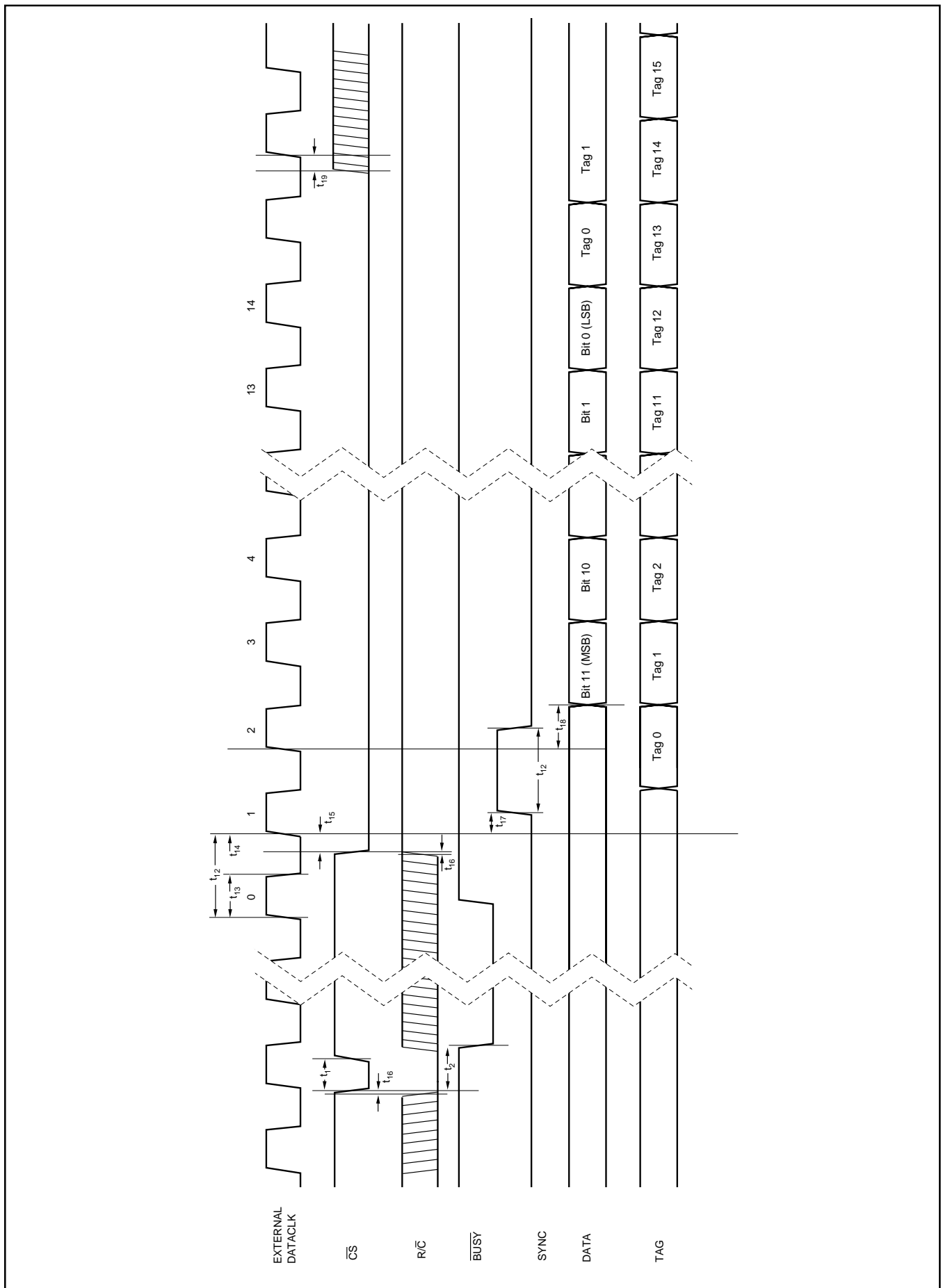


FIGURE 3a. Conversion and Read Timing with External Clock. (EXT/INT Tied HIGH). Read After Conversion.

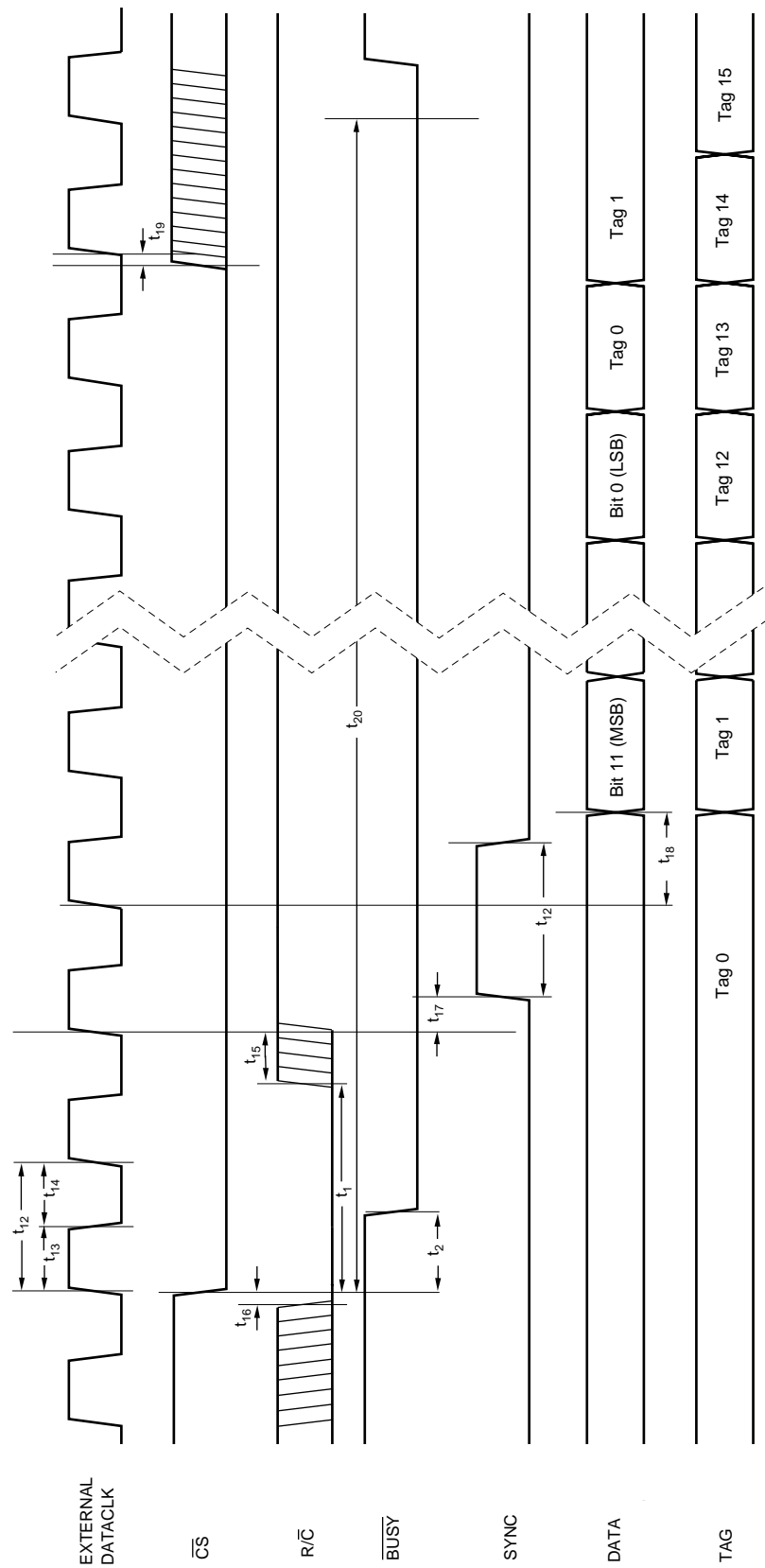


FIGURE 3b. Conversion and Read Timing with External Clock. (EXT/ $\overline{\text{INT}}$  Tied HIGH.) Read During Conversion (Previous Conversion Results).



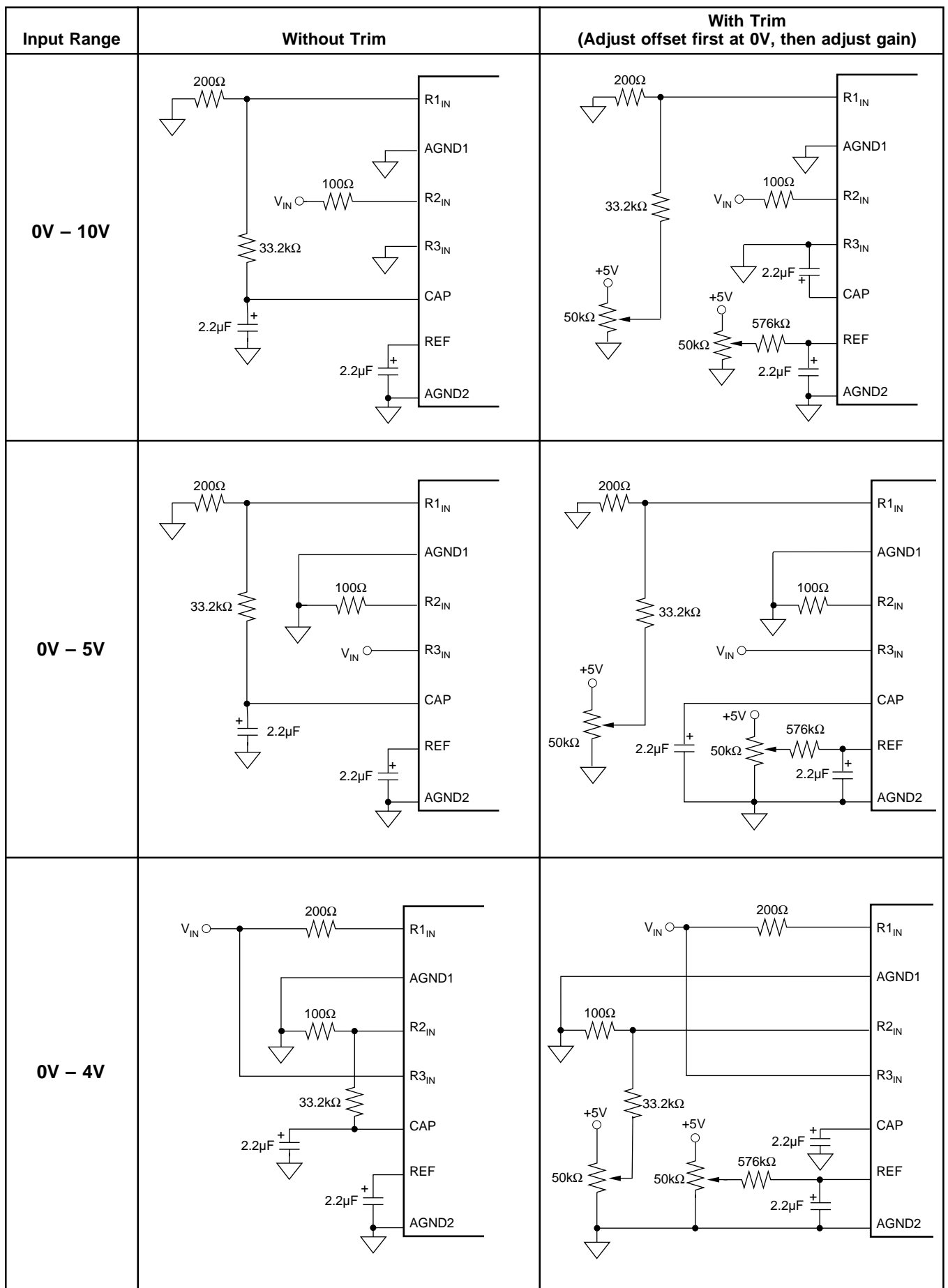


FIGURE 4a. Offset/Gain Circuits for Unipolar Input Ranges.

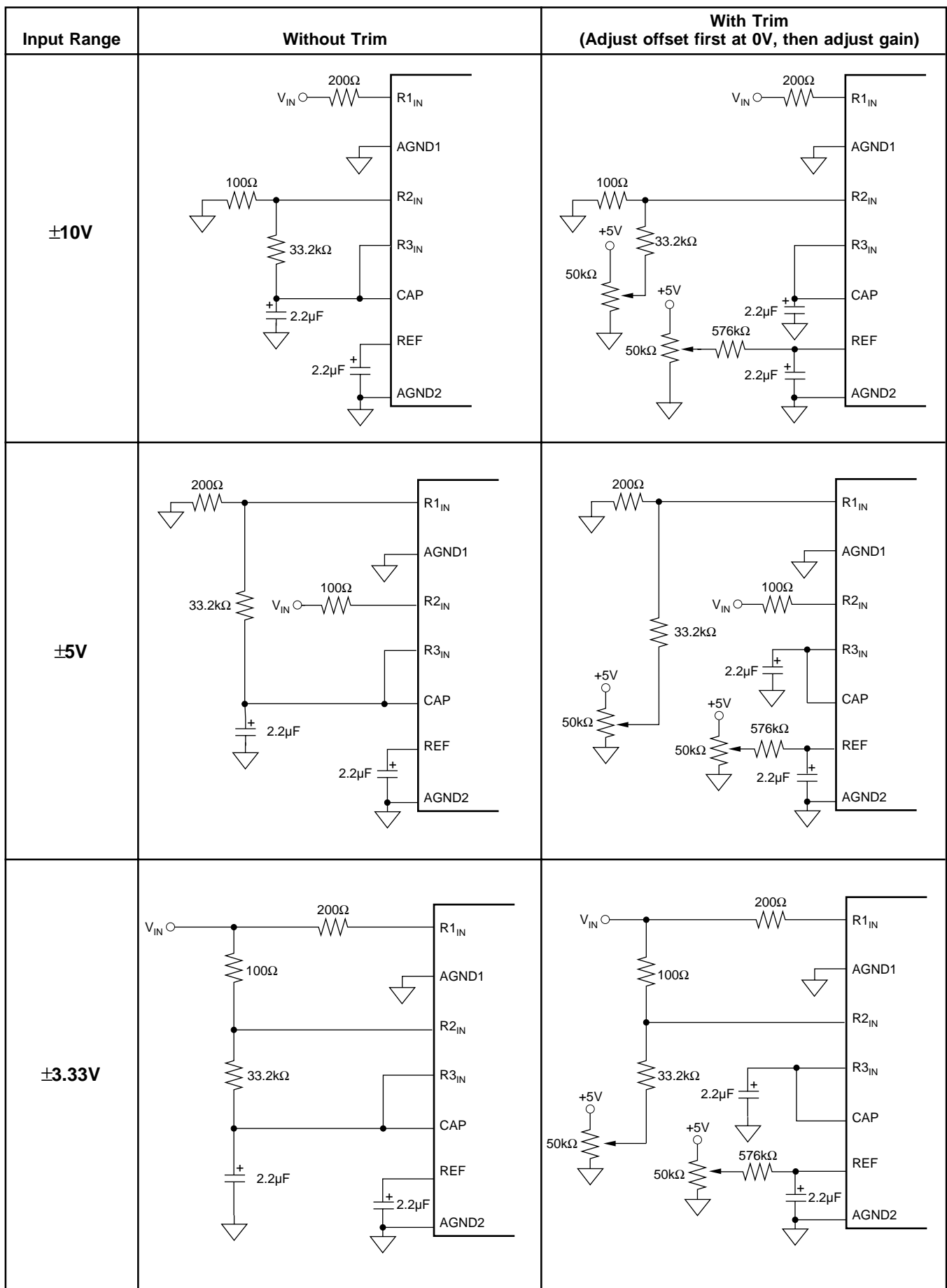


FIGURE 4b. Offset/Gain Circuits for Bipolar Input Ranges.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7808P	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI			
ADS7808PB	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI			
ADS7808U	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7808U	
ADS7808U/1K	NRND	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7808U	
ADS7808U/1KE4	NRND	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7808U	
ADS7808UB	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7808U B	
ADS7808UBG4	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7808U B	
ADS7808UE4	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7808U	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7808U/1K	SOIC	DW	20	1000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7808U/1K	SOIC	DW	20	1000	367.0	367.0	45.0

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7808U	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7808U	<a href="#">Samples</a>
ADS7808U/1K	ACTIVE	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7808U	<a href="#">Samples</a>
ADS7808U/1KE4	NRND	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7808U	
ADS7808UB	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7808U B	<a href="#">Samples</a>
ADS7808UBG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7808U B	<a href="#">Samples</a>
ADS7808UE4	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7808U	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7808U/1K	SOIC	DW	20	1000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1



**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7808U/1K	SOIC	DW	20	1000	367.0	367.0	45.0

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.