TEXAS INSTRUMENTS

bq24120, bq24123, bq24125

SLUS688H – MARCH 2006 – REVISED NOVEMBER 2015

bq2412x Single-Chip Switched-Mode, Li-Ion, and Li-Polymer Charge-Management IC With Enhanced EMI Performance (bqSWITCHER™)

1 Features

- Enhanced EMI Performance
- Integrated Power FETs For Up To 2-A Charge Rate
- Suitable For 1-, 2-, or 3-Cell Li-Ion and Li-Polymer Battery Packs
- Synchronous Fixed-Frequency PWM Controller Operating at 1.1 MHz With 0% to 100% Duty Cycle
- High-Accuracy Voltage and Current Regulation
- Status Outputs For LED or Host Processor Interface Indicates Charge-In-Progress, Charge Completion, Fault, and AC-Adapter Present Conditions
- 20-V Absolute Maximum Voltage Rating on IN and OUT Pins
- Accurate High-Side Battery Current Sensing
- Battery Temperature Monitoring
- Automatic Sleep Mode for Low Power Consumption
- Reverse Leakage Protection Prevents Battery Drainage
- Thermal Shutdown and Protection
- Built-In Battery Detection
- Available in 20-pin 3.5-mm × 4.5-mm VQFN Package

2 Applications

- Handheld Products
- Portable Media Players
- Industrial and Medical Equipment
- Portable Equipment
- Portable DVD Players

3 Description

The bqSWITCHER™ series are highly integrated Li-ion and Li-polymer switched-mode charge management devices targeted at a wide range of portable applications. The bqSWITCHER™ series offers integrated synchronous PWM controller and power FETs, high-accuracy current and voltage regulation, charge preconditioning, charge status, and charge termination, in a small, thermally enhanced QFN package.

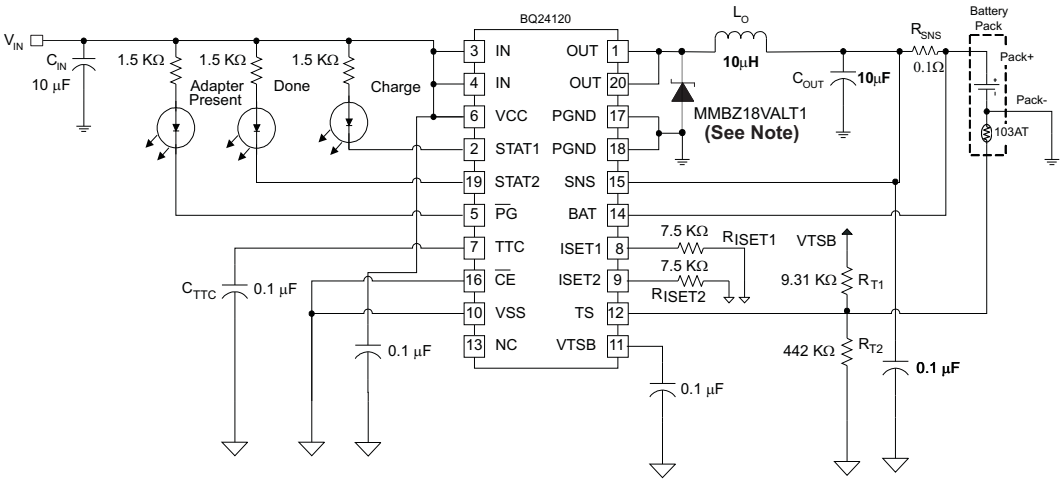
The bqSWITCHER charges the battery in three phases: conditioning, constant current, and constant voltage. Charge is terminated based on user-selectable minimum current level. A programmable charge timer provides a safety backup for charge termination. The bqSWITCHER automatically restarts the charge cycle if the battery voltage falls below an internal threshold. The bqSWITCHER automatically enters sleep mode when V_{CC} supply is removed.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq2412x	VQFN (20)	3.50 mm × 4.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical 1-Cell Application



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4 Revision History

Changes from Revision G (August 2008) to Revision H **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

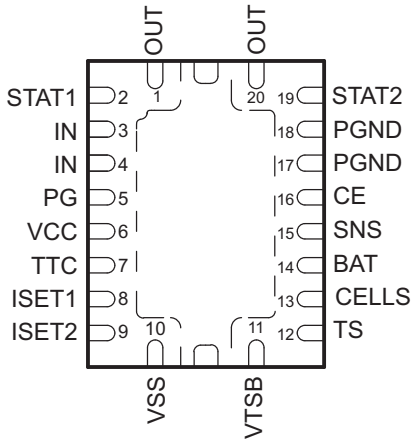
5 Device Options

PART NUMBER (1) (2)	CHARGE REGULATION VOLTAGE (V)	INTENDED APPLICATION
BQ24120RHLR / BQ24120RHLT	4.2 V	Stand-alone
BQ24123RHLR / BQ24123RHLT	4.2 V / 8.4 V	
	2.1 V to 15.5 V	Externally programmable

(1) The RHL package is available in the following options:
R - taped and reeled in quantities of 3,000 devices per reel
T - taped and reeled in quantities of 250 devices per reel
(2) This product is RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and is suitable for use in specified lead-free soldering processes.

6 Pin Configuration and Functions

RHL Package
20-Pin VQFN
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	bq24120	bq24123	bq24125		
BAT	14	14	14	I	Battery voltage sense input. Bypass it with a capacitor to VSS if there are long *inductive* leads to battery.
$\overline{CE}$	16	16	16	I	Charger enable input. This active low input, if set high, suspends charge and places the device in the low-power sleep mode. Do not pull up this input to VTSB.
CELLS		13		I	Available on parts with selectable output voltage. Ground or float for single-cell operation (4.2 V). For two-cell operation (8.4 V) pull up this pin with a resistor to V_{IN}.
FB			13	I	Output voltage analog feedback adjustment. Connect the output of a resistive voltage divider powered from the battery terminals to this node to adjust the output battery voltage regulation.
IN	3, 4	3, 4	3, 4	I	Charger input voltage. Bypass it with a 10µF capacitor from IN to PGND.
ISET1	8	8	8	I/O	Charger current set point 1 (fast charge). Use a resistor to ground to set this value.
ISET2	9	9	9	I/O	Charge current set point 2 (precharge and termination), set by a resistor connected to ground.
N/C	13			–	No connection. This pin must be left floating in the application.
OUT	1	1	1	O	Charge current output inductor connection. Connect a zener TVS diode between OUT pin and PGND to clamp the voltage spike to protect the power MOSFETs during abnormal conditions.
	20	20	20	O	
$\overline{PG}$	5	5	5	O	Power-good status output (open drain). The transistor turns on when a valid V_{CC} is detected. It is turned off in the sleep mode. $\overline{PG}$ can be used to drive a LED or communicate with a host processor.

Pin Functions (continued)

PIN				I/O	DESCRIPTION
NAME	bq24120	bq24123	bq24125		
PGND	17,18	17,18	17,18		Power ground input
SNS	15	15	15	I	Charge current-sense input. Battery current is sensed via the voltage drop developed on this pin by an external sense resistor in series with the battery pack. A 0.1µF capacitor to VSS is required.
STAT1	2	2	2	O	Charge status 1 (open-drain output). When the transistor turns on indicates charge in process. When it is off and with the condition of STAT2 indicates various charger conditions (See Table 1)
STAT2	19	19	19	O	Charge status 2 (open-drain output). When the transistor turns on indicates charge is done. When it is off and with the condition of STAT1 indicates various charger conditions (See Table 1)
TS	12	12	12	I	Temperature sense input. This input monitors its voltage against an internal threshold to determine if charging is allowed. Use an NTC thermistor and a voltage divider powered from VTSB to develop this voltage. (See Figure 9)
TTC	7	7	7	I	Timer and termination control. Connect a capacitor from this node to VSS to set the bqSWITCHER timer. When this input is low, the timer and termination detection are disabled.
VCC	6	6	6	I	Analog device input. A 0.1µF capacitor to VSS is required.
VSS	10	10	10		Analog ground input
VTSB	11	11	11	O	TS internal bias regulator voltage. Connect capacitor (with a value between a 0.1µF and 1µF) between this output and VSS.
Exposed Thermal Pad	Pad	Pad	Pad		There is an internal electrical connection between the exposed thermal pad and VSS. The exposed thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. The power pad can be used as a *star* ground connection between V_{SS} and PGND. A common ground plane may be used. VSS pin must be connected to ground at all times.

7 Specifications

7.1 Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Supply voltage (with respect to V_{SS})	IN, VCC		20	V
	Input voltage (with respect to V_{SS} and PGND)	STAT1, STAT2, $\overline{PG}$, $\overline{CE}$, CELLS, SNS, BAT	–0.3	20	V
		OUT	–0.7	20	V
		TS, TTC		7	V
		VTSB		3.6	V
		ISET1, ISET2		3.3	V
	Voltage difference between SNS and BAT inputs (V_{SNS} - V_{BAT})			±1	V
	Output sink	STAT1, STAT2, $\overline{PG}$		10	mA
	Output current (average)	OUT		2.2	A
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds			300	°C
T_A	Operating free-air temperature		–40	85	°C
T_J	Junction temperature		–40	125	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} and IN (Tie together)	4.35 (1)		16.0 (2)	V
Operating junction temperature range, T_J	–40		125	°C

(1) The IC continues to operate below V_{min}, to 3.5 V, but these conditions are not tested, and are not specified.
(2) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the IN or OUT pins. A *tight* layout minimizes switching noise.

7.4 Thermal Information

THERMAL METRIC (1)		bq2412x RHL (VQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_J = 0°C to 125°C and recommended supply voltage range (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
$I_{VCC(VCC)}$	V_{CC} supply current	$V_{CC} > V_{CC(min)}$, PWM switching		10		mA
		$V_{CC} > V_{CC(min)}$, PWM NOT switching			5	
		$V_{CC} > V_{CC(min)}$, $\overline{CE}$ = HIGH			315	µA
$I_{(SLP)}$	Battery discharge sleep current, (SNS, BAT, OUT pins)	0°C ≤ T_J ≤ 65°C, $V_{I(BAT)}$ = 4.2 V, $V_{CC} < V_{(SLP)}$ or $V_{CC} > V_{(SLP)}$ but not in charge			3.5	µA
		0°C ≤ T_J ≤ 65°C, $V_{I(BAT)}$ = 8.4 V, $V_{CC} < V_{(SLP)}$ or $V_{CC} > V_{(SLP)}$ but not in charge			5.5	
		0°C ≤ T_J ≤ 65°C, $V_{I(BAT)}$ = 12.6 V, $V_{CC} < V_{(SLP)}$ or $V_{CC} > V_{(SLP)}$ but not in charge			7.7	
VOLTAGE REGULATION						
V_{OREG}	Output voltage, bq24123	CELLS = Low, in voltage regulation		4.2		V
		CELLS = High, in voltage regulation		8.4		
	Output voltage, bq24120	Operating in voltage regulation		4.2		
V_{IBAT}	Feedback regulation REF for bq24125 only (W/FB)	I_{IBAT} = 25 nA typical into pin		2.1		
	Voltage regulation accuracy	T_A = 25°C	–0.5%		0.5%	
			–1%		1%	
CURRENT REGULATION - FAST CHARGE						
$I_{OCHARGE}$	Output current range of converter	$V_{LOWV} \le V_{I(BAT)} < V_{OREG}$, $V_{(VCC)} - V_{I(BAT)} > V_{(DO-MAX)}$	150		2000	mA
V_{IREG}	Voltage regulated across $R_{(SNS)}$ Accuracy	100 mV ≤ V_{IREG} ≤ 200 mV, (1) $V_{IREG} = \frac{1V}{RSET1} \times 1000$, Programmed Where 5 kΩ ≤ RSET1 ≤ 10 kΩ, Select RSET1 to program V_{IREG}, $V_{IREG(measured)} = I_{OCHARGE} \times R_{SNS}$ (–10% to 10% excludes errors due to RSET1 and $R_{(SNS)}$ tolerances)	–10%		10%	

(1) Inductor peak current should be less than 2.6 A. Use equations 12, 13, 15, 18, and 19 to make sure the peak inductor current is less than 2.6 A.

Electrical Characteristics (continued)

T_J = 0°C to 125°C and recommended supply voltage range (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(ISET1)}$	Output current set voltage	$V_{(LOWV)} \le V_{I(BAT)} \le V_{O(REG)}$, $V_{(VCC)} \ge V_{I(BAT)} + V_{(DO-MAX)}$		1		V
$K_{(ISET1)}$	Output current set factor	$V_{LOWV} \le V_{I(BAT)} < V_{O(REG)}$, $V_{(VCC)} \ge V_{I(BAT)} + V_{(DO-MAX)}$		1000		V/A
PRECHARGE AND SHORT-CIRCUIT CURRENT REGULATION						
V_{LOWV}	Precharge to fast-charge transition voltage threshold, BAT		68	71.4	75	$\%V_{O(REG)}$
t	Deglitch time for precharge to fast charge transition	Rising voltage; t_{RISE}, t_{FALL} = 100 ns, 2-mV overdrive	20	30	40	ms
$I_{OPRECHG}$	Precharge range	$V_{I(BAT)} < V_{LOWV}$, $t < t_{PRECHG}$	15		200	mA
$V_{(ISET2)}$	Precharge set voltage, ISET2	$V_{I(BAT)} < V_{LOWV}$, $t < t_{PRECHG}$		100		mV
$K_{(ISET2)}$	Precharge current set factor			1000		V/A
$V_{IREG-PRE}$	Voltage regulated across R_{SNS}-Accuracy	10 mV ≤ $V_{IREG-PRE}$ ≤ 100 mV, (1) $V_{IREG-PRE} = \frac{0.1V}{RSET2} \times 1000$, Where 1.0 kΩ ≤ RSET2 ≤ 10 kΩ, Select RSET2 to program $V_{IREG-PRE}$, $V_{IREG-PRE}$ (Measured) = $I_{OPRE-CHG} \times R_{SNS}$ (–20% to 20% excludes errors due to RSET2 and R_{SNS} tolerances)	–20%		20%	

Electrical Characteristics (continued)

T_J = 0°C to 125°C and recommended supply voltage range (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHARGE TERMINATION (CURRENT TAPER) DETECTION						
I_{TERM}	Charge current termination detection range	$V_{I(BAT)} > V_{OREG}$- V_{RCH}	15		200	mA
V_{TERM}	Charge termination detection set voltage, ISET2	$V_{I(BAT)} > V_{OREG}$- V_{RCH}		100		mV
$K_{(ISET2)}$	Termination current set factor			1000		V/A
	Charger termination accuracy	$V_{I(BAT)} > V_{OREG}$- V_{RCH}	–20%		20%	
$t_{dg-TERM}$	Deglitch time for charge termination	Both rising and falling, 2-mV overdrive t_{RISE}, t_{FALL} = 100 ns	20	30	40	ms
TEMPERATURE COMPARATOR AND VTSB BIAS REGULATOR						
$\%_{LTF}$	Cold temperature threshold, TS, % of bias	$V_{LTF} = V_{O(VTSB)} \times$ % LTF/100	72.8%	73.5%	74.2%	
$\%_{HTF}$	Hot temperature threshold, TS, % of bias	$V_{HTF} = V_{O(VTSB)} \times$ % HTF/100	33.7%	34.4%	35.1%	
$\%_{TCO}$	Cutoff temperature threshold, TS, % of bias	$V_{TCO} = V_{O(VTSB)} \times$ % TCO/100	28.7%	29.3%	29.9%	
	LTF hysteresis		0.5%	1.0%	1.5%	
t_{dg-TS}	Deglitch time for temperature fault, TS	Both rising and falling, 2-mV overdrive t_{RISE}, t_{FALL} = 100 ns	20	30	40	ms
$V_{O(VTSB)}$	TS bias output voltage	$V_{CC} > V_{IN(min)}$, $I_{(VTSB)}$ = 10 mA 0.1 µF ≤ $C_{O(VTSB)}$ ≤ 1 µF		3.15		V
$V_{O(VTSB)}$	TS bias voltage regulation accuracy	$V_{CC} >$ $_{IN(min)}$, $I_{(VTSB)}$ = 10 mA 0.1 µF ≤ $C_{O(VTSB)}$ ≤ 1 µF	–10%		10%	
BATTERY RECHARGE THRESHOLD						
V_{RCH}	Recharge threshold voltage	Below V_{OREG}	75	100	125	mV/cell
t_{dg-RCH}	Deglitch time	$V_{I(BAT)}$ < decreasing below threshold, t_{FALL} = 100 ns 10-mV overdrive	20	30	40	ms
STAT1, STAT2, AND $\overline{PG}$ OUTPUTS						
$V_{OL(STATx)}$	Low-level output saturation voltage, STATx	I_O = 5 mA			0.5	V
$V_{OL(\overline{PG})}$	Low-level output saturation voltage, $\overline{PG}$	I_O = 10 mA			0.1	
$\overline{CE}$, CELLS INPUTS						
V_{IL}	Low-level input voltage	I_{IL} = 5 µA	0		0.4	V
V_{IH}	High-level input voltage	I_{IH} = 20 µA	1.3		V_{CC}	
TTC INPUT						
t_{PRECHG}	Precharge timer		1440	1800	2160	s
t_{CHARGE}	Programmable charge timer range	$t_{(CHG)} = C_{(TTC)} \times K_{(TTC)}$	25		572	minutes
	Charge timer accuracy	0.01 µF ≤ $C_{(TTC)}$ ≤ 0.18 µF	-10%		10%	
K_{TTC}	Timer multiplier			2.6		min/nF
C_{TTC}	Charge time capacitor range		0.01		0.22	µF
V_{TTC_EN}	TTC enable threshold voltage	$V_{(TTC)}$ rising		200		mV
SLEEP COMPARATOR						
$V_{SLP-ENT}$	Sleep-mode entry threshold	2.3 V ≤ $V_{I(OUT)}$ ≤ V_{OREG}, for 1 or 2 cells	V_{CC} ≤ V_{IBAT} +5 mV		V_{CC} ≤ V_{IBAT} +75 mV	V
		$V_{I(OUT)}$ = 12.6 V, R_{IN} = 1kΩ, bq24125 (2)	V_{CC} ≤ V_{IBAT} –4 mV		V_{CC} ≤ V_{IBAT} +73 mV	
$V_{SLP-EXIT}$	Sleep-mode exit hysteresis,	2.3 V ≤ $V_{I(OUT)}$≤ V_{OREG}	40		160	mV
t_{dg-SLP}	Deglitch time for sleep mode	V_{CC} decreasing below threshold, t_{FALL} = 100 ns, 10-mV overdrive, PMOS turns off		5		µs
		V_{CC} decreasing below threshold, t_{FALL} = 100 ns, 10-mV overdrive, STATx pins turn off	20	30	40	ms
UVLO						
$V_{UVLO-ON}$	IC active threshold voltage	V_{CC} rising	3.15	3.30	3.50	V
	IC active hysteresis	V_{CC} falling	120	150		mV

(2) For bq24125 only. R_{IN} is connected between IN and PGND pins and needed to ensure sleep entry.

Electrical Characteristics (continued)

T_J = 0°C to 125°C and recommended supply voltage range (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM						
	Internal P-channel MOSFET on-resistance	$7\ V \le V_{CC} \le V_{CC(max)}$			400	mΩ
		$4.5\ V \le V_{CC} \le 7\ V$			500	
	Internal N-channel MOSFET on-resistance	$7\ V \le V_{CC} \le V_{CC(max)}$			130	
		$4.5\ V \le V_{CC} \le 7\ V$			150	
f_{OSC}	Oscillator frequency			1.1		MHz
	Frequency accuracy		–9%		9%	
D_{MAX}	Maximum duty cycle				100%	
D_{MIN}	Minimum duty cycle		0%			
t_{TOD}	Switching delay time (dead time)			20		ns
$t_{syncmin}$	Minimum synchronous FET on time			60		ns
	Synchronous FET minimum current-off threshold (3)		50		400	mA
BATTERY DETECTION						
I_{DETECT}	Battery detection current during time-out fault	$V_{I(BAT)} < V_{OREG} - V_{RCH}$		2		mA
$I_{DISCHRG1}$	Discharge current	$V_{SHORT} < V_{I(BAT)} < V_{OREG} - V_{RCH}$		400		µA
$t_{DISCHRG1}$	Discharge time	$V_{SHORT} < V_{I(BAT)} < V_{OREG} - V_{RCH}$		1		s
I_{WAKE}	Wake current	$V_{SHORT} < V_{I(BAT)} < V_{OREG} - V_{RCH}$		2		mA
t_{WAKE}	Wake time	$V_{SHORT} < V_{I(BAT)} < V_{OREG} - V_{RCH}$		0.5		s
$I_{DISCHRG2}$	Termination discharge current	Begins after termination detected, $V_{I(BAT)} \le V_{OREG}$		400		µA
$t_{DISCHRG2}$	Termination time			262		ms
OUTPUT CAPACITOR						
C_{OUT}	Required output ceramic capacitor range from SNS to PGND, between inductor and R_{SNS}		4.7	10	47	µF
C_{SNS}	Required SNS capacitor (ceramic) at SNS pin			0.1		µF
PROTECTION						
V_{OVP}	OVP threshold voltage	Threshold over V_{OREG} to turn off P-channel MOSFET, STAT1, and STAT2 during charge or termination states	110	117	121	$\%V_{O(REG)}$
I_{LIMIT}	Cycle-by-cycle current limit		2.6	3.6	4.5	A
V_{SHORT}	Short-circuit voltage threshold, BAT	$V_{I(BAT)}$ falling	1.95	2	2.05	V/cell
I_{SHORT}	Short-circuit current	$V_{I(BAT)} \le V_{SHORT}$	35		65	mA
T_{SHTDWN}	Thermal trip			165		°C
	Thermal hysteresis			10		

(3) N-channel always turns on for approximately 60 ns and then turns off if current is too low.

7.6 Dissipation Ratings

PACKAGE	Θ_{JA}	Θ_{JC}	T_A < 40°C POWER RATING	DERATING FACTOR ABOVE T_A = 40°C
RHL (1)	46.87°C/W	2.15°C/W	1.81 W	0.021 W/°C

(1) This data is based on using the JEDEC High-K board, and the exposed die pad is connected to a copper pad on the board. This is connected to the ground plane by a 2x3 via matrix.

7.7 Typical Characteristics

See Figure 17 for a 1-cell application test circuit schematic and Figure 21 for the standalone cells application test circuits schematic.

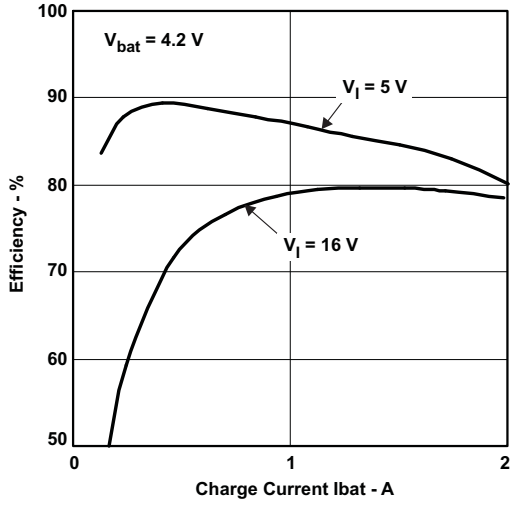


Figure 1. Efficiency 1-Cell

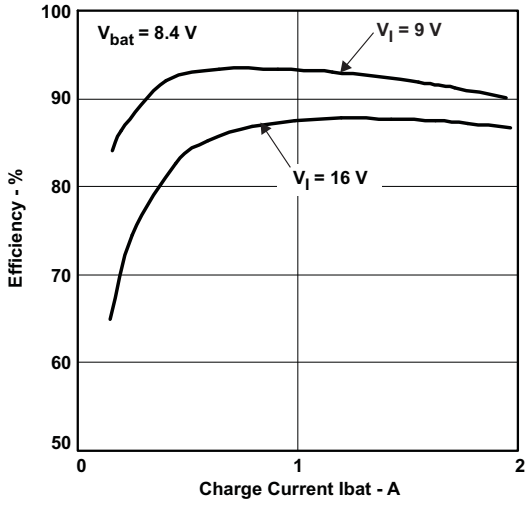


Figure 2. Efficiency 2-Cells

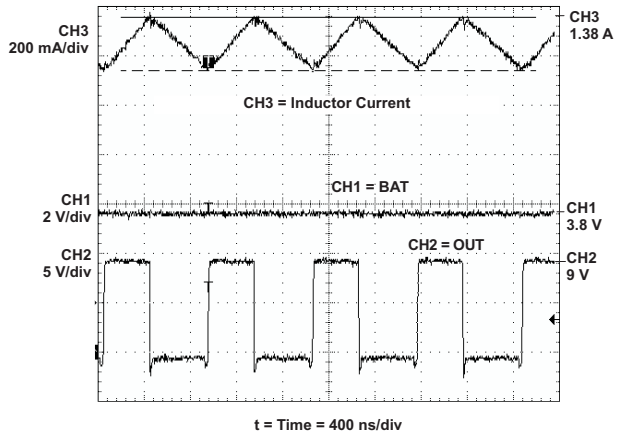


Figure 3. Switching Waveforms in Fast Charge Mode

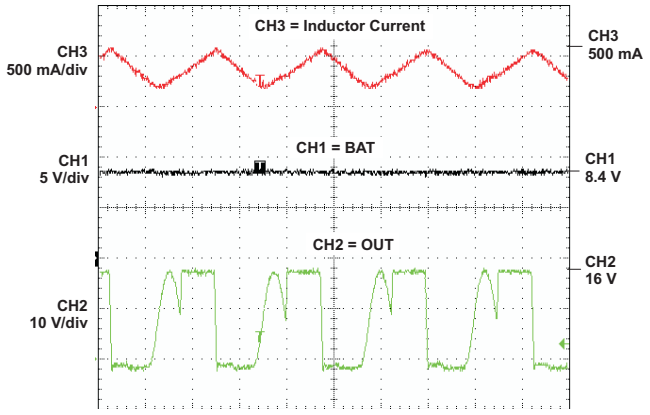


Figure 4. Switching Waveforms in Voltage Regulation Mode

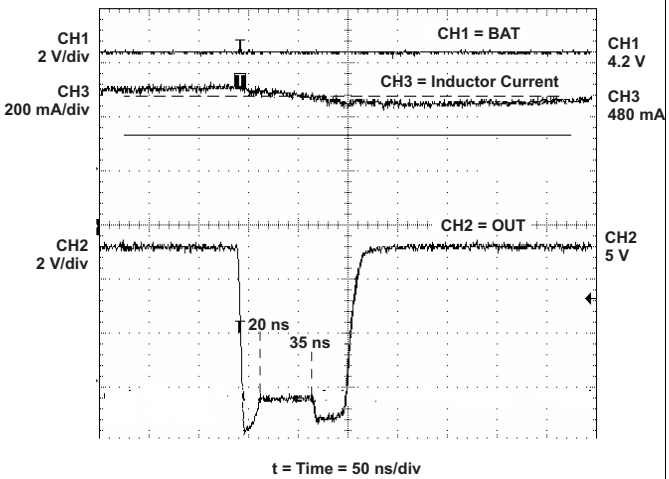


Figure 5. Dead Time

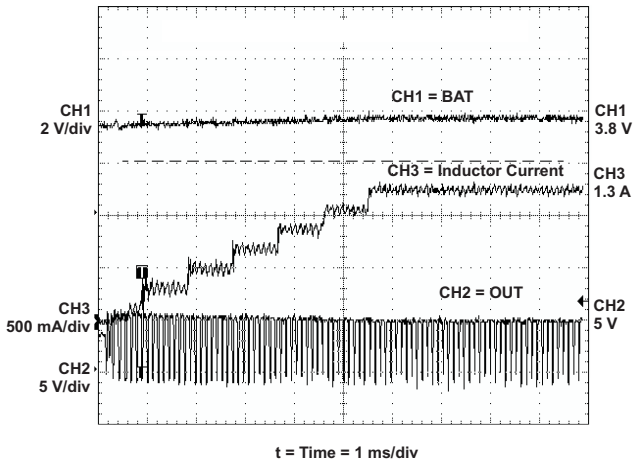


Figure 6. Soft Start Waveforms

Typical Characteristics (continued)

See Figure 17 for a 1-cell application test circuit schematic and Figure 21 for the standalone cells application test circuits schematic.

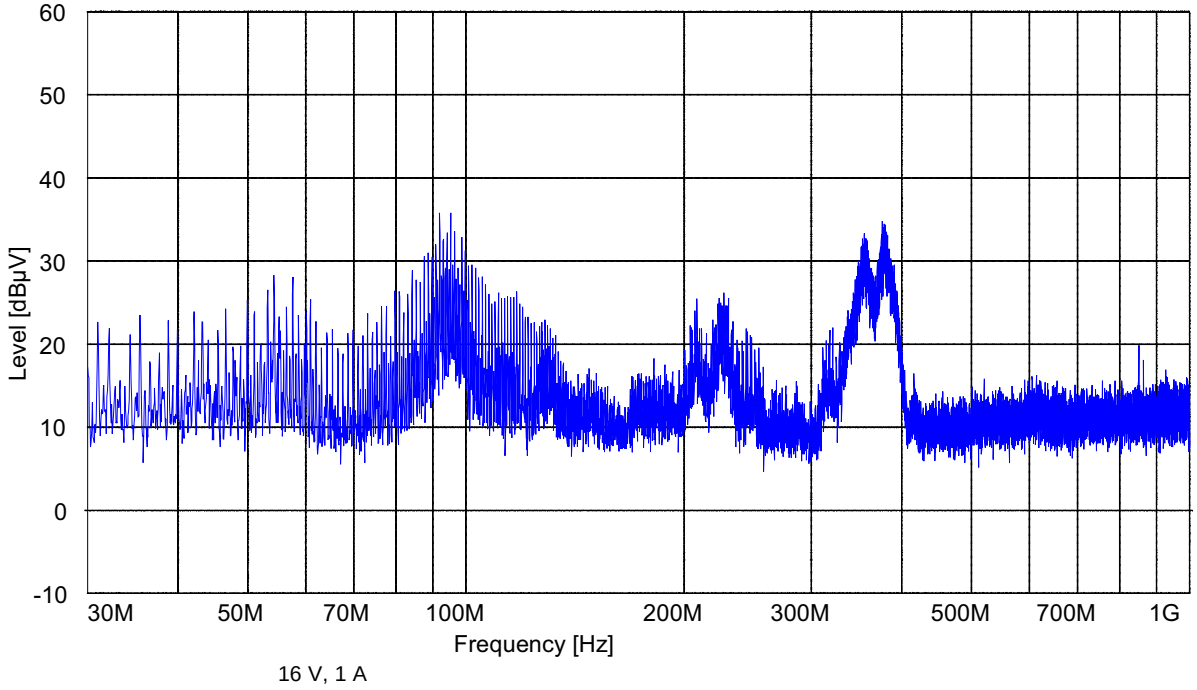


Figure 7. Typical Radiated EMI Performance Measured on EVM

8 Detailed Description

8.1 Overview

The bqSWITCHER supports a precision Li-ion or Li-polymer charging system for single cell or two cell applications. See Figure 16 and Figure 8 for a typical charge profile.

The bq2412X has enhanced EMI performance that helps minimize the number of components needed to meet the FCC-B Standard. The rise time of the OUT pin was slowed down to minimize the radiated EMI.

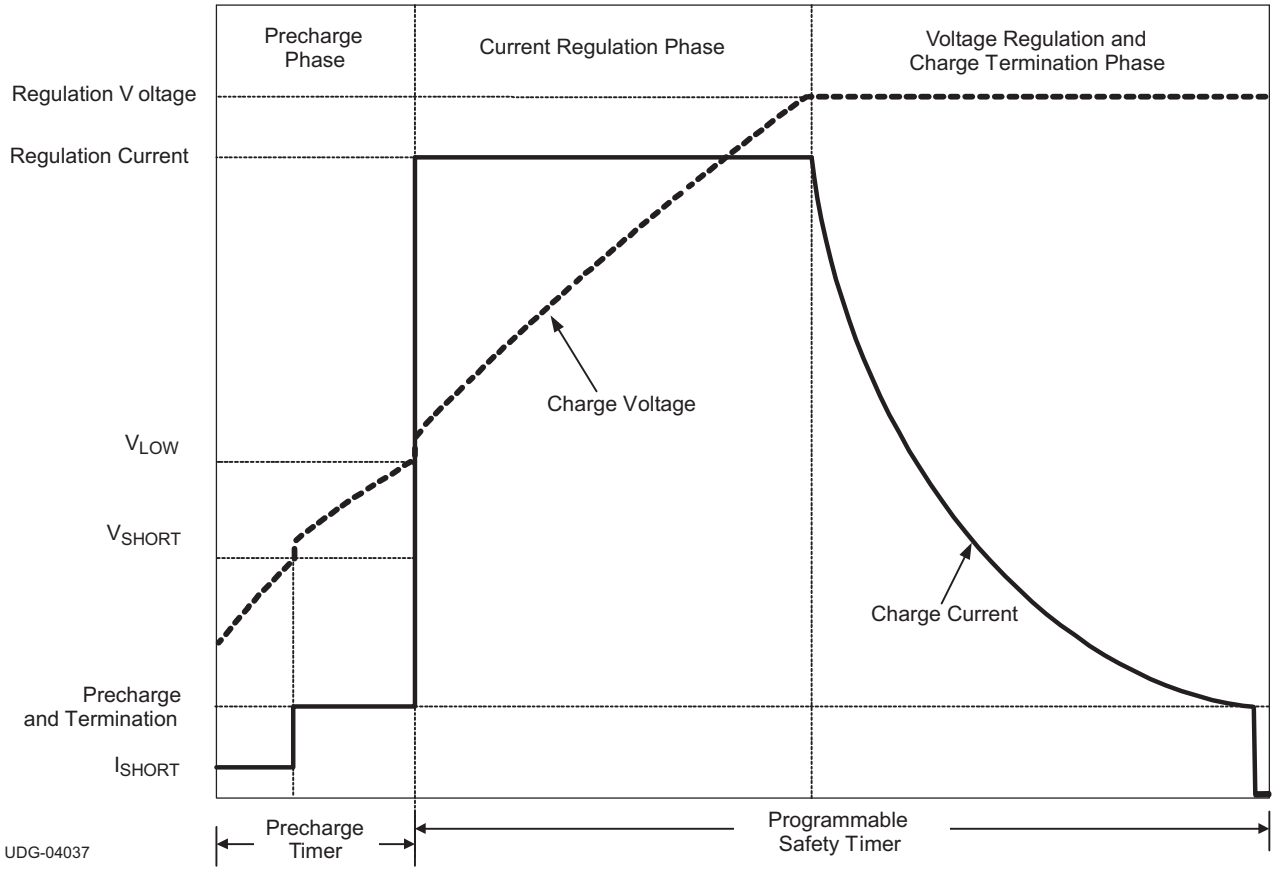
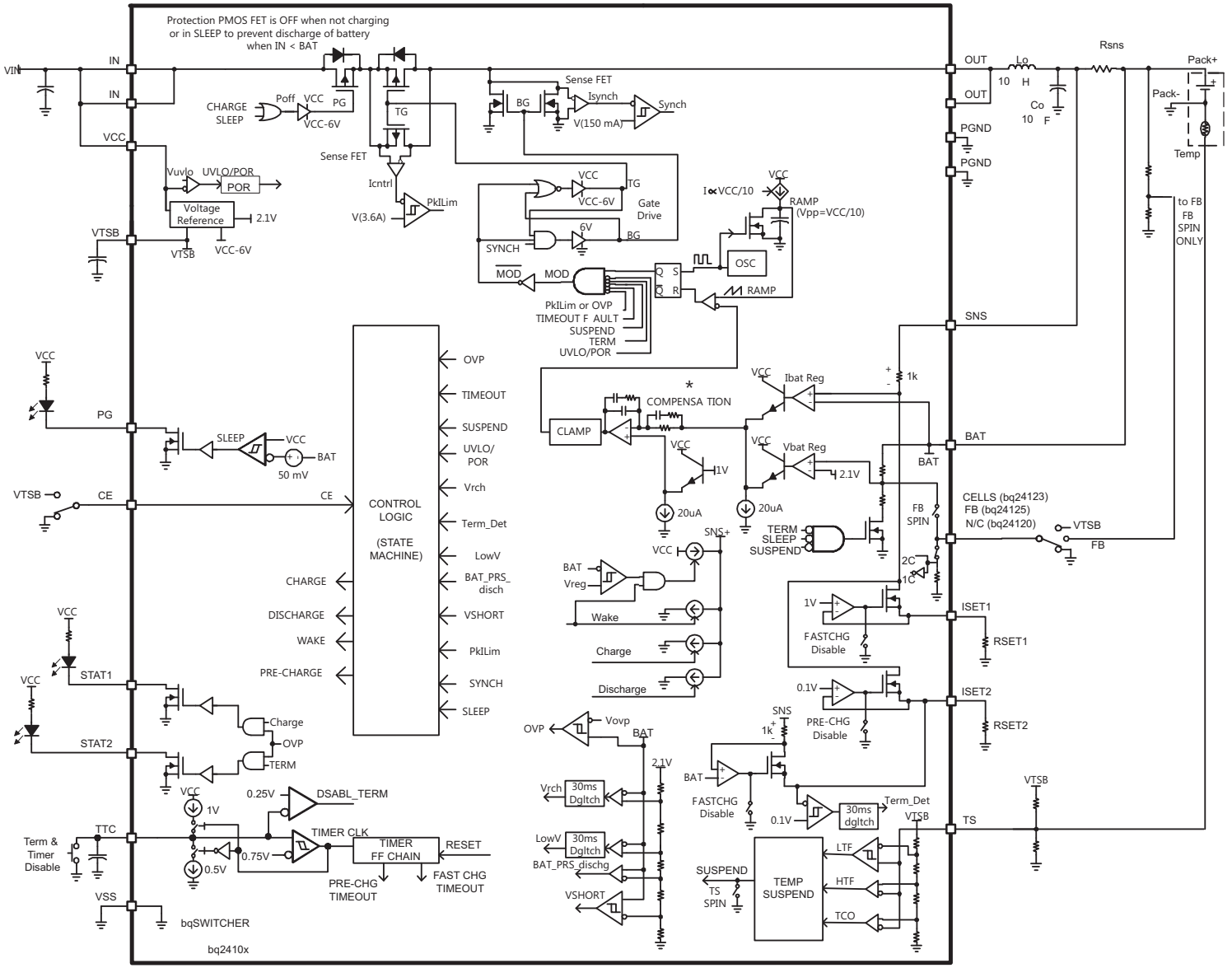


Figure 8. Typical Charging Profile

8.2 Functional Block Diagram



*Patent Pending #36889

8.3 Feature Description

8.3.1 PWM Controller

The bq2412X provides an integrated fixed 1MHz frequency voltage-mode controller with Feed-Forward function to regulate charge current or voltage. This type of controller is used to help improve line transient response, thereby simplifying the compensation network used for both continuous and discontinuous current conduction operation. The voltage and current loops are internally compensated using a Type-III compensation scheme that provides enough phase boost for stable operation, allowing the use of small ceramic capacitors with very low ESR. There is a 0.5V offset on the bottom of the PWM ramp to allow the device to operate between 0% to 100% duty cycle.

The internal PWM gate drive can directly control the internal PMOS and NMOS power MOSFETs. The high-side gate voltage swings from V_{CC} (when off), to V_{CC}-6 (when on and V_{CC} is greater than 6V) to help reduce the conduction losses of the converter by enhancing the gate an extra volt beyond the standard 5V. The low-side gate voltage swings from 6V, to turn on the NMOS, down to PGND to turn it off. The bq2412X has two back to back common-drain P-MOSFETs on the high side. An input P-MOSFET prevents battery discharge when IN is lower than BAT. The second P-MOSFET behaves as the switching control FET, eliminating the need of a bootstrap capacitor.

Cycle-by-cycle current limit is sensed through the internal high-side sense FET. The threshold is set to a nominal 3.6A peak current. The low-side FET also has a current limit that decides if the PWM Controller will operate in synchronous or non-synchronous mode. This threshold is set to 100mA and it turns off the low-side NMOS before the current reverses, preventing the battery from discharging. Synchronous operation is used when the current of the low-side FET is greater than 100mA to minimize power losses.

8.3.2 Temperature Qualification

The bqSWITCHER continuously monitors battery temperature by measuring the voltage between the TS pin and VSS pin. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develop this voltage. The bqSWITCHER compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the $V_{(LTF)}$-to-$V_{(HTF)}$ thresholds. If battery temperature is outside of this range, the bqSWITCHER suspends charge and waits until the battery temperature is within the $V_{(LTF)}$-to-$V_{(HTF)}$ range. During the charge cycle (both precharge and fast charge), the battery temperature must be within the $V_{(LTF)}$-to-$V_{(TCO)}$ thresholds. If battery temperature is outside of this range, the bqSWITCHER suspends charge and waits until the battery temperature is within the $V_{(LTF)}$-to-$V_{(HTF)}$ range. The bqSWITCHER suspends charge by turning off the PWM and holding the timer value (that is, timers are not reset during a suspend condition). Note that the bias for the external resistor divider is provided from the VTSB output. Applying a constant voltage between the $V_{(LTF)}$-to-$V_{(HTF)}$ thresholds to the TS pin disables the temperature-sensing feature.

$$RT2 = \frac{V_{O(VTSB)} \times RTH_{COLD} \times RTH_{HOT} \times \left[\frac{1}{V_{LTF}} - \frac{1}{V_{HTF}}\right]}{RTH_{HOT} \times \left(\frac{V_{O(VTSB)}}{V_{HTF}} - 1\right) - RTH_{COLD} \times \left(\frac{V_{O(VTSB)}}{V_{LTF}} - 1\right)}$$

$$RT1 = \frac{\frac{V_{O(VTSB)}}{V_{LTF}} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}}$$

Where:

$V_{LTF} = V_{O(VTSB)} \times \%_{LTF÷100} / 100$

$V_{HTF} = V_{O(VTSB)} \times \%_{HTF÷100} / 100$ (1)

Feature Description (continued)

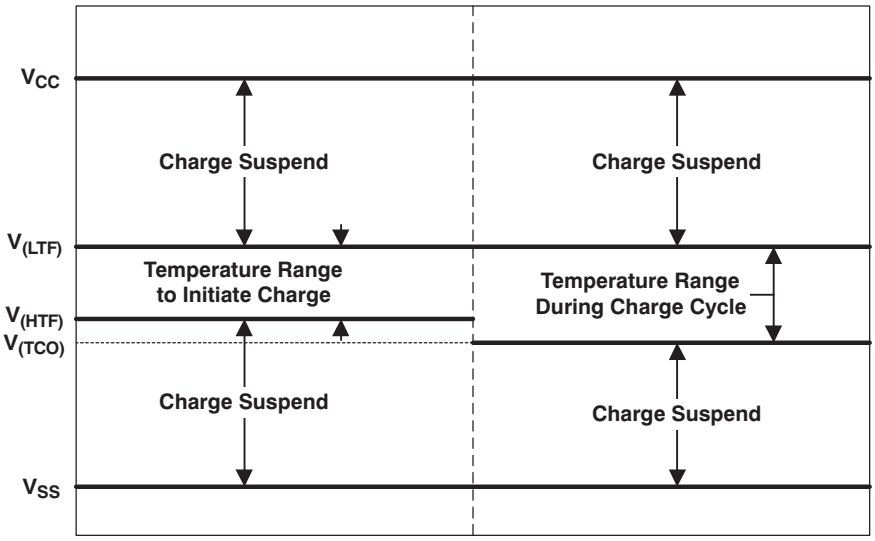


Figure 9. TS Pin Thresholds

8.3.3 Battery Preconditioning (Precharge)

On power up, if the battery voltage is below the V_{LOWV} threshold, the bqSWITCHER applies a precharge current, I_{PRECHG}, to the battery. This feature revives deeply discharged cells. The bqSWITCHER activates a safety timer, t_{PRECHG}, during the conditioning phase. If the V_{LOWV} threshold is not reached within the timer period, the bqSWITCHER turns off the charger and enunciates FAULT on the STATx pins. In the case of a FAULT condition, the bqSWITCHER reduces the current to I_{DETECT}. I_{DETECT} is used to detect a battery replacement condition. Fault condition is cleared by POR or battery replacement.

The magnitude of the precharge current, $I_{O(PRECHG)}$, is determined by the value of programming resistor, $R_{(ISET2)}$, connected to the ISET2 pin.

$$I_{O(PRECHG)} = \frac{K_{(ISET2)} \times V_{(ISET2)}}{\left(R_{(ISET2)} \times R_{(SNS)}\right)}$$

where

- R_{SNS} is the external current-sense resistor
- $V_{(ISET2)}$ is the output voltage of the ISET2 pin
- $K_{(ISET2)}$ is the V/A gain factor
- $V_{(ISET2)}$ and $K_{(ISET2)}$ are specified in the Electrical Characteristics table. (2)

8.3.4 Battery Charge Current

The battery charge current, $I_{O(CHARGE)}$, is established by setting the external sense resistor, $R_{(SNS)}$, and the resistor, $R_{(ISET1)}$, connected to the ISET1 pin.

In order to set the current, first choose $R_{(SNS)}$ based on the regulation threshold V_{IREG} across this resistor. The best accuracy is achieved whe the V_{IREG} is between 100mV and 200mV.

$$R_{(SNS)} = \frac{V_{IREG}}{I_{OCHARGE}} \quad (3)$$

If the results is not a standard sense resistor value, choose the next larger value. Using the selected standard value, solve for V_{IREG}. Once the sense resistor is selected, the ISET1 resistor can be calculated using the following equation:

$$R_{ISET1} = \frac{K_{ISET1} \times V_{ISET1}}{R_{SNS} \times I_{CHARGE}} \quad (4)$$

Feature Description (continued)

8.3.5 Battery Voltage Regulation

The voltage regulation feedback occurs through the BAT pin. This input is tied directly to the positive side of the battery pack. The bqSWITCHER monitors the battery-pack voltage between the BAT and VSS pins. The bqSWITCHER is offered in a fixed single-cell voltage version (4.2 V) and as a one-cell or two-cell version selected by the CELLS input. A low or floating input on the CELLS selects single-cell mode (4.2 V) while a high-input through a resistor selects two-cell mode (8.4 V).

8.3.6 Charge Termination And Recharge

The bqSWITCHER monitors the charging current during the voltage regulation phase. Once the termination threshold, I_{TERM}, is detected, the bqSWITCHER terminates charge. The termination current level is selected by the value of programming resistor, $R_{(ISET2)}$, connected to the ISET2 pin.

$$I_{TERM} = \frac{K_{(ISET2)} \times V_{TERM}}{\left(R_{(ISET2)} \times R_{(SNS)}\right)}$$

where

- $R_{(SNS)}$ is the external current-sense resistor
- V_{TERM} is the output of the ISET2 pin
- $K_{(ISET2)}$ is the A/V gain factor
- V_{TERM} and $K_{(ISET2)}$ are specified in the Electrical Characteristics table (5)

As a safety backup, the bqSWITCHER also provides a programmable charge timer. The charge time is programmed by the value of a capacitor connected between the TTC pin and GND by the following formula:

$$t_{CHARGE} = C_{(TTC)} \times K_{(TTC)}$$

where

- $C_{(TTC)}$ is the capacitor connected to the TTC pin
- $K_{(TTC)}$ is the multiplier (6)

A new charge cycle is initiated when one of the following conditions is detected:

- The battery voltage falls below the V_{RCH} threshold.
- Power-on reset (POR), if battery voltage is below the V_{RCH} threshold
- $\overline{CE}$ toggle
- TTC pin, described as follows.

In order to disable the charge termination and safety timer, the user can pull the TTC input below the V_{TTC_EN} threshold. Going above this threshold enables the termination and safety timer features and also resets the timer. Tying TTC high disables the safety timer only.

8.3.7 Sleep Mode

The bqSWITCHER enters the low-power sleep mode if the VCC pin is removed from the circuit. This feature prevents draining the battery during the absence of VCC.

8.3.8 Charge Status Outputs

The open-drain STAT1 and STAT2 outputs indicate various charger operations as shown in Table 1. These status pins can be used to drive LEDs or communicate to the host processor. Note that OFF indicates that the open-drain transistor is turned off.

Table 1. Status Pins Summary

CHARGE STATE	STAT1	STAT2
Charge-in-progress	ON	OFF
Charge complete	OFF	ON
Charge suspend, timer fault, overvoltage, sleep mode, battery absent	OFF	OFF

8.3.9 $\overline{\text{PG}}$ Output

The open-drain $\overline{\text{PG}}$ (power good) indicates when the AC-to-DC adapter (that is, V_{CC}) is present. The output turns on when sleep-mode exit threshold, $V_{SLP-EXIT}$, is detected. This output is turned off in the sleep mode. The $\overline{\text{PG}}$ pin can be used to drive an LED or communicate to the host processor.

8.3.10 $\overline{\text{CE}}$ Input (Charge Enable)

The $\overline{\text{CE}}$ digital input is used to disable or enable the charge process. A low-level signal on this pin enables the charge and a high-level V_{CC} signal disables the charge. A high-to-low transition on this pin also resets all timers and fault conditions. Note that the $\overline{\text{CE}}$ pin should not be tied to VTSB. This may create power-up issues.

8.3.11 Timer Fault Recovery

As shown in Figure 16, bqSWITCHER provides a recovery method to deal with timer fault conditions. The following summarizes this method.

Condition 1 $V_{I(BAT)}$ above recharge threshold (V_{OREG} - V_{RCH}) and timeout fault occurs.

Recovery method: bqSWITCHER waits for the battery voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge or battery removal. Once the battery falls below the recharge threshold, the bqSWITCHER clears the fault and enters the battery absent detection routine. A POR or $\overline{\text{CE}}$ toggle also clears the fault.

Condition 2 Charge voltage below recharge threshold (V_{OREG} – V_{RCH}) and timeout fault occurs

Recovery method: Under this scenario, the bqSWITCHER applies the I_{DETECT} current. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, then the bqSWITCHER disables the I_{DETECT} current and executes the recovery method described in Condition 1. Once the battery falls below the recharge threshold, the bqSWITCHER clears the fault and enters the battery absent detection routine. A POR or $\overline{\text{CE}}$ toggle also clears the fault.

8.3.12 Output Overvoltage Protection (Applies to All Versions)

The bqSWITCHER provides a built-in overvoltage protection to protect the device and other components against damages if the battery voltage gets too high, as when the battery is suddenly removed. When an overvoltage condition is detected, this feature turns off the PWM and STATx pins. The fault is cleared once V_{IBAT} drops to the recharge threshold (V_{OREG} - V_{RCH}).

8.3.13 Battery Detection

For applications with removable battery packs, bqSWITCHER provides a battery absent detection scheme to reliably detect insertion and/or removal of battery packs.

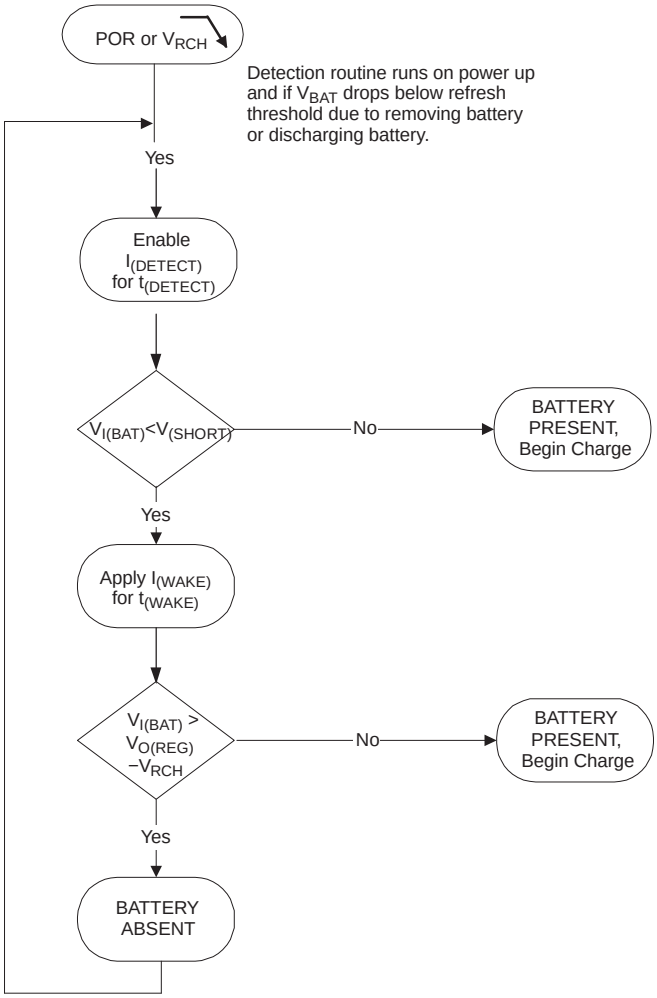


Figure 10. Battery Detection for bq2412x ICs

The voltage at the BAT pin is held above the battery recharge threshold, $V_{OREG} - V_{RCH}$, by the charged battery following fast charging. When the voltage at the BAT pin falls to the recharge threshold, either by a load on the battery or due to battery removal, the bqSWITCHER begins a battery absent detection test. This test involves enabling a detection current, $I_{DISCHARGE1}$, for a period of $t_{DISCHARGE1}$ and checking to see if the battery voltage is below the short circuit threshold, V_{SHORT}. Following this, the wake current, I_{WAKE} is applied for a period of t_{WAKE} and the battery voltage is checked again to ensure that it is above the recharge threshold. The purpose of this current is to attempt to *close* an open battery pack protector, if one is connected to the bqSWITCHER.

Passing both of the discharge and charge tests indicates a battery absent fault at the STAT pins. Failure of either test starts a new charge cycle. For the absent battery condition, typically the voltage on the BAT pin rises and falls between 0V and V_{OVP} thresholds indefinitely.

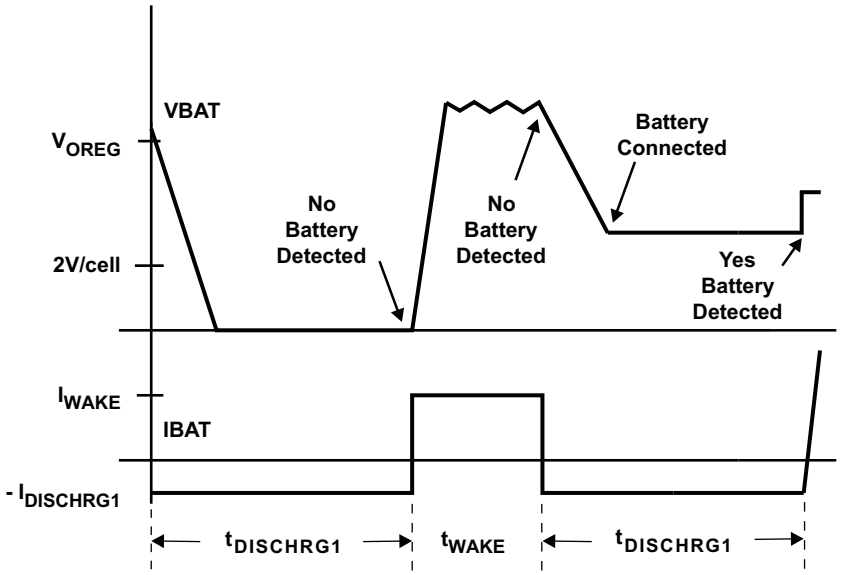


Figure 11. Battery Detect Timing Diagram

8.3.13.1 Battery Detection Example

In order to detect a *no battery* condition during the discharge and wake tests, the maximum output capacitance should not exceed the following:

a. Discharge ($I_{DISCHRG1}$ = 400 µA, $t_{DISCHRG1}$ = 1s, V_{SHORT} = 2V)

$$C_{MAX\_DIS} = \frac{I_{DISCHRG1} \times t_{DISCHRG1}}{V_{OREG} - V_{SHORT}}$$

$$C_{MAX\_DIS} = \frac{400\ \mu A \times 1\ s}{4.2\ V - 2\ V}$$

$$C_{MAX\_DIS} = 182\ \mu F \quad (7)$$

b. Wake (I_{WAKE} = 2 mA, t_{WAKE} = 0.5 s, $V_{OREG} - V_{RCH}$ = 4.1V)

$$C_{MAX\_WAKE} = \frac{I_{WAKE} \times t_{WAKE}}{(V_{OREG} - V_{RCH}) - 0\ V}$$

$$C_{MAX\_WAKE} = \frac{2\ mA \times 0.5\ s}{(4.2\ V - 0.1\ V) - 0\ V}$$

$$C_{MAX\_WAKE} = 244\ \mu F \quad (8)$$

Based on these calculations the recommended maximum output capacitance to ensure proper operation of the battery detection scheme is 100 µF which will allow for process and temperature variations.

Figure 12 shows the battery detection scheme when a battery is inserted. Channel 3 is the output signal and Channel 4 is the output current. The output signal switches between V_{OREG} and GND until a battery is inserted. Once the battery is detected, the output current increases from 0A to 1.3A, which is the programmed charge current for this application.

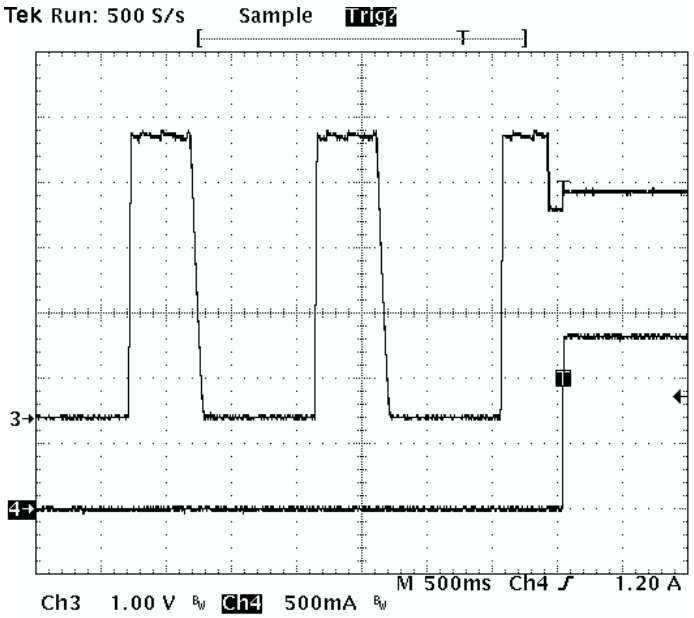


Figure 12. Battery Detection Waveform When a Battery is Inserted

Figure 13 shows the Battery Detection scheme when a battery is removed. Channel 3 is the output signal and Channel 4 is the output current. When the battery is removed, the output signal goes up due to the stored energy in the inductor and it crosses the $V_{OREG} - V_{RCH}$ threshold. At this point the output current goes to 0A and the IC terminates the charge process and turns on the $I_{DISCHG2}$ for $t_{DISCHG2}$. This causes the output voltage to fall down below the $V_{OREG} - V_{RCHG}$ threshold triggering a *Battery Absent* condition and starting the Battery Detection scheme.

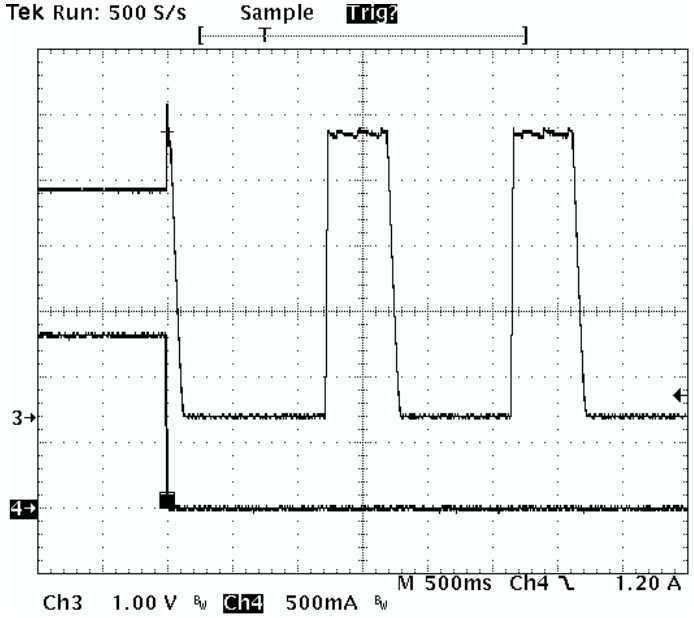


Figure 13. Battery Detection Waveform When a Battery is Removed

8.3.14 Current Sense Amplifier

BQ2412X family offers a current sense amplifier feature that translates the charge current into a DC voltage. Figure 14 is a block diagram of this feature.

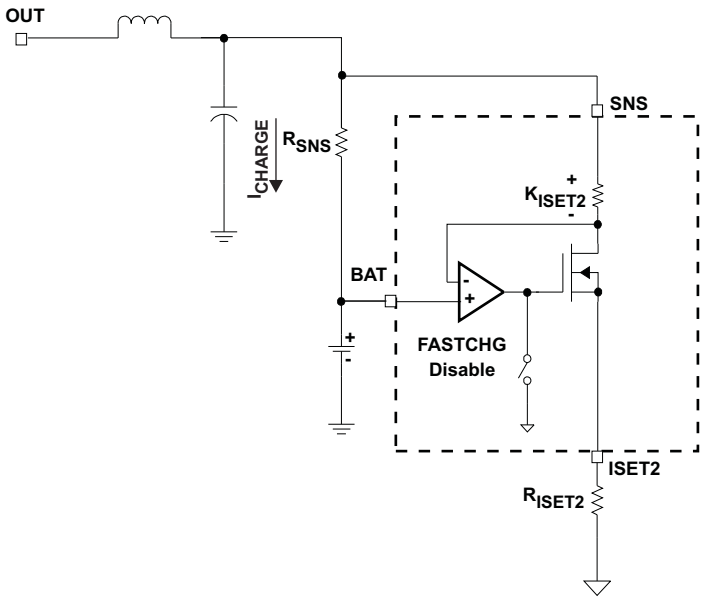


Figure 14. Current Sense Amplifier

The voltage on the ISET2 pin can be used to calculate the charge current. Equation 9 shows the relationship between the ISET2 voltage and the charge current:

$$I_{CHARGE} = \frac{V_{ISET2} \times K_{(ISET2)}}{R_{SNS} \times R_{ISET2}} \quad (9)$$

This feature can be used to monitor the charge current during the current regulation phase (Fastcharge only) and the voltage regulation phase. The schematics for the application circuit for this waveform is shown in Figure 21

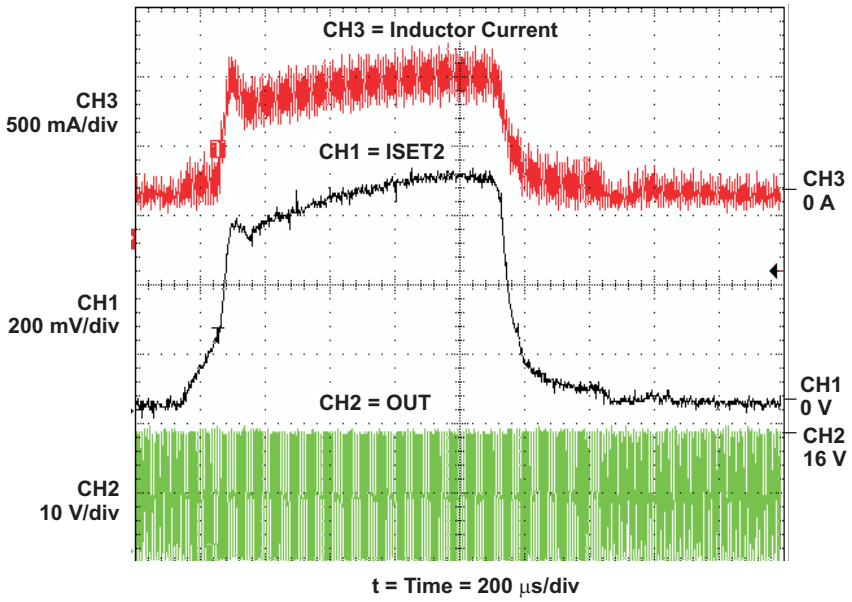


Figure 15. Current Sense Amplifier

8.4 Device Functional Modes

Figure 16 shows the operational flow chart for a typical charge operation.

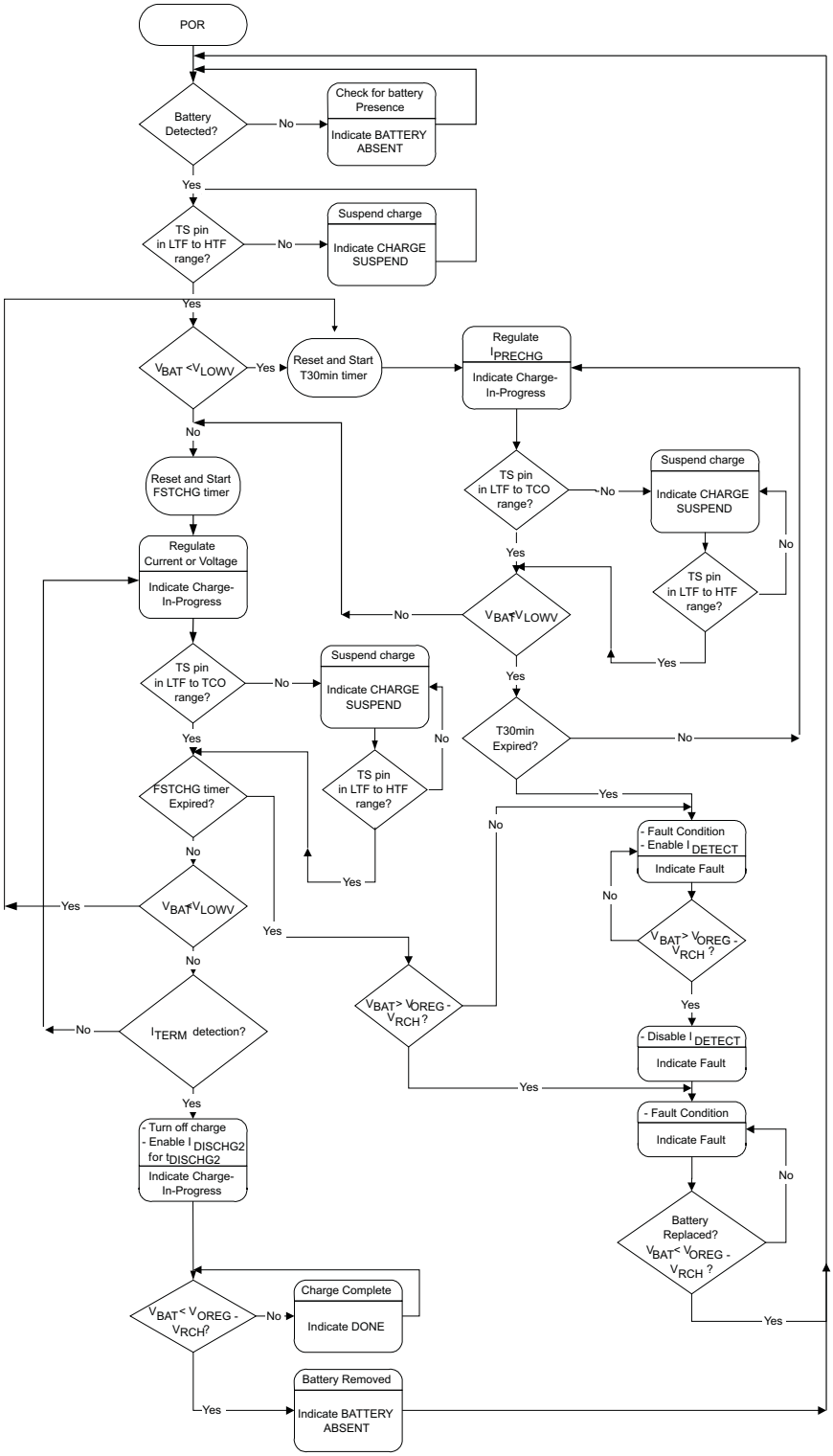


Figure 16. Operational Flow Chart

9 Application and Implementation

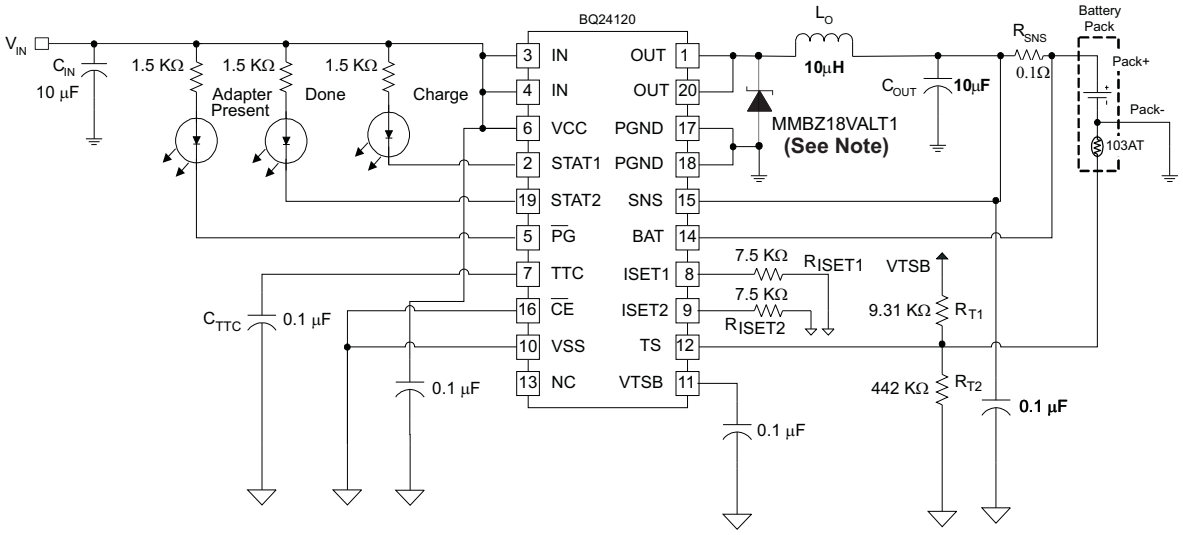
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq2412x battery charger supports precision Li-ion or Li-polymer charging system for single cell or two cell application. The design example below shows the design consideration for a 1-cell application.

9.2 Typical Application



TVS Zener diode is optional for devices with date codes effective March 2008

Figure 17. Standalone 1-Cell Application

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
AC adapter voltage (VIN)	16 V
Battery charge voltage (number of cells in series)	4.2 V (1 cell)
Battery charge current (during fast charge phase)	1.33 A
Precharge and termination current	0.133 A
Safety timer	5 hours
Inductor ripple current	30% of fast charge current (0.4 A)
Charging temperature range	0°C to 45°C

9.2.2 Detailed Design Procedure

This section provides a detailed system design example for the bq24120.

- V_{IN} = 16V
- V_{BAT} = 4.2V (1-Cell)
- I_{CHARGE} = 1.33 A
- $I_{PRECHARGE}$ = I_{TERM} = 133 mA
- Safety Timer = 5.0 hours
- Inductor Ripple Current = 30% of Fast Charge Current
- Initiate Charge Temperature = 0°C to 45°C

1. Determine the inductor value (L_{OUT}) for the specified charge current ripple:

$$\Delta I_L = I_{CHARGE} \times I_{CHARGE}\text{Ripple}$$

$$L_{OUT} = \frac{V_{BAT} \times (V_{INMAX} - V_{BAT})}{V_{INMAX} \times f \times \Delta I_L}$$

$$L_{OUT} = \frac{4.2 \times (16 - 4.2)}{16 \times (1.1 \times 10^6) \times (1.33 \times 0.3)}$$

$$L_{OUT} = 7.06\ \mu H \quad (10)$$

Set the output inductor to standard 10 µH. Calculate the total ripple current with using the 10 µH inductor:

$$\Delta I_L = \frac{V_{BAT} \times (V_{INMAX} - V_{BAT})}{V_{INMAX} \times f \times L_{OUT}}$$

$$\Delta I_L = \frac{4.2 \times (16 - 4.2)}{(16 \times 1.1 \times 10^6) \times (10 \times 10^{-6})}$$

$$\Delta I_L = 0.282\ A \quad (11)$$

Calculate the maximum output current (peak current):

$$I_{LPK} = I_{OUT} + \frac{\Delta I_L}{2}$$

$$I_{LPK} = 1.33 + \frac{0.282}{2}$$

$$I_{LPK} = 1.471\ A \quad (12)$$

Use standard 10 µH inductor with a saturation current higher than 1.471A. (that is, Sumida CDRH74-100)

2. Determine the output capacitor value (C_{OUT}) using 16 kHz as the resonant frequency:

$$f_o = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}}$$

$$C_{OUT} = \frac{1}{4\pi^2 \times f_o^2 \times L_{OUT}}$$

$$C_{OUT} = \frac{1}{4\pi^2 \times (16 \times 10^3)^2 \times (10 \times 10^{-6})}$$

$$C_{OUT} = 9.89\ \mu F \quad (13)$$

Use standard value 10 µF, 25V, X5R, ±20% ceramic capacitor (that is, Panasonic 1206 ECJ-3YB1E106M)

3. Determine the sense resistor using the following equation:

$$R_{SNS} = \frac{V_{RSNS}}{I_{CHARGE}} \quad (14)$$

In order to get better current regulation accuracy (±10%), let V_{RSNS} be between 100 mV and 200 mV. Use V_{RSNS} = 100 mV and calculate the value for the sense resistor.

$$R_{SNS} = \frac{100\ mV}{1.33\ A}$$
$$R_{SNS} = 0.075\ \Omega \quad (15)$$

This value is not standard in resistors. If this happens, then choose the next larger value which in this case is 0.1Ω. Using the same equation (15) the actual V_{RSNS} will be 133mV. Calculate the power dissipation on the sense resistor:

$$P_{RSNS} = I_{CHARGE}^2 \times R_{SNS}$$
$$P_{RSNS} = 1.33^2 \times 0.1$$
$$P_{RSNS} = 176.9\ mW \quad (16)$$

Select standard value 100 mΩ, 0.25W 0805, 1206 or 2010 size, high precision sensing resistor. (that is, Vishay CRCW1210-0R10F)

4. Determine ISET 1 resistor using the following equation:

$$R_{ISET1} = \frac{K_{ISET1} \times V_{ISET1}}{R_{SNS} \times I_{CHARGE}}$$
$$R_{ISET1} = \frac{1000 \times 1.0}{0.1 \times 1.33}$$
$$R_{ISET1} = 7.5\ k\Omega \quad (17)$$

Select standard value 7.5 kΩ, 1/16W ±1% resistor (that is, Vishay CRCWD0603-7501-F)

5. Determine ISET 2 resistor using the following equation:

$$R_{ISET2} = \frac{K_{ISET2} \times V_{ISET2}}{R_{SNS} \times I_{CHARGE}}$$
$$R_{ISET2} = \frac{1000 \times 1.0}{0.1 \times 1.33}$$
$$R_{ISET2} = 7.5\ k\Omega \quad (18)$$

Select standard value 7.5 kΩ, 1/16W ±1% resistor (that is, Vishay CRCWD0603-7501-F)

6. Determine TTC capacitor (C_{TTC}) for the 5.0 hours safety timer using the following equation:

$$C_{TTC} = \frac{tCHARGE}{KTTC}$$
$$C_{TTC} = \frac{300\ m}{2.6\ m/nF}$$
$$C_{TTC} = 115.4\ nF \quad (19)$$

Select standard value 100 nF, 16V, X7R, ±10% ceramic capacitor (that is, Panasonic ECJ-1VB1C104K). Using this capacitor the actual safety timer will be 4.3 hours.

7. Determine TS resistor network for an operating temperature range from 0°C to 45°C.

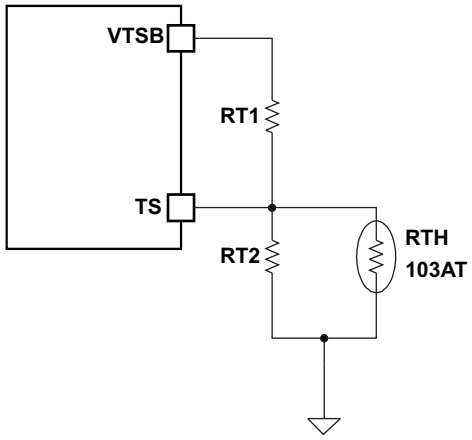


Figure 18. TS Resistor Network

Assuming a 103AT NTC Thermistor on the battery pack, determine the values for RT1 and RT2 using the following equations:

$$RT2 = \frac{V_{O(VTSB)} \times RTH_{COLD} \times RTH_{HOT} \times \left[\frac{1}{V_{LTF}} - \frac{1}{V_{HTF}}\right]}{RTH_{HOT} \times \left(\frac{V_{O(VTSB)}}{V_{HTF}} - 1\right) - RTH_{COLD} \times \left(\frac{V_{O(VTSB)}}{V_{LTF}} - 1\right)}$$

$$RT1 = \frac{\frac{V_{O(VTSB)}}{V_{LTF}} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}}$$

Where:

$V_{LTF} = V_{O(VTSB)} \times \%_{LTF÷100} / 100$

$V_{HTF} = V_{O(VTSB)} \times \%_{HTF÷100} / 100$

(20)

$RTH_{COLD} = 27.28\ k\Omega$

$RTH_{HOT} = 4.912\ k\Omega$

$RT1 = 9.31\ k\Omega$

$RT2 = 442\ k\Omega$

(21)

9.2.2.1 Inductor, Capacitor, and Sense Resistor Selection Guidelines

The bqSWITCHER provides internal loop compensation. With this scheme, best stability occurs when LC resonant frequency, f_0 is approximately 16 kHz (8 kHz to 32 kHz). Equation 22 can be used to calculate the value of the output inductor and capacitor. Table 3 provides a summary of typical component values for various charge rates.

$$f_0 = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

(22)

Table 3. Output Components Summary

CHARGE CURRENT	0.5 A	1 A	2 A
Output inductor, L_{OUT}	22 µH	10 µH	4.7 µH
Output capacitor, C_{OUT}	4.7 µF	10 µF	22 µF (or 2 × 10 µH) ceramic
Sense resistor, $R_{(SNS)}$	0.2 Ω	0.1 Ω	0.05 Ω

9.2.3 Application Curves

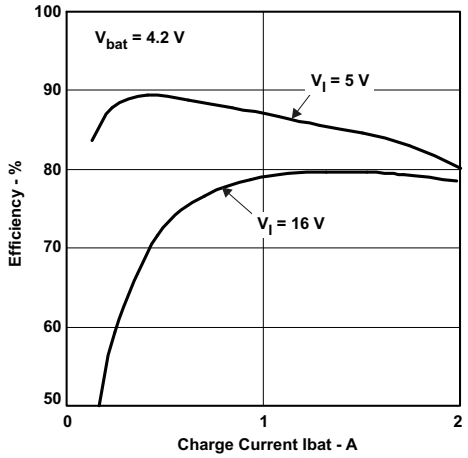


Figure 19. Efficiency 1-Cell

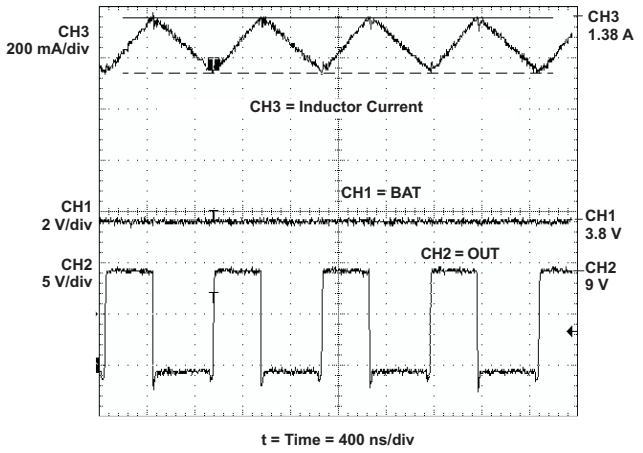
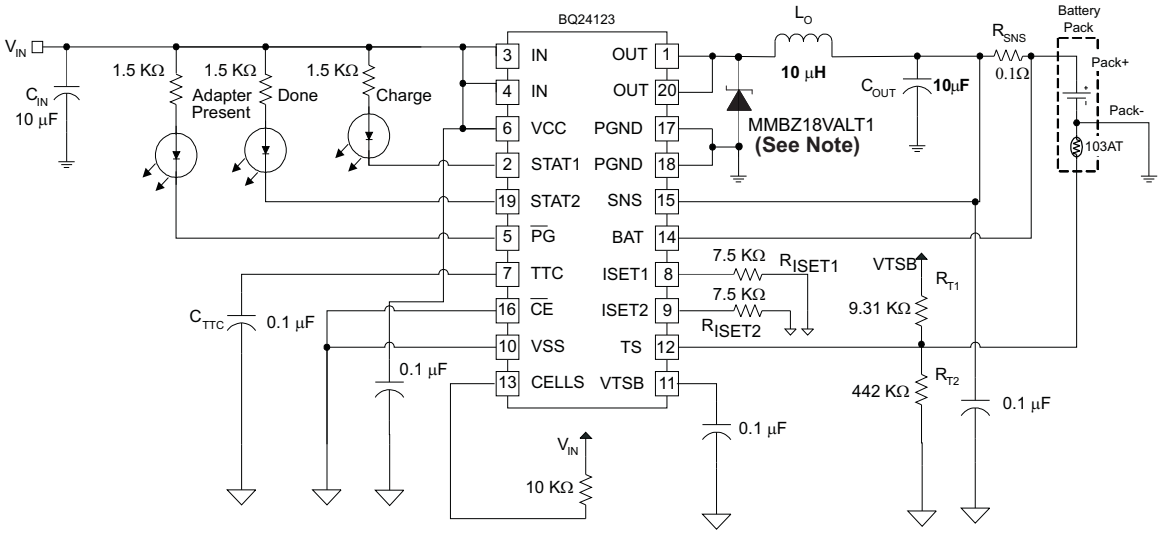


Figure 20. Switching Waveforms in Fast Charge Mode

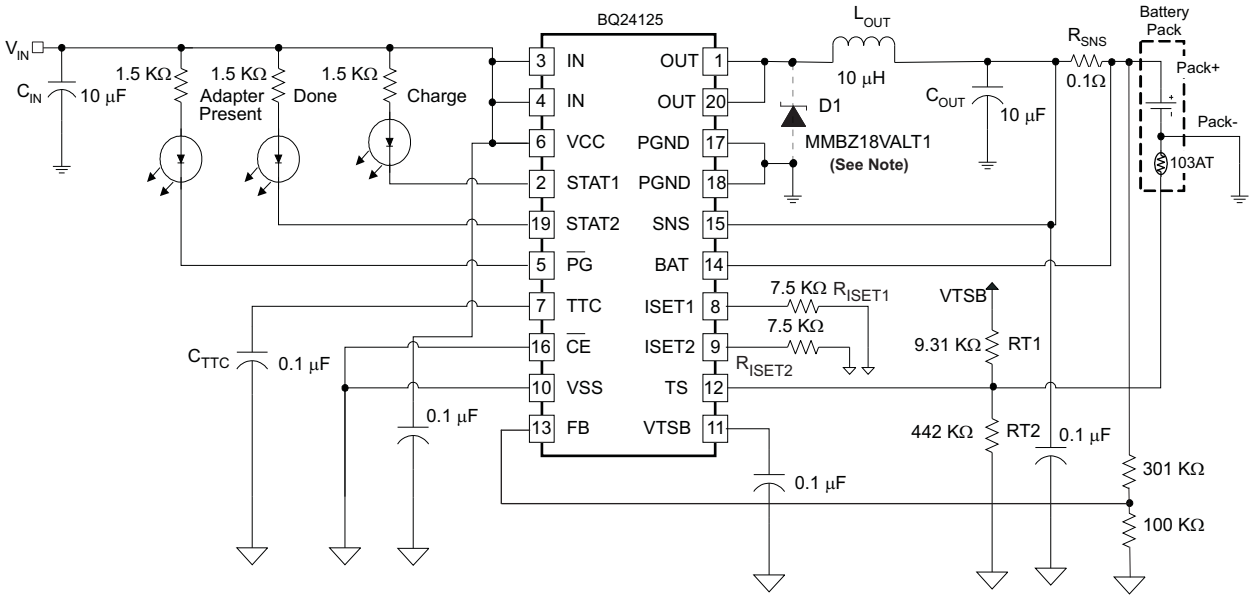
9.3 System Examples



TVS Zener diode is optional for devices with date codes effective March 2008

Figure 21. Standalone 2-Cells Application

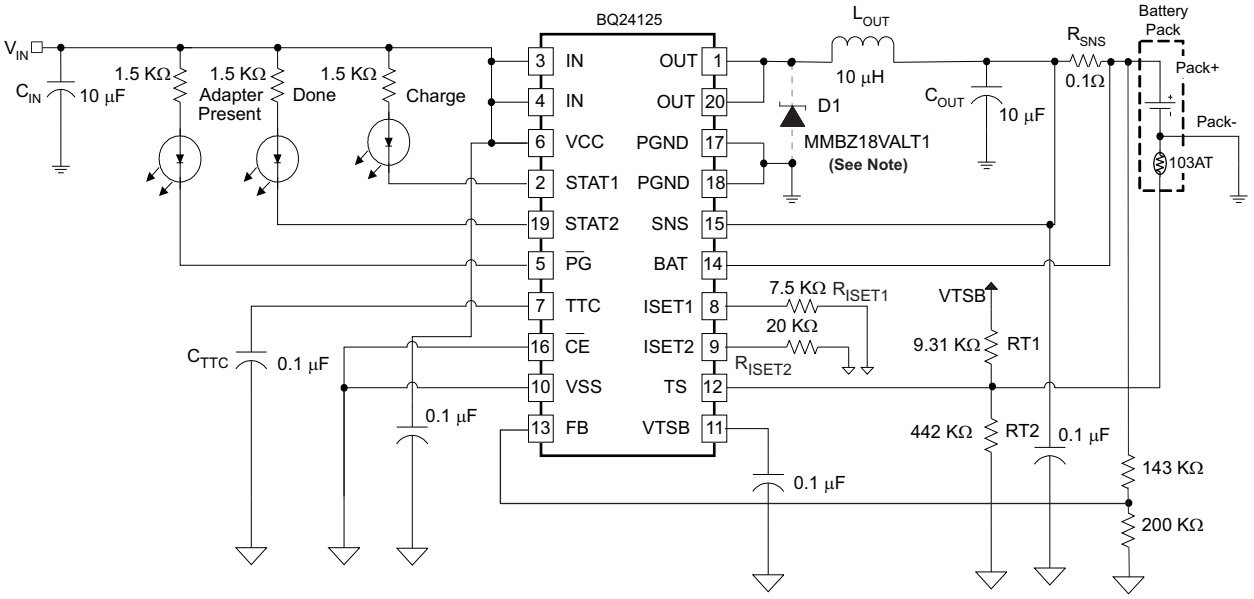
System Examples (continued)



Zener diode not needed for bq24125.

Figure 22. Externally Programmable Application

Using bq24125 to charge a LiFePO4 battery



Zener diode not needed for bq24125.

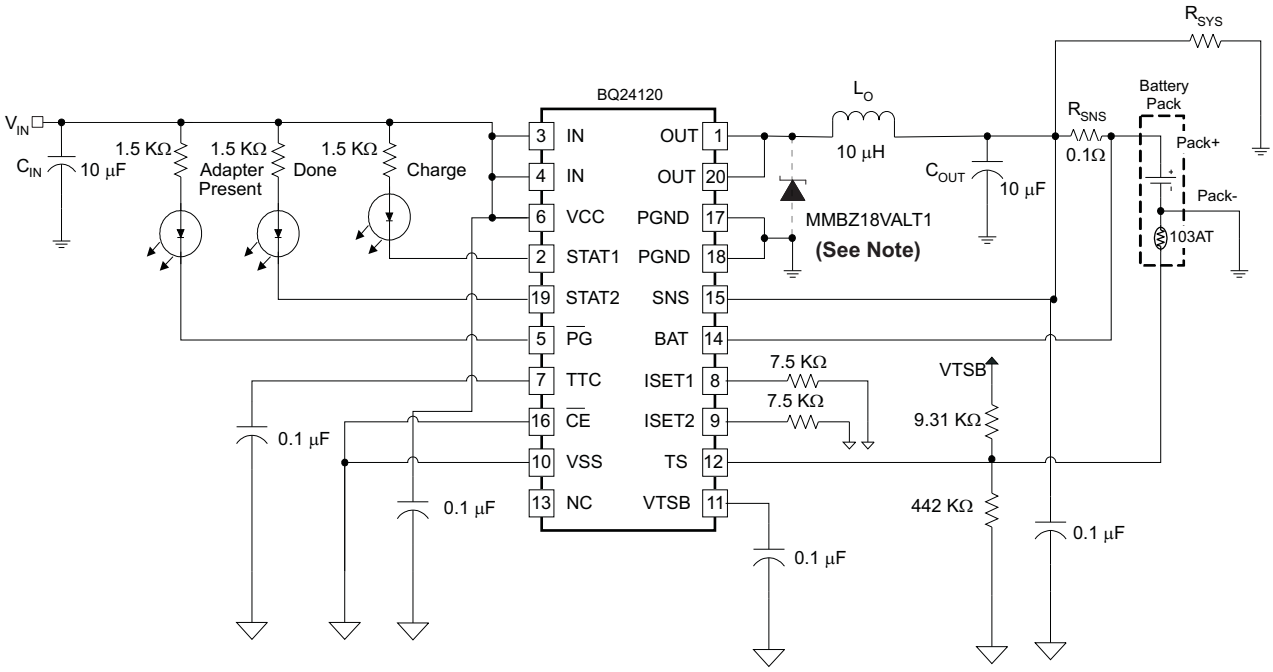
Figure 23. 1-Cell LiFePO4 Application

The LiFePO4 battery has many unique features such as a very high thermal runaway temperature, high discharge current capability, and high charge current. These special features make it attractive in many applications such as power tools. The recommended charge voltage is 3.6 V and termination current is 50 mA. Figure 23 shows an application circuit for charging one cell LiFePO4 using bq24105. The charge voltage is 3.6 V and recharge voltage is 3.516 V. The fast charging current is set to 1.33 A while the termination current is 50 mA. This circuit can be easily changed to support two or three cell applications. However, only 84 mV

System Examples (continued)

difference between regulation set point and rechargeable threshold makes it frequently enter into recharge mode when small load current is applied. This can be solved by lower down the recharge voltage threshold to 200 mV to discharge more energy from the battery before it enters recharge mode again. See the application report, *Using the bq24105/25 to Charge LiFePO4 Battery,* SLUA443, for additional details. The recharge threshold should be selected according to real application conditions.

Figure 24 shows charging a battery and powering system without affecting battery charge and termination.



TVS Zener diode is optional for devices with date codes effective March 2008.

Figure 24. Application Circuit for Charging a Battery and Powering a System Without Affecting Termination

The bqSWITCHER was designed as a stand-alone battery charger but can be easily adapted to power a system load, while considering a few minor issues.

Advantages:

1. The charger controller is based only on what current goes through the current-sense resistor (so precharge, constant current, and termination all work well), and is not affected by the system load.
2. The input voltage has been converted to a usable system voltage with good efficiency from the input.
3. Extra external FETs are not needed to switch power source to the battery.
4. The TTC pin can be grounded to disable termination and keep the converter running and the battery fully charged, or let the switcher terminate when the battery is full and then run off of the battery via the sense resistor.

Other Issues:

1. If the system load current is large (≥ 1 A), the IR drop across the battery impedance causes the battery voltage to drop below the refresh threshold and start a new charge. The charger would then terminate due to low charge current. Therefore, the charger would cycle between charging and termination. If the load is smaller, the battery would have to discharge down to the refresh threshold resulting in a much slower cycling. Note that grounding the TTC pin keeps the converter on continuously.
2. If TTC is grounded, the battery is kept at 4.2 V (not much different than leaving a fully charged battery set unloaded).
3. Efficiency declines 2-3% hit when discharging through the sense resistor to the system.

10 Power Supply Recommendations

For proper operation of bq2421x, VCC and IN (tied together) must be from 4.35 V to 16 V. Power limit for the input supply must be greater than the maximum power required for charging the battery (plus any additional load on the output of the switch-mode converter).

11 Layout

11.1 Layout Guidelines

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the power input capacitors, connected from input to PGND, should be placed as close as possible to the bqSWITCHER. The output inductor should be placed directly above the IC and the output capacitor connected between the inductor and PGND of the IC. The intent is to minimize the current path loop area from the OUT pin through the LC filter and back to the PGND pin. The sense resistor should be adjacent to the junction of the inductor and output capacitor. Route the sense leads connected across the R_{SNS} back to the IC, close to each other (minimize loop area) or on top of each other on adjacent layers. BAT and SNS traces should be away from high di/dt traces such as the OUT pin. Use an optional capacitor downstream from the sense resistor if long (inductive) battery leads are used.
- Place all small-signal components (C_{TTC}, RSET1/2 and TS) close to their respective IC pin (do not place components such that routing interrupts power stage currents). All small *control* signals should be routed away from the high current paths.
- The PCB should have a ground plane (return) connected directly to the return of all components through vias (3 vias per capacitor for power-stage capacitors, 3 vias for the IC PGND, 1 via per capacitor for small-signal components). A *star* ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With this small layout and a single ground plane, there is not a ground-bounce issue, and having the components segregated minimizes coupling between signals.
- The high-current charge paths into IN and from the OUT pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. The PGND pins should be connected to the ground plane to return current through the internal low-side FET. The *thermal* vias in the IC PowerPAD™ provide the return-path connection.
- The bqSWITCHER is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the PCB. Full PCB design guidelines for this package are provided in the application report entitled: *QFN/SON PCB Attachment,* SLUA271. Six 10-13 mil vias are a minimum number of recommended vias, placed in the IC's power pad, connecting it to a ground *thermal* plane on the opposite side of the PWB. This plane must be at the same potential as V_{SS} and PGND of this IC.
- See user's guide, *Using the bq241xx (bqSWITCHER™),* SLUU200 for an example of good layout.

11.2 Layout Example

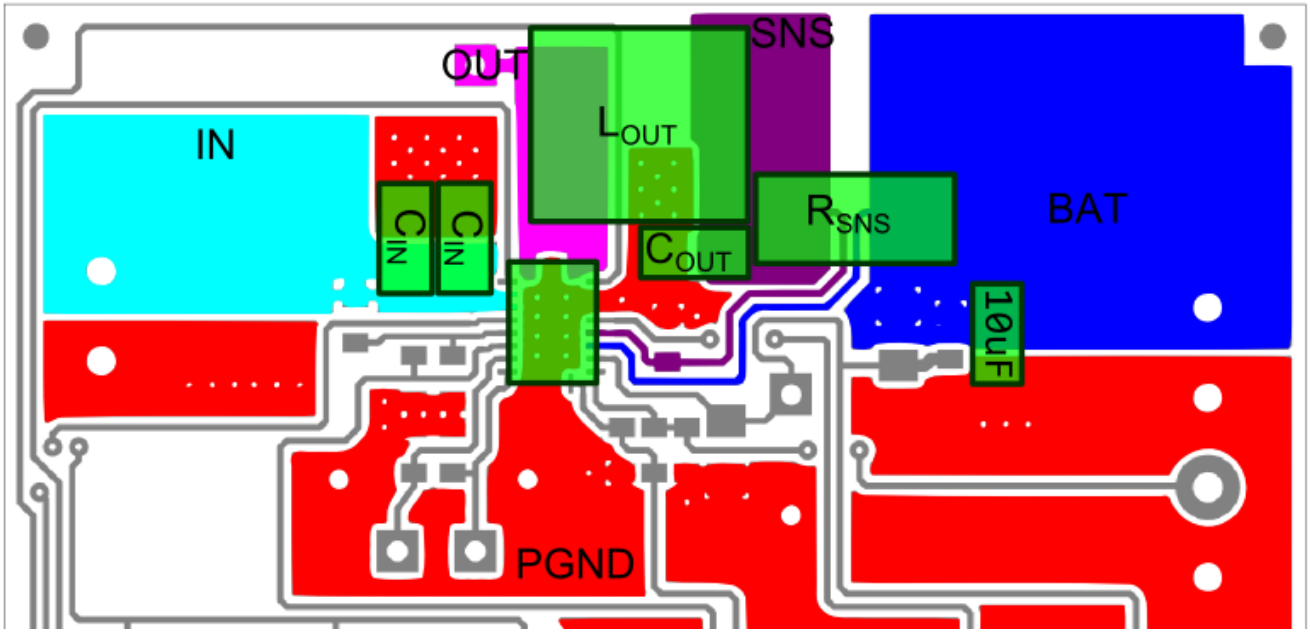


Figure 25. bq2412x PCB Layout

11.3 Thermal Considerations

The SWITCHER is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application report entitled: *QFN/SON PCB Attachment* , SLUA271.

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{(JA)} = \frac{T_J - T_A}{P} \quad (23)$$

where

- T_J = chip junction temperature
- T_A = ambient temperature
- P = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether or not other surfaces are in close proximity to the device being tested

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal power FET. It can be calculated from the following equation:

P = [Vin × Iin - Vbat × Ibat]

Due to the charge profile of Li-xx batteries, the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. (See Figure 8).

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *Using the bq24105/25 to Charge LiFePO4 Battery*, SLUA443
- *QFN/SON PCB Attachment* , SLUA271
- *Using the bq241xx (bqSWITCHER™)*, SLUU200

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
bq24120	Click here	Click here	Click here	Click here	Click here
bq24123	Click here	Click here	Click here	Click here	Click here
bq24125	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

bqSWITCHER, PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24120RHLR	ACTIVE	VQFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQU	Samples
BQ24120RHLRG4	ACTIVE	VQFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQU	Samples
BQ24120RHLT	ACTIVE	VQFN	RHL	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQU	Samples
BQ24120RHLTG4	ACTIVE	VQFN	RHL	20		TBD	Call TI	Call TI	-40 to 85		Samples
BQ24123RHLR	ACTIVE	VQFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQV	Samples
BQ24123RHLRG4	ACTIVE	VQFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQV	Samples
BQ24123RHLT	ACTIVE	VQFN	RHL	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQV	Samples
BQ24123RHLTG4	ACTIVE	VQFN	RHL	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQV	Samples
BQ24125RHLR	ACTIVE	VQFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CDZ	Samples
BQ24125RHLRG4	ACTIVE	VQFN	RHL	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CDZ	Samples
BQ24125RHLT	ACTIVE	VQFN	RHL	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CDZ	Samples
BQ24125RHLTG4	ACTIVE	VQFN	RHL	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	CDZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

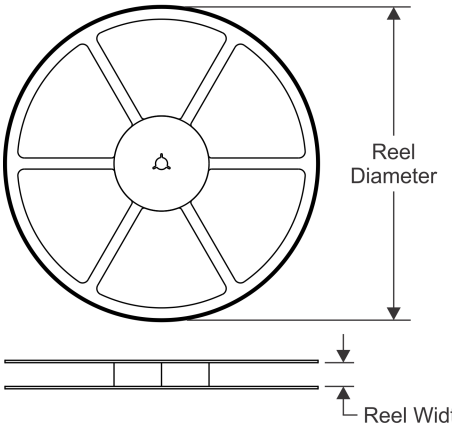
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

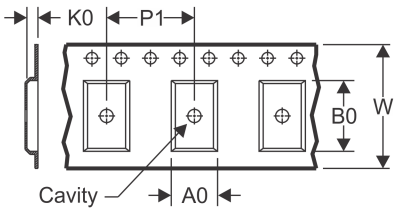
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

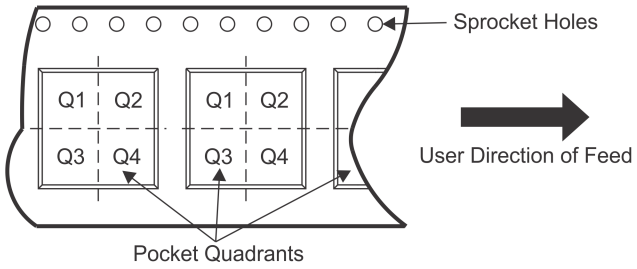


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

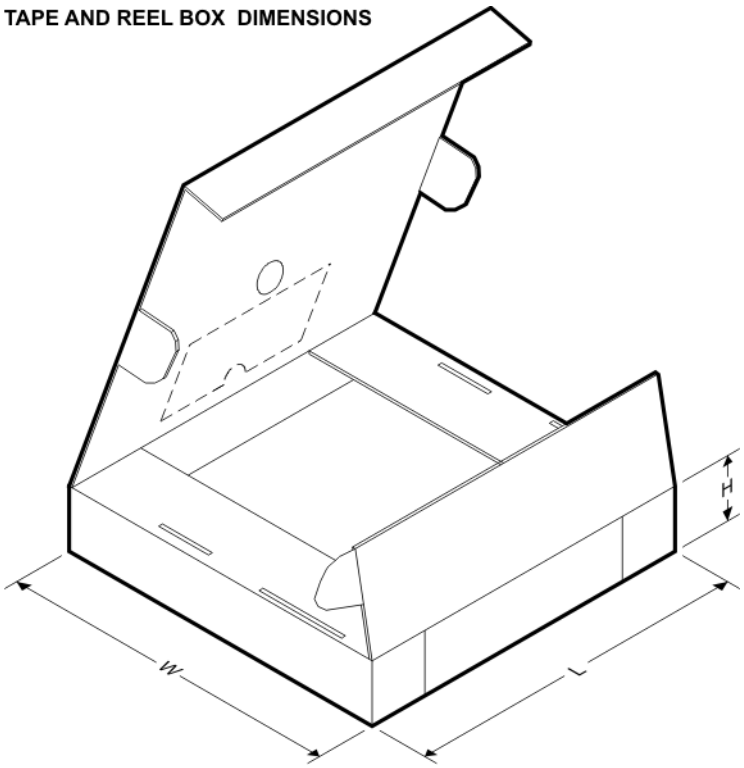
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24120RHLR	VQFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
BQ24120RHLT	VQFN	RHL	20	250	180.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
BQ24123RHLR	VQFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
BQ24123RHLT	VQFN	RHL	20	250	180.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
BQ24125RHLR	VQFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.3	8.0	12.0	Q1
BQ24125RHLR	VQFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
BQ24125RHLT	VQFN	RHL	20	250	180.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
BQ24125RHLT	VQFN	RHL	20	250	180.0	12.4	3.8	4.8	1.3	8.0	12.0	Q1

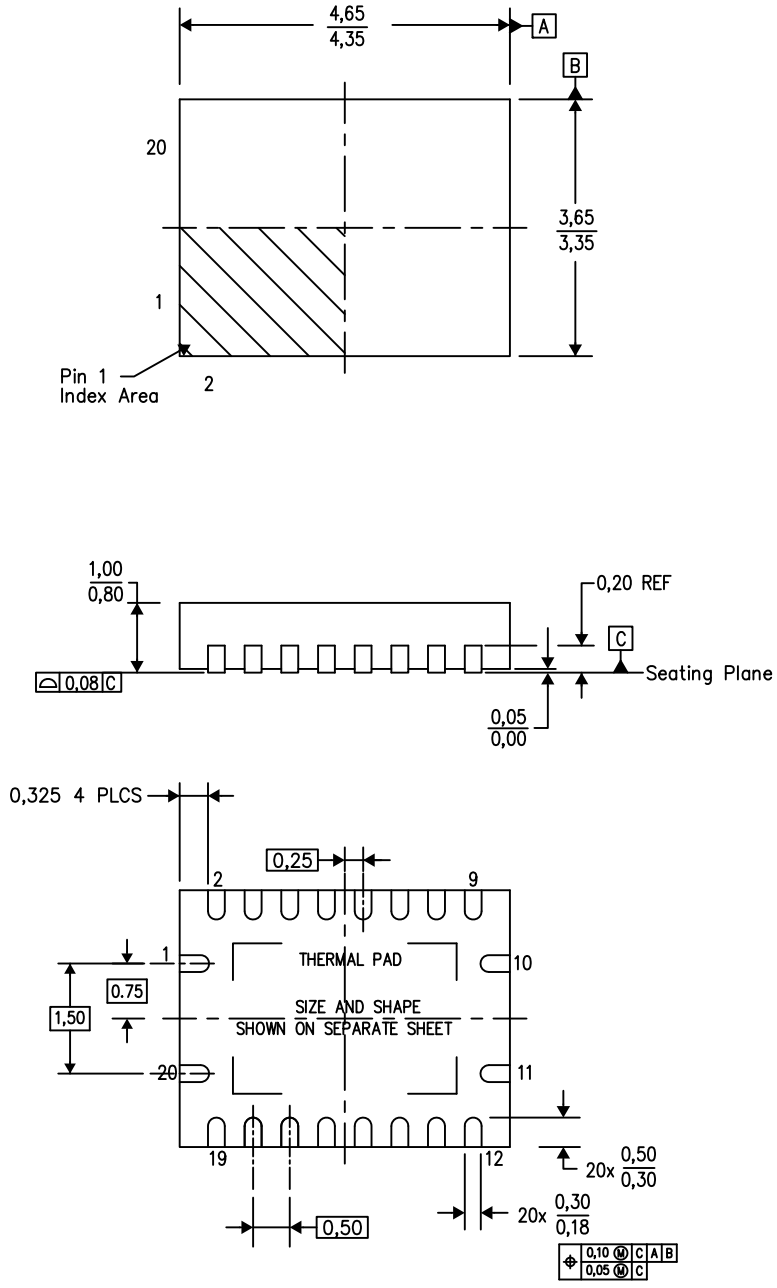
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24120RHLR	VQFN	RHL	20	3000	367.0	367.0	35.0
BQ24120RHLT	VQFN	RHL	20	250	210.0	185.0	35.0
BQ24123RHLR	VQFN	RHL	20	3000	367.0	367.0	35.0
BQ24123RHLT	VQFN	RHL	20	250	210.0	185.0	35.0
BQ24125RHLR	VQFN	RHL	20	3000	370.0	355.0	55.0
BQ24125RHLR	VQFN	RHL	20	3000	367.0	367.0	35.0
BQ24125RHLT	VQFN	RHL	20	250	210.0	185.0	35.0
BQ24125RHLT	VQFN	RHL	20	250	195.0	200.0	45.0

RHL (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

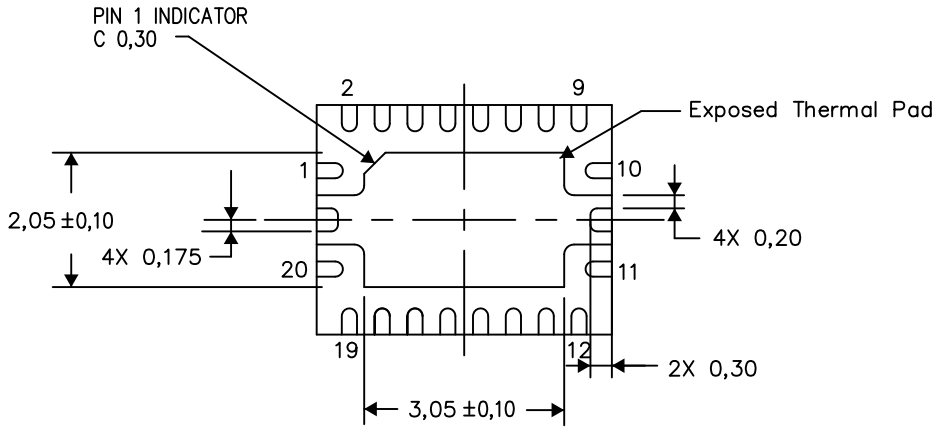
RHL (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



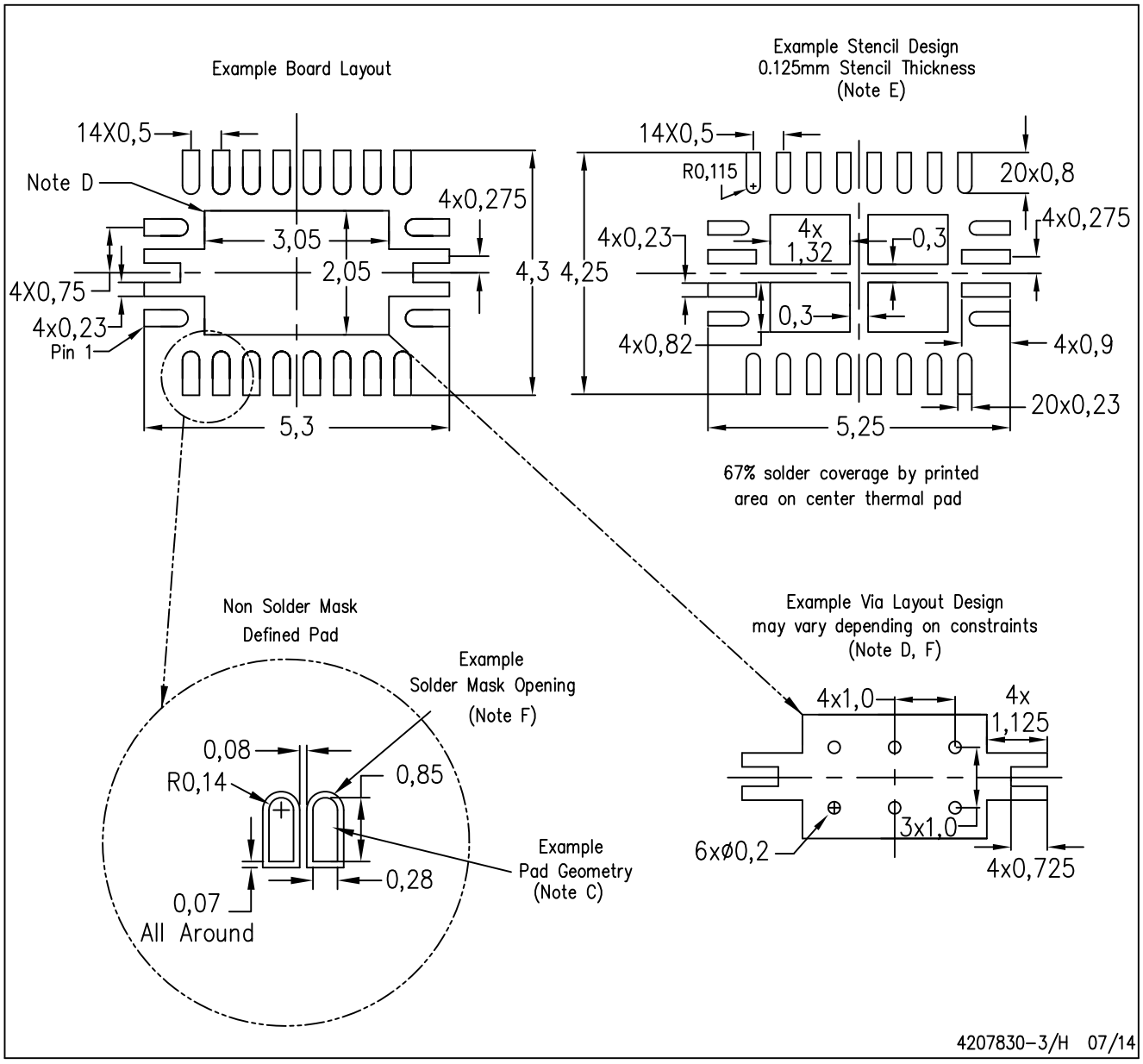
Bottom View

Exposed Thermal Pad Dimensions

4206363–3/N 07/14

NOTE: All linear dimensions are in millimeters

RHL (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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