



## CC1201 Low-Power, High-Performance RF Transceiver

### 1 Device Overview

#### 1.1 Features

- RF Performance and Analog Features:
  - High-Performance, Single-Chip Transceiver
    - Excellent Receiver Sensitivity:
      - –120 dBm at 1.2 kbps
      - –109 dBm at 50 kbps
    - Blocking Performance: 85 dB at 10 MHz
    - Adjacent Channel Selectivity: Up to 62 dB at 50-kHz Offset
    - Very Low Phase Noise: –114 dBc/Hz at 10-kHz Offset (169 MHz)
  - Programmable Output Power Up to +16 dBm With 0.4-dB Step Size
  - Automatic Output Power Ramping
  - Supported Modulation Formats: 2-FSK, 2-GFSK, 4-FSK, 4-GFSK, MSK, OOK
  - Supports Data Rate Up to 1.25 Mbps in Transmit and Receive
- Low Current Consumption:
  - Enhanced Wake-On-Radio (eWOR) Functionality for Automatic Low-Power Receive Polling
  - Power Down: 0.12  $\mu$ A (0.5  $\mu$ A With eWOR Timer Active)
    - RX: 0.5 mA in RX Sniff Mode
    - RX: 19 mA Peak Current in Low-Power Mode
    - RX: 23 mA Peak Current in High-Performance Mode
    - TX: 46 mA at +14 dBm
- Other:
  - Data FIFOs: Separate 128-Byte RX and TX
  - Support for Seamless Integration With the CC1190 Device for Increased Range Providing up to 3-dB Improvement in RX Sensitivity and up to +27 dBm TX Output Power
- Digital Features:
  - WaveMatch: Advanced Digital Signal Processing for Improved Sync Detect Performance
  - Autonomous Image Removal
  - Security: Hardware AES128 Accelerator
  - Data FIFOs: Separate 128-Byte RX and TX
  - Includes Functions for Antenna Diversity Support
  - Support for Retransmission
  - Support for Auto-Acknowledge of Received Packets
  - Automatic Clear Channel Assessment (CCA) for Listen-Before-Talk (LBT) Systems
  - Built-in Coding Gain Support for Increased Range and Robustness
  - Digital RSSI Measurement
  - Improved OOK Shaping for Less Occupied Bandwidth, Enabling Higher Output Power While Meeting Regulatory Requirements
- Dedicated Packet Handling for 802.15.4g:
  - CRC 16/32
  - FEC, Dual Sync Detection (FEC and non-FEC Packets)
  - Whitening
- General:
  - RoHS-Compliant 5-mm  $\times$  5-mm No-Lead QFN 32-Pin Package (RHB)
  - Pin-Compatible With the CC1120 Device
- Regulations – Suitable for Systems Targeting Compliance With:
  - **Europe:** ETSI EN 300 220
  - **US:** FCC CFR47 Part 15
  - **Japan:** ARIB STD-T108

#### 1.2 Applications

- Low-Power, High-Performance, Wireless Systems With Data Rate up to 1250 kbps
- ISM/SRD Bands: 169, 433, 868, 915, and 920 MHz
- Possible Support for Additional Frequency Bands: 137 to 158.3 MHz, 205 to 237.5 MHz, and 274 to 316.6 MHz
- Smart Metering (AMR/AMI)
- Home and Building Automation
- Wireless Alarm and Security Systems
- Industrial Monitoring and Control
- Wireless Healthcare Applications
- Wireless Sensor Networks and Active RFID
- IEEE 802.15.4g Applications



### 1.3 Description

The CC1201 device is a fully integrated single-chip radio transceiver designed for high performance at very low-power and low-voltage operation in cost-effective wireless systems. All filters are integrated, thus removing the need for costly external SAW and IF filters. The device is mainly intended for the ISM (Industrial, Scientific, and Medical) and SRD (Short Range Device) frequency bands at 164–190 MHz, 410–475 MHz, and 820–950 MHz.

The CC1201 device provides extensive hardware support for packet handling, data buffering, burst transmissions, clear channel assessment, link quality indication, and Wake-On-Radio. The main operating parameters of the CC1201 device can be controlled through an SPI interface. In a typical system, the CC1201 device will be used with a microcontroller and only few external passive components.

The CC1201 offers the same performance as the CC1200 for channel filter bandwidths of 50 kHz or more, and therefore presents a lower cost option for applications that do not require narrowband support.

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE   | BODY SIZE         |
|-------------|-----------|-------------------|
| CC1201RHB   | VQFN (32) | 5.00 mm x 5.00 mm |

(1) For more information, see [Section 8, Mechanical Packaging and Orderable Information](#)

### 1.4 Functional Block Diagram

Figure 1-1 shows the system block diagram of the CC120x family of devices.

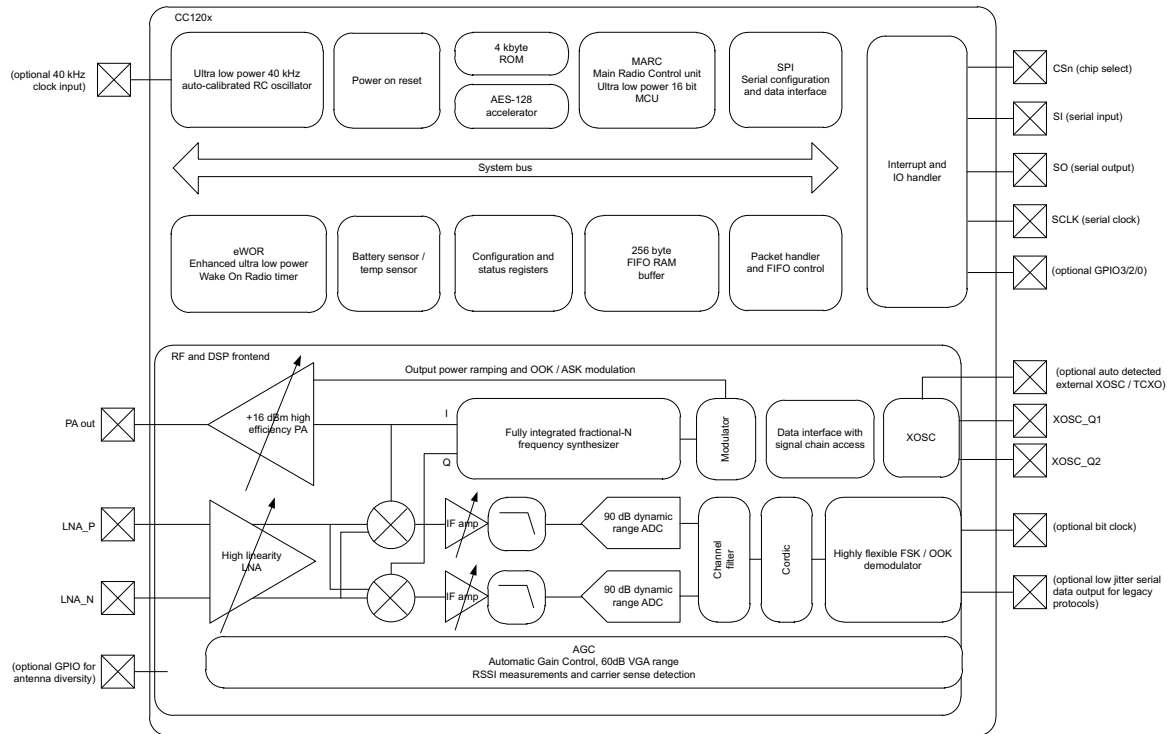


Figure 1-1. System Block Diagram

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## 2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This data manual revision history highlights the changes made to the SWRS154A device-specific data manual to make it an SWRS154B revision.

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| <b>Changes from Revision A (June 2014) to Revision B</b>                                       | <b>Page</b>        |
|--|--------------------|
| • Added Ambient to the temperature range condition and removed Tj from Temperature range ..... | <a href="#">7</a>  |
| • Added data to TCXO table .....   | <a href="#">16</a> |

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### 3 Terminal Configuration and Functions

#### 3.1 Pin Diagram

Figure 3-1 shows pin names and locations for the CC1201 device.

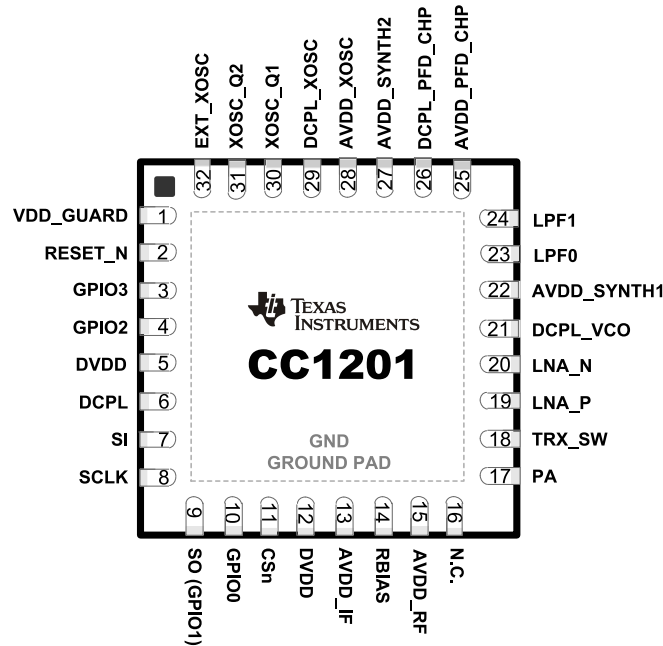


Figure 3-1. Package 5-mm x 5-mm QFN

## 3.2 Pin Configuration

The following table lists the pin-out configuration for the CC1201 device.

| PIN NO. | PIN NAME     | TYPE / DIRECTION | DESCRIPTION  |
|---------|--------------|------------------|--|
| 1       | VDD_GUARD    | Power            | 2.0–3.6 V VDD  |
| 2       | RESET_N      | Digital input    | Asynchronous, active-low digital reset   |
| 3       | GPIO3        | Digital I/O      | General-purpose I/O  |
| 4       | GPIO2        | Digital I/O      | General-purpose I/O  |
| 5       | DVDD         | Power            | 2.0–3.6 VDD to internal digital regulator  |
| 6       | DCPL         | Power            | Digital regulator output to external decoupling capacitor  |
| 7       | SI           | Digital input    | Serial data in   |
| 8       | SCLK         | Digital input    | Serial data clock  |
| 9       | SO(GPIO1)    | Digital I/O      | Serial data out (general-purpose I/O)  |
| 10      | GPIO0        | Digital I/O      | General-purpose I/O  |
| 11      | CSn          | Digital input    | Active-low chip select   |
| 12      | DVDD         | Power            | 2.0–3.6 V VDD  |
| 13      | AVDD_IF      | Power            | 2.0–3.6 V VDD  |
| 14      | RBIAS        | Analog           | External high-precision resistor   |
| 15      | AVDD_RF      | Power            | 2.0–3.6 V VDD  |
| 16      | N.C.         |                  | Not connected  |
| 17      | PA           | Analog           | Single-ended TX output (requires DC path to VDD)   |
| 18      | TRX_SW       | Analog           | TX and RX switch. Connected internally to GND in TX and floating (high-impedance) in RX.                         |
| 19      | LNA_P        | Analog           | Differential RX input (requires DC path to ground)   |
| 20      | LNA_N        | Analog           | Differential RX input (requires DC path to ground)   |
| 21      | DCPL_VCO     | Power            | Pin for external decoupling of VCO supply regulator  |
| 22      | AVDD_SYNTH1  | Power            | 2.0–3.6 V VDD  |
| 23      | LPF0         | Analog           | External loopfilter components   |
| 24      | LPF1         | Analog           | External loopfilter components   |
| 25      | AVDD_PFD_CHP | Power            | 2.0–3.6 V VDD  |
| 26      | DCPL_PFD_CHP | Power            | Pin for external decoupling of PFD and CHP regulator   |
| 27      | AVDD_SYNTH2  | Power            | 2.0–3.6 V VDD  |
| 28      | AVDD_XOSC    | Power            | 2.0–3.6 V VDD  |
| 29      | DCPL_XOSC    | Power            | Pin for external decoupling of XOSC supply regulator   |
| 30      | XOSC_Q1      | Analog           | Crystal oscillator pin 1 (must be grounded if a TCXO or other external clock connected to EXT_XOSC is used)      |
| 31      | XOSC_Q2      | Analog           | Crystal oscillator pin 2 (must be left floating if a TCXO or other external clock connected to EXT_XOSC is used) |
| 32      | EXT_XOSC     | Digital input    | Pin for external clock input (must be grounded if a regular crystal connected to XOSC_Q1 and XOSC_Q2 is used)    |
| –       | GND          | Ground pad       | The ground pad must be connected to a solid ground plane.  |

## 4 Specifications

All measurements performed on CC1200EM\_868\_930 rev.1.0.0, CC1200EM\_420\_470 rev.1.0.1, or CC1200EM\_169 rev.1.2.

### 4.1 Absolute Maximum Ratings<sup>(1)(2)</sup>

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                       | MIN  | MAX     | UNIT | CONDITION                                  |
|---|------|---------|------|--|
| Supply voltage (VDD, AVDD_x)                    | -0.3 | 3.9     | V    | All supply pins must have the same voltage |
| Input RF level                                  |      | +10     | dBm  |  |
| Voltage on any digital pin                      | -0.3 | VDD+0.3 | V    | max 3.9 V                                  |
| Voltage on any analog Pin (including DCPL pins) | -0.3 | 2.0     | V    |  |

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to  $V_{SS}$ , unless otherwise noted.

### 4.2 Handling Ratings

|           |  | MIN  | MAX  | UNIT |    |
|-----------|--|--|------|------|----|
| $T_{stg}$ | Storage temperature range                  | -40  | 125  | °C   |    |
| $V_{ESD}$ | Electrostatic discharge (ESD) performance: | Human body model (HBM), per ANSI/ESDA/JEDEC JS001 <sup>(1)</sup> | -2   | 2    | kV |
|           |  | Charged device model (CDM), per JESD22-C101 <sup>(2)</sup>       | -500 | 500  | V  |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V HBM allows safe manufacturing with a standard ESD control process.

### 4.3 Recommended Operating Conditions (General Characteristics)

| PARAMETER                 | MIN | TYP | MAX | UNIT | CONDITION                                  |
|---------------------------|-----|-----|-----|------|--|
| Voltage supply range      | 2.0 |     | 3.6 | V    | All supply pins must have the same voltage |
| Voltage on digital inputs | 0   |     | VDD | V    |  |
| Temperature range         | -40 |     | 85  | °C   | Ambient                                    |

### 4.4 Thermal Resistance Characteristics for RHB Package

|  | °C/W <sup>(1)</sup> | AIR FLOW (m/s) <sup>(2)</sup> |
|--|---------------------|-------------------------------|
| $R\theta_{JC}$ Junction-to-case (top)    | 21.1                | 0.00                          |
| $R\theta_{JB}$ Junction-to-board         | 5.3                 | 0.00                          |
| $R\theta_{JA}$ Junction-to-free air      | 31.3                | 0.00                          |
| $\Psi_{jT}$ Junction-to-package top      | 0.2                 | 0.00                          |
| $\Psi_{jB}$ Junction-to-board            | 5.3                 | 0.00                          |
| $R\theta_{JC}$ Junction-to-case (bottom) | 0.8                 | 0.00                          |

- (1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [ $R\theta_{JC}$ ] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
  - JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
  - JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
  - JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*
- Power dissipation of 40 mW and an ambient temperature of 25°C is assumed.
- (2) m/s = meters per second

## 4.5 RF Characteristics

| PARAMETER            | MIN   | TYP | MAX     | UNIT | CONDITION   |
|----------------------|-------|-----|---------|------|---|
| Frequency bands      | 820   |     | 950     | MHz  | Contact TI for more information about the use of these frequency bands. |
|                      | 410   |     | 475     | MHz  |   |
|                      | 164   |     | 190     | MHz  |   |
|                      | (274) |     | (316.6) | MHz  |   |
|                      | (205) |     | (237.5) | MHz  |   |
|                      | (137) |     | (158.3) | MHz  |   |
| Frequency resolution |       | 30  |         | Hz   | In 820–950 MHz band   |
|                      |       | 15  |         | Hz   | In 410–475 MHz band   |
|                      |       | 6   |         | Hz   | In 164–190 MHz band   |
| Data rate            | 0     |     | 1250    | kbps | Packet mode   |
|                      | 0     |     | 625     | kbps | Transparent mode  |

## 4.6 Regulatory Standards

| PERFORMANCE MODE      | FREQUENCY BAND | SUITABLE FOR COMPLIANCE WITH   | COMMENTS  |
|-----------------------|----------------|--|---|
| High-performance mode | 820–950 MHz    | ARIB STD-T108<br>ETSI EN 300 220 receiver categories 2 and 3<br>FCC PART 15.247<br>FCC PART 15.249 | Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender such as the CC1190 |
|                       | 410–475 MHz    | ETSI EN 300 220 receiver categories 2 and 3  | Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender                    |
|                       | 164–190 MHz    | ETSI EN 300 220  | Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender                    |
| Low-power mode        | 820–950 MHz    | ETSI EN 300 220 receiver categories 2 and 3<br>FCC PART 15.247<br>FCC PART 15.249                  |   |
|                       | 410–475 MHz    | ETSI EN 300 220 receiver categories 2 and 3  |   |
|                       | 164–190 MHz    | ETSI EN 300 220  |   |



## 4.7 Current Consumption, Static Modes

 $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  (unless otherwise noted)

| PARAMETER                 | MIN | TYP  | MAX | UNIT          | CONDITION  |
|---------------------------|-----|------|-----|---------------|--|
| Power down with retention |     | 0.12 | 1   | $\mu\text{A}$ |  |
|                           |     | 0.5  |     | $\mu\text{A}$ | Low-power RC oscillator running                      |
| XOFF mode                 |     | 180  |     | $\mu\text{A}$ | Crystal oscillator / TCXO disabled                   |
| IDLE mode                 |     | 1.5  |     | $\text{mA}$   | Clock running, system waiting with no radio activity |

## 4.8 Current Consumption, Transmit Modes

### 4.8.1 868-, 915-, and 920-MHz Bands (High-Performance Mode)

 $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  (unless otherwise noted)

| PARAMETER                      | MIN | TYP | MAX | UNIT        | CONDITION |
|--------------------------------|-----|-----|-----|-------------|-----------|
| TX current consumption +14 dBm |     | 46  |     | $\text{mA}$ |           |
| TX current consumption +10 dBm |     | 36  |     | $\text{mA}$ |           |

### 4.8.2 433-MHz Band (High-Performance Mode)

 $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  (unless otherwise noted)

| PARAMETER                      | MIN | TYP | MAX | UNIT        | CONDITION |
|--------------------------------|-----|-----|-----|-------------|-----------|
| TX current consumption +15 dBm |     | 49  |     | $\text{mA}$ |           |
| TX current consumption +14 dBm |     | 46  |     | $\text{mA}$ |           |
| TX current consumption +10 dBm |     | 35  |     | $\text{mA}$ |           |

### 4.8.3 169-MHz Band (High Performance Mode)

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  (unless otherwise noted)

| PARAMETER                      | MIN | TYP | MAX | UNIT | CONDITION |
|--------------------------------|-----|-----|-----|------|-----------|
| TX current consumption +15 dBm |     | 54  |     | mA   |           |
| TX current consumption +14 dBm |     | 50  |     | mA   |           |
| TX current consumption +10 dBm |     | 39  |     | mA   |           |

### 4.8.4 Low-Power Mode

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$ ,  $f_c = 869.5\text{ MHz}$  (unless otherwise noted)

| PARAMETER                      | MIN | TYP  | MAX | UNIT | CONDITION |
|--------------------------------|-----|------|-----|------|-----------|
| TX Current Consumption +10 dBm |     | 33.6 |     | mA   |           |

## 4.9 Current Consumption, Receive Modes

### 4.9.1 High-Performance Mode

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$ ,  $f_c = 869.5\text{ MHz}$  (unless otherwise noted)

| PARAMETER  | MIN | TYP  | MAX | UNIT          | CONDITION  |
|--|-----|------|-----|---------------|--|
| RX wait for sync<br>1.2 kbps, 4-byte preamble                                  |     | 0.5  |     | mA            | Using RX Sniff Mode, where the receiver wakes up at regular intervals looking for an incoming packet. Sniff mode configured to terminate on carrier sense, and is measured using <code>RSSI_VALID_COUNT = 1</code> (0 for 1.2 kbps), <code>AGC_WIN_SIZE = 0</code> , and <code>SETTLE_WAIT = 1</code> . <sup>(1)</sup> |
| 38.4 kbps, 12-byte preamble  |     | 3.5  |     | mA            |  |
| 50 kbps, 24-byte preamble  |     | 2.1  |     | mA            |  |
| RX peak current<br>1.2 kbps  |     | 23.6 |     | mA            | Peak current consumption during packet reception   |
| Average current consumption<br>Check for data packet every 1 second using eWOR |     | 8    |     | $\mu\text{A}$ | 50 kbps, 5-byte preamble, 40-kHz RC oscillator used as eWOR timer  |

(1) See the sniff mode design note for more information ([SWRA428](#))

### 4.9.2 Low-Power Mode

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$ ,  $f_c = 869.5\text{ MHz}$  (unless otherwise noted)

| PARAMETER                                    | MIN | TYP | MAX | UNIT | CONDITION   |
|--|-----|-----|-----|------|---|
| RX Peak current low-power RX mode<br>50 kbps |     | 19  |     | mA   | Peak current consumption during packet reception at the sensitivity limit |

## 4.10 Receive Parameters

All RX measurements made at the antenna connector, to a bit error rate (BER) limit of 1%. Selectivity and blocking is measured with the desired signal 3 dB above the sensitivity level.

### 4.10.1 General Receive Parameters (High-Performance Mode)

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$ ,  $f_c = 869.5\text{ MHz}$  (unless otherwise noted)

| PARAMETER   | MIN | TYP   | MAX  | UNIT                             | CONDITION   |
|---|-----|---|------|----------------------------------|---|
| Saturation  |     | +10   |      | dBm                              |   |
| Digital channel filter programmable bandwidth   | 50  |   | 1600 | kHz                              |   |
| IIP3  |     | -14   |      | dBm                              | At maximum gain   |
| Data rate offset tolerance  |     | $\pm 14$<br>$\pm 1600$  |      | %<br>ppm                         | With carrier sense detection enabled<br>With carrier sense detection disabled         |
| Spurious emissions<br>1–13 GHz (VCO leakage at 3.5 GHz)<br>30 MHz to 1 GHz                |     | < -56<br>< -57  |      | dBm<br>dBm                       | Radiated emissions measured according to ETSI<br>EN 300 220, $f_c = 869.5\text{ MHz}$ |
| Optimum source impedance<br>868-, 915-, and 920-MHz bands<br>433-MHz band<br>169-MHz band |     | $60 + j60 / 30 + j30$<br>$100 + j60 / 50 + j30$<br>$140 + j40 / 70 + j20$ |      | $\Omega$<br>$\Omega$<br>$\Omega$ | (Differential or Single-Ended RX Configurations)                                      |

#### 4.10.2 RX Performance in 868-, 915-, and 920-MHz Bands (High-Performance Mode)

T<sub>A</sub> = 25°C, VDD = 3.0 V (unless otherwise noted)

| PARAMETER  | MIN | TYP  | MAX | UNIT | CONDITION   |
|--|-----|------|-----|------|---|
| Sensitivity  |     | -119 |     | dBm  | 1.2 kbps 2-FSK, DEV=20 kHz CHF=50 kHz <sup>(1)</sup>      |
|  |     | -113 |     | dBm  | 4.8 kbps OOK CHF=128 kHz <sup>(1)</sup>                   |
|  |     | -108 |     | dBm  | 32.768 kbps 2-GFSK, DEV=50 kHz CHF=208 kHz <sup>(1)</sup> |
|  |     | -110 |     | dBm  | 38.4 kbps 2-GFSK, DEV=20 kHz CHF=104 kHz <sup>(1)</sup>   |
|  |     | -109 |     | dBm  | 50 kbps 2-GFSK, DEV=25 kHz, CHF=104 kHz <sup>(1)</sup>    |
|  |     | -97  |     | dBm  | 500 kbps 2-GMSK, CHF=833 kHz <sup>(1)</sup>               |
|  |     | -97  |     | dBm  | 1 Mbps 4-GFSK, DEV=400 kHz, CHF=1.66 MHz <sup>(1)</sup>   |
| Blocking and selectivity<br>1.2-kbps 2-FSK, 50-kHz channel<br>separation, 20-kHz deviation, 50-kHz<br>channel filter   |     | 50   |     | dB   | ± 50 kHz (adjacent channel)                               |
|  |     | 50   |     | dB   | ± 100 kHz (alternate channel)                             |
|  |     | 75   |     | dB   | ± 2 MHz   |
|  |     | 80   |     | dB   | ± 10 MHz  |
| Blocking and selectivity<br>32.768-kbps 2-GFSK, 200-kHz channel<br>separation, 50-kHz deviation, 208-kHz<br>channel filter   |     | 38   |     | dB   | ± 200 kHz   |
|  |     | 46   |     | dB   | ± 400 kHz   |
|  |     | 66   |     | dB   | ± 2 MHz   |
|  |     | 70   |     | dB   | ± 10 MHz  |
| Blocking and selectivity<br>38.4-kbps 2-GFSK, 100-kHz channel<br>separation, 20-kHz deviation, 104-kHz<br>channel filter   |     | 44   |     | dB   | + 100 kHz (adjacent channel)                              |
|  |     | 44   |     | dB   | ± 200 kHz (alternate channel)                             |
|  |     | 64   |     | dB   | ± 2 MHz   |
|  |     | 72   |     | dB   | ± 10 MHz  |
| Blocking and selectivity<br>50-kbps 2-GFSK, 200-kHz channel<br>separation, 25-kHz deviation, 104-kHz<br>channel filter (Same modulation format as<br>802.15.4g Mandatory Mode) |     | 41   |     | dB   | ± 200 kHz (adjacent channel)                              |
|  |     | 46   |     | dB   | ± 400 kHz (alternate channel)                             |
|  |     | 65   |     | dB   | ± 2 MHz   |
|  |     | 71   |     | dB   | ± 10 MHz  |
| Blocking and selectivity<br>100-kbps 2-GFSK, 50-kHz deviation,<br>208-kHz channel filter   |     | 45   |     | dB   | ± 400 kHz (adjacent channel)                              |
|  |     | 54   |     | dB   | ± 800 kHz (alternate channel)                             |
|  |     | 63   |     | dB   | ± 2 MHz   |
|  |     | 68   |     | dB   | ± 10 MHz  |
| Blocking and selectivity<br>500-kbps GMSK, 833-kHz channel filter  |     | 42   |     | dB   | + 1 MHz (adjacent channel)                                |
|  |     | 42   |     | dB   | ± 2 MHz (alternate channel)                               |
|  |     | 57   |     | dB   | ± 10 MHz  |
| Blocking and selectivity<br>1-Mbps 4-GFSK, 400-kHz deviation,<br>1.6-MHz channel filter  |     | 46   |     | dB   | ± 2 MHz (adjacent channel)                                |
|  |     | 52   |     | dB   | ± 4 MHz (alternate channel)                               |
|  |     | 59   |     | dB   | ± 10 MHz  |

(1) DEV is short for deviation, CHF is short for Channel Filter Bandwidth

### 4.10.3 RX Performance in 433-MHz Band (High-Performance Mode)

 $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  (unless otherwise noted)

| PARAMETER  | MIN | TYP  | MAX | UNIT | CONDITION   |
|--|-----|------|-----|------|---|
| Sensitivity  |     | -120 |     | dBm  | 1.2 kbps 2-FSK, DEV=20 kHz<br>CHF=50 kHz <sup>(1)</sup> |
|  |     | -111 |     | dBm  | 38.4 kbps 2-GFSK, DEV=20 kHz CHF=104 kHz <sup>(1)</sup> |
| Blocking and selectivity<br>1.2-kbps 2-FSK, 50-kHz channel<br>separation, 20-kHz deviation, 50-kHz<br>channel filter     |     | 56   |     | dB   | ± 50 kHz (adjacent channel)                             |
|  |     | 56   |     | dB   | ± 100 kHz (alternate channel)                           |
|  |     | 79   |     | dB   | ± 2 MHz   |
|  |     | 84   |     | dB   | ± 10 MHz  |
| Blocking and selectivity<br>38.4-kbps 2-GFSK, 100-kHz channel<br>separation, 20-kHz deviation, 104-kHz<br>channel filter |     | 49   |     | dB   | + 100 kHz (adjacent channel)                            |
|  |     | 48   |     | dB   | ± 200 kHz (alternate channel)                           |
|  |     | 66   |     | dB   | ± 2 MHz   |
|  |     | 74   |     | dB   | ± 10 MHz  |

(1) DEV is short for deviation, CHF is short for Channel Filter Bandwidth

### 4.10.4 RX Performance in 169-MHz Band (High-Performance Mode)

 $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  (unless otherwise noted)

| PARAMETER  | MIN | TYP  | MAX | UNIT | CONDITION   |
|--|-----|------|-----|------|---|
| Sensitivity  |     | -119 |     | dBm  | 1.2 kbps 2-FSK, DEV=20 kHz CHF=50 kHz <sup>(1)</sup>                  |
| Blocking and Selectivity<br>1.2 kbps 2-FSK, 50 kHz channel<br>separation, 20 kHz deviation, 50 kHz<br>channel filter |     | 62   |     | dB   | ± 50 kHz (adjacent channel)   |
|  |     | 62   |     | dB   | ± 100 kHz (alternate channel)   |
|  |     | 81   |     | dB   | ± 2 MHz   |
|  |     | 85   |     | dB   | ± 10 MHz  |
| Image rejection<br>(Image compensation enabled)  |     | 67   |     | dB   | 1.2 kbps, DEV=20 kHz, CHF=50 kHz, image at<br>-417 kHz <sup>(1)</sup> |

(1) DEV is short for deviation, CHF is short for Channel Filter Bandwidth

### 4.10.5 RX Performance in Low-Power Mode

 $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$ ,  $f_c = 869.5\text{ MHz}$  (unless otherwise noted)

| PARAMETER   | MIN | TYP | MAX | UNIT | CONDITION  |
|---|-----|-----|-----|------|--|
| Sensitivity   |     | -96 |     | dBm  | 50 kbps 2-GFSK, DEV=25 kHz, CHF=119 kHz <sup>(1)</sup> |
| Blocking and selectivity<br>50 kbps 2-GFSK, 200-kHz channel<br>separation, 25-kHz deviation, 104-kHz<br>channel filter<br>(Same modulation format as 802.15.4g<br>Mandatory Mode) |     | 41  |     | dB   | + 200 kHz (adjacent channel)                           |
|   |     | 45  |     | dB   | + 400 kHz (alternate channel)                          |
|   |     | 62  |     | dB   | ± 2 MHz  |
|   |     | 60  |     | dB   | ± 10 MHz   |
| Saturation  |     | 10  |     | dBm  |  |

(1) DEV is short for deviation, CHF is short for Channel Filter Bandwidth

## 4.11 Transmit Parameters

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$ ,  $f_c = 869.5\text{ MHz}$  (unless otherwise noted)

| PARAMETER                                   | MIN | TYP      | MAX | UNIT     | CONDITION   |
|---|-----|----------|-----|----------|---|
| Max output power                            |     | +14      |     | dBm      | At 915/920 MHz  |
|   |     | +15      |     | dBm      | At 915/920 MHz with $V_{DD} = 3.6\text{ V}$   |
|   |     | +15      |     | dBm      | At 868 MHz  |
|   |     | +16      |     | dBm      | At 868 MHz with $V_{DD} = 3.6\text{ V}$   |
|   |     | +15      |     | dBm      | At 433 MHz  |
|   |     | +16      |     | dBm      | At 433 MHz with $V_{DD} = 3.6\text{ V}$   |
| Min output power                            |     | -12      |     | dBm      | Within fine step size range   |
|   |     | -38      |     | dBm      | Within coarse step size range   |
| Output power step size                      |     | 0.4      |     | dB       | Within fine step size range   |
| Adjacent channel power                      |     | -60      |     | dBc      | 4-GFSK 9.6 kbps in 12.5 kHz channel, measured in 8.75 kHz bandwidth (ETSI 300 220 compliant)  |
| Spurious emissions<br>(Excluding harmonics) |     |          |     |          | Transmission at +14 dBm<br>Suitable for systems targeting compliance with ETSI EN 300-220, FCC part 15, ARIB STD-T108<br>Measured in 1 MHz bandwidth  |
| 30 MHz–1 GHz                                |     | < -57    |     | dBm      |   |
| 1–12.75 GHz                                 |     | < -50    |     | dBm      |   |
| Harmonics                                   |     |          |     |          | Transmission at +14 dBm (or maximum allowed in applicable band where this is less than +14 dBm) using TI reference design<br>Suitable for systems targeting compliance with ETSI EN 300-220, FCC part 15, ARIB STD-T108 |
| Second Harm, 169 MHz (ETSI)                 |     | -43      |     | dBm      |   |
| Third Harm, 169 MHz (ETSI)                  |     | -57      |     | dBm      |   |
| Fourth Harm, 169 MHz (ETSI)                 |     | -63      |     | dBm      |   |
| Second Harm, 433 MHz (ETSI)                 |     | -59      |     | dBm      |   |
| Third Harm, 433 MHz (ETSI)                  |     | -51      |     | dBm      |   |
| Fourth Harm, 433 MHz (ETSI)                 |     | -63      |     | dBm      |   |
| Second Harm, 868 MHz (ETSI)                 |     | -50      |     | dBm      |   |
| Third Harm, 868 MHz (ETSI)                  |     | -44      |     | dBm      |   |
| Fourth Harm, 868 MHz (ETSI)                 |     | -56      |     | dBm      |   |
| Second Harm, 915 MHz (FCC)                  |     | -58      |     | dBm      |   |
| Third Harm, 915 MHz (FCC)                   |     | -46      |     | dBm      |   |
| Fourth Harm, 915 MHz (FCC)                  |     | -62      |     | dBm      |   |
| Second Harm, 920 MHz (ARIB)                 |     | -65      |     | dBm      |   |
| Third Harm, 920 MHz (ARIB)                  |     | -60      |     | dBm      |   |
| Optimum load impedance                      |     |          |     |          |   |
| 868-, 915-, and 920-MHz bands               |     | 35 + j35 |     | $\Omega$ |   |
| 433-MHz band                                |     | 55 + j25 |     | $\Omega$ |   |
| 169-MHz band                                |     | 80 + j0  |     | $\Omega$ |   |

## 4.12 PLL Parameters

### 4.12.1 High Performance Mode

 $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  (unless otherwise noted)

| PARAMETER  | MIN | TYP  | MAX | UNIT   | CONDITION                   |
|--|-----|------|-----|--------|-----------------------------|
| Phase noise in 868-, 915-, and 920-MHz Bands<br>200-kHz loop bandwidth setting |     | -94  |     | dBc/Hz | $\pm 10\text{ kHz offset}$  |
|  |     | -96  |     | dBc/Hz | $\pm 100\text{ kHz offset}$ |
|  |     | -123 |     | dBc/Hz | $\pm 1\text{ MHz offset}$   |
|  |     | -137 |     | dBc/Hz | $\pm 10\text{ MHz offset}$  |
| Phase noise in 868-, 915-, and 920-MHz Bands<br>300-kHz loop bandwidth setting |     | -100 |     | dBc/Hz | $\pm 10\text{ kHz offset}$  |
|  |     | -102 |     | dBc/Hz | $\pm 100\text{ kHz offset}$ |
|  |     | -121 |     | dBc/Hz | $\pm 1\text{ MHz offset}$   |
|  |     | -136 |     | dBc/Hz | $\pm 10\text{ MHz offset}$  |
| Phase noise in 868-, 915-, and 920-MHz Bands<br>400-kHz loop bandwidth setting |     | -103 |     | dBc/Hz | $\pm 10\text{ kHz offset}$  |
|  |     | -104 |     | dBc/Hz | $\pm 100\text{ kHz offset}$ |
|  |     | -119 |     | dBc/Hz | $\pm 1\text{ MHz offset}$   |
|  |     | -133 |     | dBc/Hz | $\pm 10\text{ MHz offset}$  |
| Phase noise in 868-, 915-, and 920-MHz Bands<br>500-kHz loop bandwidth setting |     | -104 |     | dBc/Hz | $\pm 10\text{ kHz offset}$  |
|  |     | -106 |     | dBc/Hz | $\pm 100\text{ kHz offset}$ |
|  |     | -116 |     | dBc/Hz | $\pm 1\text{ MHz offset}$   |
|  |     | -130 |     | dBc/Hz | $\pm 10\text{ MHz offset}$  |
| Phase noise in 433-MHz band<br>300-kHz loop bandwidth setting                  |     | -106 |     | dBc/Hz | $\pm 10\text{ kHz offset}$  |
|  |     | -107 |     | dBc/Hz | $\pm 100\text{ kHz offset}$ |
|  |     | -127 |     | dBc/Hz | $\pm 1\text{ MHz offset}$   |
|  |     | -141 |     | dBc/Hz | $\pm 10\text{ MHz offset}$  |
| Phase noise in 169-MHz band<br>300-kHz loop bandwidth setting                  |     | -114 |     | dBc/Hz | $\pm 10\text{ kHz offset}$  |
|  |     | -114 |     | dBc/Hz | $\pm 100\text{ kHz offset}$ |
|  |     | -132 |     | dBc/Hz | $\pm 1\text{ MHz offset}$   |
|  |     | -142 |     | dBc/Hz | $\pm 10\text{ MHz offset}$  |

### 4.12.2 Low-Power Mode

| PARAMETER  | MIN | TYP  | MAX | UNIT   | CONDITION                   |
|--|-----|------|-----|--------|-----------------------------|
| Phase noise in 868-, 915-, and 920-MHz bands<br>200-kHz loop bandwidth setting |     | -99  |     | dBc/Hz | $\pm 10\text{ kHz offset}$  |
|  |     | -101 |     | dBc/Hz | $\pm 100\text{ kHz offset}$ |
|  |     | -121 |     | dBc/Hz | $\pm 1\text{ MHz offset}$   |
|  |     | -135 |     | dBc/Hz | $\pm 10\text{ MHz offset}$  |

### 4.13 Wake-up and Timing

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$ ,  $f_c = 869.5\text{ MHz}$  (unless otherwise noted)

The turnaround behavior to and from RX and/or TX is highly configurable, and the time it takes will depend on how the device is set up. See the CC120X user guide ([SWRU346](#)) for more information.

| PARAMETER  | MIN | TYP  | MAX | UNIT          | CONDITION   |
|--|-----|------|-----|---------------|---|
| Powerdown to IDLE  |     | 0.24 |     | ms            | Depends on crystal  |
| IDLE to RX/TX  |     | 133  |     | $\mu\text{s}$ | Calibration disabled  |
|  |     | 369  |     | $\mu\text{s}$ | Calibration enabled   |
| RX/TX turnaround   |     | 43   |     | $\mu\text{s}$ |   |
| RX-to-RX turnaround  |     | 369  |     | $\mu\text{s}$ | With PLL calibration  |
|  |     | 0    |     | $\mu\text{s}$ | Without PLL calibration   |
| TX-to-TX turnaround  |     | 369  |     | $\mu\text{s}$ | With PLL calibration  |
|  |     | 0    |     | $\mu\text{s}$ | Without PLL calibration   |
| RX/TX to IDLE time   |     | 237  |     | $\mu\text{s}$ | Calibrate when leaving RX/TX enabled  |
|  |     | 0    |     | $\mu\text{s}$ | Calibrate when leaving RX/TX disabled   |
| Frequency synthesizer calibration  |     | 314  |     | $\mu\text{s}$ | When using SCAL strobe  |
| Minimum required number of preamble bytes  |     | 0.5  |     | bytes         | Required for RF front end gain settling only. Digital demodulation does not require preamble for settling |
| Time from start RX until valid RSSI <sup>(1)</sup><br>Including gain settling (function of channel bandwidth. Programmable for trade-off between speed and accuracy) |     | 0.25 |     | ms            | 120-kHz channels  |

(1) See the design note on RSSI and response time. It is written for the CC112X devices, but the same principles apply for the CC1201 device.

### 4.14 40-MHz Crystal Oscillator

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  (unless otherwise noted)

| PARAMETER                  | MIN  | TYP  | MAX | UNIT     | CONDITION   |
|----------------------------|------|------|-----|----------|---|
| Crystal frequency          | 38.4 |      | 40  | MHz      | It is expected that there will be degraded sensitivity at multiples of XOSC/2 in RX, and an increase in spurious emissions when the RF channel is close to multiples of XOSC in TX. We recommend that the RF channel is kept RX_BW/2 away from XOSC/2 in RX, and that the level of spurious emissions be evaluated if the RF channel is closer than 1 MHz to multiples of XOSC in TX. |
| Load capacitance ( $C_L$ ) |      | 10   |     | pF       |   |
| ESR                        |      |      | 60  | $\Omega$ | Simulated over operating conditions   |
| Start-up time              |      | 0.24 |     | ms       | Depends on crystal  |

### 4.15 40-MHz Clock Input (TCXO)

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  if nothing else stated

| PARAMETER                            | MIN  | TYP | MAX | UNIT | CONDITION  |
|--------------------------------------|------|-----|-----|------|--|
| Clock frequency                      | 38.4 |     | 40  | MHz  |  |
| TCXO with CMOS output                |      |     |     |      | TCXO with CMOS output directly coupled to pin EXT_OSC                      |
| High input voltage                   | 1.4  |     | VDD | V    |  |
| Low input voltage                    | 0    |     | 0.6 | V    |  |
| Rise / Fall time                     |      |     | 2   | ns   |  |
| Clipped sine output                  |      |     |     |      | TCXO clipped sine output connected to pin EXT_OSC through series capacitor |
| Clock input amplitude (peak-to-peak) | 0.8  |     | 1.5 | V    |  |



#### 4.16 32-kHz Clock Input

 $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  (unless otherwise noted)

| PARAMETER                                 | MIN                 | TYP | MAX                 | UNIT | CONDITION |
|---|---------------------|-----|---------------------|------|-----------|
| Clock frequency                           |                     | 32  |                     | kHz  |           |
| 32-kHz clock input pin input high voltage | $0.8 \times V_{DD}$ |     |                     | V    |           |
| 32-kHz clock input pin input low voltage  |                     |     | $0.2 \times V_{DD}$ | V    |           |

#### 4.17 40-kHz RC Oscillator

 $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  (unless otherwise noted)

| PARAMETER                            | MIN | TYP       | MAX | UNIT | CONDITION   |
|--------------------------------------|-----|-----------|-----|------|---|
| Frequency                            |     | 40        |     | kHz  | After calibration (frequency calibrated against the 40-MHz crystal or TCXO) |
| Frequency accuracy after calibration |     | $\pm 0.1$ |     | %    | Relative to frequency reference (that is, 40-MHz crystal or TCXO)           |
| Initial calibration time             |     | 1.32      |     | ms   |   |

#### 4.18 I/O and Reset

 $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  (unless otherwise noted)

| PARAMETER                 | MIN                 | TYP | MAX                 | UNIT | CONDITION                   |
|---------------------------|---------------------|-----|---------------------|------|-----------------------------|
| Logic input high voltage  | $0.8 \times V_{DD}$ |     |                     | V    |                             |
| Logic input low voltage   |                     |     | $0.2 \times V_{DD}$ | V    |                             |
| Logic output high voltage | $0.8 \times V_{DD}$ |     |                     | V    | At 4-mA output load or less |
| Logic output low voltage  |                     |     | $0.2 \times V_{DD}$ | V    |                             |
| Power-on reset threshold  |                     | 1.3 |                     | V    | Voltage on DVDD pin         |

#### 4.19 Temperature Sensor

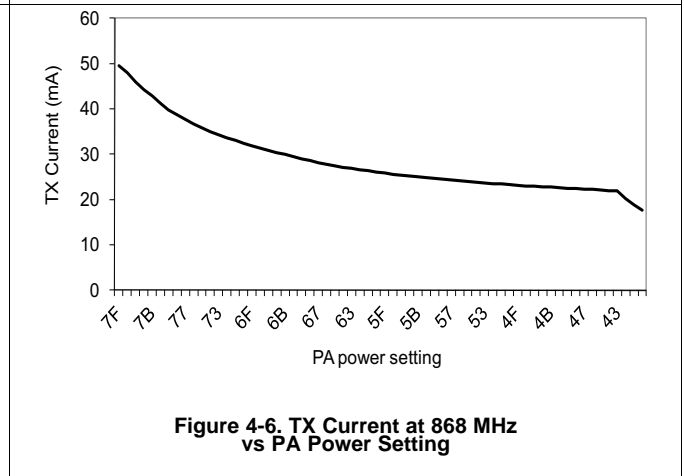
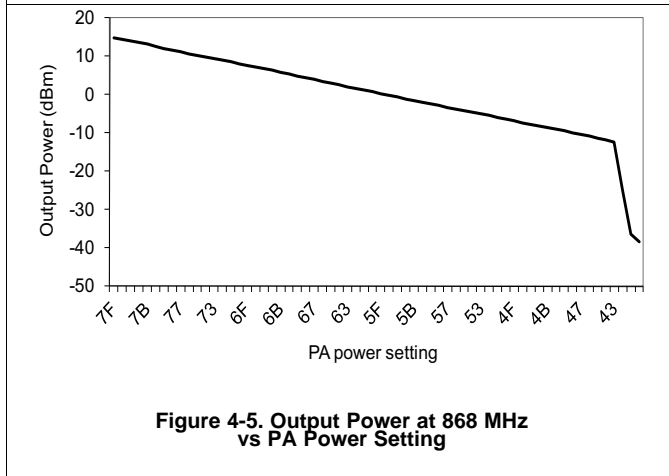
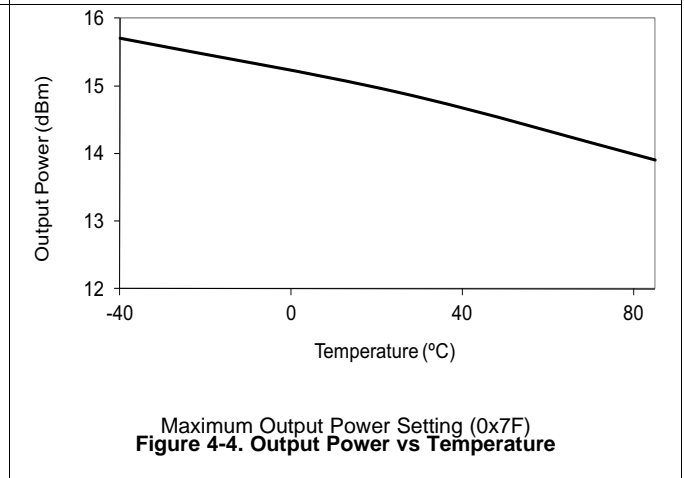
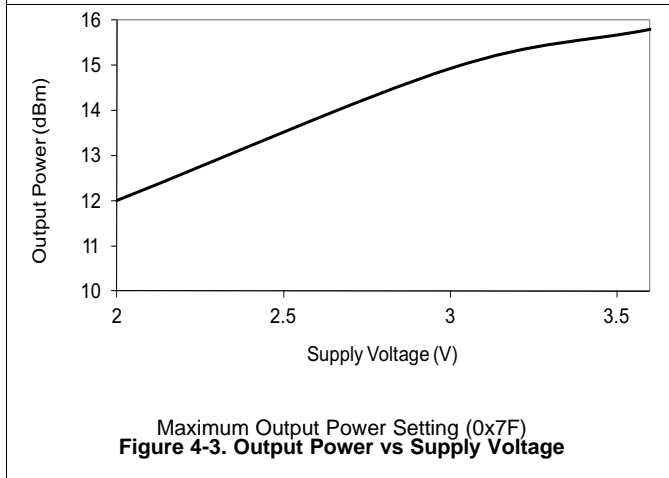
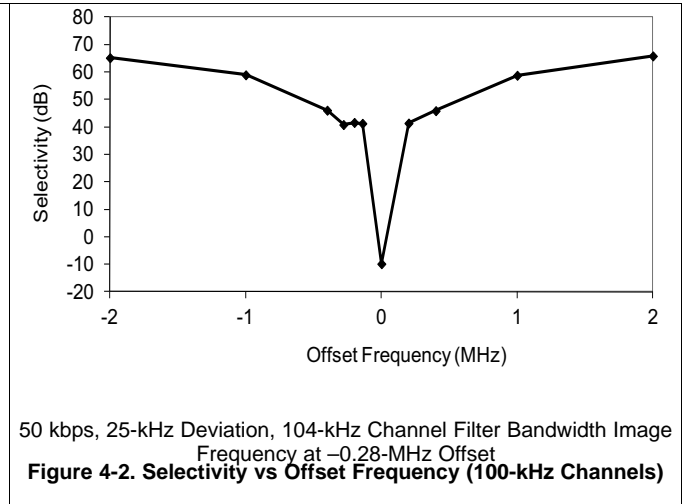
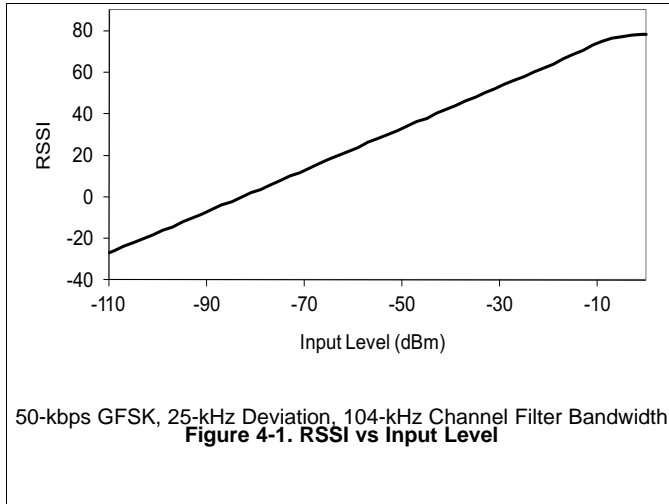
 $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.0\text{ V}$  (unless otherwise noted).

| PARAMETER                | MIN | TYP  | MAX | UNIT                         | CONDITION   |
|--------------------------|-----|------|-----|------------------------------|---|
| Temperature sensor range | -40 |      | 85  | $^\circ\text{C}$             |   |
| Temperature coefficient  |     | 2.66 |     | $\text{mV} / ^\circ\text{C}$ | Change in sensor output voltage versus change in temperature                        |
| Typical output voltage   |     | 794  |     | mV                           | Typical sensor output voltage at $T_A = 25^\circ\text{C}$ , $V_{DD} = 3.0\text{ V}$ |
| VDD coefficient          |     | 1.17 |     | $\text{mV} / \text{V}$       | Change in sensor output voltage versus change in VDD                                |

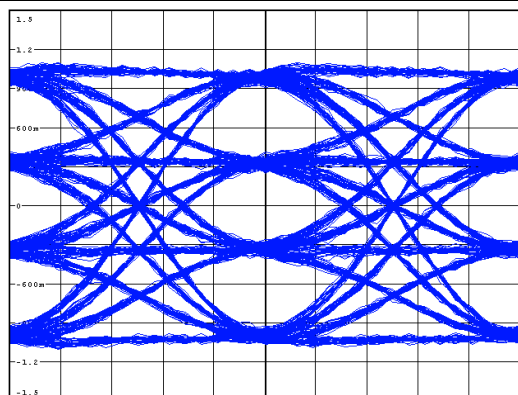
The CC1201 device can be configured to provide a voltage proportional to temperature on GPIO1. The temperature can be estimated by measuring this voltage (see [Section 4.19, Temperature Sensor](#)). For more information, see the temperature sensor design note ([SWRA415](#)).

### 4.20 Typical Characteristics

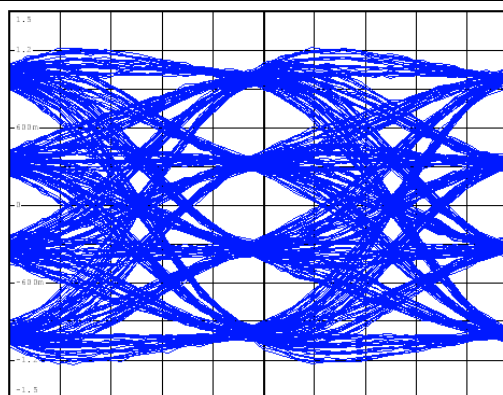
TA = 25°C, VDD = 3.0 V,  $f_c$  = 869.5 MHz (unless otherwise noted)



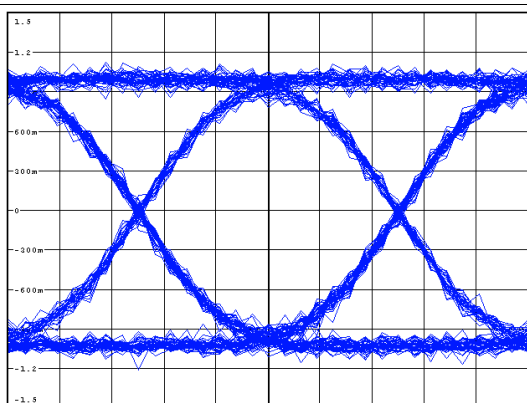
Typical Characteristics (continued)



1 Mbps 4-GFSK, 400-kHz Deviation 500-kHz Loop Bandwidth  
Figure 4-7. Eye Diagram



1 Mbps 4-GFSK, 400-kHz Deviation 300-kHz Loop Bandwidth  
Figure 4-8. Eye Diagram



1 kbps GFSK, 25-kHz Deviation 200-kHz Loop Bandwidth  
Figure 4-9. Eye Diagram

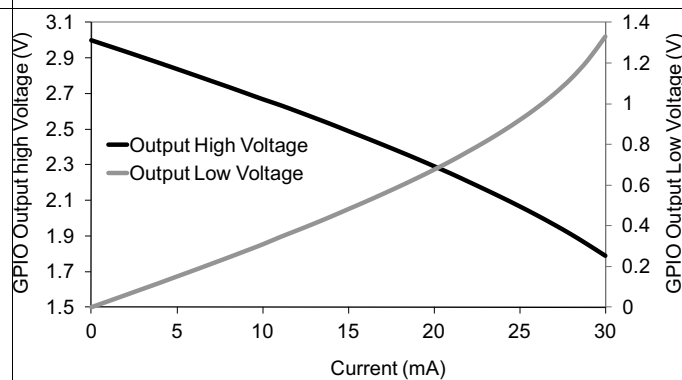
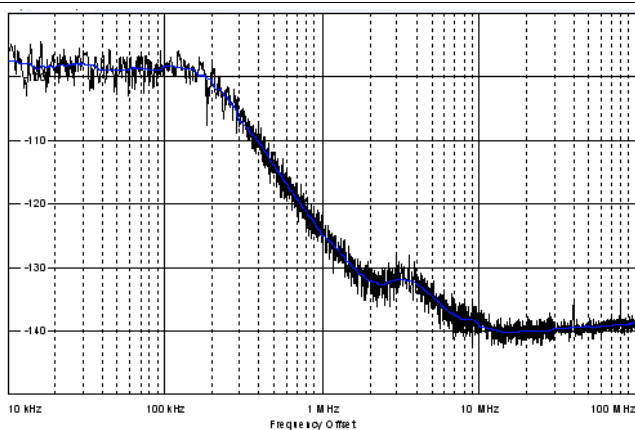
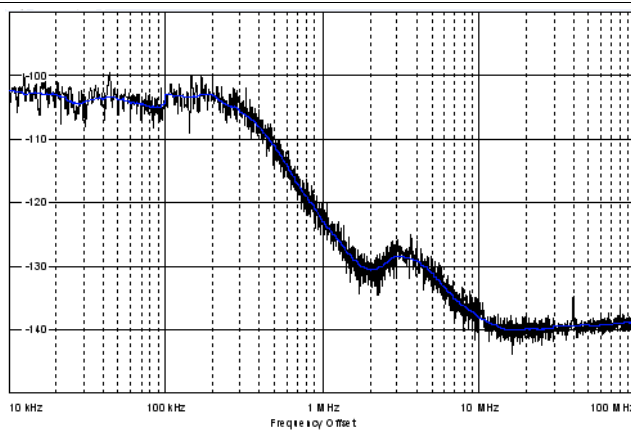


Figure 4-10. GPIO Output High and Low Voltage vs Current Being Sourced and Sunk

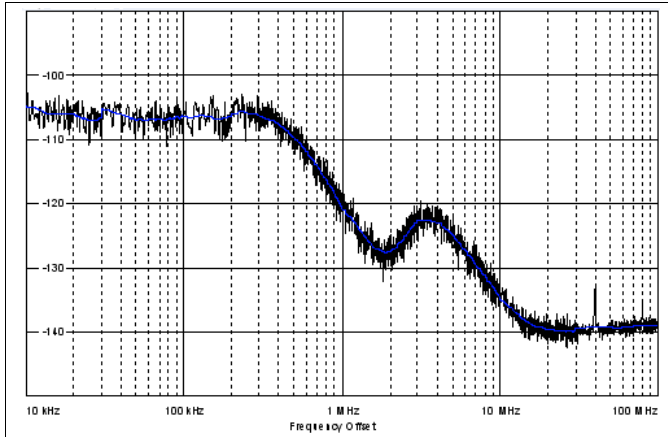


200-kHz Loop Bandwidth  
Figure 4-11. Phase Noise 869.5 MHz (10-kHz to 100-MHz Offset)

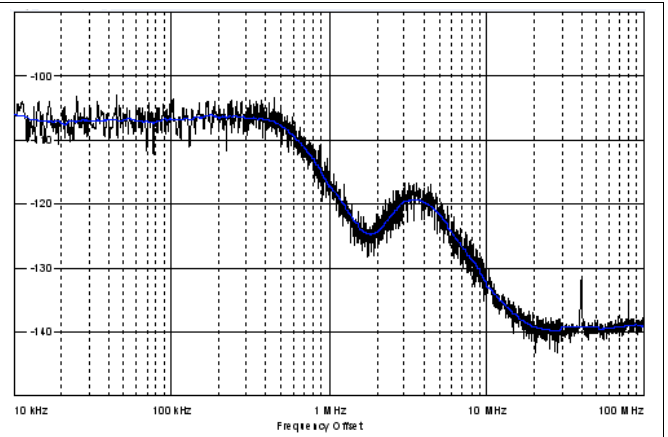


300-kHz Loop Bandwidth  
Figure 4-12. Phase Noise 869.5 MHz (10-kHz to 100-MHz Offset)

**Typical Characteristics (continued)**



400-kHz Loop Bandwidth  
**Figure 4-13. Phase Noise 869.5 MHz (10-kHz to 100-MHz Offset)**



500-kHz Loop Bandwidth  
**Figure 4-14. Phase Noise 869.5 MHz (10-kHz to 100-MHz Offset)**

## 5 Detailed Description

### 5.1 Block Diagram

Figure 5-1 shows the system block diagram of the CC120x family of devices.

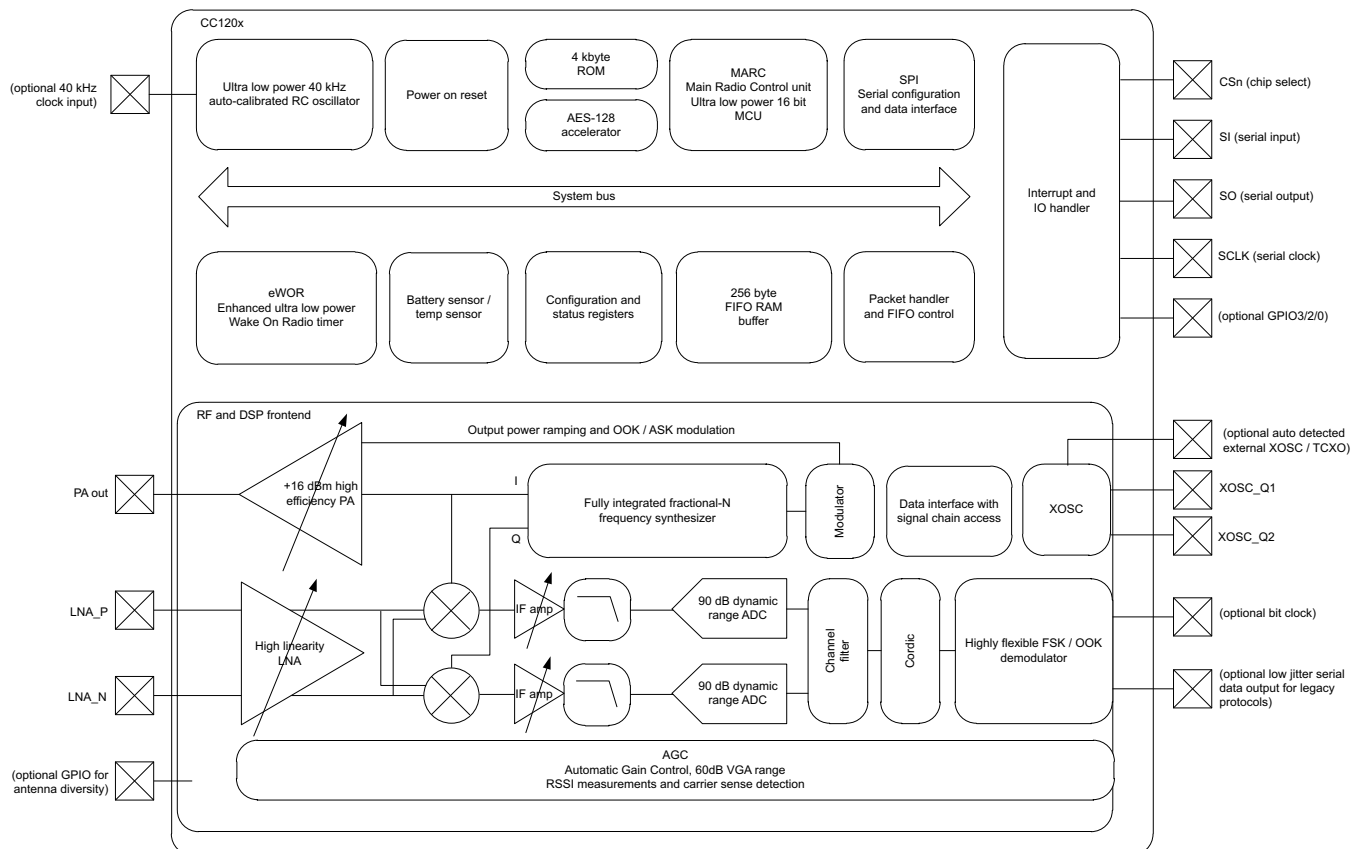


Figure 5-1. System Block Diagram

### 5.2 Frequency Synthesizer

At the center of the CC1201 device there is a fully integrated, fractional-N, ultra-high-performance frequency synthesizer. The frequency synthesizer is designed for excellent phase noise performance, providing very high selectivity and blocking performance. The system is designed to comply with the most stringent regulatory spectral masks at maximum transmit power.

Either a crystal can be connected to XOSC\_Q1 and XOSC\_Q2, or a TCXO can be connected to the EXT\_XOSC input. The oscillator generates the reference frequency for the synthesizer, as well as clocks for the analog-to-digital converter (ADC) and the digital part. To reduce system cost, the CC1201 device has high-accuracy frequency estimation and compensation registers to measure and compensate for crystal inaccuracies. This compensation enables the use of lower cost crystals. If a TCXO is used, the CC1201 device automatically turns on and off the TCXO when needed to support low-power modes and Wake-On-Radio operation.

### 5.3 Receiver

The CC1201 device features a highly flexible receiver. The received RF signal is amplified by the low-noise amplifier (LNA) and is down-converted in quadrature (I/Q) to the intermediate frequency (IF). At IF, the I/Q signals are digitized by the high dynamic-range ADCs.

An advanced automatic gain control (AGC) unit adjusts the front-end gain, and enables the CC1201 device to receive strong and weak signals, even in the presence of strong interferers. High-attenuation channel and data filtering enable reception with strong neighbor channel interferers. The I/Q signal is converted to a phase and magnitude signal to support the FSK and OOK modulation schemes.

---

#### NOTE

A unique I/Q compensation algorithm removes any problem of I/Q mismatch, thus avoiding time-consuming and costly I/Q image calibration steps.

---

### 5.4 Transmitter

The CC1201 transmitter is based on direct synthesis of the RF frequency (in-loop modulation). To use the spectrum effectively, the CC1201 device has extensive data filtering and shaping in TX mode to support high throughput data communication in narrowband channels. The modulator also controls power ramping to remove issues such as spectral splattering when driving external high-power RF amplifiers.

### 5.5 Radio Control and User Interface

The CC1201 digital control system is built around the main radio control (MARC), which is implemented using an internal high-performance, 16-bit ultra-low-power processor. MARC handles power modes, radio sequencing, and protocol timing.

A 4-wire SPI serial interface is used for configuration, strobe commands, and FIFO access. The digital baseband includes support for channel configuration, packet handling, and data buffering. The host MCU can stay in sleep mode until a valid RF packet is received. This greatly reduces power consumption. When the host MCU receives a valid RF packet, it burst-reads the data. This reduces the required computing power.

The CC1201 radio control and user interface are based on the widely used CC1101 transceiver. This relationship enables an easy transition between the two platforms. The command strobes and the main radio states are the same for the two platforms.

For legacy formats, the CC1201 device also supports two serial modes.

- Synchronous serial mode: The CC1201 device performs bit synchronization and provides the MCU with a bit clock with associated data.
- Transparent mode: The CC1201 device outputs the digital baseband signal using a digital interpolation filter to eliminate jitter introduced by digital filtering and demodulation.

### 5.6 Enhanced Wake-On-Radio (eWOR)

eWOR, using a flexible integrated sleep timer, enables automatic receiver polling with no intervention from the MCU. When the CC1201 device enters RX mode, it listens and then returns to sleep if a valid RF packet is not received. The sleep interval and duty cycle can be configured to make a trade-off between network latency and power consumption. Incoming messages are time-stamped to simplify timer re-synchronization.

The eWOR timer runs off an ultra-low-power RC oscillator. To improve timing accuracy, the RC oscillator can be automatically calibrated to the RF crystal in configurable intervals.

## 5.7 RX Sniff Mode

The CC1201 device supports quick start up times, and requires few preamble bits. RX Sniff Mode uses these conditions to dramatically reduce the current consumption while the receiver is waiting for data.

Because the CC1201 device can wake up and settle much faster than the duration of most preambles, it is not required to be in RX mode continuously while waiting for a packet to arrive. Instead, the Enhanced Wake On Radio feature can be used to put the device into sleep mode periodically. By setting an appropriate sleep time, the CC1201 device can wake up and receive the packet when it arrives with no performance loss. This sequence removes the need for accurate timing synchronization between transmitter and receiver, and lets the user trade off current consumption between the transmitter and receiver.

For more information, see the sniff mode design note ([SWRA428](#)).

## 5.8 Antenna Diversity

Antenna diversity can increase performance in a multipath environment. An external antenna switch is required. The CC1201 device uses one of the GPIO pins to automatically control the switch. This device also supports differential output control signals typically used in RF switches.

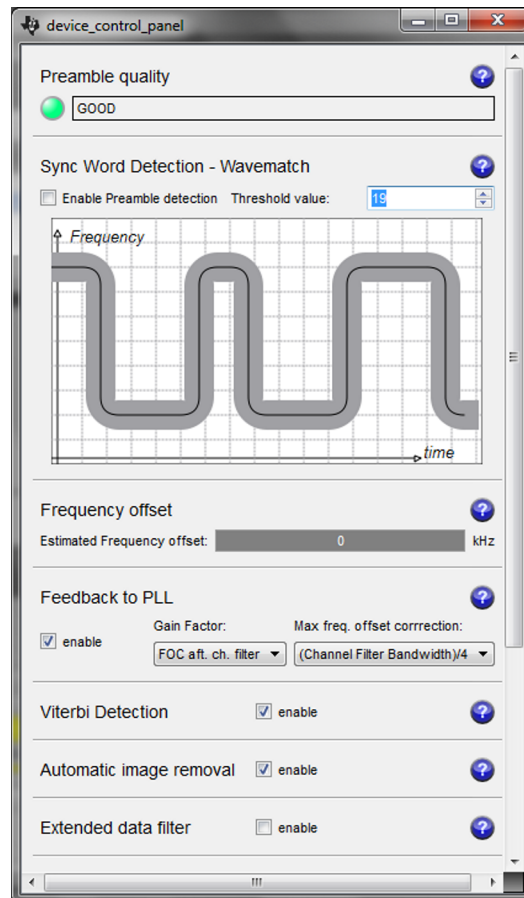
If antenna diversity is enabled, the GPIO alternates between high and low states until a valid RF input signal is detected. An optional acknowledge packet can be transmitted without changing the state of the GPIO.

An incoming RF signal can be validated by received signal strength or by using the automatic preamble detector. Using the automatic preamble detector ensures a more robust system and avoids the need to set a defined signal strength threshold (such a threshold sets the sensitivity limit of the system).

## 5.9 WaveMatch

Advanced capture logic locks onto the synchronization word and does not require preamble settling bytes. Therefore, receiver settling time is reduced to the settling time of the AGC, typically 4 bits.

The WaveMatch feature also greatly reduces false sync triggering on noise, further reducing the power consumption and improving sensitivity and reliability. The same logic can also be used as a high-performance preamble detector to reliably detect a valid preamble in the channel.



See [swrc046](#) for more information.

**Figure 5-2. Receiver Configurator in SmartRF™ Studio**



## 6 Typical Application Circuit

### NOTE

This section is intended only as an introduction.

Very few external components are required for the operation of the CC1201 device. [Figure 6-1](#) shows a typical application circuit. The board layout will greatly influence the performance of the CC1201 device. [Figure 6-1](#) does not show decoupling capacitors for power pins.

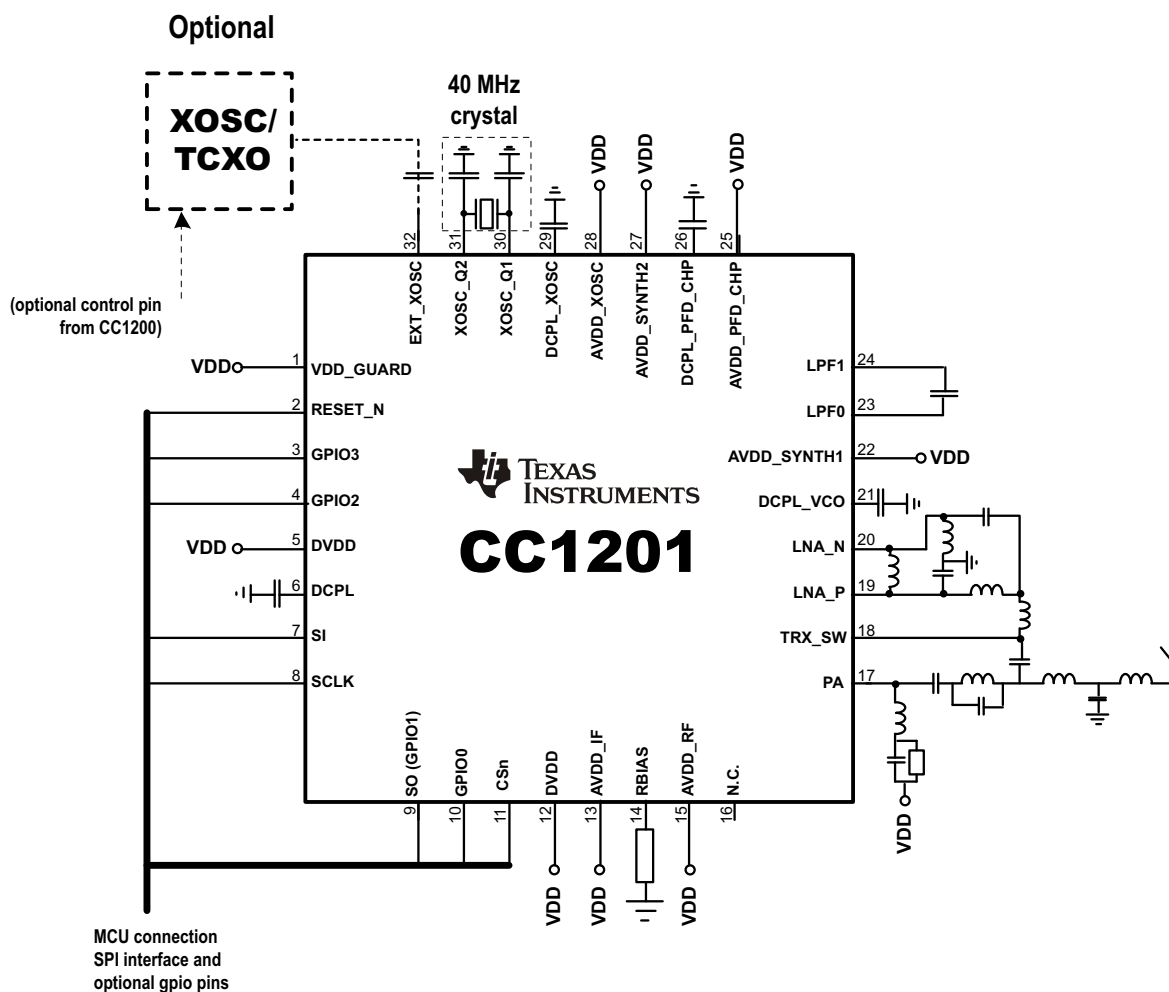


Figure 6-1. Typical Application Circuit

For more information, see the reference designs available for the CC1201 device in [Section 7.2, Documentation Support](#).

## 7 Device and Documentation Support

### 7.1 Device Support

#### 7.1.1 Development Support

##### 7.1.1.1 Configuration Software

The CC1201 device can be configured using the SmartRF Studio software ([SWRC046](#)). The SmartRF Studio software is highly recommended for obtaining optimum register settings, and for evaluating performance and functionality.

#### 7.1.2 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, CC1201). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, RHB), the temperature range (for example, blank is the default commercial temperature range), and the device speed range, in megahertz. provides a legend for reading the complete device name for any CC1201 device.

For orderable part numbers of CC1201 devices in the QFN package types, see the Package Option Addendum of this document, the TI website ([www.ti.com](http://www.ti.com)), or contact your TI sales representative.

## 7.2 Documentation Support

The following documents describe the CC1201 processor. Copies of these documents are available on the Internet at [www.ti.com](http://www.ti.com). *Tip:* Enter the literature number in the search box provided at [www.ti.com](http://www.ti.com).

[SWRR106](#) CC112x IPC 868- and 915-MHz 2-layer Reference Design

[SWRR107](#) CC112x IPC 868- and 915-MHz 4-layer Reference Design

[SWRR122](#) CC1201EM 420- to 470-MHz Reference Design

[SWRR121](#) CC1201EM 868- to 930-MHz Reference Design

[SWRC046](#) SmartRF Studio Software

[SWRA428](#) CC112x/CC120x Sniff Mode Application Note

## 7.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

[TI E2E™ Online Community](#) *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

[TI Embedded Processors Wiki](#) *Texas Instruments Embedded Processors Wiki*. Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 7.4 Trademarks

SmartRF, E2E are trademarks of Texas Instruments.  
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## 7.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 7.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 8 Mechanical Packaging and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CC1201RHBR       | ACTIVE        | VQFN         | RHB             | 32   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 85    | CC1201                  | <a href="#">Samples</a> |
| CC1201RHBT       | ACTIVE        | VQFN         | RHB             | 32   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 85    | CC1201                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CC1201RHBR | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.5     | 8.0     | 12.0   | Q2            |
| CC1201RHBT | VQFN         | RHB             | 32   | 250  | 180.0              | 12.4               | 5.3     | 5.3     | 1.5     | 8.0     | 12.0   | Q2            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CC1201RHBR | VQFN         | RHB             | 32   | 3000 | 336.6       | 336.6      | 28.6        |
| CC1201RHBT | VQFN         | RHB             | 32   | 250  | 210.0       | 185.0      | 35.0        |

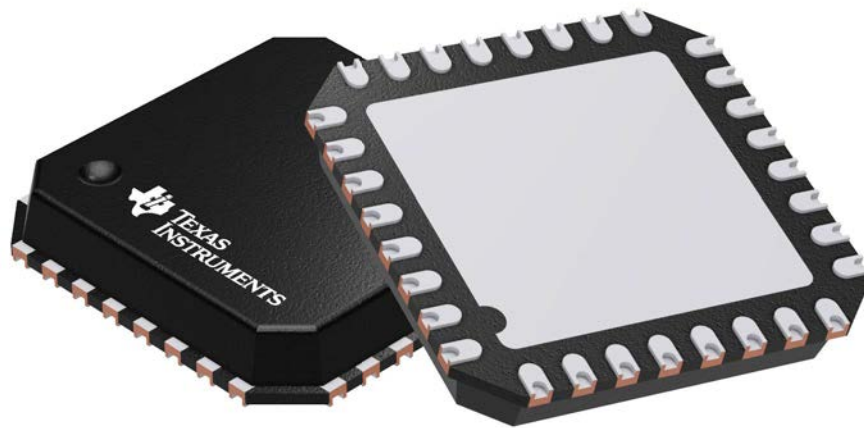


## GENERIC PACKAGE VIEW

RHM 32

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4205347/C

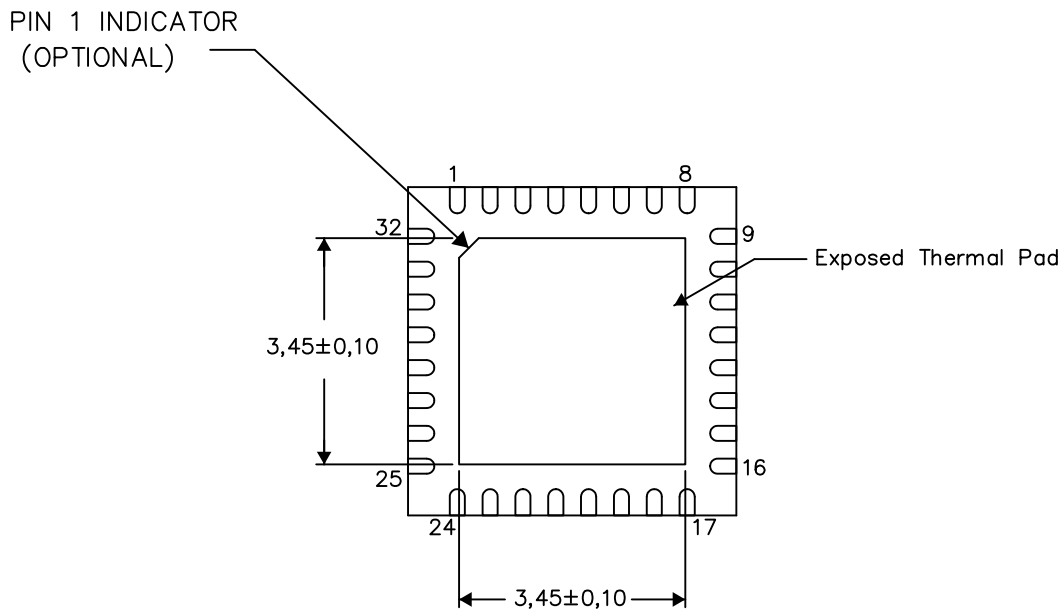


THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206356-2/AC 05/15

NOTE: A. All linear dimensions are in millimeters



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